Energy-Efficient Ferroelectric Field-Effect Transistor-Based Oscillators for Neuromorphic System Design

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ABSTRACT Neuromorphic or bioinspired computational platforms, as an alternative for von-Neumann structures, have benefitted from the excellent features of emerging technologies in order to emulate the behavior of the biological brain in an accurate and energy-efficient way. Integrability with CMOS technology and low power consumption make ferroelectric field-effect transistor (FEFET) an attractive candidate to perform such paradigms, particularly for image processing. In this article, we use the FEFET device to make energy-efficient oscillatory neurons as the main parts of neural networks for image processing applications, especially for edge detection. Based on our simulation results, we estimated a significant energy efficiency compared with other technologies, which shows roughly 5–120× reduction, depending on the design.

INDEX TERMS CMOS technology, coupled oscillator, ferroelectric field-effect transistor (FEFET) device, frequency modulation, neuromorphic computing.

I. INTRODUCTION

BRAIN-INSPIRED neuromorphic computing provides a strong platform to implement computationally intensive operations, such as associative memory, recognition, and classification, in which traditional von-Neumann paradigms lack computational efficiency due to higher power consumption, big area, reduced accuracy, and poor parallelism [1]–[17]. A variety of computing strategies have been demonstrated in this regard to implement such non-Boolean computing systems. Cellular neural networks (CNNs) and oscillatory neural networks (ONNs) are some examples [7]. Among them, ONNs earn us significant area reduction, simpler structures, fast recognition speed, and high energy efficiency [1], [4], [9], [10], [14]. Over the last few decades, CMOS technology has been the basis of both traditional Boolean computing and modern oscillatory networks. However, the implementation of ONNs in CMOS technology becomes a looming challenge since each oscillator comprises tens of transistors, and a large number of oscillator arrays are needed for ONNs. This issue is more challenging when we are close to the end of the silicon road map. Nevertheless, novel beyond-CMOS technologies are emerging,

with characteristics suited for new computing architectures [1], [2], [4], [5], [8], [10]–[13], [15], [18]–[21].

Coupled-oscillator neurons have become critical parts of ONNs with the possibility of performing low-power computations and offering interesting features, such as synchronization dynamics. To date, modern oscillatory neurons have been physically implemented using the emerging nanoscale technologies, such as spin-torque (ST), memristors, and metal–insulator transitions (MITs) oxides, because of their unique properties where even the most advanced CMOS nodes are left behind [1]–[14], [22], [23]. Both ST and MIT technologies show hysteretic behavior, synchronization capabilities, and acceptable sensitivity to image contrast compared with the CMOS-based implementation. Considering these features, arrays of coupled oscillators comprised by MIT and MOSFET devices are used to perform visual saliency [4], [5], compare the images of faces and handwritten numbers (pattern recognition) [1], [5], [6], [9], and generate locomotion gait patterns [23] and spoken vowel recognition [22]. In [14], it is shown that scaling the number of oscillators can implement a variety of image processing applications, including salience detection (two oscillators), color

interpretation (three oscillators), morphological operation (five oscillators), and pattern matching (nine oscillators). The coupled ST oscillators (STOs) are also considered for edge detection, pattern, and spoken digit recognition in [7], [8], [11]–[13], and [24]. Neurons are designed to operate at realistic/biologic time constants (a few milliseconds) or accelerated biological time scales (i.e., 10^5 times faster than the biosystems) [25]. Although the ST- and MIT-based neurons are implemented for accelerated processing speed, integrability with CMOS is not currently available in these technologies. Note that the hysteretic behavior of MIT oxide is static and cannot be controlled by the physical parameters [10]. This causes fewer degrees of freedom to perform computing operations.

The aim of this work is to explore the potential of the ferroelectric field-effect transistor (FEFET) in the design of coupled oscillators for image processing applications. The FEFET-based oscillators can be integrated with the traditional CMOS flow with ease while providing simple circuit topologies with comparable power consumption to ST and MIT devices and presenting biologically realistic time constants to mimic the functionality of the biological brain. In addition, the hysteresis loop in FEFET devices can be dynamically controlled by its input bias, which is a unique feature of these devices [10]. When configured with MOSFET, this controllability can also be tuned via the MOSFET gate voltage, thus presenting the second degree of freedom [10]. We will use this behavior to modulate the oscillation frequency required to perform computing states. The rest of this article is organized as follows. The device modeling and I–V characteristics of the FEFET and the voltage controllability of the hysteresis loop are presented in Section II. In Section III, the proposed FEFET-based oscillator, the frequency modulation, and the physical mechanism of this property are presented. Following this, a detailed explanation about the design methodology of the coupled oscillatory-based edge-detection structure along with the simulation results is presented in Section IV. Finally, the conclusions are drawn in Section V.

II. DEVICE MODEL AND CHARACTERISTICS

The self-consistent compact model presented in [26]–[28] is used here to model the FEFET device. The underlying baseline 14-nm FinFET device is modeled using the industry-standard BSIM-CMG model. The ferroelectric (Fe) physics part is modeled with experimentally calibrated Landau–Khalatnikov (L-K) formulations. This model is based on the single domain Fe approximation. The L-K formulations, the Fe model, and transistor behavior are then self-consistently solved in this model.

Hysteresis behavior in NCFETs is exploited in the work to create energy-efficient circuits. NCFET hysteresis is dependent on the Fe thickness used in the device. A higher T_{fe} reduces the Fe negative capacitance causing hysteresis. The model used here accounts for this behavior. In Fig. 1(a), the transfer characteristics at the drain–source voltage $V_{dd} = 1.2$ V is shown, while T_{fe} is swept from 10 to 19 nm.

NCFET does not show the hysteresis loop for T_{fe} lower than 13 nm. Ensuring that there is no hysteretic behavior for $T_{fe} < 13$ nm, we did not show the characteristics for thicknesses lower than 10 nm. In addition, the width of the hysteresis loop becomes larger with T_{fe}.

From these simulation results, we arbitrarily select $T_{fe} = 15$ nm for our designs. This guarantees the hysteretic behavior, which is necessary for the design of the oscillator. A thicker or thinner Fe layer will just affect the operation frequency of the oscillator. The Fe thickness may also change the allowable variations of NCFET gate voltage to modulate frequency. This relation between the hysteresis loop and frequency modulation will be explained in detail in Section III. Fig. 1(b) shows the I_d–V_{gs} characteristics while sweeping the drain voltage V_d. We note that, as reported in [10], the NCFET hysteresis in the I_d–V_{gs} characteristics become narrower and move to the right for higher V_d. This tunability of the hysteretic window is an NCFET feature, which is exploited in our design.
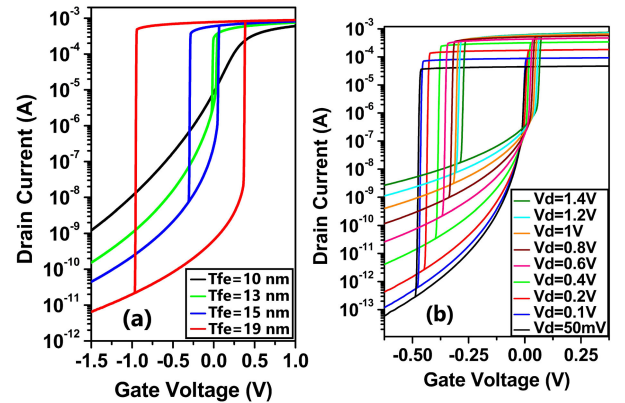

FIGURE 1. DC current–voltage characteristics of the NCFET model for different (a) Fe layer thicknesses and (b) drain voltages with $T_{fe} = 15$ nm.

III. FEFET-BASED OSCILLATOR NEURONS

To evaluate the frequency behavior of Fe oscillator neurons, we use the neuron circuit, reported in [21] and shown in Fig. 2(a). An output capacitor C_o is connected in parallel with the drain–source channel of the MOSFET device M_1 that represents the membrane capacitor of the silicon neuron. M_2 presents the FEFET device. Fig. 2(b) shows the load line including both the output characteristic of M_1 for the FET gate-voltage V_{gm} set as 0.3, 0.4, 0.5, and 0.6 V and the drain-current waveform of M_2 as a function of the neuron membrane voltage V_{mem} for three values of V_{gf} equal to 0.2, 0.4, and 0.6 V. The oscillatory operation of the proposed circuit shown in Fig. 2(a) is adjusted by analyzing the load line [10], [21]. For constant bias voltages $V_{gf} = 0.2$ V and $V_{gm} = 0.5$ V and before oscillating, V_{mem} is zero, and the oscillator case corresponds to point A in Fig. 2(b). C_o is charged by M_2 and reaches the voltage at points C. Due to the abrupt FEFET transition here, drain current decreases
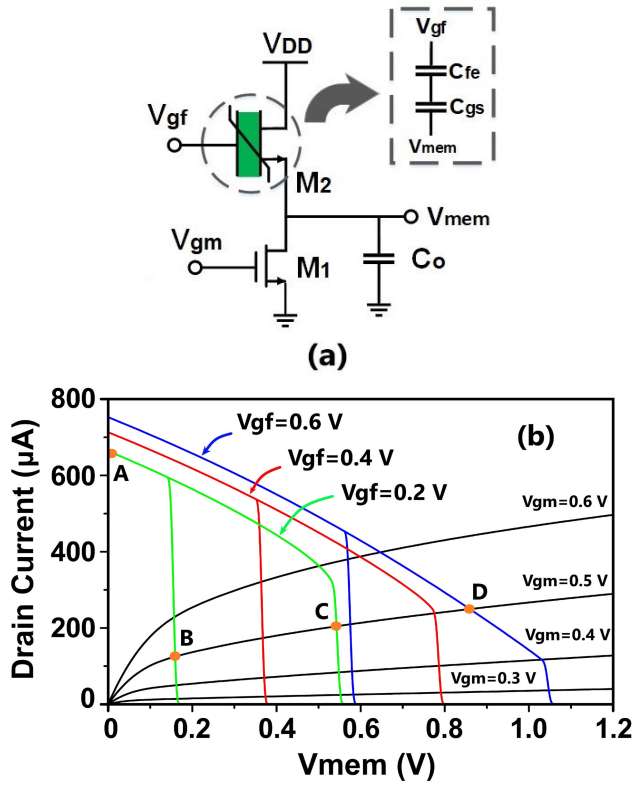
FIGURE 2. (a) Circuit diagram of FEFET-based oscillator neuron and (b) load-line of the combination of FEFET and FET devices in (a).

FIGURE 3. Membrane voltage for FEFET gate voltage equal to (a) 500 and (b) 100 mV. (c) Oscillation frequency versus V_{gf}.

FIGURE 4. Schematic of the proposed coupled oscillator neuron.

suddenly, leading C_o to be discharged by M_1. V_{mem}, then, reaches the voltage at point B, and the second abrupt transition in this part increases the current, which will force C_o to be charged again. This explains the oscillatory behavior of the circuit. An interesting aspect is that the oscillation frequency being dependent on hysteresis window can be tuned with V_{gf}. Fig. 3(a) and (b) illustrates such frequency modulation once FEFET bias voltage is changed, for example, from 200 to 600 mV for $V_{gm} = 0.3$ V and $C_o = 1$ nF and with the FET channel width and length of 20 μm and 180 nm, respectively. Values of C_o and the FET dimension are kept fixed for all simulations. The variation of oscillations frequency as a function of V_{gf} is also plotted in Fig. 3(c). As seen, the oscillation frequency approximately gets three times greater when V_{gf} rises from 100 to 650 mV. This provides a near-linear input voltage to the output frequency operating range.

Therefore, the oscillator in Fig. 2(a) is a voltage-controlled oscillator (VCO). In this VCO, the oscillation frequency can be controlled by its gate voltage. In addition, the proposed oscillator dissipates the maximum averaged power, including both static and dynamic powers, of 20 μW when V_{gf} is set to its maximum value (see Fig. 3). Based on our simulation and analysis, this results in ~5–120 times reduction of power consumption compared with some ST- and MIT-based neurons reported in [1], [6], and [30]–[33]. The energy ef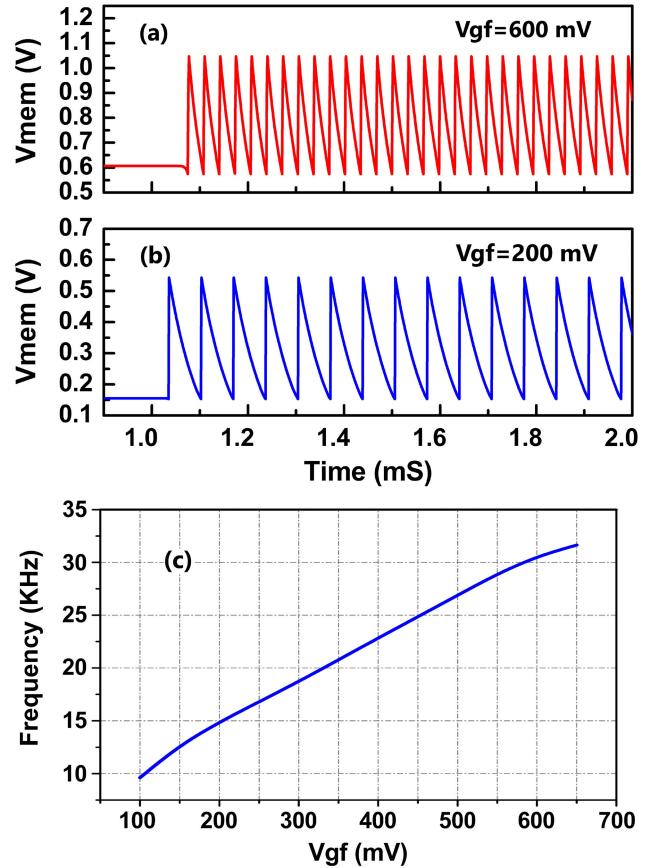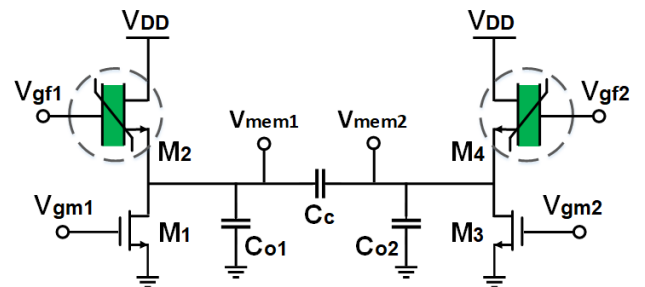ficiency of the proposed oscillator is also obtained by averaged power dissipation and frequency [34]. Such a power regime corresponds to the energy efficiency per cycle of 0.63 nJ/cycle for each oscillator.

IV. FEFET-BASED COUPLED OSCILLATOR FOR IMAGE PROCESSING APPLICATIONS

There are different possible ways to connect oscillators and create coupled oscillatory networks. Two regular cases are the resistive and the capacitive coupling [5], [9], [10], [35]–[38]. Here, we electrically connect two oscillator neurons to a common node using a coupling capacitor C_c, forming the proposed coupled-oscillator neuron, as shown in Fig. 4. For image processing applications, the proposed
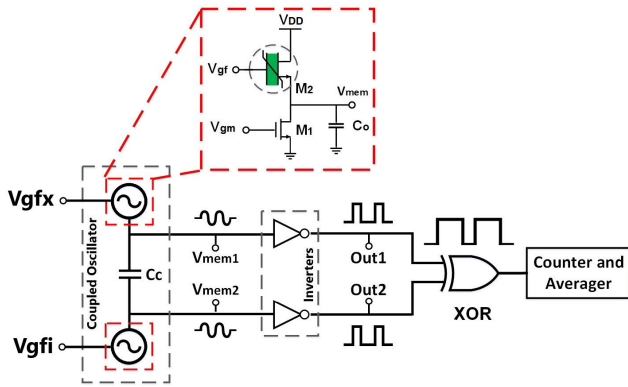
FIGURE 5. Circuit implementation of XOR measure for image processing. $C_C = 100$ fF is, therefore, chosen to meet the need for coupling only.

coupled oscillator should be sensitive enough to sense small differences between incoming voltages as consequences of the shift in pixels' color or intensity [10]. As a result, the coupling mechanism should not be as strong as it necessarily synchronizes two oscillators even when the delta between FEFET gate voltages of the oscillators is not negligible.

Frequency modulation due to the voltage-controllable hysteresis of FeFET was evaluated in the previous section. Here, we use this feature to design tunable oscillators for edge detection. The intensity of each pixel can be mapped to electrical voltages. Each voltage leads to a specific output frequency, and the difference between those pixels will be sensed through the frequency and/or phase differences between oscillator neurons. Differences in pixels cause a larger difference in oscillator frequencies. We apply this feature of the coupled oscillator to calculate the distance norm or Euclidean distances through the averaged XOR measure for the applications of image processing, such as visual saliency and pattern recognition [4], [5], [39], [40]. Averaged XOR has been shown to be a reliable vehicle to test whether the oscillators are locked or not [4], [5]. This measure includes the pixel intensity to frequency conversion, performed through coupled oscillators, creation of binary values from the output of oscillators that can be implemented by two inverters, applying XOR operation on those binary values, and averaging the XOR outputs. Fig. 5 shows an implementation of such a measure [4], designed by using our proposed FEFET-based coupled oscillator, which is used to evaluate the level of pixel similarity. For each neighboring n pixels, a number of $n - 1$ testing circuits are needed, and each pixel is compared with the reference one through a separated circuit. As long as pixels are similar in terms of intensity, the XORs will output logic zero, as illustrated in Fig. 6(a). Here, V_{mem1} and V_{mem2} are the outputs of the oscillators, and Out_1 and Out_2 present output waveforms of inverters in Fig. 5. A larger difference between pixels yields longer logic one in the XOR output, indicating how much the input pixels are different. An example of the outputs of the oscillators, inverters, and XOR gate is shown
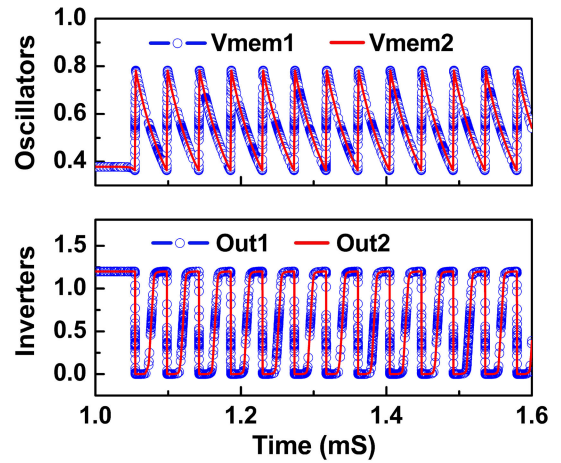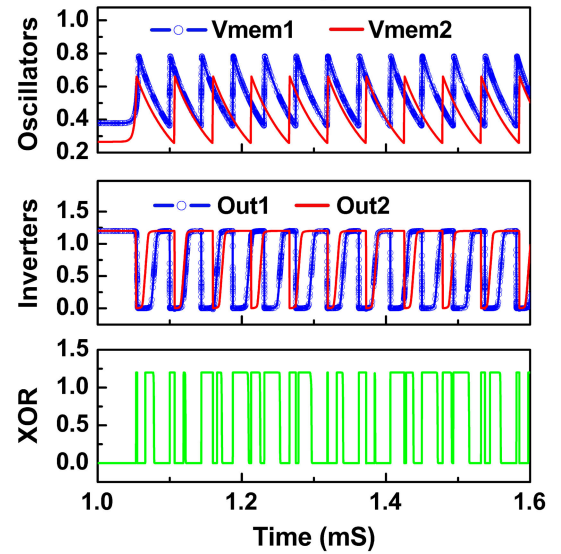
FIGURE 6. Example of XOR measure when (a) similar pixels and (b) two different pixels are compared. Averaging over the outputs of all XORs in a segment of the image can be a criterion to detect the edge. Such a measure is similar to the calculation of the Euclidean distances.

in Fig. 6(b) when two different voltages are applied to the oscillators.

Also, the variation of averaged XOR as a function of the difference between input voltages ΔV_{gf} is presented in Fig. 7, showing the operation of this XOR metric as a fractional distance norm to evaluate pixels similarity. The averaging over the whole XOR characteristics, for example, eight XOR outputs for nine pixels, will be either high, which indicates an edge, or low, meaning that there is no edge in the given neighboring pixels. In addition to showing the promise of FEFET-based oscillator in well-known average XOR implementation, we propose a new design.

Fig. 8 simply shows the digital-to-analog conversion for the implementation of the edge-detection mechanism. First, the input image is divided into smaller segments of nine
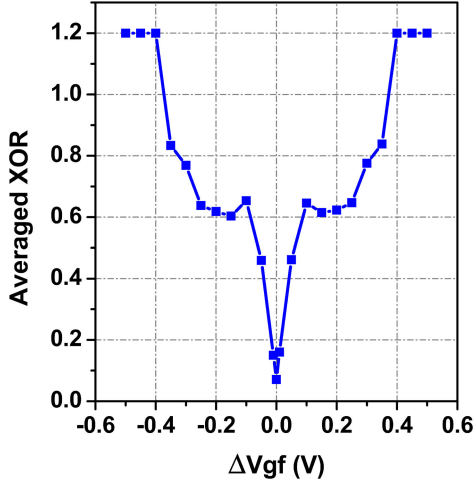
FIGURE 7. Averaged XOR of the oscillatory network in Fig. 5 as a function of ΔV_{gf}. The output of the averaged XOR is a fractional distance norm to calculate the similarity between two pixels.
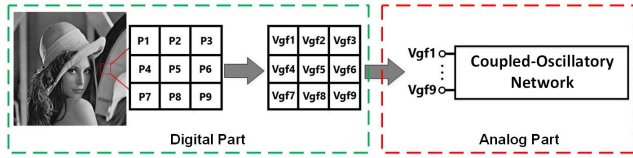

FIGURE 8. Simple demonstration of the digital-to-analog conversion for edge detection.
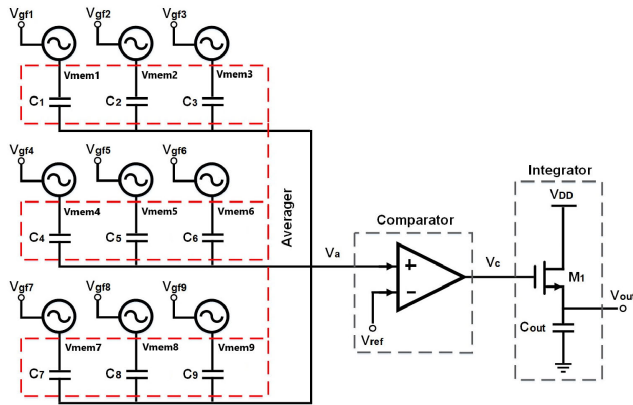

FIGURE 9. Proposed coupled-oscillatory network for edge detection.

pixels (arrays of 3×3 pixels). The pixel's intensity to dc voltage conversion is performed in MATLAB, and all corresponded dc voltages will be applied to the oscillatory network for processing. The pixels' intensities are also subdivided into 55 ranges, correspondingly, relative to the steps of 10 mV in the input voltages, which is the lowest sensible voltage change in our proposed coupled-oscillatory network. We design the circuit schematic of edge detection presented in Fig. 9 as the analog part of the Fig. 8, which is similar to the circuit reported in [11]–[13] for
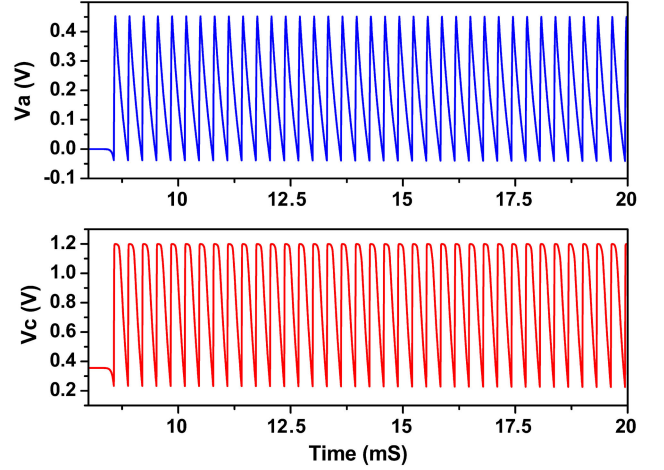

FIGURE 10. Output characteristics of the averager (blue) and the comparator (red) when all oscillators are locked.

neuronal computing. The comparator and the integrator circuits are both implemented in CMOS technology. Voltages V_{gf1-9} represent the dc voltages over the gate terminals of the FEFET devices in each oscillator (V_{gf}), corresponding to the intensity of each pixel in a given segment. The minimum and maximum possible values of these input bias voltages are set based on the variation range of V_{gf} in Fig. 3. Also, we consider the minimum and the maximum voltages as absolute black and white colors, respectively, and all color spectra of pixels will vary between these two borders. The outputs of the oscillators are, then, coupled capacitively using a capacitor bank shown by red dash lines in Fig. 9. This capacitor bank works as an averager to combine all output voltages to just one characteristic, which passes through the comparator. The relation between V_a and the membrane voltages V_{mem} of all oscillators can be obtained as follows by using KVL in the V_a node:

$$\sum_{i=1}^{n} j\omega C_i(V_a - V_{memi}) = 0 \qquad (1)$$

where ω is the angular frequency, $C_i(i = 1, \ldots n)$ are capacitors of the capacitive bank in Fig. 9, and n is the number of oscillators. Equation (1) is rewritten for V_a based on V_{memi} as

$$V_a = \frac{1}{n} \cdot \sum_{i=1}^{n} V_{memi} \qquad (2)$$

where V_a is the output voltage of the averager. Equation (2) indicates how the averager behaves to combine the output characteristics of the oscillators. The output of the comparator will be a digitized version of the averager voltage, feeding the integrator to charge the output capacitor C_{out}. Fig. 10 shows the averager waveform V_a and the output of the comparator V_c once all oscillators are supplied by close input voltages (locked case), corresponding to similar intensities of all pixels in the segment. As seen, when oscillators operate

TABLE 1. Comparison between our proposed NCFE-based oscillator neuron and other technologies reported in state of the art in terms of power consumption.
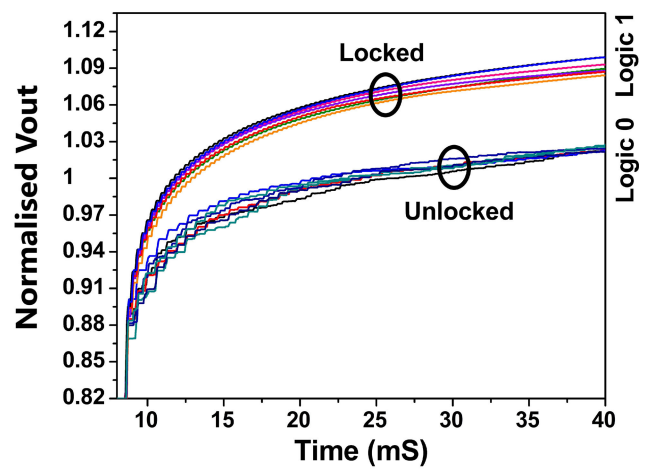
References	[1]	[6]	[22]	[41]		[30]	[31]	[42]	[33]	[43]	[44]	[45]	This Work
Technology	TaO_x	NbO_2	VO_2	TMR ST^2	GMR ST^3	ST	VO_2	$HfTaO_x$	TaO_x	28 nm CMOS	180 nm CMOS	350 nm CMOS	FEFET
Supply Voltage (V)	1	1.6	0.7	0.7	0.01	1	0.8	1	1	1	1.8	3.3	1.2
Power (μW)	<200	1600	32	50.6	2000	200	2400	50	<100	1900^4	$2-50$	60	$6.4-20$
Energy per Cycle ($\frac{nJ}{cycle}$)	–	–	2670	–	–	–	–	–	–	$2.3-30$	–	30000	<0.63

1. Reported for the whole stochastic IMT-based Oscillatory Neuron. 2. TMR-ST: Tunneling Magneto-Resistance Spin-Torque. 3- GMR-STNO: Giant Magneto-Resistance Spin-Torque. 4. Energy per spike of the whole neuromorphic system.
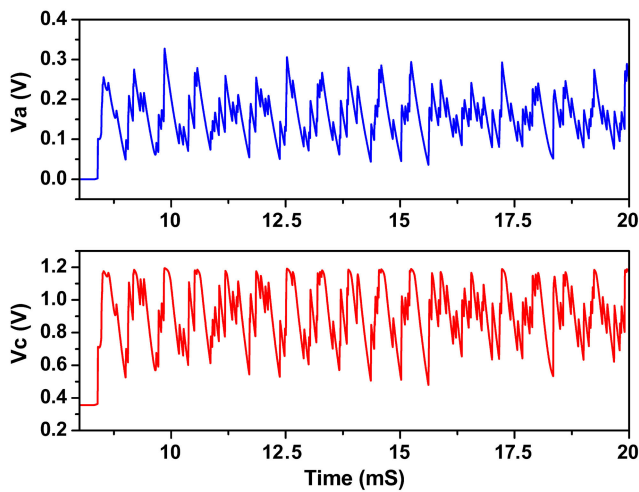
FIGURE 11. Output characteristics of the averager (blue) and the comparator (red) in the unlocked case.

FIGURE 12. Output characteristics of the edge-detection circuitry in Fig. 8. The highest (logic 1) and lowest (logic 0) values correspond to those segments of the image without (locked case) and with (unlocked case) edge, respectively.

at the same frequency, a fine and clear wave is created by averager.

This waveform is able to exceed the reference voltage of the comparator, set to the threshold voltage of the MOSFET device as $V_{rf} = 180$ mV, and activate it frequently. This will cause the output capacitor to be changed faster toward the highest value (so-called logic one or white color). Such an output voltage indicates that the proposed segment does not show an edge in the input image. On the other hand, if oscillators sense different pixel intensities, they will oscillate at a variety of frequencies (unlocked case), and consequently, the averager will output an out of shape characteristic, which rarely passes V_{rf}. Therefore, C_{out} will be charged less and slower than a locked case. We conclude that the given segment represents an edge and decipher this minimum output voltage as a logic zero, equivalent to black color. Fig. 11 shows an example of the averager and comparator outputs in the unlocked case. The normalized output

waveform V_{out} is also presented in Fig. 12 for some segments with similar pixels (highest values) and those presenting edge (minimum values). To show the ability of our FEFET-based edge-detection topology, we have worked on a simple input image presented in the top-left side of Fig. 13. The 2-D frequency contour of this image is also shown in the top right. The abovementioned process is applied to all the segments (each has 3×3 pixels) of this picture, and the final result is illustrated in the bottom left of Fig. 13. As seen, the proposed topology in Fig. 9 can extract the edges of the input image well with acceptable accuracy. Table 1 presents a comparison between our FEFET-based oscillator with state of the art in terms of the power consumption and energy per cycle. It is clear that the performance of the proposed oscillator in this report is comparable with literature. It must be noted that this oscillatory behavior can be affected by the manufacturing process variations, which is not studied in this work.
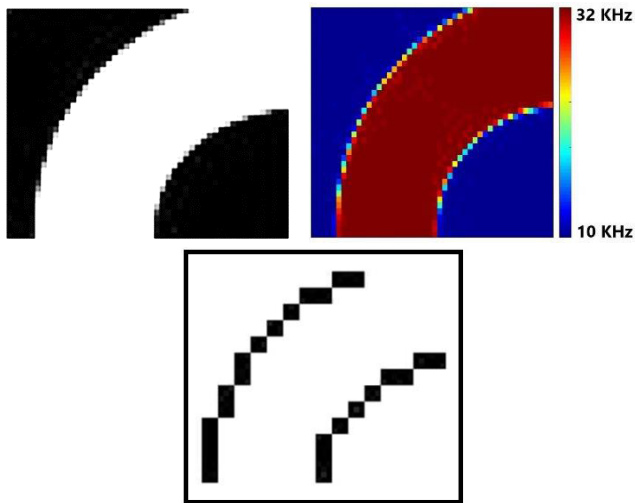
FIGURE 13. Input image (top left) and its frequency 2-D contour (top right). The bottom image is the output of edge detection performed by our proposed FEFET-based edge-detection structure in Fig. 8.

As shown in [36] for VO2-based oscillators, techniques for simulation, analysis, and design will need to be developed to address these challenges.

V. CONCLUSION

The benefits of the FEFET-based coupled oscillator neurons in the implementation of non-Boolean computational paradigms are elaborated in this article. Besides the integrability with the CMOS technology and low power consumption, the dynamically controllable hysteresis window through input bias voltage is a unique feature of FEFETs. This property makes FEFET an exciting device that can help propel the next advances in neuromorphic computing. We have, then, used this unique feature to approximate visual saliency and detect the edges of a simple image. Simulation results show that FEFET-based coupled oscillators are able to sense the difference between pixel intensities well. Also, they dissipate low power, which is comparable to the MIT- and ST-implemented counterparts.

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