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Benchmarking and Optimization of Spintronic Memory Arrays

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ABSTRACT In this article, we present a cross-layer optimization and benchmarking of various spintronic memory devices, including spin-transfer-torque magnetic random access memory (STT-MRAM), spin-orbit-torque (SOT) MRAM, voltage-controlled exchange coupling (VCEC) MRAM, and magnetoelectric (ME) MRAM. Various material, device, and circuit parameters are optimized to maximize array-level READ and WRITE performances and to benchmark spintronic devices against static random access memory (SRAM). It is shown that the optimized parameters, such as magnetic tunnel junction (MTJ) oxide thickness or transistor size, are quite different for various device options. The optimal oxide thickness of VCEC-MRAM is 1.6 nm because it is a voltage-controlled device; thus, thicker oxide gives smaller READ energy-delay product (EDP), whereas, for STT-MRAM, the optimal oxide thickness is 1.3 nm to keep the WRITE voltage low while avoiding READ disturbs. In addition, we find that the co-optimization of material, device, and circuit analyses are critical because it is not enough to identify the most promising material for various device options with only material- or device-level metrics. For instance, SOT materials with the highest spin conductivity may not result in the best array-level WRITE performance because of their large resistivity and, in some cases, READ disturb issues. We also present a new design and cell layout for ME-MRAM in which the number of access transistors depends on the WRITE voltage. The benchmarking results show that SOT-MRAM can be fast and low energy but would suffer from a 25% larger cell area compared with STT-MRAM. VCEC-MRAM can be denser than STT-MRAM (2T1MTJ) and dissipate less energy but would suffer from slower READ operations because of its large oxide thickness. ME-MRAM can be fast, low energy, and dense compared with all other options.

INDEX TERMS Magnetoelectric (ME), nonvolatile memory, spintronics, spin-orbit torque (SOT), spin-transfer torque (STT), voltage-controlled exchange coupling (VCEC).

I. INTRODUCTION

SPINTRONIC devices are promising candidates for embedded memory due to their nonvolatility and small footprint compared with static random access memory (SRAM) [1]. They also offer high endurance and faster WRITE operations compared with resistive random access memory (RRAM) and embedded nand flash and better scalability of their WRITE currents compared with phase-change memory (PCRAM) [2]. Spin-transfer-torque magnetic random access memory (STT-MRAM), which is gradually moving into production, uses a two-terminal magnetic tunnel junction (MTJ). When large currents pass through the device, spin-polarized electrons are injected from a fixed ferromagnet to a free ferromagnet. The switching of the free ferromagnet depends on the direction of the current and the magnetic order of the fixed ferromagnet. Recently, perpendicular MTJs with diameters as small as 16 nm and WRITE currents as low as ~40–90 μA [3] have been reported. However, several major challenges remain for the creation of scalable and reliable STT-MRAM. It is generally not energy efficient to switch a magnet using spin-transfer torque because large WRITE currents for several nanoseconds are required. Hence, relatively large access transistors must be used, and reliability issues may arise when large currents pass through the oxide layers in MTJs [4]. Finally, the fact that the WRITE and READ currents pass through the same path does not allow for the independent optimization of the READ and WRITE operations.

To address these challenges, other MRAM device options have been proposed based on various WRITE mechanisms, such as spin-orbit torque (SOT-MRAM), voltage-controlled magnetic anisotropy (VCMA-MRAM) [5], voltage-controlled exchange coupling (VCEC-MRAM) [6], and magnetoelectric effect (ME-MRAM) [7]. In all these devices, the READ operation is based on the tunnel magnetoresistance (TMR) effect [8], [9].

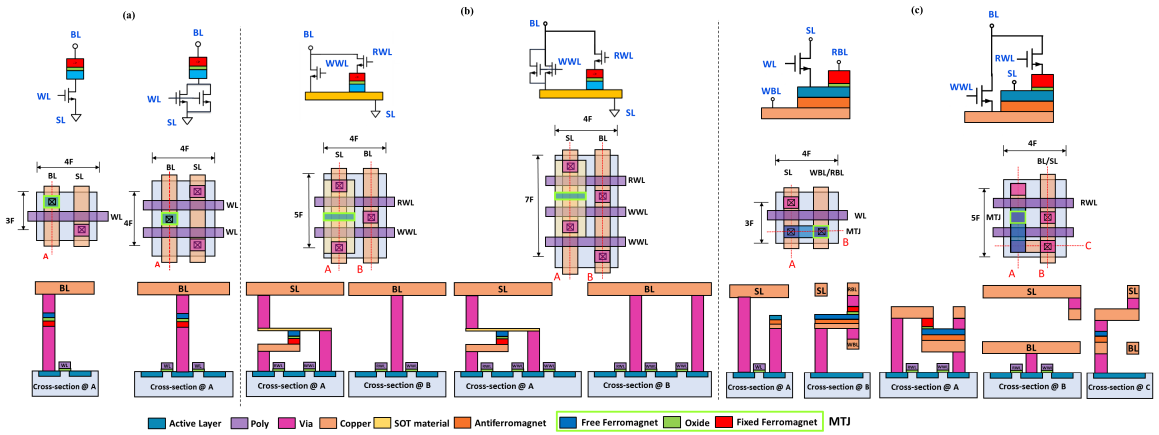

FIGURE 1. **Schematics and layouts of various spintronic memory cells. (a) STT-MRAM or VCEC-MRAM. (b) SOT-MRAM. (c) ME-MRAM.**

SOT-MRAM utilizes an inherently more energy-efficient mechanism compared with STT-MRAM; hence, it may permit faster and more energy-efficient operations. Theoretically, when a charge current I_C passes through an SOT channel, the generated spin current I_S is written as

$$I_S = \frac{\hbar}{2e}\frac{W_{\mathrm{FM}}}{t_{\mathrm{SO}}}\theta_{\mathrm{SH}} I_C \tag{1}$$

where e is the electron charge, $\hbar$ is the reduced Planck's constant, W_{FM} is the width of the ferromagnet, t_{SO} is the thickness of the SOT material, θ_{SH} is the spin Hall angle of the SOT material, and the length of the free layer ferromagnet is equal to the width of the SOT material. With the right geometrical and material parameters, this spin current can be several times larger than the spin-polarized current in STT-MRAM whose upper limit is [10]

$$I_{\mathrm{s}} = \frac{\hbar}{2\mathrm{e}} I_c. \tag{2}$$

In addition to the current-controlled devices, researchers are pursuing voltage-controlled devices that are potentially more energy efficient because of the much lower WRITE currents involved. VCEC-MRAM is a bidirectional voltage-controlled device in which the polarity of the applied voltage across the MTJ determines the magnetization direction of the free ferromagnet. The *ab initio* calculations show that the applied voltage close to the oxide interface can modulate the interlayer exchange coupling in the synthetic antiferromagnet, thus changing the magnetization direction of the free ferromagnet [6]. Another candidate is ME-MRAM that uses multiferroic materials, such as $BiFeO_3$ [11], [12] or Cr_2O_3 [13], in contact with a free ferromagnet of an MTJ. Once the applied voltage across the ME layer is larger than its coercive voltage, its ferroelectric polarization and the antiferromagnetic order will switch. If the interface exchange coupling or the exchange bias effect is large enough, the magnetic order of the adjacent ferromagnet will also switch.

To understand the limits and opportunities offered by these novel WRITE mechanisms, various materials, technology, and design parameters must be optimized, and various tradeoffs must be evaluated. Prior publications have compared the potential performance of SOT-MRAM versus STT-MRAM [14], [10]. In addition, researchers have studied several spintronic device candidates and have quantified their array level performances [15]–[17]. However, many new SOT and ME materials have been reported since then, and several important factors, such as current splitting between the SOT and ferromagnet layers, domain nucleation/propagation and thermal noise during the switching process, and the impact of field-like torque, have not been considered in these studies. The array-level potential performances of VCEC-MRAM and ME-MRAM have not been quantified. Finally, a comprehensive cross-layer optimization and benchmarking of all MRAM technology options are lacking. Each spintronic memory option offers vastly different tradeoffs at the material, device, and circuit levels, and a fair comparison requires comprehensive modeling and optimization at all levels.

To fill these gaps, this article presents a uniform cross-layer optimization and benchmarking of various spintronic memory devices in a 256 × 128 bits array. The simulation framework uses SPICE simulations, analytical equations, a macrospin model, and micromagnetic simulations. We also explore various material candidates for SOT-MRAM, such as heavy metals, alloys, semimetals, and topological insulators. Note that VCMA-MRAM has not been considered in this work since it requires precise pulsewidth control [18], [19], or it needs to be combined with STT [19], [20] or SOT for a deterministic magnetization switching. The parameters for each type of MRAM are chosen from the recent state-of-the-art experiments, as will be discussed in Table 2.

The rest of this article is organized as follows. Section II shows the schematics and layout of various types of memory cells. Section III describes the modeling methods for the READ and WRITE operations. Section IV discusses the results and comparisons in terms of READ/WRITE delay/energy for various spintronic memory cells. Section V summarizes the findings and suggests future directions.

II. SCHEMATICS AND LAYOUT

The two key factors needed for array-level modeling of MRAM options are the cell area and the number of transistors per cell as they determine the interconnect lengths and parasitic capacitances. The schematics and the layout designs of the spintronic memory cells are shown in Fig. 1. We define $F = 30$ nm as the half-metal pitch in the 15-nm CMOS technology is consistent with the beyond-CMOS benchmarking presented in [21]. We also consider various numbers of WRITE transistors with a fixed current flowing per transistor to evaluate the WRITE speed.

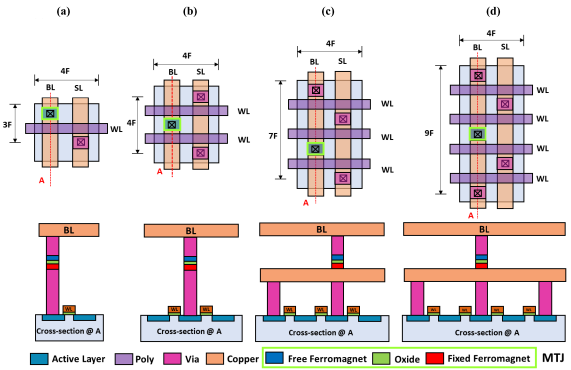

FIGURE 2. Layout of STT-MRAM with (a) one, (b) two, (c) three, and (d) four access transistors, and their cross-sectional areas at line A. (a) 1T1MTJ. (b) 2T1MTJ. (a) 3T1MTJ. (a) 4T1MTJ.

For the STT-MRAM and the VCEC-MRAM, the layout area can be as small as 12 F^2 if only one-access transistor is used since the READ and WRITE operations share the same path. Layout designs of STT-MRAM with one to four access transistors are shown in Fig. 2, as will be discussed later in Section IV For the SOT-MRAM, since the READ and the WRITE operations are separated, two transistors are needed to avoid sneak currents. The layout area unavoidably increases to 20 F^2 in the case of one WRITE access transistor.

For the ME-MRAM, the READ and WRITE operations are separated by two access transistors to prevent READ disturb, as shown in Fig. 3(a). The cell area is 20 F^2, which is similar to the SOT-MRAM using one WRITE and one READ access transistor, as shown in the right-hand side of Fig. 1(c). Interestingly, when the WRITE voltage (V_{WRITE}) of the ME material is as large as 0.4–0.5V, which is higher than the typical READ voltage of an MTJ (∼0.1–0.15 V), a single access transistor can be used for both READ and WRITE operations, as shown in Fig. 3(b). In this one-access transistor scheme, a leakage current passes through the MTJ during the WRITE operation and the READ voltage is applied to the ME stack. As will be discussed later, the leakage current during the WRITE operation can be kept small by a proper choice of MTJ oxide thickness, and a WRITE voltage larger than 0.4 V would ensure no READ disturbs. The benefit of using a one-access transistor comes with a smaller layout area of the ME-MRAM down to 12 F^2, as shown in the left-hand side of Fig. 1(c).

III. MODELING APPROACHES

We consider a 256 × 128-bits array memory, including the memory cells, sense amplifiers, and parasitics, such as wire resistances and wire capacitances in our simulations. The simulation parameters are listed in Table 1. To compare various spintronic memory cells using different WRITE mechanisms, the oxide thickness must be optimized since it affects the READ performances of all the options and the WRITE performances of STT-MRAM and VCEC-MRAM. We will later show that the oxide thickness of SOT-MRAM and ME-MRAM can be optimized especially for the READ operation to take advantage of the separated READ and WRITE paths. As we vary the MTJ oxide thickness, we use the measured resistance–area (RA) product reported in [22].

In addition, to compare the performances of spintronic memory devices in the embedded memory application,

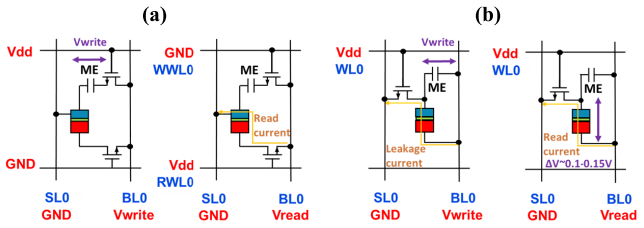

FIGURE 3. Schematic of the ME-MRAM in an array level with (a) one-access transistor or (b) separated access transistors for READ and WRITE operations. (a) 2T1MTJ. (b) 1T1MTJ.

TABLE 1. Modeling parameters used in READ and WRITE operations.

Parameters	Value
Half metal pitch (F)	30 nm
CMOS driving voltage	1V
Transistor resistance@ W=60 nm	5kΩ
Transistor capacitance@ W=60 nm	60 aF
Interconnect capacitance	0.15 fF/um
BL resistance	20.5 Ω/um
WL resistance	53 Ω/um
Magnet damping coefficient α	0.01
Spin injection coefficient β	0.5
Conductivity of the CoFeB	$7.4\times10^5\ \Omega^{-1}\cdot m^{-1}$
Conductivity of the Co	$1.54\times10^6\ \Omega^{-1}\cdot m^{-1}$
Conductivity of the MnGa	$5\times10^5\ \Omega^{-1}\cdot m^{-1}$

we simulate the READ and WRITE performances of SRAM considering that the fin ratio of the pull-down, pass gate, and the pull-up transistors is 1:1:1 using a 16-nm predictive technology model (PTM) established by Arizona State University [23]. The current-latch-based sense amplifier is used to simulate the READ performance of SRAM.

A. READ OPERATION

Following our previous work [15], [16], we use HSPICE to simulate the READ delay and energy with the READ circuit adapted from [24], and the offset voltages of the sense amplifier are chosen to be 50 mV. The READ delay time is estimated as $t_{\mathrm{READ}} = t_{\mathrm{WL}} + t_{\mathrm{sense}}$, where $t_{\mathrm{WL}} = 0.7\ R_{\mathrm{drive}}C_{\mathrm{WL}} + 0.4R_{\mathrm{WL}}\ C_{\mathrm{WL}}$ is the delay time of the word line (WL), and t_{sense} is the delay time of the sense amplifier. Here, R_{drive} is the resistance of the driver that is a 5× minimum-sized inverter, R_{WL} is the interconnect resistance, and C_{WL} is the interconnect capacitance.

The READ energy is estimated as

$$E_{\mathrm{READ}} = 2V_{\mathrm{READ}}I_{\mathrm{bias}}t_{\mathrm{READ}} + E_{\mathrm{WL}} + E_{\mathrm{SA}} \tag{3}$$

where the first term is the Joule heating associated with the currents passing through the controlled and the reference MTJs, $E_{\mathrm{WL}} = (C_{\mathrm{WL}}/N_{\mathrm{bit}} + C_{\mathrm{tran}})V_{\mathrm{READ}}^2$ is the energy dissipation to charge the WL and the associated gate capacitance per cell, and $E_{\mathrm{SA}} = P_{\mathrm{SA}}t_{\mathrm{READ}}$ is the energy dissipation of the output latch of the sense amplifier. P_{SA} is the sense amplifier power, which is estimated to be 0.3 μW based on the previous SPICE simulation results [15]. Note that the READ energy is calculated for a single cell in a row by averaging the READ energy of the selected row per column.

B. WRITE OPERATION

The WRITE delay and energy of a single bit in an array are calculated specifically for each type of memory cells,

TABLE 2. Model dimensions and parameters of various spintronic memory cells.

Memory Types	Size of FM (nm^3)	Thermal Barrier E_b (kT)	Thickness (nm)	M_s (A/m)	K_u (J/m^3)	Critical Current/Field	t_{mag}	Reference
STT	30×30×4.6 (PMA)	60	N/A	3×10^5	6×10^4	$I_C = \frac{2e\alpha K_u V}{\hbar}$	[28]	[13]
VCEC	30×30×4.6 (PMA)	60	N/A	3×10^5	6×10^4	$E_c = 425MV/m$	5, 10, 20 ns	[3]
SOT (W)	15×60×2 (IMA)	40	4	1.2×10^6	0	OOMMF	OOMMF	[14]
SOT ($Au_{0.25}Pt_{0.75}$)	15×60×2 (IMA)	40	4	1.2×10^6	0	OOMMF	OOMMF	[17]
SOT (WTe_2)	15×60×2 (IMA)	40	4	1.2×10^6	0	OOMMF	OOMMF	[18]
SOT ($Bi_{0.9}Sb_{0.1}$)	15×60×2 (IMA)	40	10	10^6	0	OOMMF	OOMMF	[19]
SOT (Bi_xSe_{1-x})	15×60×2 (IMA)	40	4, 8, 16	1.2×10^6	0	OOMMF	OOMMF	[20]
ME	90×50×2(IMA)	-	10-50	-	-	$V_{write} = 0.1\sim0.5V$	1, 2, 5 ns	[21], [22]

as explained in the following. We assume that bits in each row are written simultaneously and calculate the WRITE energy per bit by dividing the WRITE energy of an entire row by the number of cells per row. The parameters that we use and the corresponding references are listed in Table 2.

1) STT-MRAM AND VCEC-MRAM

For both the STT-MRAM and the VCEC-MRAM, the WRITE current passes through the MTJ, and the set and reset are determined by the applied voltage on the BL and the SL. For the set operation, BL is biased to V_{WRITE}, while SL is connected to the ground, and the reset operation is done the other way around. The WRITE access time is estimated as $t_{\text{WRITE}} = t_{\text{WL}} + t_{\text{BL}} + t_{\text{mag}}$ where t_{WL} is the delay time to charge WL, t_{BL} is the delay time to charge or discharge BL, and t_{mag} is the magnet switching time that is calculated by a macrospin model [25]. We have validated the models with the experimental results from [3]. Note that since there are no experimental data available on the magnet switching time of the VCEC-MRAM, three hypothetical values of 5, 10, and 20 ns are considered.

The WRITE access energy is calculated as

$$E_{\text{WRITE}} = I_{\text{WRITE}}^2(R_{\text{BL}}+R_{\text{SL}}+R_{\text{tran}}+R_{\text{MTJ}})\cdot t_{\text{mag}} + (C_{\text{WL}}/N_{\text{bit}}+C_{\text{tran}})V_{\text{dd}}^2 + (C_{\text{BL}}+C_{\text{tran}}/3)V_{\text{WRITE}}^2. \quad (4)$$

The first term is the Joule heating energy associated with the WRITE current (I_{WRITE}) flowing through the corresponding BL, SL, select transistor, and MTJ. The second term is the energy dissipation to charge the WL capacitance and the associated gate capacitance (C_{tran}) to V_{dd}. The last term is the energy dissipation to charge the capacitance associated with the BL and the total capacitance associated with the source/drain of transistors connected to the BL, which is approximately $C_{\text{tran}}/3$ per transistor.

2) SOT-MRAM

We consider four types of SOT materials: 1) heavy metals such as W [26], [27]; 2) alloys such as $Au_{0.25}Pt_{0.75}$ [28]; 3) semimetals such as WTe_2 [29]; and 4) topological insulators such as $Bi_{0.9}Sb_{0.1}$ [30] and Bi_xSe_{1-x} [31]. To perform the WRITE operation, the WRITE access transistor is turned on, and a charge current flows through the SOT channel, which generates a transverse spin current into the MTJ. The ferromagnet shunts a fraction of the current flowing in the SOT channel. This shunt current needs to be accounted for when the conductivity of the magnet is comparable to or smaller than that of the channel. Another factor that affects the current efficiency is the spin transparency at the interface effects, such as spin scattering and spin mixing, which become prominent when the thickness of the SOT material is too thin [32]–[35]. To switch a ferromagnet with perpendicular magnetic anisotropy (PMA) using spin-orbit torque, an external magnetic field is needed to break the symmetry. Other approaches, such as using antiferromagnet/ferromagnet heterostructures [36], wedging the interface [37], or utilizing interlayer exchange coupling [38], have also been proposed. However, much work is needed in this area, and here, we only consider SOT-MRAM with in-plane ferromagnets.

The WRITE access time is estimated as $t_{\text{WRITE}} = t_{\text{WL}} + t_{\text{BL}} + t_{\text{mag}}$, where t_{mag} is calculated by micromagnetic simulations using the Object Oriented MicroMagnetic Framework (OOMMF) [39]. This is because macrospin models tend to overestimate the required currents for spin-orbit switching of ferromagnets since they neglect the domain nucleation and propagation during switching [40]. We also validate our micromagnetic model by comparing it with the magnet switching times reported in the experiments in [26]. The WRITE access energy is then calculated as

$$E_{\text{WRITE}} = I_{\text{WRITE}}^2 (R_{\text{BL}} + R_{\text{SL}} + R_{\text{tran}} + R_{\text{SOT}}) \cdot t_{\text{mag}} + (C_{\text{WL}}/N_{\text{bit}} + C_{\text{tran}})V_{\text{dd}}^2 + (C_{\text{BL}} + C_{\text{tran}})V_{\text{WRITE}}^2 \quad (5)$$

where R_{SOT} is the resistance of the SOT material, and the effective spin-polarized current is $I_S = \hbar/2e(W_{\text{FM}}/t_{\text{SO}})\theta_{\text{SH}}I_C$ and $I_c = I_{c,\text{tot}} \times 1/(1+s)$. Here, $I_{C,\text{tot}}$ is the total charge current flowing through the WRITE access transistor, I_C is the effective charge current flowing through the SOT channel, and the ratio of the shunting current (I_{shunt}) to I_C can be written as

$$s = \frac{I_{\text{shunt}}}{I_c} = \frac{\rho_{\text{SO}}}{t_{\text{SO}}}\frac{t_{\text{FM}}}{\rho_{\text{FM}}} \quad (6)$$

where ρ_{SO} is the resistivity of the SOT material, ρ_{FM} is the resistivity of the ferromagnet, t_{FM} is the thickness of the ferromagnet, and t_{SO} is the thickness of the SOT material. To reduce the current shunting effect, the thickness of the ferromagnet is chosen to be 2 nm except for the case of $Bi_{0.9}Sb_{0.1}$, and a 4-nm-thick MnGa is used. The ratio between the length and the width of the ferromagnet must be increased to four in order to maintain a sufficient energy barrier of $E_b \sim 40$ kT.

3) ME-MRAM

Although current experiments on multiferroic materials have been on micrometer samples, here, we assume that the device lateral dimensions can be scaled down to below 100 nm to

fit in our compact layout designs. We also assume the ME material to be intrinsically an insulator (such as $BiFeO_3$ or Cr_2O_3).

The total WRITE access time is estimated as

$$t_{\text{WRITE}} = t_{\text{WL}} + t_{\text{BL}} + 0.7\,(R_{\text{BL}} + R_{\text{tran}})\,C_{\text{AFM}} + t_{\text{mag}} \quad (7)$$

where C_{AFM} is the capacitance of the antiferromagnet. In this study, C_{AFM} is calculated as $\kappa_{\text{AFM}} \cdot A/d$, where $\kappa_{\text{AFM}} = 40$ is the dielectric constant of $BiFeO_3$ [41], A is the area of $BiFeO_3$, and $d = 30$ nm is the thickness of $BiFeO_3$ thin film. Since there is no experimental report about the switching time of the ferromagnet using the ME effect, we consider three hypothetical t_{mag} values of 1, 2, and 5 ns, which are longer than the theoretical switching time limit from the previous study [42].

The total WRITE access energy of ME-MRAM depends on the WRITE voltage of the ME material as discussed previously. The WRITE voltage depends on the coercive field and the thickness. Ideally, one can make the multiferroic material very thin to achieve low WRITE voltages. However, thin ME layers may suffer from large leakage currents, or they may lose their multiferroic properties. Here, we assume that the ME layer is insulating, and we consider WRITE voltages ranging from 0.1 to 0.5 V. For the case in which $V_{\text{WRITE}} = 0.4\sim0.5$ V, the WRITE access energy is calculated as

$$\begin{aligned} E_{\text{WRITE}} &= V_{\text{WRITE}}^2/\,(R_{\text{BL}} + R_{\text{SL}} + R_{\text{tran}} + R_{\text{MTJ}})\cdot t_{\text{mag}} \\ &\quad + (C_{\text{WL}}/N_{\text{bit}} + C_{\text{tran}})V_{\text{dd}}^2 + (C_{\text{BL}} + C_{\text{tran}})V_{\text{WRITE}}^2 \\ &\quad + C_{\text{AFM}}V_{\text{WRITE}}^2 \end{aligned} \quad (8)$$

For the other case of $V_{\text{WRITE}} = 0.1 \sim 0.3$ V, the WRITE energy is the same as the case of $V_{\text{WRITE}} = 0.4 \sim 0.5$ V except that we need to exclude the first term since there is no leakage current from the MTJ during the WRITE operation.

IV. RESULTS AND DISCUSSION

To compare the READ and WRITE performances of various MRAM options, we first quantify the impact of the MTJ oxide thickness on the READ delay and energy. Next, we calculate the WRITE delay and energy based on the physical models described in Section III and reported experimental parameters. Afterward, we study various tradeoffs to select the optimal oxide thickness and discuss the READ disturb issue for each memory type. Finally, we compare various spintronic memory cells and summarize the pros and cons of each cell in terms of density, READ and WRITE delay, and READ and WRITE energies. Note that while the WRITE mechanism is different for each cell, the READ operation is the same for all options even though the parasitic resistance and capacitance values may vary depending on the layout area and cell design.

A. STT-MRAM

To improve the WRITE speed of STT-MRAM, the number of access transistors is varied from 1 to 4, and the corresponding layouts are shown in Fig. 2. The WRITE current per transistor is kept constant as the MTJ oxide thickness varies such that the magnet switching time remains constant, as shown in Fig. 4(a) (by increasing the WRITE voltage linearly as the MTJ resistance increases). Fig. 4(a) also shows that four

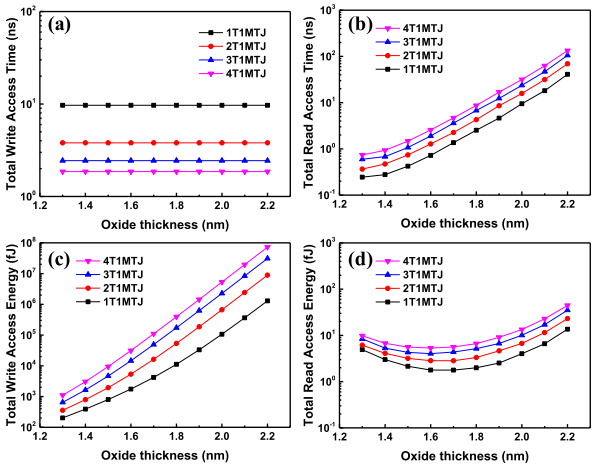

FIGURE 4. (a) and (c) WRITE and (b) and (d) READ performance of STT-MRAM with varying number of access transistors.

access transistors (4T1MTJ) offer the fastest WRITE operation since the magnet switching time is inversely proportional to the overdrive spin-polarized current passing through the free layer. Next, for the WRITE performance, Fig. 4(c) presents that the WRITE energy increases exponentially with increasing oxide thicknesses because of the exponential increase in the resistance. In addition, as the number of access transistors increases, the layout area increases, leading to larger parasitic resistances and capacitances and higher WRITE energy. Similarly, Fig. 4(b) shows that the READ delay also increases with the increase of oxide thickness and the number of access transistors. However, as shown in Fig. 4(d), the READ energy initially decreases with the increase in the oxide thickness because of a larger READ voltage and then increases as the MTJ resistance and the READ time become too large.

A previous study [15] has demonstrated that using an oxide thickness below 1.3 nm may lead to READ disturb issues. To achieve the best tradeoff among fast READ access time and low READ/WRITE access energies, we choose an oxide thickness of 1.3 nm for STT-MRAM. It should be noted that for very large oxide thicknesses (>1.7 nm), the READ current is too low for typical sense amplifiers. Also, the WRITE voltage becomes prohibitively large. Hence, there are practical reasons to avoid such large oxide thicknesses in addition to the very large WRITE/READ energies and delays.

To summarize, using 2T1MTJ for the STT-MRAM provides a minimum WRITE energy-delay product (EDP) at the cost of a small increase in READ and WRITE energies. Note that this 2T1MTJ scheme of STT-MRAM had also been proved to increase WRITE speed in [43].

B. VCEC-MRAM

VCEC-MRAM has the same READ performance as the STT-MRAM for any given oxide thicknesses since they use the same layout designs. For the WRITE operation, we consider three hypothetical magnet switching times (t_{mag}) of 5, 10, and 20 ns due to the lack of physical models or experimental data at this point. The electric field is kept fixed as we increase the oxide thickness such that the magnet switching time is not affected as shown in Fig. 5(a). Fig. 5(b) reveals that the WRITE energy increases with the oxide thickness when the oxide is thicker than 2 nm. This is due to the increase in the

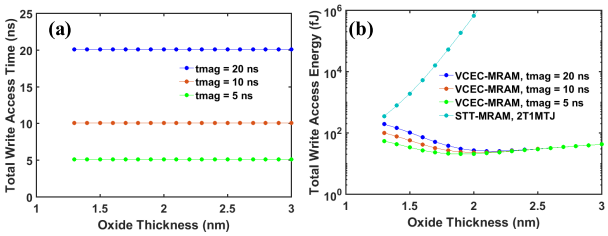

FIGURE 5. (a) WRITE access time with a varying oxide thickness of VCEC-MRAM. (b) Comparison of the WRITE access energy with varying oxide thickness for VCEC-MRAM and STT-MRAM.

WRITE voltage. However, when the oxide thickness is thinner than 2 nm, the WRITE energy again increases because the Joule heating term (E_J)

$$E_J = V_{\text{WRITE}}^2/(R_{\text{BL}} + R_{\text{SL}} + R_{\text{tran}} + R_{\text{MTJ}}) \cdot t_{\text{mag}} \quad (9)$$

becomes dominant compared with the dynamic energy, which is equal to $(C_{\text{BL}}+C_{\text{tran}})V_{\text{WRITE}}^2$. We choose an oxide thickness of 1.6 nm to achieve both low WRITE and READ EDP since the READ delay time increases when the oxide thickness is too thick, as shown in Fig. 4(b).

Next, we compare the WRITE energy of VCEC-MRAM and STT-MRAM in Fig. 5(b). A large reduction in the WRITE energy is evident even for a large t_{mag} of 20 ns. This is because VCEC-MRAM is a voltage-controlled device, and its WRITE voltage increases linearly with the oxide thickness, whereas STT-MRAM is a current-controlled device, and the WRITE voltage increases exponentially with resistance at a constant overdrive current. Note that since VCEC-MRAM is a voltage-controlled device, it only needs a one-access transistor during the WRITE operation, leading to a high cell density. Overall, VCEC-MRAM offers lower WRITE energy, small layout area, and better READ disturb margin compared with STT-MRAM. However, its READ access time is two to three times larger because of the larger MTJ resistance.

C. SOT-MRAM

Fig. 6(a) presents the READ performance of the SOT-MRAM considering one or two WRITE access transistors. The results show that the READ access time increases exponentially with the oxide thickness. The cell with two WRITE access transistors (3T1MTJ) has a higher READ delay time and READ energy compared with the cell with one WRITE access transistor (2T1MTJ) because of the larger footprint area and the larger gate capacitance, which results in a higher *RC* delay.

To study the WRITE operation, we consider four categories of SOT materials: heavy metals, alloys, Weyl semimetals, and topological insulators. Heavy metals, Weyl semimetals, and alloys usually have higher conductivities but lower spin Hall angles, whereas topological insulators are quite resistive but have larger spin Hall angles. Table 3 summarizes important parameters for various SOT materials studied in this work.

From Table 3, Au_xPt_{1-x} has the smallest $s = 0.64$ because it has the lowest resistivity among all the candidates, whereas topological insulators, such as Bi_xSe_{1-x}, have the largest s of 47.34, when the thickness is 4 nm. This is because the thinner Bi_xSe_{1-x} suffers from a more severe current shunting problem. Note that $Bi_{0.9}Sb_{0.1}$ has an exceptionally high bulk conductivity $\sigma = 2.5 \times 10^5 \Omega^{-1}\text{m}^{-1}$, which is comparable to the

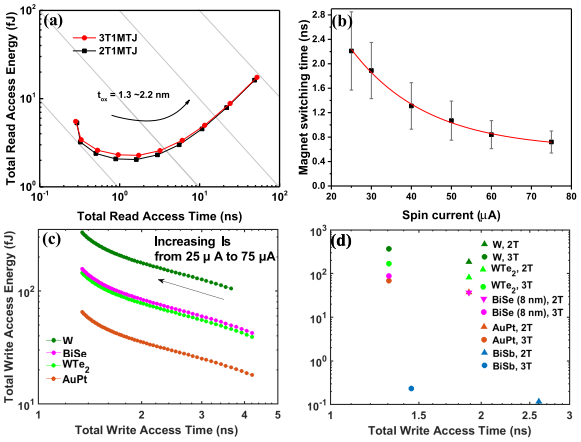

FIGURE 6. (a) READ access energy versus the READ access time of the SOT-RAM. (b) Switching time of a 60-nm-long, 15-nm-wide, and 2-nm-thick ferromagnet with varying spin current after 100 tests. (c) WRITE access energy versus WRITE access time when spin current increases from 25 to 75 μA. (d) Comparison of the WRITE energy and delay time of various SOT materials using optimum WRITE voltages.

conductivity of the ferromagnet MnGa $\sigma = 5 \times 10^5 \Omega^{-1}\text{m}^{-1}$; hence, a small shunting factor $s = 0.8$ is obtained.

Next, to evaluate the charge to spin conversion efficiency without considering the current shunting problem, the spin conductivity σ_s is used, which is expressed as the product of conductivity and θ_{SH}. Our calculations show that $Bi_{0.9}Sb_{0.1}$ with a high σ and θ_{SH} has the highest σ_s. Moreover, we incorporate the current shunting effect, as shown in Fig. 7 by considering the normalized WRITE current flowing through the SOT channel, which is defined as $I_{\text{WRITE,nor}} = (s+1)t_{\text{SO}}/(\theta_{\text{SH}}W_{\text{FM}})$. It is noticed that $Bi_{0.9}Sb_{0.1}$ still shows the lowest $I_{\text{WRITE,nor}}$, and a 4-nm-thick Bi_xSe_{1-x} shows the second lowest $I_{\text{WRITE,nor}}$. However, if we compare the ratio of the READ current I_{READ} to the WRITE current I_{WRITE}, we find that I_{READ} is 4× larger than I_{WRITE} for the case of $Bi_{0.9}Sb_{0.1}$. Generally, $I_{\text{READ}}/I_{\text{WRITE}}$ should be lower than 0.1 such that there is enough margin to separate the READ and WRITE operations. The READ current is typically on the order of a few μA. In the case of $Bi_{0.9}Sb_{0.1}$, the READ current flowing through the MTJ and the topological insulator may generate a spin current as large as 100 μA, which could flip the free layer ferromagnet. Therefore, $Bi_{0.9}Sb_{0.1}$ may not be a suitable candidate for real applications. Finally, to compare the total WRITE energy of these SOT materials, we calculate the normalized $RI_{\text{WRITE,nor}}^2$, where R includes the resistance of ferromagnet and SOT channel following the layout design in Fig. 1(b). Table 3 indicates that Au_xPt_{1-x} has the second-lowest normalized WRITE energy and the second-lowest $I_{\text{READ}}/I_{\text{WRITE}}$ of 0.06. Note that even though 4-nm-thick Bi_xSe_{1-x} has the second-lowest $I_{\text{WRITE,nor}}$, it has a higher SOT channel

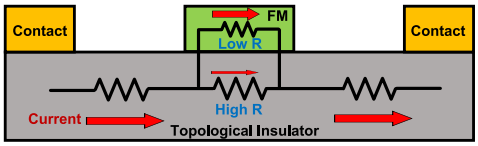

FIGURE 7. Schematic of the current shunting problem in SOT-MRAM using a topological insulator.

TABLE 3. Comparison of various materials for SOT-MRAM.

Class of Materials	Materials	σ ($\Omega^{-1}\cdot m^{-1}$)	s	θ_{SH}	$\sigma_s = \theta_{SH}\cdot\sigma$ ($\Omega^{-1}\cdot m^{-1}$)	Normalized I_{write} ($I_{write,nor}$)	Normalized $RI_{write,nor}^2$	I_{read}/I_{write}
Heavy Metal	β-W (4 nm)	3.85×10^5	0.96	0.2	7.7×10^4	19.6	3.43×10^5	0.03
Alloy	Au_xPt_{1-x} (4 nm)	1.2×10^6	0.64	0.35	4.22×10^5	9.37	2.55×10^4	0.06
Weyl Semimetal	WTe_2 (4 nm)	2.5×10^5	1.48	0.4	10^5	12.4	2.07×10^5	0.07
Topological Insulator	Bi_xSe_{1-x} (4 nm)	7.8×10^3	47.34	18.62	1.45×10^5	5.19	1.08×10^6	6.43
	Bi_xSe_{1-x} (8 nm)	4.65×10^4	3.97	2.88	1.34×10^5	6.91	1.67×10^5	0.26
	Bi_xSe_{1-x} (16 nm)	6.13×10^4	1.51	1.56	9.56×10^4	12.9	2.27×10^5	0.07
	$Bi_{0.9}Sb_{0.1}$ (4 nm)	2.5×10^5	0.8	52	1.3×10^7	0.09	4.16	4.49

resistivity compared with Au_xPt_{1-x}; thus, it generally has larger WRITE energy. Also, while the 4-nm-thick Bi_xSe_{1-x} channel offers higher spin conductivity compared with the 8-nm-thick Bi_xSe_{1-x} channel, it suffers from very poor resistivity, which results in a higher energy dissipation due to the large voltage drop across the channel.

To further evaluate the total WRITE performance of various SOT candidates in an array, the optimal WRITE voltages or WRITE currents are calculated to achieve the minimum WRITE EDP for each option. The magnet switching time of a 60-nm-long, 15-nm-wide, and 2-nm-thick ferromagnet with varying spin currents after 100 tests are simulated in OOMMF marked as black squares in Fig. 6(b). Next, we fit the sample data at each WRITE voltage under thermal noise ($T = 300$ K) and extract the switching time based on three times a standard deviation above the median value. With varying applied WRITE voltages, the corresponding magnetization switching time is fit to calculate the total WRITE access energy. Fig. 6(c) shows that Au_xPt_{1-x} and 8-nm-thick Bi_xSe_{1-x} have lower WRITE energy compared with W and WTe_2 when I_S varies from 25 to 75 μA. We then use the optimal WRITE voltages to calculate the total WRITE access time versus the total WRITE energy, as shown in Fig. 6(d). Similar to the calculation that we discuss in Table 3, $Bi_{0.9}Sb_{0.1}$ has the lowest WRITE energy and WRITE delay time, but it suffers from the READ disturb issue. It is interesting to note that while Au_xPt_{1-x} offers a spin conductivity almost three times larger than 8-nm-thick Bi_xSe_{1-x}, the two channels offer almost similar WRITE energies at the array level. This is because of the smaller current needed in the case of Bi_xSe_{1-x}, which results in smaller voltage drop and energy dissipation in the select transistor and the BL. This fact highlights the need for array-level evaluations of various materials.

We then quantify the WRITE performances of SOT-MRAM when the number of WRITE access transistors increases from one to two such that the total spin current is doubled. It can be seen in Fig. 6(d) that the WRITE delay time goes down when the number of WRITE access transistors increases, but the WRITE energy increases by 2× because of the larger layout area, larger gate capacitances, and longer interconnects. Overall, the WRITE EDP of the two WRITE access transistor case is larger than the one-access transistor case. Therefore, using one WRITE access transistor (2T1MTJ) is better for SOT-MRAM in terms of area and WRITE energy efficiency.

D. ME-MRAM

For the ME-MRAM, we consider the READ delay and energy with two different numbers of access transistors, as shown in Fig. 8(a). The results show that both the READ delay and energy increase as the number of access transistors increased because of the larger layout area and the associated higher

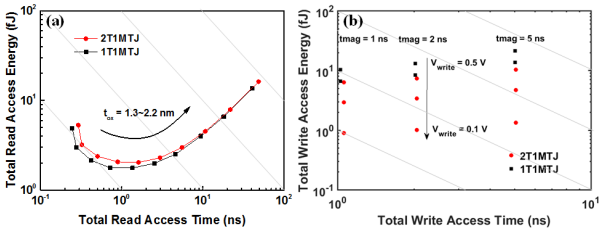

FIGURE 8. (a) WRITE access time and (b) WRITE access energy with a varying oxide thickness of ME-MRAM.

RC delay. To reduce the READ EDP, we choose the oxide thickness to be 1.4 nm. For the WRITE operation, we consider hypothetical magnet switching delay of 1, 2, and 5 ns. Similarly, the WRITE voltage of the ME material is assumed to vary from 0.1 to 0.5 V. Fig. 8(b) illustrates that the WRITE access energy is dominated by the WRITE voltage that charges or discharges BL and SL since there is no charge current flowing through the MTJ. For $V_{\mathrm{WRITE}} = 0.4\sim0.5$ V, the WRITE access time is smaller than the case of $V_{\mathrm{WRITE}} = 0.1\sim0.3$ V because of the smaller layout area. Overall, the WRITE access energy of the ME-MRAM can be reduced to a few femtojoules if the WRITE voltage is as small as 0.1 to 0.2 V.

E. COMPARISON OF THE READ AND WRITE PERFORMANCE OF SPINTRONIC MEMORY CELLS

Using the optimal oxide thickness and WRITE voltage for each type of memory cell, we compare the READ and WRITE performances of various devices. Fig. 9 shows that STT-MRAM has higher WRITE access energy compared with other spintronic memory cells. Although the READ access energy of the STT-MRAM is small in the 1T1MTJ case, its WRITE delay is large, and 2T1MTJ is a better option when the WRITE speed is a primary concern, as seen in the literature [43]. The VCEC-MRAM shows much lower WRITE access energy compared with STT-MRAM, especially when the magnet switching time is fast. The READ access energy of VCEC-MRAM is also small because of its small footprint area, but the READ delay time is larger because of a thicker oxide. SOT-MRAM can offer smaller WRITE delay and energy values than those of STT-MRAM, as seen in [10] and [14]–[17]; however, the READ delay time is longer, and the layout area is larger than STT-MRAM since SOT-MRAM is a three-terminal device. Furthermore, SOT-MRAM using alloy SOT channels presents the lowest WRITE energy among all the SOT materials since it has a larger spin Hall angle compared with heavy metals and Weyl semimetals and higher conductivity compared with topological insulators, leading to a weaker current shunting effect. ME-MRAM has a potentially small WRITE access energy and higher cell density compared with other candidates. Because of the small footprint

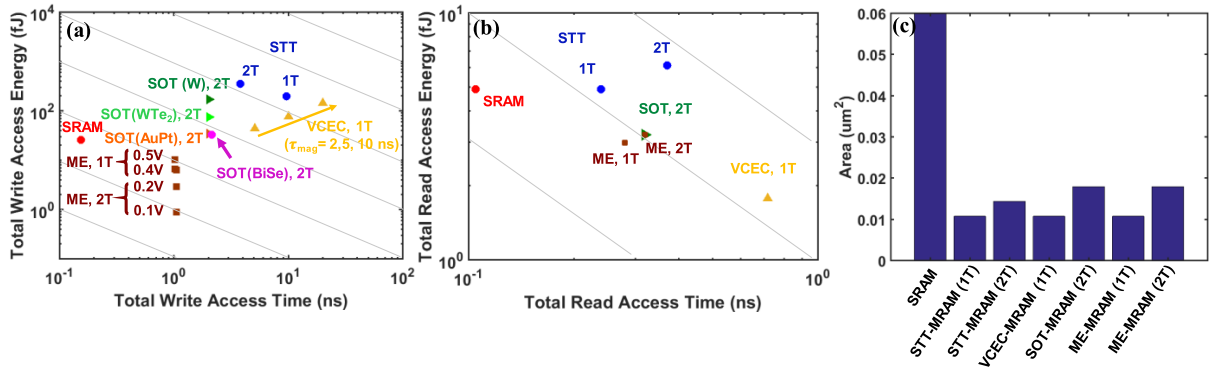

FIGURE 9. Total (a) WRITE and (b) READ performance and (c) layout area of various spintronic memory cells.

TABLE 4. Comparison of various spintronic memory cells and SRAM.

Memory Types	SRAM	STT	VCEC	SOT	ME
Area (F^2)	120	16	12	20	12
E_{write} (fJ)	26.36	357.22	43.95	15.13	10.38
t_{write} (ns)	0.15	3.80	5.13	1.39	1.03
E_{read} (fJ)	4.93	6.15	1.78	3.22	2.99
t_{read} (ns)	0.11	0.37	0.72	0.32	0.28

area, the READ access energy of ME-MRAM can be as low as that of the VCEC-MRAM when the same oxide thickness is used. Overall, voltage-controlled devices, such as VCEC-MRAM and ME-MRAM, have lower WRITE access energy and also lower READ access energy because of their thicker oxide thicknesses and small footprints compared with other devices.

Finally, we perform a comprehensive benchmarking for all spintronic devices investigated in this article and CMOS SRAM in terms of the READ and WRITE performances. Fig. 9 shows that SRAM still offers the fastest WRITE and READ delay because it is a charge-based device with positive feedback, whereas spintronic memory devices have slow WRITE and READ operations because of the precessional switching behavior of ferromagnets and their inherently low TMR ratio. Nevertheless, SRAM consumes more energy and area compared with the spintronic memory devices, including STT-MRAM with 2T1MTJ, VCEC-MRAM, SOT-MRAM using $Au_{0.25}Pt_{0.75}$, and ME-MRAM with $V_{WRITE} = 0.5$ V, as shown in Table 4. Our results exhibit that spintronic memory devices using novel physical mechanisms, such as VCEC-MRAM, SOT-MRAM, and ME-MRAM, are promising options to be used in the last level of cache because of the nonvolatility, low WRITE and READ energies, and smaller layout area.

It is important to note that the studied MRAM technology options are at different levels of maturity. SOT-MRAM using β-W as the SOT channel has been successfully fabricated in 55-nm CMOS technology with a thermal budget of 400 °C [44]. Therefore, SOT-MRAM is a promising candidate that may be adopted in the near future. On the other hand, VCEC-MRAM and ME-MRAM that offer the largest benefits in terms of density and possibly energy are still at the early stages of research and may be considered as long-term potential candidates.

V. CONCLUSION

In this article, a comprehensive modeling and optimization framework for various current- and voltage-controlled magnetic memory devices is presented based on experimentally validated physical models considering a range of recently reported materials and devices. For material choices of SOT-MRAM, our cross-layer optimization and benchmarking highlight that common metrics, such as the spin Hall conductivity (σ_s) and normalized WRITE current ($I_{WRITE,nor}$), may not be sufficient. For instance, Au_xPt_{1-x} offers a spin conductivity more than three times larger than 8-nm-thick Bi_xSe_{1-x}. However, the two-channel materials offer almost similar WRITE energies at the array level. This is because of the smaller current needed in the case of Bi_xSe_{1-x}, which results in smaller voltage drop and energy dissipation in the select transistor and the bitline. The extraordinarily high spin Hall efficiency reported for $Bi_{0.9}Sb_{0.1}$ and its high electrical conductivity result in a very high spin conductivity. However, the very low WRITE current can cause high READ disturb rates. A 4-nm-thick Bi_xSe_{1-x} layer offers a very large spin Hall angle but suffers from large current shunting effects because of its high resistivity and is not a promising option. In general, alloys with large spin Hall angles and high conductivity are promising SOT channel materials.

The design of the ME-MRAM cell can be simplified from 2T1MTJ to 1T1MTJ if the WRITE voltage of the ME layer is adequately larger than the READ voltage, which is typically around 0.1–0.2V. Hence, there is a tradeoff between memory density and WRITE energy. The benchmarking results show that SOT-MRAM can be fast and low energy but would suffer from a 25% larger cell area compared with STT-MRAM. VCEC-MRAM can be denser than STT-RMAM (2T1MTJ) and dissipate less energy but would suffer from slower READ operations because of its large oxide thickness. ME-MRAM can be fast, low energy, and dense compared with all other options. Although spintronic memory devices have slower WRITE and READ operations compared with SRAM, the characteristics of nonvolatility and smaller layout area make them promising options for memory applications.

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