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Hybrid-Phase-Transition FET Devices for Logic Computation

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ABSTRACT Hybrid-phase-transition FETs (HyperFETs), built by connecting a phase transition material (PTM) to the source terminal of a FET, are able to increase the ON-to-OFF current ratio. In this article, we describe a comprehensive study carried out to explore the potential of these devices for low-power and energy-limited logic applications. HyperFETs with different ON–OFF current tradeoffs are evaluated at the circuit level. The results show limited improvement over conventional transistors in terms of power and energy. However, based on this analysis, this article proposes different design techniques to overcome the drawbacks identified in the study and thereby make better use of HyperFETs. Hybrid circuits, using both FinFETs and HyperFETs, and circuits combining different HyperFET devices are introduced and evaluated. At some frequencies, reductions of over 40% were obtained with respect to FinFET-only implementations, while minimum energy per operation values were obtained, which were lower than those achieved with low standby power (LSTP) FinFETs and high-performance (HP) FinFETs. This article also evaluates the impact of PTM transition time on the power performance of HyperFET circuits.

INDEX TERMS Device-circuit codesign, hybrid-phase-transition FET (HyperFET), low power, phase transition devices, steep-slope devices.

I. INTRODUCTION

CMOS technology has power density and energy inefficiency limitations associated with the minimum subthreshold slope (SS) of CMOS transistors (SS $>$ 60 mV/decade). This makes it impossible to achieve efficient tradeoffs between low threshold voltages and acceptable leakage currents that could allow supply voltage to be reduced without degrading circuit speed. Research is being carried out into steep SS devices to overcome these limitations. Hybrid-phase-transition FET (HyperFET) transistors are steep-slope devices built by connecting a phase transition material (PTM) to the source terminal of a FET (see Fig. 1). The abrupt insulator–metal transitions of the PTM are used as a mechanism to boost the ratio of the ON current (I_{ON}) to the OFF current (I_{OFF}) [1], thereby achieving a steep SS.

Several experimental HyperFETs with SS $<$ 60 mV/decade have been reported [2]–[4]. Researchers are beginning to look at specific HyperFET features to enhance specific circuit topologies [5], [6] and implementing nonconventional computing paradigms [7], [8].

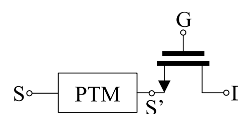

FIGURE 1. HyperFET transistor.

In conventional logic computation, two different scenarios are possible. PTMs can be combined with conventional FETs to reduce their leakage (OFF) current without significantly reducing their ON currents or the HyperFET can be designed to increase the ON current by lowering the threshold voltage of its intrinsic transistor with respect to conventional FETs while avoiding excessive I_{OFF} due to the high resistance of the PTM in the insulating state. Clearly, different tradeoffs are possible. Evaluation of devices at the circuit level is critical to provide guidance for device design. Up to now, this has been addressed only in a small number of studies and, even then, with some limitations.

In [9], a preliminary circuit experiment was carried out using a HyperFET with an I_{ON} larger than that of its intrinsic FinFET transistor and similar I_{OFF} (iso-I_{OFF}). The authors

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reported using a ring oscillator that, with appropriate materials selection and design, allowed Hyper-FETs to have 25%–68% less iso-delay power at low-voltage operation. With this experimental setup, however, it was impossible to explore the impact of key parameters, such as the circuit's operating frequency or switching activity profile.

In [10] and [11], experiments were performed, which demonstrated the impact of these two factors. In this case, a HyperFET with an I_{OFF} lower than that of its intrinsic FinFET and similar I_{ON} (iso-I_{ON}) was evaluated. The power savings obtained were found to be smaller than those expected from device-level estimations, or even power penalties were found in low output switching activity sceneries, due to the degraded dc output voltages (different from the supply and zero voltage) exhibited by HyperFET transistors [9].

In this article, a more comprehensive experiment was carried out with HyperFETs. Several HyperFET devices with different I_{ON}–I_{OFF} tradeoffs were evaluated. Both the iso-I_{ON} and the iso-I_{OFF} analyzed in previously mentioned articles were included in the study along with others to provide guidelines that could be useful for device design. They were also analyzed with an identical experimental setup. Because of the high impact of switching activity on power results reported in [10] and [11], the evaluations were done at the circuit level so that a realistic switching activity profile could be used.

The rest of this article is organized as follows. Section II provides some background on HyperFET transistors and their operation. Section III describes the devices and circuits used in our experiments. Section IV reports and analyses the results obtained for power and energy. Section V proposes the hybrid HyperFET circuits to improve power performance. Finally, some conclusions are given in Section VI.

II. BACKGROUND

A. HyperFET DEVICE

The HyperFET transistor is built by adding a PTM to the source terminal of a conventional, or host, transistor, as shown in Fig. 1.

PTMs tend to stabilize in the insulating phase with no electrical stimuli. When a voltage is applied, the current circulating through the PTM increases, as can be seen in the I–V curve in Fig. 2. When the current density (J_{IMT}) is sufficiently high, insulator-to-metal transition (IMT) occurs. Because of the large reduction in PTM resistivity, the current then rises abruptly. Increasing the applied voltage further again produces an increment in the current.

Likewise, reducing the applied voltage produces a linear decrease in the current. When the current density (J_{MIT}) is sufficiently low, metal-to-insulator transition (MIT) takes place.

The I–V characteristic of the PTM device shown in Fig. 2 was obtained with a Verilog-A model inspired by the macromodel proposed in [12] (denoted as "PTM-Sim" in this article) and conforms very well to the curve provided in this reference. According to [12], the critical currents and the resistivity ratio are of the same order of magnitude than single-crystal VO_2. The physical properties of the PTM-Sim and the electrical parameters of its model are shown in Table 1. V_{IMT} (V_{MIT}) is the voltage at which the IMT (MIT) transition occurs. These electrical parameters were calculated from the material and geometrical properties of the PTM-Sim device. Note the 10^5 ratio between the two resistance values. Since MIT and IMT transitions are abrupt but not instantaneous, a transition time (TT) was considered using the value reported in [9], together with a parasitic capacitance C in parallel with the PTM terminals.

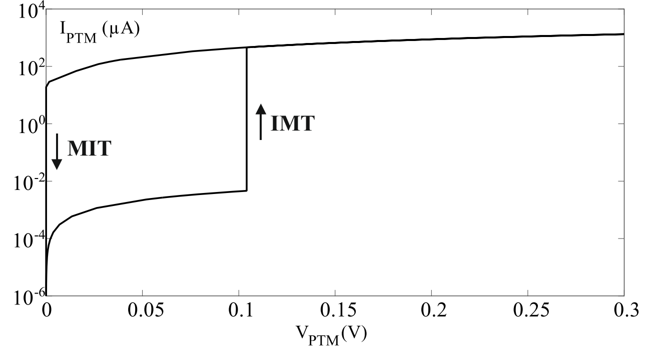

FIGURE 2. Current–voltage characteristic of a PTM reported in [12] (PTM-Sim).

TABLE 1. Parameters of the PTM device.

PTM parameters			
Physical		*Electrical*	
ρ_{INS}	100Ω•cm	R_{INS}	22.6MΩ
ρ_{MET}	0.001Ω•cm	R_{MET}	226Ω
$J_{C,MIT}$	8000A/cm^2	V_{MIT}	16μV
$J_{C,IMT}$	520A/cm^2	V_{IMT}	104mV
L	20nm	C	1fF
A	42•21nm^2	TT	50ps

With the HyperFET, when the host transistor is in the OFF state, the small current flowing through the HyperFET forces the PTM into the insulating state. The effective gate-to-source and drain-to-source voltages ($V_{GS'}$ and $V_{DS'}$, respectively, in Fig. 1) seen by the intrinsic transistor are thus reduced and I_{OFF} is also decreased. When the gate-to-source voltage is increased, the current through the HyperFET also rises, switching the PTM to the metallic state. For a sufficiently low PTM resistance in the metallic state, I_{ON} of the HyperFET is almost equal to that of the intrinsic transistor.

Correct tuning of the PTM and the intrinsic transistor is critical to achieve the operating principle described earlier for the HyperFET and to boost the current ratio. In [12], the PTM-Sim was combined with a predictive 14-nm high-performance (HP) FinFET transistor (model available from [13]). Fig. 3 shows the I–V characteristic of three different transistors: 1) the abovementioned 14-nm HP FinFET transistor (FinFET); 2) a HyperFET built from that same transistor using the PTM-Sim (HyperFET E); and 3) a HyperFET built from the PTM-Sim and the 14-nm HP FinFET but with

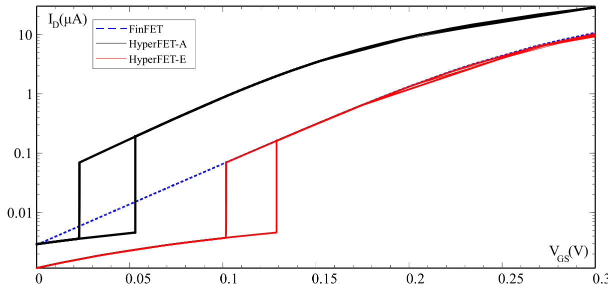

FIGURE 3. Current–voltage characteristic of the simulated FinFET and its iso-I_{ON} and iso-I_{OFF} HyperFET counterparts.

reduced threshold voltage (HyperFET A). Note that one of the HyperFETs (E) is iso-I_{ON} with the stand-alone HP FinFET and the other one (A) is iso-I_{OFF}.

B. HyperFET CIRCUITS

1) IDEAL OPERATION OF HyperFET LOGIC GATES

Fig. 4(b) shows the waveforms for the HyperFET inverter shown in Fig 4(a). A load capacitance of 10 fF has been included in the simulation. The two waveforms at the bottom represent the state of each of the PTMs in the inverter. The one corresponding to the p-type HyperFET is denoted "STATE P" and the one corresponding to the n-type HyperFET is denoted "STATE N". The lower levels mean the PTM is in the metallic state (MET), and the higher levels indicate that it is in the insulating state (INS). During transitions, a single PTM—the p PTM for rising output transitions and the n PTM for falling output transitions—switches to the metallic state. Once the output transition has taken place, the current decreases and the PTM that switched to the metallic state switches back to the insulating state. With both PTMs in the insulating state, static/leakage currents decrease.

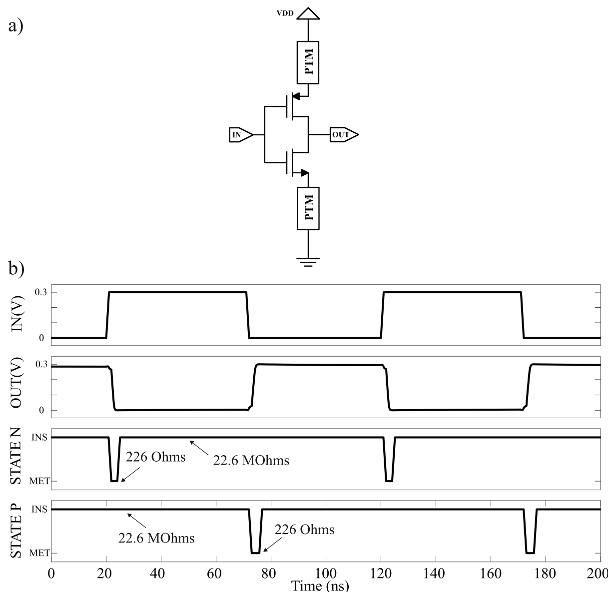

FIGURE 4. HyperFET inverter. (a) Schematic. (b) Waveforms of the input–output and states of the PTMs of the p and n HyperFETs.

This operating principle for logic gates has advantages in terms of power for both of the newly introduced HyperFETs. For the iso-I_{ON} HyperFET, the power savings are associated with reductions in static leakage current. For the iso-I_{OFF} HyperFET, savings could be achieved due to the reductions in supply voltage facilitated by the larger ON current available during transitions. However, HyperFET logic gates deviate from this ideal operating principle because of the different reasons described below.

2) DEVIATIONS FROM IDEAL BEHAVIOR

First, it is known that static logic voltages associated with logic 0 and logic 1 are not Ground and V_{DD} [9]. To illustrate this, Fig. 5(a) shows the voltage transfer characteristic for both a HyperFET inverter (blue solid line) and a single-transistor inverter (FinFET, red dashed line). $V_{DD} = 0.3$ V was used. The differences can clearly be seen. The output voltage for IN equal to 0 V (0.3 V) is not 0.3 V (0 V), as it is in the FinFET inverter. The dc voltage for logic 1 (logic 0) output is determined by R_{INS} of the PTM and the I_{OFF} current of the p (n) transistor. The larger I_{OFF}, the more the voltage drops in the PTM and, therefore, the greater the deviation from the ideal voltages associated with the logic values.

Note that no degradation of voltage levels can be seen in Fig. 4(b) because it takes some time to reach the static state. Degradation occurs at lower input switching rates than the one applied in that figure.

Static voltages are further degraded when gates are connected [11]. This is shown in Fig. 5(b), which shows the static logic 1 and logic 0 voltage levels as observed through a 15-stage inverter chain.

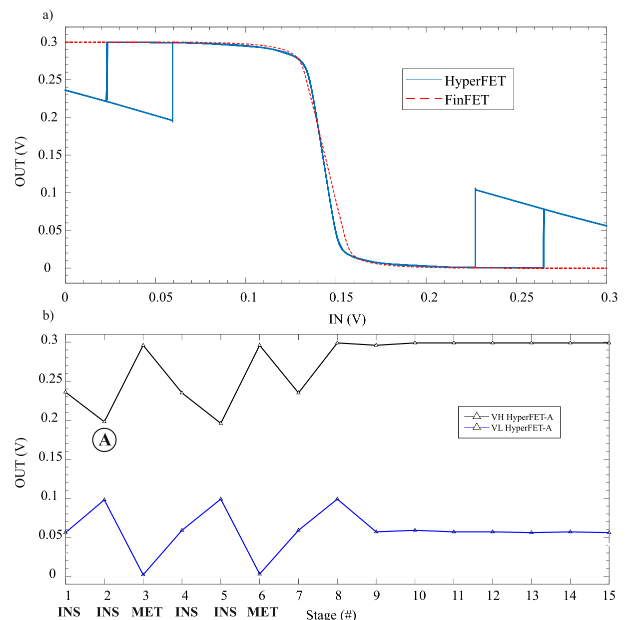

FIGURE 5. *I–V* characteristic of the five HyperFET devices and the FinFET. (a) Voltage transfer characteristic of the HyperFET inverter. (b) Voltage level degradation of the output of each gate of a fifteen-stage chain of HyperFET inverters.

TABLE 2. Parameters of each simulated HyperFET transistor.

Parameter	*H-A*	*H-B*	*H-C*	*H-D*	*H-E*
L (nm)	21	21	18	21	18
$\lvert\Delta V_{TH}\rvert$ (mV)	110	90	60	60	0

Deviations from the ideal operating principle translate into power and speed penalties [11]. There are different reasons for this, which is given in the following.

1) On the one hand, power overheads are caused because, due to the degraded input voltage seen by embedded gates, the gates' PTMs operate in metallic state in the static state. This can be seen in Fig. 5(b). For example, the very much degraded dc high output voltage in Stage 2 (labeled A) causes the PTMs in the next gate to work in the metallic state. Note that 0 V is the dc low output voltage in Stage 3, which is only possible if the PTM associated with its n transistor is in the metallic state. This is why static power does not decrease as expected.
2) On the other hand, static power increases with respect to conventional circuit counterparts because of the voltage levels seen at the gate inputs, which, as has been explained, are not Ground and V_{DD}.
3) Degraded static voltage levels also impact circuit speed. This impact can be both positive and negative. There are advantages in terms of reduced logic swing, but at the same time, available currents decrease and therefore so does speed.

Also, gate delays do not depend exclusively on the transistor's I_{ON} current. The position of the IMT transition is critical. Note that, before that transition occurs, the HyperFET current is significantly lower than in its host transistor. This translates into speed degradation for circuits built with the iso-I_{ON} HyperFET. For iso-delay operations, the supply voltage must be raised, therefore lessening the expected power reductions. Speed is also determined by the TT of the PTM.

In summary, although ideally the larger I_{ON}–I_{OFF} ratio displayed by HyperFETs in relation to conventional transistors has the potential for reducing power, several factors limit the improvement that can actually be achieved in power values. In this article, since it was not easy to analytically evaluate the final power results with so many interrelated factors involved, a set of HyperFETs with different characteristics were evaluated.

III. DEVICE AND CIRCUIT DESCRIPTIONS

We evaluated five different n and p HyperFETs built from the PTM-Sim device and the 14-nm HP FinFET, but with different reduced threshold voltages and channel lengths, as detailed in Table 2. Fig. 6 shows the I–V characteristic of the n devices at $V_{DS} = 0.3$ V. As a reference, a minimum length single FinFET was considered. All transistors had two fingers.

Note that HyperFET-A and HyperFET-E are, respectively, the iso-I_{OFF} and iso-I_{ON} transistors discussed in Section II. The other three represent different I_{ON}–I_{OFF} tradeoffs. HyperFET-A had the highest I_{ON} current and HyperFET-E had the lowest I_{ON} and I_{OFF}. Note that hysteresis shifts to the left when I_{ON} increases.

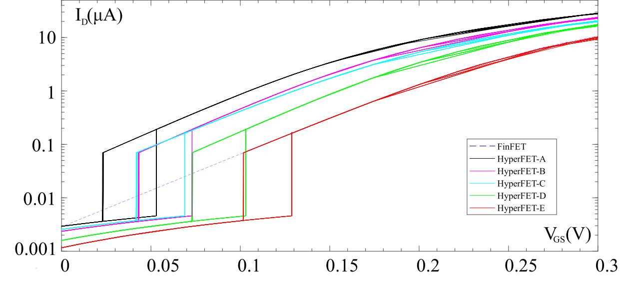

FIGURE 6. ***I–V*** **characteristic of the five HyperFET devices and the FinFET.**

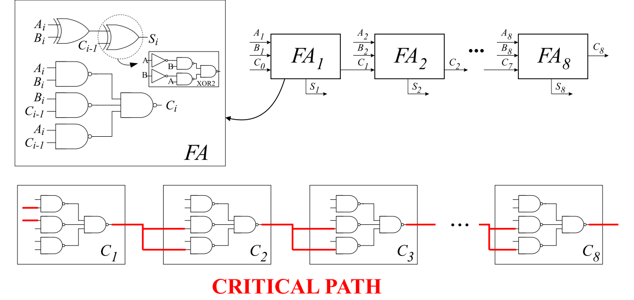

FIGURE 7. Logic diagram of an 8-bit RCA. Gate level description of the FA has also been included.

An 8-bit ripple carry adder (RCA) was chosen for our experiments. Fig. 7 shows its architectures and the logic implementation of the full adders (FAs). The figure shows how the RCA was built from inverters, two-input NAND gates, and three-input NAND gates. Although it was possible to implement the FAs more compactly, the implementation used was suitable for the comparison experiments which were the aim of this article.

To evaluate the HyperFETs fairly, iso-delay experiments were necessary. Power comparisons at equal supply voltages were not suitable because the I_{ON} values of four of the analyzed HyperFETs were higher than that of the reference FinFET, and therefore, the potential of the HyperFETs to operate at lower supply voltages had to be considered. Neither could the iso-I_{ON} HyperFET power comparison be carried out at equal supply voltages. As it has already been explained, this transistor has a lower current than the FinFET for low gate-to-drain voltages, and so, circuits incorporating it were expected to require larger supply voltages than FinFET circuits.

It was also important to select the minimum and maximum supply voltages allowed for the different devices. We chose 100 mV as the minimum allowed logic swing. For the FinFETs, this was, therefore, the minimum V_{DD} value used. For the HyperFETs, since static logic voltages are not Ground and V_{DD} ([see Fig. 5(b)], 300 mV was used. The maximum V_{DD} for the HyperFETs was limited to 0.6 V. This value was chosen based on the transistor's I–V characteristic. Over that voltage, the MIT transition disappears in some of the devices.

IV. EVALUATION OF HyperFET CIRCUITS

The critical path of the RCAs (see Fig. 7) was simulated to determine the minimum supply voltage required to enable operation at different target frequencies. Table 3 shows the results obtained. Note that for HyperFET D and HyperFET E, supply voltage cannot be reduced because of the different minimum supply voltages allowed for HyperFETs and FinFETs. HyperFETs A–C had frequency ranges in which lower supply voltages were required than in the HP FinFET (the shaded cells) and so power savings could be obtained. However, these reductions disappeared when the frequency was increased, due to the effect of the PTM TT. Note the frequencies up to the point for which no HyperFET supply voltage reductions were reported.

TABLE 3. RCA supply voltage versus target frequencies.

	VDD (V)						
f(MHz)	**H-A**	**H-B**	**H-C**	**H-D**	**H-E**	**HP FinFET**	**LSTP FinFET**
0.01	0.300	0.300	0.300	0.300	0.300	0.100	0.175
0.1	0.300	0.300	0.300	0.300	0.300	0.100	0.250
0.5	0.300	0.300	0.300	0.300	0.300	0.100	0.325
1	0.300	0.300	0.300	0.300	0.300	0.100	0.350
2	0.300	0.300	0.300	0.300	0.300	0.125	0.350
5	0.300	0.300	0.300	0.300	0.300	0.175	0.450
20	0.300	0.300	0.300	0.300	0.300	0.225	0.450
50	0.300	0.300	0.300	0.300	0.300	0.275	0.500
100	0.300	0.300	0.300	0.300	0.350	0.300	0.550
150	0.300	0.300	0.325	0.350	0.400	0.350	0.575
200	0.325	0.350	0.375	0.375	0.425	0.375	0.625
250	0.350	0.400	0.425	0.425	0.500	0.400	0.650
300	0.425	0.45	0.475	0.5	0.55	0.425	0.7

The average total power was then measured using the V_{DD} values in Table 3 and the long random input stimulus. Table 4 shows the results obtained. It is interesting to note that the low standby power (LSTP) FinFET was the best up to 1 MHz, with huge power savings compared with the HP FinFET at the lowest frequencies. For example, it consumed just 1% of the HP FinFET power at 10 kHz.

Fig. 8 shows the previous average HyperFET power values normalized with respect to the HP FinFET (dashed line).

The lowest frequencies are shown in Fig. 8(a). Note that a logarithmic scale was used to be able to accommodate the large ratios obtained for some of the HyperFETs. It can be seen that none of the HyperFET devices were advantageous in terms of power. Normalized values were over 1 for all of them. Power overheads were significantly lower for HyperFETs D and E than for the others.

Note also that normalized values of over 100 were obtained for devices A–C. For D and E, the penalties were due to the larger supply voltages that they used in comparison with the FinFET and to the degraded voltage levels at their gate inputs. For these low frequencies, supply voltage differences are important because of the different minimum values allowed for each technology, as previously explained. Larger supply voltages override the power savings expected from the reduced leakage current in these devices.

TABLE 4. Average power consumption of the HyperFET designs.

	P (µW)						
f(MHz)	**H-A**	**H-B**	**H-C**	**H-D**	**H-E**	**HP FinFET**	**LSTP FinFET**
0.01	4.138	2.224	1.854	0.0822	0.0530	0.0175	0.0001
0.1	4.047	2.182	1.824	0.0826	0.0538	0.0177	0.0010
0.5	3.663	1.959	1.677	0.0846	0.0575	0.0183	0.0080
1	3.315	1.694	1.505	0.087	0.062	0.019	0.018
2	2.810	1.218	1.199	0.094	0.072	0.028	0.037
5	2.125	0.798	0.792	0.124	0.107	0.062	0.105
20	1.267	0.447	0.495	0.326	0.308	0.212	0.602
50	1.195	0.840	0.859	0.767	0.736	0.659	1.866
100	1.852	1.582	1.570	1.509	2.024	1.473	4.541
150	2.533	2.327	2.764	3.123	4.052	2.958	7.463
200	3.934	4.273	5.020	4.814	6.142	4.498	11.821
250	5.640	7.122	8.159	7.840	10.830	6.388	16.034

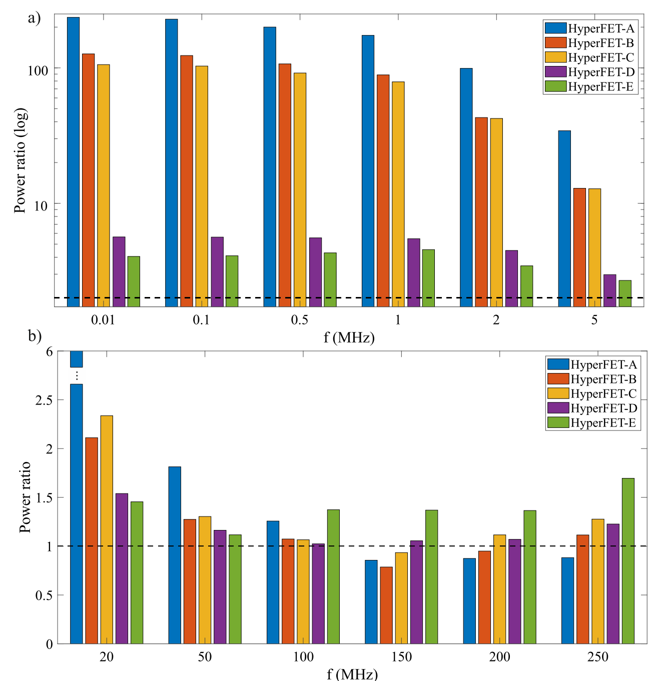

FIGURE 8. Average power ratio (normalized with respect to FinFET) of the five implementations of the RCA with HyperFETs for (a) lowest and (b) highest frequencies reached in the experiment.

The results for the other three HyperFETs (A–C) cannot, however, be attributed solely to supply voltage differences and nonideal gate inputs (due to the degraded output voltages at the HyperFET gates). The very large overheads were due to the deviations from the ideal gate operating principle mentioned earlier. As explained in Section II, some gates operate in static with both PTMs in the metallic state. As long as both PTMs' resistance has a low (metallic) value, the gate will have a large, uncontrolled leakage as the threshold voltage of the host transistor is reduced.

Fig. 8(b) shows the highest frequencies explored. As expected, no power advantages were obtained for HyperFETs D and E. Penalties decreased with respect to the lowest frequencies because the supply voltage differences were

lower (see the values in Table 3). In addition, gate input degradation was reduced or even nonexistent. Power savings were observed for HyperFETs A–C over a given frequency range [the shaded cells in Table 4 or the bars under the dotted line in Fig. 8(b)]. Note that, in all cases, they correspond to frequencies for which the corresponding HyperFET circuit can be operated at a lower supply voltage than the FinFET circuit. It can also be seen that the advantageous frequency range widens as the HyperFET I_{ON} increases. Power savings up to the frequency of 250 MHz were obtained with HyperFET-A, which had the highest ON current of all the studied HyperFETs. However, savings from the supply voltage reduction were smaller than expected (under 15% for HyperFET-A). Assuming that dynamic power dominates at such frequencies, and since it depends on the square of the supply voltage, a reduction of 26% should be obtained. The explanation for this is that consumption in some gates is penalized by their degraded inputs and by the larger I_{ON} of the HyperFETs, which aggravates short-circuit power. Note that different circuit nodes can have different switching activities.

The power results were used to calculate different power (P)–frequency (F) metrics. Table 5 summarizes the values obtained for minimum P/F (minimum energy per operation, E), minimum P/F^2 [minimum energy-delay product (EDP)], and minimum P^2/F [minimum power–energy product (PEP)]. The best result for each of the metrics is marked in bold print and underlined. The LSTP FinFET was the best option in terms of E and PEP, whereas HyperFET-A showed the lowest EDP. Comparing the HyperFETs with the HP FinFET, worse results were obtained with the HyperFETs for all three metrics, except for EDP with HyperFET-A (shaded cell). The HyperFET-A EDP was around 6% lower than the HP FinFET EDP.

Clearly, the results reported in this article could be impacted by variability. In particular, one major concern is the reduction of absolute values for transistor threshold voltage in a low operating frequency. If this variation occurs, it could lead to some gates in the circuit working with their PTMs in the metallic state even though this may not be seen in the nominal case. This would be like an E device being transformed into one similar to an A, B, C, or D device, and therefore, it would manifest the undesirable behavior that has already been described. Moreover, devices with very much reduced MIT voltage (e.g., HyperFET-A) may be more susceptible to this threshold voltage variations, leading that transition to disappear in some cases and consequently to operate sustainedly with the PTM in the metallic state. Thus, the HyperFET degenerates to a conventional device with very low threshold voltage and so exhibits large leakage currents which could cancel the power benefits of supply voltage reduction enabled by larger ON currents.

In summary, limited advantages were obtained with the HyperFETs. Our analysis, however, suggested some design techniques that might be adopted to improve HyperFET performance in terms of power and energy. These are described and evaluated in Section V.

TABLE 5. **Average power–speed tradeoff metrics.**

	H-A	H-B	H-C	H-D	H-E	HP FinFET	LSTP FinFET
E (pJ)	0.017	0.016	0.016	0.015	0.015	0.011	**<u>0.009</u>**
EDP (zJ*s)	**<u>0.090</u>**	0.103	0123	0.120	0.154	0.096	0.250
PEP (zJ*W)	28.6	10	12.2	3	2.3	0.364	**<u>0.001</u>**

V. IMPROVEMENT OF HyperFET CIRCUITS

A. HYBRID HyperFET CIRCUITS

Analysis of the results described in Section IV indicated that the following holds.

1) The degraded inputs seen by the HyperFET gates translate into power penalties. These power penalties are more severe at low frequencies and increase with the HyperFET leakage current. Reducing this degradation would contribute greatly to improving HyperFET circuit performance. Since it has been shown that degradation increases with logic depth [see Fig. 5(b)], we propose a hybrid CMOS–HyperFET architecture, with selected gates in the HyperFET circuit being substituted by conventional CMOS gates. The idea behind this proposal is to completely regenerate the voltage levels associated with logic 1 and logic 0 after a smaller number of cascaded gates. For our RCA, the output gate of each XOR and carry circuit was implemented with HP FinFET transistors. Let us call this RCA implementation Hybrid_1.
2) HyperFETs with higher I_{ON} and IMT more to the left make it possible to reduce supply voltage, but the power savings to be expected from that reduction are not achieved. At the same time, for HyperFETs with lower I_{ON} and an IMT transition more to the right, there are no power penalties other than those caused by the higher supply voltage required. We propose a Hybrid design with HyperFET-A transistors being used for the critical path in the circuit, in order to reduce supply voltage but HyperFET-E devices being used for the gates not in the critical path, in order to minimize power overheads. For the RCA, HyperFET-A was used for the carry chain and HyperFET-E for the exors. Let us call this RCA implementation Hybrid_2.

Hybrid_1 designs with each of the HyperFET devices and the Hybrid_2 design were evaluated, as it was done in Section IV. Table 6 shows the results obtained, with values normalized with respect to the HP FinFET. Cells with values under 1 (power savings) are shaded.

With Hybrid_1, a large improvement was observed for low frequencies, especially for HyperFETs A–C, with normalized values of over 100 for the original designs. For these three devices, the frequency range in which power

TABLE 6. Average power of hybrid RCA designs, normalized to HP FinFET.

	Hybrid_1					Hybrid_2
f(MHz)	**H-A**	**H-B**	**H-C**	**H-D**	**H-E**	
0.01	4.46	2.28	2.36	1.46	0.96	51.23
0.1	4.44	2.27	2.35	1.47	0.97	50.10
0.5	4.39	2.24	2.31	1.48	1.01	45.28
1	4.32	2.20	2.27	1.49	1.06	41.08
2	3.08	1.56	1.60	1.11	0.84	25.39
5	1.31	1.01	0.87	0.67	0.57	10.01
20	0.99	0.94	0.79	0.73	0.70	2.60
50	0.99	0.81	0.82	0.80	0.77	1.21
100	1.01	1.00	0.86	0.98	0.80	1.01
150	0.87	0.86	0.86	0.85	0.81	0.74
200	0.99	0.86	0.86	0.85	0.81	0.77
250	0.98	0.86	0.86	0.85	0.83	0.80
300	0.98	0.96	0.86	0.95	0.93	1.07
350	0.97	0.96	0.96	0.94	0.92	1.34
400	0.96	0.95	0.95	1.03	1.01	1.76

TABLE 7. Average power–speed tradeoffs metrics for hybrids designs.

	Hybrid_1					Hybrid_2	HP FinFET	LSTP FinFET
	H-A	**H-B**	**H-C**	**H-D**	**H-E**			
E (pJ)	0.011	0.010	0.008	0.008	**0.007**	0.015	0.011	0.009
EDP (zJ*s)	0.087	0.086	0.083	0.087	0.085	**0.081**	0.091	0.230
PEP (zJ*W)	1.312	0.784	0.574	0.340	0.247	12.8	0.364	**0.001**

savings were achieved (shaded cells) is widened. However, the amount by which power was reduced did not increase and, in certain cases, even decreased. This is because Hybrid_1 requires a higher supply voltage than the nonhybrid design for these devices. The most interesting result was that power advantages were now obtained for HyperFETs D and E. Reductions of over 40% were obtained for HyperFET-E at some frequencies. Interestingly, this occurred at frequencies at which the LSTP FinFET was no longer advantageous (over 1 MHz).

To illustrate these observations, Fig. 9(a) and (b) compares Hybrid_1 versions with their corresponding nonhybrid circuits.

Hybrid_2, with a maximum power savings of around 25%, obtained better results than both the original HyperFET-A and the original HyperFET-E designs. Fig. 9(c) compares the Hybrid_2 design with the best Hybrid_1 (the version implemented with HyperFET-E). It can clearly be seen that the Hybrid_1E power savings were practically more competitive over the whole range of frequencies analyzed.

Table 7 shows the power–speed metrics. Shaded cells indicate that the value shown is better than with both HP and LSTP FinFETs. Note that there are now many more shaded cells than in Table 5 (the original designs). Neither of the HyperFET designs outperformed the LSTP FinFET in terms of PEP, but both HyperFET D and E outperformed the HP FinFET in the three evaluated metrics.

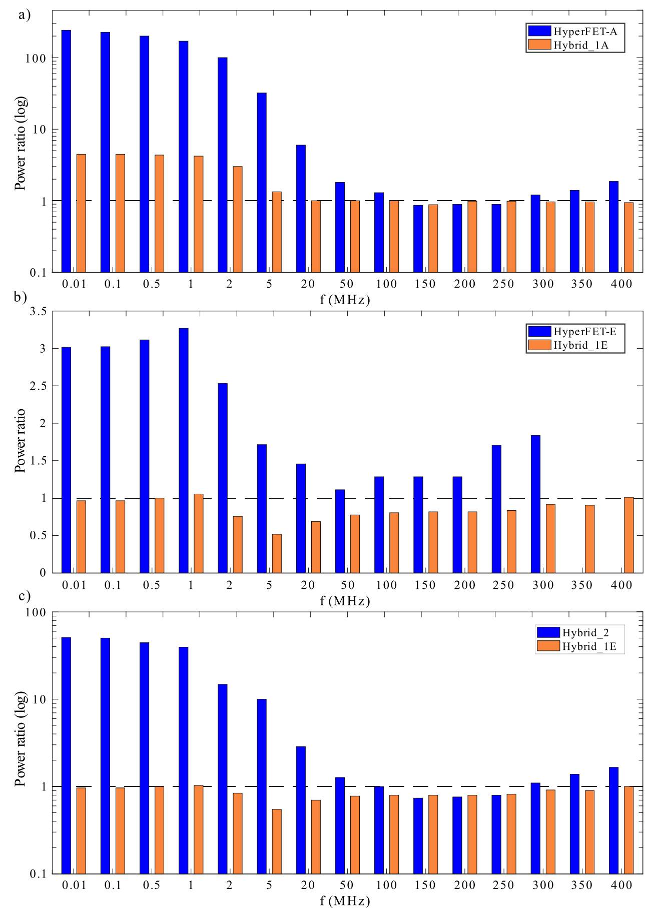

FIGURE 9. RCA average power ratio comparisons. (a) HyperFET-A versus Hybrid_1A. (b) HyperFET-E versus Hybrid_1E. (c) Hybrid_1E versus Hybrid_2.

It can be seen that the Hybrid_1 version with HyperFET-E (Hybrid_1E) was the design with the best E result. The minimum energy of Hybrid_1E was 37% lower than that of HP FinFET and 23% lower than the LSTP FinFET. Moreover, unlike the LSTP FinFET, Hybrid_1E also had a minimum EDP lower than the HP FinFET (12%). Hybrid_2 had the smallest minimum EDP: 16% lower than the HP FinFET and 68% lower than the LSTP FinFET.

The impact of variability was also explored, using design Hybrid_1E and taking 5 MHz as the target frequency. This frequency was chosen because it gives a very favorable power ratio (0.57). Four corner designs were evaluated: 1) fast N transistor, fast P transistor; 2) fast N, slow P; 3) slow N, fast P; and 4) slow N, slow P. Fast and slow versions of the devices were built, assuming that threshold voltage can vary by 60 mV. The minimum supply voltage was determined with which the four designs can operate at the target frequency. The same experiment was conducted for the HP FinFET. Supply voltage for the HyperFET (HP FinFET) circuit required to be increased by 25% (29%) to achieve a correct operation for the fourth corner. HyperFET power ratios with respect to the HP FinFET at those supply voltages were evaluated for the four defined corners. The ratios obtained were 0.18 (first corner), 0.25 (second corner), 0.27 (third corner), and 0.86

TABLE 8. RCA with fast HyperFET supply voltage and average power normalized to original HyperFET-A and HP FinFET RCAs.

	Normalized to HyperFET-A		Normalized to HP FinFET	
f(MHz)	VDD	Power	VDD	Power
0.01	1.00	1.00	3.00	235.48
0.1	1.00	1.00	3.00	228.36
0.5	1.00	1.00	3.00	199.67
1	1.00	1.00	3.00	173.15
2	1.00	1.00	2.40	98.93
5	1.00	1.02	1.71	34.93
20	1.00	0.98	1.33	5.88
50	1.00	1.00	1.09	1.82
100	1.00	0.97	1.00	1.22
150	1.00	0.98	0.86	0.84
200	0.92	1.00	0.80	0.87
250	0.91	0.85	0.80	0.75
300	0.80	0.67	0.80	0.79
350	0.74	0.55	0.82	0.78
400	0.65	0.45	0.82	0.82

(fourth corner). The average value for the four designs was 0.39. These numbers should be compared with the 0.57 ratio of the nominal design. A similar experiment carried out with the Hybrid_1A at 150 MHz showed a ratio over 1 for the first (fast P, fast N) corner, supporting the arguments on variability in the previous section.

B. FAST HyperFETs

Circuit speed is also impacted by the TT of PTMs. It was of interest to evaluate how power performance can be improved if TT is reduced. We expected a reduction in TT to contribute to a reduction in supply voltage. The RCA was evaluated with HyperFET-A with TT = 10 ps. Previous experiments used the value shown in Table 1. Table 8 shows the results obtained, with the supply voltages and average power consumption normalized with respect to the HP FinFET and the original HyperFET-A design. The advantages achieved by reducing TT can thus be evinced as expected.

VI. CONCLUSION

Different HyperFET devices were evaluated at the circuit level. For those devices designed to increase the ON current with respect to the host transistor, the reductions achieved in supply power for the iso-delay operation did not completely translate into power savings because of the nonideal static voltage levels at the HyperFET gates' output. Marginal power reductions were, however, obtained for some of the HyperFETs analyzed. For those devices designed to reduce the OFF current with respect to the host transistor, the higher supply voltage required for iso-delay operation (due to the position of the insulating to metallic transition in their I–V characteristic) counterbalanced the advantages of the reduced leakage and short-circuit currents, leading to power penalties. Very significant power penalties were also encountered in low operating frequency or low switching activity scenarios when using devices designed to increase I_{ON}. These were due to the fact that the gates deviated from the desired mode of operation and had their PTMs working in the metallic state, with a very high I_{OFF}.

Two solutions were proposed to improve the power and energy performance of HyperFET circuits. The hybrid solution using HyperFETs and FinFETs (Hybrid_1) proved to be effective in improving the power performance of HyperFET circuits with the lowest I_{OFF} devices. Power savings of over 40% with respect to HP FinFET were achieved with HyperFET-E. These were achieved at frequencies at which the LSTP FinFET technology is no longer advantageous. The best result in terms of minimum energy per operation was obtained with HyperFET-E, with values almost 40% lower than those obtained with the HP FinFET.

Although the lowest minimum EDP value was achieved with a design that combined iso-I_{ON} and iso-I_{OFF} HyperFETs, devices with higher I_{ON} are not suitable for circuits containing nodes with a low switching rate. It would be interesting to exploit larger ON current by redesigning the PTM to mitigate the excessive drop in voltage that occurs when the OFF current of a transistor with reduced threshold voltage circulates through it. PTM and transistor tuning should also consider variability.

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