

Write Margin Analysis of Spin–Orbit Torque Switching Using Field-Assisted Method

YA-JUI TSOU¹ (Graduate Student Member, IEEE), JIH-CHAO CHIU¹, HUAN-CHI SHIH¹,
and CHEE WEE LIU^{1,2,3} (Fellow, IEEE)

¹Graduate Institute of Electronics Engineering, National Taiwan University, Taipei 106, Taiwan

²Department of Electrical Engineering, Graduate Institute of Electronics Engineering, National Taiwan University, Taipei 106, Taiwan

³Graduate Institute of Photonics and Optoelectronics, National Taiwan University, Taipei 106, Taiwan

CORRESPONDING AUTHOR: CHEE WEE LIU (cliu@ntu.edu.tw)

This work was supported in part by the Ministry of Science and Technology, Taiwan, under Grant 108-2622-8-002-016, Grant 108-2218-E-002-027, and Grant 108-2218-E-002-016 and in part by the Ministry of Education, Taiwan, under Grant NTU-CC-108L891701.

ABSTRACT Switching dynamics of perpendicular magnetic tunnel junction (MTJ) driven by spin–orbit torque (SOT) are investigated by the Landau–Lifshitz–Gilbert (LLG)-based physical model considering the temperature dependence. The field-assisted switching method is proposed to develop the reliable sub-ns writing of SOT-magnetoresistive random-access memory (SOT-MRAM) by removing the plateau time. The conventional method of SOT-MTJ requires the large write current, leading to the area increase of access transistors and the penalty of memory density. The write current and the switching time of SOT-MTJ can be efficiently reduced at the same time by our field-assisted method using the enhanced magnetic field. The magnetic field can be provided by the Co magnetic hard mask above the MTJ. Considering an SOT-MRAM array, the surrounded Co metals have the insignificant influence of stray magnetic field on an MTJ at the center. With the write time of 0.2 ns, the 60% reduction of write current is achieved by our field-assisted method compared to the conventional method. The required write current for the SOT switching decreases with the increasing temperature due to the lowering of thermal stability factor. The write Shmoo plots are further analyzed to calculate the write current margin at the various working temperature. The write time of 0.2 ns exhibits the narrow margin of write current (2.6 μA) in the temperature range from 25 °C to 85 °C, while the write time of 0.8 ns has the wide write margin of 102 μA . The switching behavior and the write margin are also sensitive to the magnetic field.

INDEX TERMS Failure analysis, magnetic memory, magnetic tunnel junction (MTJ), spin–orbit torque (SOT), spintronics.

I. INTRODUCTION

MAGNETORESISTIVE random-access memory (MRAM) is a promising candidate among emerging memories for the microcontroller unit [1], automotive applications [2], and cache replacement [3] due to its fast switching, high endurance, and low energy consumption. Since static random-access memory (SRAM) has the large leakage power and the large cell size, magnetic tunnel junction (MTJ) is an attractive solution of nonvolatile last level cache (LLC) for power saving and area reduction [3], [4]. Recently, spin–transfer torque (STT) MRAM using perpendicular MTJ is demonstrated to show good compatibility with the CMOS logic platform [5]–[8]. The perpendicular MTJ prefers the circular shape to have the lower write current and the better scalability than the in-plane MTJ with the

elliptical shape [9]. An MTJ consists of the MgO tunnel barrier sandwiched by the free layer (storage layer) and the pinned layer. The MTJ resistance is determined by the directions of magnetization in the free layer and the pinned layer. The parallel (P) and antiparallel (AP) magnetization of MTJ exhibits the low-resistance state (logic 0) and the high-resistance state (logic 1), respectively.

However, cache replacement by STT-driven MTJ faces some issues, such as limited switching time, MgO reliability, and read disturbance. The limited switching time of STT-MTJ is due to the large incubation delay (several ns) of STT mechanism [10]. To further reduce the switching time below ~ 10 ns, the required write current increases exponentially [9]. In addition, the large current tunneling through the thin tunnel barrier of MgO (~ 1 nm) leads to the dielectric

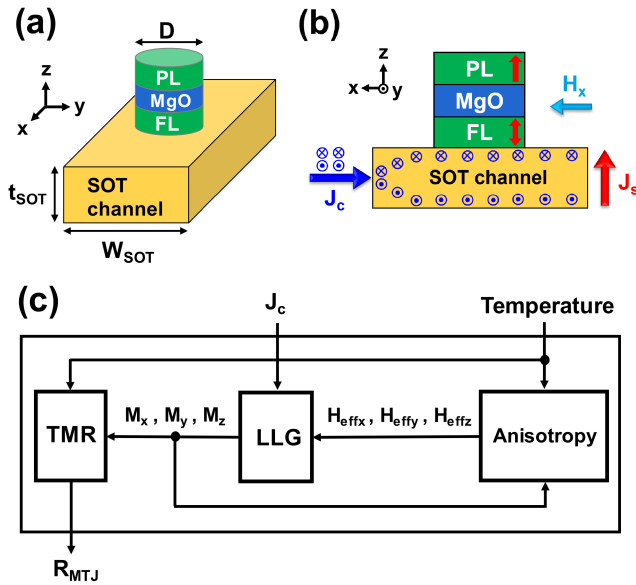


FIGURE 1. (a) Structure of SOT-MTJ and (b) mechanism of SOT switching (along the xz plane). FL and PL are the free layer and pinned layer, respectively. (c) LLG-based physical model of SOT-MTJ considering the temperature dependence.

breakdown and the degraded endurance. Due to the same write current path and read current path in STT-MTJ, the undesired switching during the read operation occurs easily (i.e., read disturbance) [11].

The next-generation MRAM using spin-orbit torque (SOT) can mitigate the aforementioned issues of STT-MRAM. In SOT-MRAM, the write current flows through the SOT channel instead of MTJ [see Fig. 1(a)], while the read current still needs to pass through the MTJ to sense the resistance. The decoupled write path and read path highly improve the MgO reliability and the read disturbance. Note that MgO hardly breaks down during the read operation due to the low read current. The material of the SOT channel can be a nonmagnetic heavy metal, such as tungsten (W) and tantalum (Ta), which are the common materials used in the CMOS back-end-of-line process. In the write operation of SOT-MTJ, the in-plane charged current flows through the SOT channel induces the spin Hall effect (SHE) [12], where spin-up and spin-down electrons are separated in the out-of-plane direction [see Fig. 1(b)]. The direction of spin current density (J_s) is perpendicular to the direction of charged current density (J_c). The accumulated spins under the free layer exert a spin torque by the spin-orbit interaction to flip the magnetization of the free layer. The SOT switching mechanism can eliminate the incubation delay [10].

The comparisons between state-of-the-art STT-MRAM and SOT-MRAM regarding the performance, power, area, and reliability are shown in Table 1 [13]–[16]. The write speed and the reliability of SOT-MRAM can outperform the STT-MRAM. At array level, SOT-MRAM has the lower write energy-delay product than STT-MRAM [17], where the write delay includes the switching time of MTJ and the delay

TABLE 1. Comparisons between STT-MRAM and SOT-MRAM

Item	STT-MRAM	SOT-MRAM
Write time	5 ns [13] ~ 20 ns [14]	0.28 ns ~ 5 ns [15]
Write current density	$\sim 10^7$ A/cm ² [14]	$\sim 10^8$ A/cm ² [15]
Write energy	470 fJ @ $t_{\text{write}} = 5$ ns [16]	350 fJ @ $t_{\text{write}} = 0.28$ ns [16]
Cell size	Small (2-terminal)	Large (3-terminal)
Reliability	Poor (MgO TDDB)	Good
Endurance	Limited	Unlimited
Read disturbance	Poor	Good

time of metal line. The optimized energy-delay product of SOT-MRAM can be achieved by the write access time of several nanoseconds, while the write access time of STT-MRAM is limited by ~ 10 ns [18]. Due to the different write path from the read path in SOT-MRAM, two access transistors are required to individually control write/read operations, leading to an increase of cell size. The area of SOT-MRAM can be saved by the replacement of read access transistors with diodes [19] and the shared bitline architecture [20]. The read disturbance of SOT-MRAM can be mitigated by tuning the MgO thickness, which is independent of the write performance [17], [21], while STT-MRAM has difficulty co-optimizing the write and read performance. The write error rate of SOT-MRAM decreases dramatically when the write current is larger than the critical current [22], while STT-MRAM has a serious write error due to the thermal fluctuations. However, the SOT switching still needs the larger current density (\sim one order magnitude) than STT-MRAM due to the low charge-to-spin conversion efficiency of SOT channel.

The perpendicular MTJ driven by SOT needs the external magnetic field to break the symmetry [23], and several field-free methods have been proposed, such as asymmetric structure [24], STT assistance [25], in-plane MTJ [26], and exchange bias [27]. However, these field-free methods face manufacturing or reliability issues. The asymmetric structure of gradient film thickness (a wedge shape) [24] is difficult to control during fabrication. For STT-assisted SOT switching [25], the STT current through MTJ may cause the MgO dielectric breakdown. The in-plane SOT-MTJ with type-y structure [26] (MTJ easy axis perpendicular to charged current flow) has the larger energy-delay product than perpendicular SOT-MTJ [18]. The exchange bias can be induced by PtMn (antiferromagnetic) [27], but this expensive material increases the manufacturing cost [28].

Reportedly, magnetic Co metal, a common material in CMOS BEOL, was used as a magnetic hard mask [15] to etch the SOT channel and can generate the magnetic field through the underneath MTJ. Since the metallic hard mask is required to pattern MTJ-based devices, the Co magnetic hard mask can be implemented without the additional mask for

cost efficiency. Due to the Co magnetization to generate the magnetic field, no additional current (power) is required. As a result, the Co magnetic hard mask with CMOS integration friendly [29] can be an alternative field-free solution for SOT-MRAM. However, the large current requirement of SOT-MTJ is a critical issue in the embedded SOT-MRAM applications. In this article, the field-assisted method of SOT switching is proposed to remove the plateau time and decrease the write current. The distribution of the magnetic field from the magnetic hard mask array is studied. The write margin considering write current, write time, temperature, and magnetic field is investigated.

II. LLG-BASED PHYSICAL MODEL

The physical model of SOT-MTJ includes the Landau–Lifshitz–Gilbert (LLG) equation, magnetic anisotropy, and tunnel magnetoresistance ratio (TMR) [see Fig. 1(c)]. The time evolution of magnetization in the free layer is solved by the LLG equation [26], [30], [31] [in centimeter-gram-second (CGS) unit]

$$\frac{d\mathbf{M}}{dt} = -\gamma\mathbf{M} \times \mathbf{H}_{\text{eff}} + \alpha\mathbf{M} \times \frac{d\mathbf{M}}{dt} + \frac{\gamma\hbar J_c \theta_{\text{SH}}}{2e t_F M_s} \mathbf{M} \times (\mathbf{M} \times \hat{\sigma}_{\text{SHE}}) \quad (1)$$

where \mathbf{M} is the normalized magnetization with respect to the saturation magnetization (M_s), γ is the gyromagnetic ratio, α is the damping constant, \mathbf{H}_{eff} is the effective magnetic field, \hbar is the reduced Planck constant, θ_{SH} is the spin Hall angle, e is the elementary charge, t_F is the free layer thickness, and $\hat{\sigma}_{\text{SHE}}$ [$-y$ -axis in Fig. 1(b)] is the direction of accumulated spins near the free layer induced by SHE. Note that the direction of spins is determined by the materials of the SOT channel. The first term in the LLG equation is the field-like torque, which depicts the precession along the effective magnetic field. The second term is the damping-like torque toward the effective magnetic field. The last term is the spin torque from the accumulated spins near the free layer by SHE. The spin Hall angle is defined as $\theta_{\text{SH}} = \tan^{-1}(|J_s|/|J_c|)$. The experimental θ_{SH} of optimized W SOT channel is 32% reportedly [16]. Note that there are other choices of SOT channel with the large $\theta_{\text{SH}} > 100\%$, such as the topological insulator (e.g., Bi_2Se_3 [32]). However, the novel materials are difficult to integrate with the perpendicular MTJ and not considered in this article.

The magnetic anisotropy of perpendicular MTJ originates from the interfacial anisotropy and the shape anisotropy. The Fe(Co)-O hybridization at the CoFeB/MgO interface mainly contributes to the out-of-plane (z -axis) magnetization [33]. On the other hand, the magnetization direction favors the long axis of shape due to the demagnetization. For example, the magnetization of a ferromagnetic thin film tends to lie in-plane (xy plane). As a result, the interfacial anisotropy and the shape anisotropy compete with each other, and the large interfacial anisotropy is preferred for the perpendicular MTJ. The x -direction magnetic field (H_x) [see Fig. 1(b)] is

required to break the symmetry of SOT-driven perpendicular MTJ [23]. The additional magnetic field can come from the embedded magnetic Co hard mask on the top of MTJ [15]. The effective magnetic field of MTJ is the combination of internal effective magnetic anisotropy field and external magnetic field, given by

$$\mathbf{H}_{\text{eff}}(t) = \begin{bmatrix} 0 \\ 0 \\ 2K_i M_z(t)/M_s t_F \end{bmatrix} - 4\pi M_s \begin{bmatrix} N_{dx} M_x(t) \\ N_{dy} M_y(t) \\ N_{dz} M_z(t) \end{bmatrix} + \begin{bmatrix} H_x \\ 0 \\ 0 \end{bmatrix} \quad (2)$$

where K_i is the interfacial anisotropy. N_{dx} , N_{dy} , and N_{dz} are the x -, y -, and z -directions' demagnetizing factors, respectively. Note that M_x , M_y , and M_z are the normalized magnetization with respect to M_s . Both M_s and K_i are temperature-dependent reportedly [34], [35], and the models are given by [36], [37]

$$M_s(T) = M_s(0) \left[1 - \left(\frac{T}{T_C} \right)^\beta \right] \quad (3)$$

$$K_i(T) = K_i(0) \cdot (1 - \eta T) \quad (4)$$

where T is the absolute temperature and T_C is the Curie temperature. $M_s(0)$ and $K_i(0)$ are M_s and K_i at $T = 0$ K, respectively. The coefficient β in Bloch's law is 1.73 from the experimental data [36]. The coefficient η is fit by the temperature variation rate of thermal stability factor (Δ) [34]. The shape-dependent demagnetizing factors of a ferromagnetic cylinder are given by [38]

$$N_{dz} = \frac{1}{\frac{2t_F}{r\sqrt{\pi}} + 1}, \quad N_{dx} = N_{dy} = \frac{1 - N_{dz}}{2} \quad (5)$$

where r is the radius of the free layer.

The TMR related to the spin polarization (P) [39] can be derived from Julliere's model [40]. The TMR is defined as the difference of parallel-state resistance (R_P) and AP-state resistance (R_{AP}) over R_P . The TMR considering the voltage and temperature dependence can be modeled as

$$\text{TMR} = \frac{\text{TMR}_0}{1 + (V/V_h)^2} = \frac{2P^2/(1 - P^2)}{1 + (V/V_h)^2} \quad (6)$$

$$P = P_0(1 - \alpha_{\text{sp}} T^{1.5}) \quad (7)$$

where P_0 is the spin polarization at $T = 0$ K, α_{sp} is the spin-wave parameter, and V_h is the MTJ voltage at the half value of zero-biased TMR [41]. Note that α_{sp} is fit by the temperature variation rate of TMR data [34]. The MTJ resistance (R_{MTJ}) depends on the free layer magnetization, which is given by [30]

$$R_{\text{MTJ}} = \left(\frac{1 + \cos\theta}{2} \right) R_P + \left(\frac{1 - \cos\theta}{2} \right) R_{\text{AP}} \quad (8)$$

where θ is the angle between the magnetization of the free layer and the fixed magnetization of the pinned layer ($+z$ -axis). The R_{MTJ} is equal to R_P and R_{AP} at $\theta = 0^\circ$ and

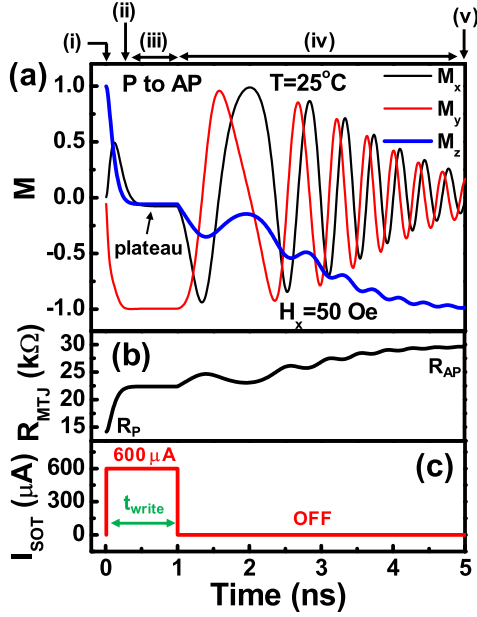


FIGURE 2. Waveforms of (a) magnetization, (b) MTJ resistance, and (c) SOT current ($600 \mu\text{A}$) of SOT-MTJ using the conventional method in the write_1 operation (P to AP switching). The upper axis is labeled from (i) to (v), corresponding to Fig. 3(a)–(e), respectively.

$\theta = 180^\circ$, respectively. Without the applied charged current, the magnetization keeps precessing around the effective magnetic field due to the thermal fluctuation. The initial angle (θ_i) of magnetization is determined by the thermal stability factor, which is given by [42]

$$\theta_i = \sqrt{\frac{1}{2\Delta}} \quad (9)$$

$$\Delta = \frac{K_{\text{eff}}V}{k_B T} = \frac{H_{\text{eff}}M_S V}{2k_B T} \quad (10)$$

where K_{eff} is the effective magnetic anisotropy and k_B is the Boltzmann constant.

III. SOT SWITCHING

A. CONVENTIONAL METHOD

The dimensions and the parameters of SOT-driven perpendicular MTJ in our simulation are shown in Table 2. The SOT write current (I_{SOT}) is equivalent to the charged current through the SOT channel ($J_c \times W_{\text{SOT}} \times t_{\text{SOT}}$) [see Fig. 1(a) and (b)]. In the write_1 operation (P to AP switching), with I_{SOT} of $600 \mu\text{A}$ and the write time (t_{write}) of 1 ns [see Fig. 2(c)], the magnetization can be driven to the $-y$ -axis by the SHE torque [see Figs. 2(a) and 3(a) and (b)]. The initial spin torque is maximum, and the incubation delay is negligible in SOT switching (spin torque $\sim \sin\varphi$, where φ is the angle between the magnetization of the free layer and the spin induced by SHE). Note that the magnetization of the free layer is parallel or antiparallel to the magnetization of the pinned layer in STT-MTJ, and this leads to the minimum initial spin torque and the large incubation delay. During the I_{SOT} pulse, the mag-

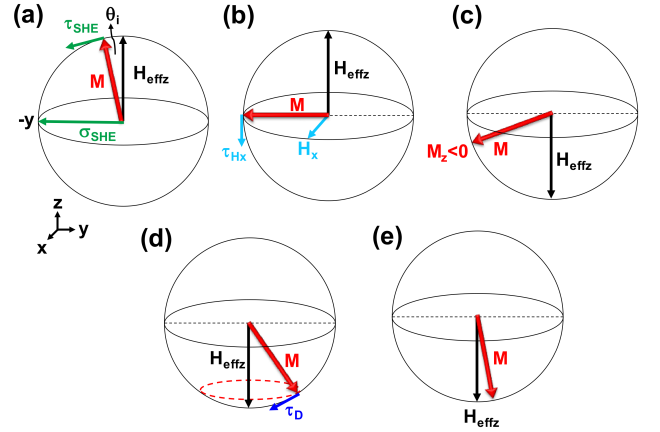


FIGURE 3. Schematic magnetization dynamics of SOT switching using the conventional method in the write_1 operation. (a) Initial P state ($\theta = \theta_i$). With the I_{SOT} pulse, the magnetization starts to motion away from $H_{\text{eff}z}$ by the SHE torque, $-M \times (M \times \hat{\sigma}_{\text{SHE}})$. (b) Magnetization alignment in the $-y$ -direction during the I_{SOT} pulse. The magnetization has the same direction as the $\hat{\sigma}_{\text{SHE}}$. (c) Magnetization deviation toward the $-z$ -axis ($M_z < 0$) by the H_x torque (τ_{Hx}) along the $-z$ -axis. (d) Magnetization precession along $H_{\text{eff}z}$ without the I_{SOT} pulse. The magnetization moves toward $H_{\text{eff}z}$ by the damping torque (τ_D). (e) Final AP state.

TABLE 2. Parameters of SOT-MTJ

Symbol	Parameter	Value (@300 K)
D	MTJ diameter	60 nm ^[15]
t_f	Free layer thickness	1 nm ^[15]
W_{SOT}	SOT channel width	170 nm ^[15]
t_{SOT}	SOT channel thickness	3.5 nm ^[15]
RA	Resistance-area product	40 $\Omega\text{-}\mu\text{m}^2$ ^[15]
TMR	Tunnel magnetoresistance	110% ^[15]
α	Damping constant	0.05
γ	Gyromagnetic ratio	$2\pi \cdot 2.8 \times 10^6$ Hz/G
θ_{SH}	Spin Hall angle	32% ^[15]
Δ	Thermal stability factor	48 ^[15]
K_i	Interfacial anisotropy	1 erg/cm ²
M_S	Saturation magnetization	1250 emu/cm ³
P	Spin polarization	0.596
β	Temperature coefficient of M_s	1.73
η	Temperature coefficient of K_i	1.61×10^{-3} K ⁻¹
T_C	Curie temperature	750 K ^[36]
α_{sp}	Spin-wave parameter	3.02×10^{-5} K ^{-1.5}

netization and the resistance have a plateau until I_{SOT} becomes zero [see Figs. 2(a) and (b) and 3(b)]. Thus, R_{MTJ} maintains its value at $\theta = 90^\circ$ (8). The magnetic field H_x is required to induce the $-z$ -direction torque ($-M \times H_x$) for the magnetization deviation toward the $-z$ -axis ($M_z < 0$) [43] [see Fig. 3(c)]. When I_{SOT} is turned OFF, the magnetization starts precession along the effective magnetic field in the $-z$ -direction ($H_{\text{eff}z}$) and moves toward $H_{\text{eff}z}$ by natural damping [see Fig. 3(d)]. Finally, R_{MTJ} changes to R_{AP} [see Fig. 2(c) and 3(e)]. Due to the thermal fluctuation, the magnetization cannot completely align to the $-z$ -axis. The critical current, defined as the minimum I_{SOT} value for the successful switching with no magnetization

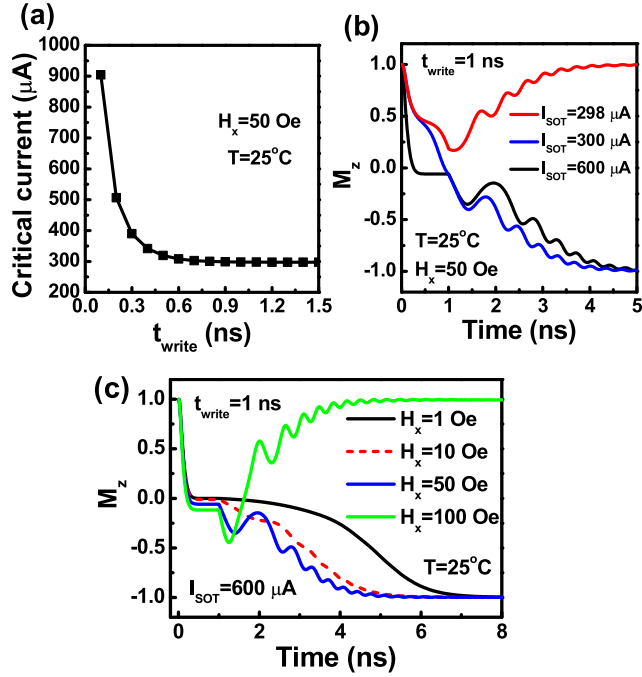


FIGURE 4. (a) Critical current as a function of t_{write} using the conventional method. M_z dynamics of the conventional method with the different (b) I_{SOT} and (c) H_x .

rebound [see Fig. 2(a)], decreases with the increasing t_{write} and reaches the saturation (~ 300 μA) at t_{write} of 0.8 ns [see Fig. 4(a)]. When I_{SOT} is below the critical current, the magnetization is unable to reach $M_z < 0$, leading to the write failure and the magnetization rebound back to the initial P state [see Fig. 4(b)]. Note that the increase of I_{SOT} from 300 to 600 μA results in the unchanged switching time (5 ns). With the increasing H_x from 1 to 50 Oe, the magnetization further moves close to the $-z$ -axis, and the switching time decreases [see Fig. 4(c)]. The magnetization close to the $-z$ -axis can induce the large $H_{\text{eff}z}$ and accelerate the switching. However, when H_x increases to 100 Oe, the large H_x leads to the magnetic field disturbance on $H_{\text{eff}z}$, and the magnetization rebounds to the initial P state (write failure). Therefore, the H_x enhancement has the ability to decrease the switching time but may cause the interference of magnetic field simultaneously.

The analytical critical current (I_c) of SOT switching can be expressed as [44]

$$I_c = \frac{2e M_s t_F}{\hbar \theta_{\text{SH}}} \left(\frac{H_{\text{eff}}}{2} - \frac{H_x}{\sqrt{2}} \right) t_{\text{SOT}} W_{\text{SOT}} \quad (11)$$

where the large damping constant ($\alpha = 0.1$) is assumed. The critical current increases with the increasing H_{eff} due to the strong interfacial magnetic anisotropy. In our case, relatively small damping constant of 0.05 is considered to simulate the critical current by the LLG-based model [see Fig. 4(a)]. The comparison between the analytic (11) and the simulated critical current is shown in Fig. 5. The parameters given in Table 2 result in H_{eff} of 0.83 kOe with the difference of $\sim 10\%$. The difference between the analytic and simulated critical

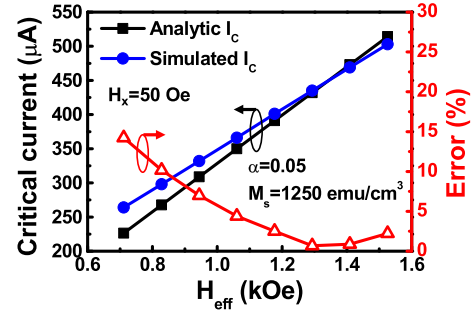


FIGURE 5. Analytic and simulated critical current (I_c) with various H_{eff} at the fixed M_s . Error is defined as $\Delta I_c / \text{simulated } I_c$. H_{eff} increases with the increasing interfacial magnetic anisotropy.

current is due to the lack of field-like torque consideration in the analytic critical current (11) [45]. Both the field-like torque and the damping-like torque during SOT switching are included in our LLG-based model.

B. FIELD-ASSISTED METHOD

In our field-assisted method, H_x increases to 320 Oe [15] to remove the plateau region shown in Fig. 2(a) and (b) ($H_x = 50$ Oe in the conventional method). The strong increase of H_x induces a strong torque in the $-y$ -direction, which is the same as the SHE torque, to compensate for the decrease of I_{SOT} and pull the magnetization down to the $-z$ -axis without the plateau time [see Fig. 6(a)]. The R_{MTJ} quickly switches to R_{AP} within around 1 ns (similar to t_{write}) during the I_{SOT} pulse [see Fig. 6(b) and (c)], which outperforms the switching time (5 ns) of the conventional method [see Fig. 6(d)]. The comparison of write performance between the conventional method and the field-assisted method is shown in Fig. 7. Compared to the conventional method, the critical current of SOT-MTJ using the field-assisted method can be reduced by 51% and 60% at t_{write} of 1 and 0.2 ns, respectively. The reduction of write time and write current by the field-assisted method saves the write energy consumption (Energy = $I_{\text{SOT}} \times V_{\text{dd}} \times t_{\text{write}}$).

C. MAGNETIC FIELD DISTRIBUTION

H_x can be generated by the Co magnetic hard mask above the MTJ [see Fig. 8(a)]. The magnetization of Co is fixed along the $-x$ -direction, which induces the magnetic field through the free layer in the $+x$ -direction. H_x from a single Co magnet [see Fig. 8(a)] and a 3×3 Co magnet array [see Fig. 8(b)] is simulated using the finite element method. The saturation magnetization of Co magnet is 1440 emu/cm³ [46]. The length, width, and thickness of the Co magnetic hard mask are 390, 120, and 50 nm, respectively [15]. The x -direction and y -direction pitches of the Co array are 540 and 260 nm [15], respectively. H_x of 320 Oe at the center of the free layer is obtained by the spacing of 68.4 nm between the Co magnetic hard mask and the free layer along the z -direction [see Fig. 8(c)]. In addition, the single Co magnet and the Co array have similar H_x for the spacing less than 250 nm.

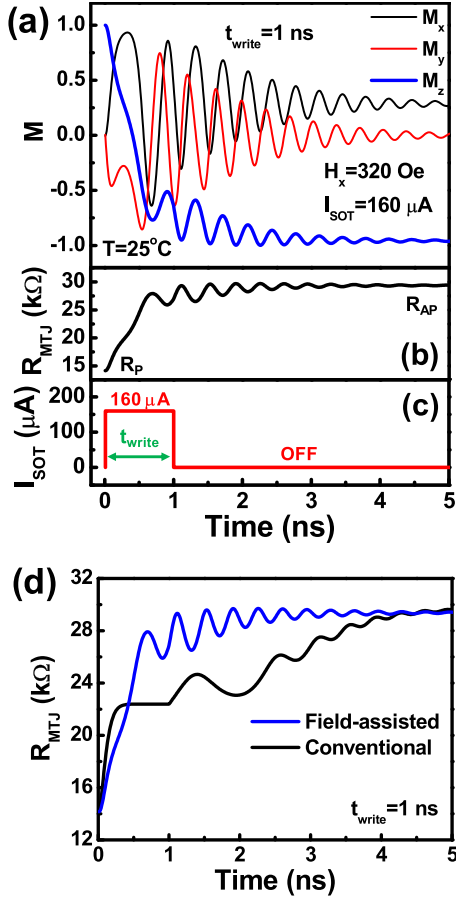


FIGURE 6. Waveforms of (a) magnetization, (b) MTJ resistance, and (c) I_{SOT} of SOT-MTJ using the field-assisted method with H_x of 320 Oe. (d) R_{MTJ} versus time with the conventional method and the field-assisted method.

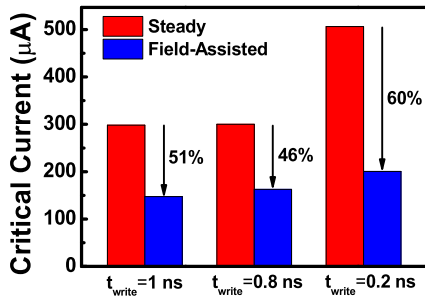


FIGURE 7. Critical current versus t_{write} using the conventional method and the field-assisted method.

The interference of stray magnetic field in a Co array can be suppressed since the north (N) magnetic pole of a Co magnet is close to the south (S) magnetic pole of the adjacent Co magnet along the x -direction [see Fig. 8(b)]. The H_x distribution in the cylindrical free layer ($t_{FL} = 1$ nm, $D = 60$ nm) along the xy plane is shown in Fig. 8(d) and (e), and it has a slight variability between center and edge. H_x ranging from 315.8 to 325.4 Oe in the cylindrical free layer has the small variation (1.7%) with respect to H_x (320 Oe) at the center of the free layer. Therefore, the field-assisted method has little

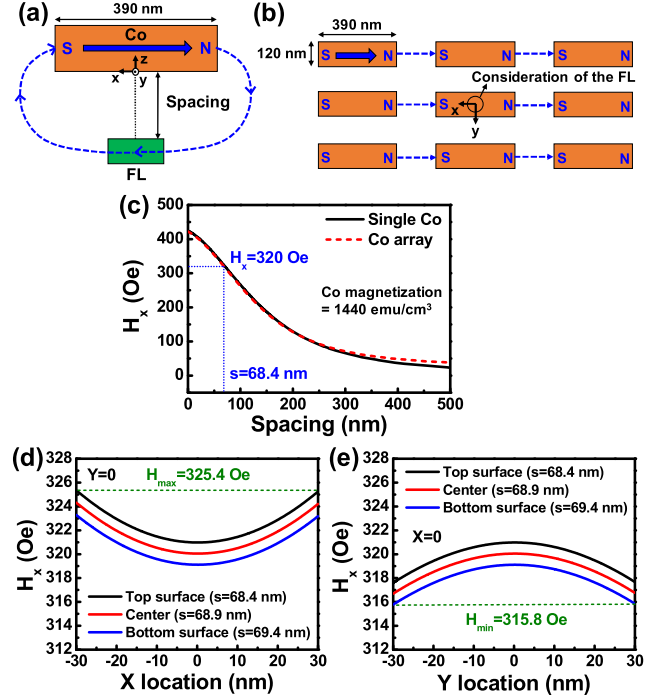


FIGURE 8. (a) Single Co magnetic hard mask above the free layer (cross-sectional view). (b) 3×3 Co array (top view) with the MTJ underneath the center. The dashed arrows represent the stray magnetic field from Co magnets. (c) H_x at the center of free layer versus spacing (defined as s) between the Co magnet and the free layer along the z -direction. H_x in the free layer along (d) x -axis and (e) y -axis. The origin is at the center of the free layer, as labeled in Fig. 8(b). The thickness and the diameter of the free layer are 1 and 60 nm, respectively.

impact on the write stability at the array level. H_x of 320 Oe decreases the TMR from 110% to 103% to gently degrade the read performance.

IV. WRITE MARGIN ANALYSIS

I_{SOT} needs to be larger or equal to the critical current for the successful SOT switching. For the conventional method, there is only one critical current value at the fixed t_{write} [see Fig. 4(a)]. For the field-assisted method, the write failure occurs occasionally with I_{SOT} below 365 μ A [see Fig. 9(a)], due to the magnetic field interference by H_x . Note that there is no write error when I_{SOT} is larger than 365 μ A. The SOT switching toward the $-z$ -axis can be disturbed by the increase of H_x , and the competition between H_{effz} and H_x leads to the irregular oscillations of magnetization. There are three successful write windows for the fixed t_{write} of 1 ns [see Fig. 9(a)]. With the fixed I_{SOT} , there are also write failures within t_{write} of 1.5 ns [see Fig. 9(b)]. Consequently, the write failure due to the inadequate I_{SOT} and t_{write} should be taken into account to achieve the error-free SOT switching.

The Shmoo plot of SOT-MTJ at 25 $^\circ$ C using the field-assisted method is shown in Fig. 10(a). The increase of t_{write} decreases the required I_{SOT} , which has a similar trend to the conventional method [see Fig. 4(a)], and results in the saturated I_{SOT} value (145 μ A) at the t_{write} of 1 ns.

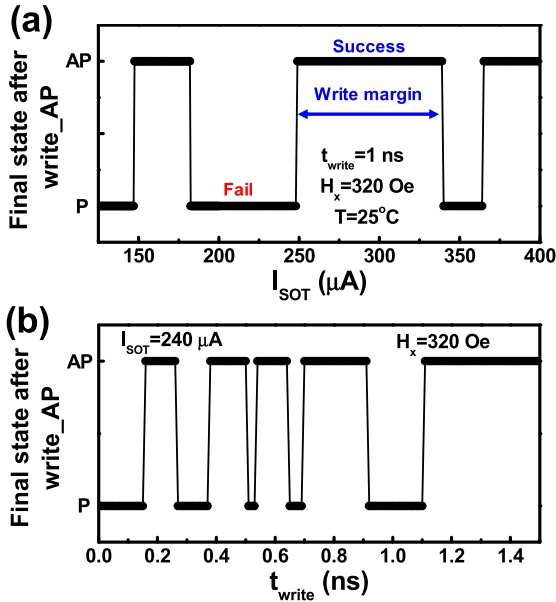


FIGURE 9. MTJ final state after write_1 at 25 °C with various (a) I_{SOT} and (b) t_{write} using the field-assisted method. The AP state and the P state represent the successful switching and write failure, respectively.

The SOT-MTJ can be switched successfully by the t_{write} within 1 ns and the I_{SOT} less than 200 μA . The ultrashort t_{write} of 0.2 ns is achieved by the I_{SOT} of 200 μA [see Figs. 9 and 10(a)]. The low current can reduce the footprint of access transistors for the high-density memory applications since the MRAM cell size is dominated by the access transistors instead of the MTJ. Therefore, the field-assisted method with the low write current facilitates the integration of SOT-MTJ with CMOS transistors. In our simulation, the width of the SOT channel (W_{SOT}) is 170 nm from the experimental device structure [15] (see Table 2). If W_{SOT} keeps scaling down to the half by improving the patterning technology, the required I_{SOT} can be further reduced to below 100 μA .

Considering the elevated temperature at 85 °C, the Shmoo plot of SOT-MTJ using the field-assisted method is shown in Fig. 10(b). The required I_{SOT} for successful writing decreases with the increasing temperature. The thermal stability factor of MTJ at 85 °C is 30.4, which is lower than that at room temperature ($\Delta = 48$). The low thermal stability factor is equivalent to the high thermal fluctuation, and the switching from P state to AP state becomes easier. As a result, the increase in temperature decreases the critical current. The saturated critical current at 25 °C and 85 °C is 145 and 84.5 μA , respectively. Furthermore, the Shmoo plot at -40 °C for low-temperature applications is shown in Fig. 10(c). Compared to the room temperature, the critical current increases due to the increasing thermal stability factor.

However, the write margin shift at a different temperature [see Fig. 11(a) and (b)] is an issue. With t_{write} of 0.2 ns, the overlapping region of the write current margin is 200~203 μA in the temperature range of 25 °C~85 °C,

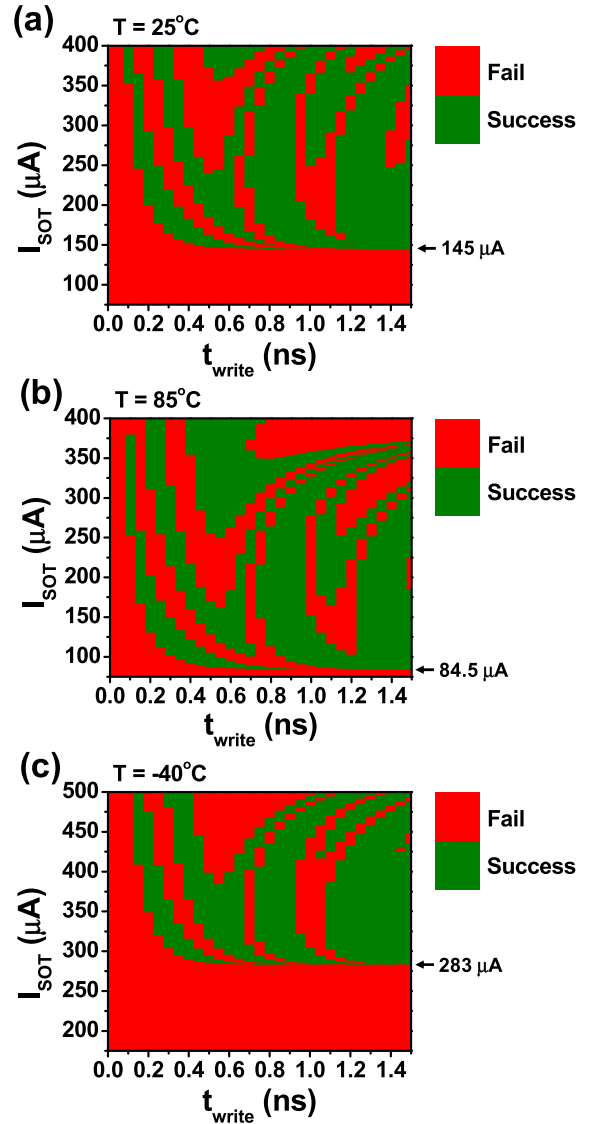


FIGURE 10. Shmoo plots of SOT switching using the field-assisted method at (a) 25 °C, (b) 85 °C, and (c) -40 °C with H_x of 320 Oe.

while it disappears at the temperature lower than 25 °C [see Fig. 11(a)]. With t_{write} of 0.8 ns, the overlapping write margin (162.5~264.5 μA) in the temperature range of 25 °C~85 °C is much wider compared to t_{write} of 0.2 ns, while it starts to vanish at the temperature lower than -30 °C [see Fig. 11(b)]. t_{write} of 0.8 ns with the sufficient write margin likely meets the specification with the large temperature range for automotive applications. Therefore, I_{SOT} of SOT devices using the field-assisted method needs to be controlled within the temperature-dependent write margin to avoid the undesirable write failure. With the decrease of H_x to 290 Oe, the insufficient H_x -induced torque causes the magnetization rebound back to the initial P state for I_{SOT} of 160 μA and t_{write} of 1 ns [see Fig. 12(a)]. The write behavior of the field-assisted method is sensitive to H_x [see Fig. 12(b)], and the required I_{SOT} increases with the decrease of H_x . This leads to the narrowing of the success write window.

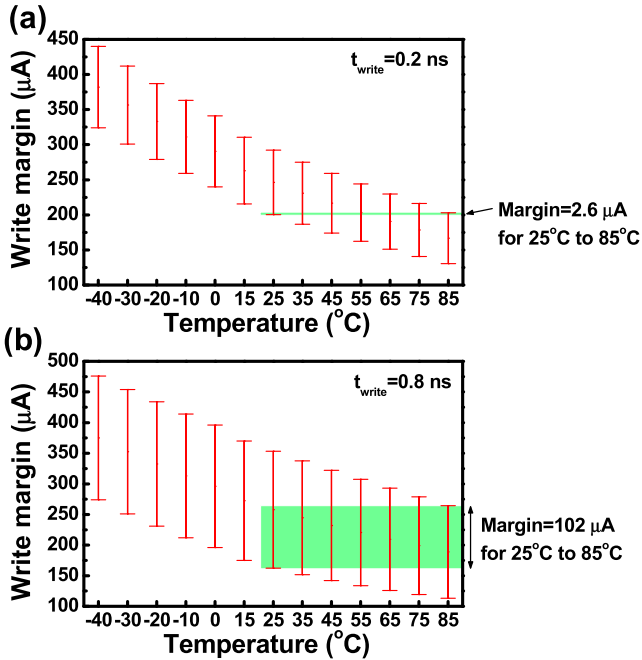


FIGURE 11. Write margin versus temperature with (a) $t_{\text{write}} = 0.2$ ns and (b) $t_{\text{write}} = 0.8$ ns using the field-assisted method. The current interval (write margin) with the red line represents the required I_{SOT} for the successful switching at the given temperature. The green region shows the write margin considering the temperature range of $25^\circ\text{C} \sim 85^\circ\text{C}$.

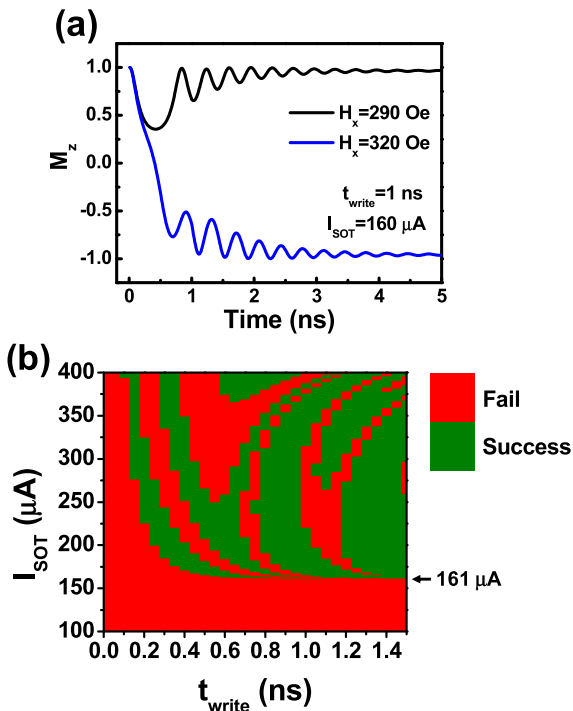


FIGURE 12. (a) M_z dynamics of the field-assisted method with the different H_x . (b) Shmoo plot of the field-assisted method with H_x of 290 Oe at 25°C .

V. CONCLUSION

The switching characteristics and the write Shmoo plots of SOT-MTJ considering the proposed field-assisted method are

simulated using the LLG-based physical model. The magnetic field assist reduces the write current and the write time by removing the plateau time during the SOT switching. In the SOT-MTJ array, the crosstalk and the variability of the magnetic field from the Co magnets are negligible. The shift of the write current margin with the increasing temperature should be considered carefully in the circuit design for the write stability. The proposed field-assisted method to achieve low-current switching and the temperature effects on the write margin can be considered for SOT-MRAM technology.

REFERENCES

- [1] D. Shum *et al.*, "CMOS-embedded STT-MRAM arrays in 2x nm nodes for GP-MCU applications," in *Proc. Symp. VLSI Technol.*, Jun. 2017, pp. T208–T209.
- [2] K. Lee *et al.*, "22-nm FD-SOI embedded MRAM technology for low-power automotive-grade-1 MCU applications," in *IEDM Tech. Dig.*, Dec. 2018, pp. 27.1.1–27.1.4.
- [3] S. Fujita, S. Takaya, S. Takeda, and K. Ikegami, "Circuit and systems based on advanced MRAM for near future computing applications," in *Proc. Symp. VLSI Circuits*, Jun. 2019, pp. C278–C279.
- [4] H. Noguchi *et al.*, "4Mb STT-MRAM-based cache with memory-access-aware power optimization and write-verify-write/read-modify-write scheme," in *IEEE ISSCC Dig. Tech. Papers*, Jan./Feb. 2016, pp. 132–133.
- [5] W. J. Gallagher *et al.*, "Recent progress and next directions for embedded MRAM technology," in *Proc. Symp. VLSI Circuits*, Jun. 2019, pp. T190–T191.
- [6] O. Golonzka *et al.*, "MRAM as embedded non-volatile memory solution for 22FFL FinFET technology," in *IEDM Tech. Dig.*, Dec. 2018, pp. 18.1.1–18.1.4.
- [7] Y. J. Song *et al.*, "Demonstration of highly manufacturable STT-MRAM embedded in 28nm logic," in *IEDM Tech. Dig.*, Dec. 2018, pp. 18.2.1–18.2.4.
- [8] K. Lee *et al.*, "22-nm FD-SOI embedded MRAM with full solder reflow compatibility and enhanced magnetic immunity," in *Proc. IEEE Symp. VLSI Technol.*, Jun. 2018, pp. 183–184.
- [9] A. V. Khvalkovskiy *et al.*, "Basic principles of STT-MRAM cell operation in memory arrays," *J. Phys. D, Appl. Phys.*, vol. 46, no. 7, pp. 074001-1–074001-20, 2013.
- [10] K. Garello *et al.*, "Ultrafast magnetization switching by spin-orbit torques," *Appl. Phys. Lett.*, vol. 105, no. 21, pp. 212402-1–212402-5, Nov. 2014.
- [11] Y. Ran, W. Kang, Y. Zhang, J.-O. Klein, and W. Zhao, "Read disturbance issue for nanoscale STT-MRAM," in *Proc. NVMSA*, Aug. 2015, pp. 1–6.
- [12] J. Sinova, S. O. Valenzuela, J. Wunderlich, C. H. Back, and T. Jungwirth, "Spin Hall effects," *Rev. Mod. Phys.*, vol. 87, no. 4, pp. 1213–1259, Oct. 2015.
- [13] G. Hu *et al.*, "Reliable five-nanosecond writing of spin-transfer torque magnetic random-access memory," *IEEE Magn. Lett.*, vol. 10, 2019, Art. no. 4504304, doi: 10.1109/LMAG.2019.2928243.
- [14] G. Jan *et al.*, "Demonstration of ultra-low voltage and ultra low power STT-MRAM designed for compatibility with 0x node embedded LLC applications," in *Proc. Symp. VLSI Technol.*, Jun. 2018, pp. 65–66.
- [15] K. Garello *et al.*, "Manufacturable 300mm platform solution for field-free switching SOT-MRAM," in *Proc. Symp. VLSI Circuits*, Jun. 2019, pp. T194–T195.
- [16] K. Garello, F. Yasin, and G. S. Kar, "Spin-orbit torque MRAM for ultrafast embedded memories: From fundamentals to large scale technology integration," in *Proc. IEEE Int. Memory Workshop (IMW)*, May 2019, pp. 101–104.
- [17] C. Pan and A. Naemi, "Nonvolatile spintronic memory array performance benchmarking based on three-terminal memory cell," *IEEE J. Explor. Solid-State Comput. Devices Circuits*, vol. 3, no. 2, pp. 10–17, Feb. 2017.
- [18] S. Manipatruni, D. E. Nikonov, and I. A. Young, "Energy-delay performance of giant spin Hall effect switching for dense magnetic memory," *Appl. Phys. Express*, vol. 7, no. 10, pp. 103001-1–103001-4, 2014.
- [19] Y. Seo, K.-W. Kwon, and K. Roy, "Area-efficient SOT-MRAM with a Schottky diode," *IEEE Electron Device Lett.*, vol. 37, no. 8, pp. 982–985, Aug. 2016.

- [20] Y. Seo and K. Roy, "High-density SOT-MRAM based on shared bitline structure," *IEEE Trans. Very Large Scale Integr. (VLSI) Syst.*, vol. 26, no. 8, pp. 1600–1603, Aug. 2018.
- [21] A. Aziz, W. Cane-Wissing, M. S. Kim, S. Datta, V. Narayanan, and S. K. Gupta, "Single-ended and differential MRAMs based on spin Hall effect: A layout-aware design perspective," in *Proc. IEEE Comput. Soc. Annu. Symp. VLSI*, Jul. 2015, pp. 333–338.
- [22] S. Ganguly, Y. Xie, and A. Ghosh, "Energy-delay-reliability of present and next generation STT-RAM technology," in *Proc. 17th IEEE Int. Conf. Nanotechnol.*, Jul. 2017, pp. 1010–1013.
- [23] L. Liu, O. J. Lee, T. J. Gudmundsen, D. C. Ralph, and R. A. Buhrman, "Current-induced switching of perpendicularly magnetized magnetic layers using spin torque from the spin Hall effect," *Phys. Rev. Lett.*, vol. 109, Aug. 2012, Art. no. 096602.
- [24] G. Yu et al., "Switching of perpendicular magnetization by spin-orbit torques in the absence of external magnetic fields," *Nature Nanotechnol.*, vol. 9, pp. 548–554, May 2014.
- [25] A. van den Brink et al., "Spin-Hall-assisted magnetic random access memory," *Appl. Phys. Lett.*, vol. 104, no. 1, 2014, Art. no. 012403.
- [26] S. Fukami, T. Anekawa, C. Zhang, and H. Ohno, "A spin-orbit torque switching scheme with collinear magnetic easy axis and current configuration," *Nature Nanotechnol.*, vol. 11, pp. 621–625, Mar. 2016.
- [27] S. Fukami, C. Zhang, S. DuttaGupta, A. Kurenkov, and H. Ohno, "Magnetization switching by spin-orbit torque in an antiferromagnet-ferromagnet bilayer system," *Nature Mater.*, vol. 15, pp. 535–541, Feb. 2016.
- [28] S. V. Pietambaram, B. J. Akerman, R. Whig, J. A. Janesky, N. D. Rizzo, and J. M. Slaughter, "Methods of manufacturing magnetoresistive MTJ stacks having an unpinned, fixed synthetic anti-ferromagnetic structure," U.S. Patent 10 199 571 B2, Feb. 5, 2019.
- [29] C. Auth et al., "A 10nm high performance and low-power CMOS technology featuring 3rd generation FinFET transistors, self-aligned quad patterning, contact over active gate and cobalt local interconnects," in *IEDM Tech. Dig.*, Dec. 2017, pp. 29.1.1–29.1.4.
- [30] J. Kim, A. Chen, B. Behin-Aein, S. Kumar, J.-P. Wang, and C. H. Kim, "A technology-agnostic MTJ SPICE model with user-defined dimensions for STT-MRAM scalability studies," in *Proc. IEEE CICC*, Sep. 2015, pp. 1–4.
- [31] K. Jabeur, G. Di Pendina, G. Prenat, L. D. Buda-Prejbeanu, and B. Dieny, "Compact modeling of a magnetic tunnel junction based on spin orbit torque," *IEEE Trans. Magn.*, vol. 50, no. 7, Jul. 2014, Art. no. 4100208.
- [32] A. R. Mellnik et al., "Spin-transfer torque generated by a topological insulator," *Nature*, vol. 511, pp. 449–451, Jul. 2014.
- [33] B. Dieny and M. Chshiev, "Perpendicular magnetic anisotropy at transition metal/oxide interfaces and applications," *Rev. Mod. Phys.*, vol. 89, no. 2, pp. 025008-1–025008-54, Jun. 2017.
- [34] C. Park et al., "Temperature dependence of critical device parameters in 1 Gb perpendicular magnetic tunnel junction arrays for STT-MRAM," *IEEE Trans. Magn.*, vol. 53, no. 2, Feb. 2017, Art. no. 3400104.
- [35] J. Kim et al., "Layer thickness dependence of the current-induced effective field vector in TaCoFeB/MgO," *Nature Mater.*, vol. 12, pp. 240–245, Dec. 2012.
- [36] K.-M. Lee, J. W. Choi, J. Sok, and B.-C. Min, "Temperature dependence of the interfacial magnetic anisotropy in W/CoFeB/MgO," *AIP Adv.*, vol. 7, no. 6, pp. 065107-1–065107-7, Jun. 2017.
- [37] M. Kazemi, G. E. Rowlands, E. Ipek, R. A. Buhrman, and E. G. Friedman, "Compact model for spin-orbit magnetic tunnel junctions," *IEEE Trans. Electron Devices*, vol. 63, no. 2, pp. 848–855, Feb. 2016.
- [38] M. Sato and Y. Ishii, "Simple and approximate expressions of demagnetizing factors of uniformly magnetized rectangular rod and cylinder," *J. Appl. Phys.*, vol. 66, no. 2, pp. 983–985, 1989.
- [39] J. Schmalhorst and G. Reiss, "Temperature and bias-voltage dependent transport in magnetic tunnel junctions with low energy Ar-ion irradiated barriers," *Phys. Rev. B, Condens. Matter*, vol. 68, pp. 224437-1–224437-9, Dec. 2003.
- [40] M. Julliere, "Tunneling between ferromagnetic films," *Phys. Lett. A*, vol. 54, no. 3, pp. 225–226, Sep. 1975.
- [41] Y. Zhang et al., "Compact modeling of perpendicular-anisotropy CoFeB/MgO magnetic tunnel junctions," *IEEE Trans. Electron Devices*, vol. 59, no. 3, pp. 819–826, Mar. 2012.
- [42] L. Zhang et al., "Addressing the thermal issues of STT-MRAM from compact modeling to design techniques," *IEEE Trans. Nanotechnol.*, vol. 17, no. 2, pp. 345–352, Mar. 2018.
- [43] Z.-Y. Luo, Y.-J. Tsou, Y.-C. Dong, C. Lu, and C. W. Liu, "Field-free spin-orbit torque switching of perpendicular magnetic tunnel junction utilizing voltage-controlled magnetic anisotropy pulse width optimization," in *Proc. NVMTS*, Oct. 2018, pp. 1–5.
- [44] K.-S. Lee, S.-W. Lee, B.-C. Min, and K.-J. Lee, "Threshold current for switching of a perpendicular magnetic layer induced by spin Hall effect," *Appl. Phys. Lett.*, vol. 102, no. 11, p. 112410, 2013.
- [45] C. Zhang, S. Fukami, H. Sato, F. Matsukura, and H. Ohno, "Spin-orbit torque induced magnetization switching in nano-scale Ta/CoFeB/MgO," *Appl. Phys. Lett.*, vol. 107, no. 1, p. 012401, 2015.
- [46] R. C. O'Handley, "Classical and quantum phenomenology of magnetism," in *Modern Magnetic Materials: Principles and Applications*. Hoboken, NJ, USA: Wiley, 1999, p. 99.



YA-JUI TSOU (GS'17) received the B.S. degree in electrical engineering from National Cheng Kung University, Tainan, Taiwan, in 2016. He is currently pursuing the Ph.D. degree with the Graduate Institute of Electronics Engineering, National Taiwan University, Taipei, Taiwan.

His current research interests include the modeling of spin-transfer torque and spin-orbit torque MRAM, fabrication of magnetic tunnel junctions, ferromagnetic resonance, and GeSn/Ge gate-all-around transistors.



JIH-CHAO CHIU received the B.S. degree in mechanical engineering from National Taiwan University, Taipei, Taiwan, in 2018. He is currently pursuing the Ph.D. degree with the Graduate Institute of Electronics Engineering, National Taiwan University, Taipei, Taiwan.

His current research interests include the modeling and micromagnetic simulation of spin-transfer torque and spin-orbit torque MRAM.



HUAN-CHI SHIH received the B.S. degree in electrical engineering from National Taiwan University, Taipei, Taiwan, in 2018. He is currently pursuing the M.S. degree with the Graduate Institute of Electronics Engineering, National Taiwan University, Taipei, Taiwan.

His current research interests include the modeling of spin-transfer torque and spin-orbit torque MRAM.



CHEE WEE LIU (M'99–SM'00–F'18) received the B.S. and M.S. degrees in electrical engineering from National Taiwan University, Taipei, Taiwan, in 1985 and 1987, respectively, and the Ph.D. degree in electrical engineering from Princeton University, Princeton, NJ, USA, in 1994.

He is currently a Distinguished Professor with National Taiwan University. His current research interests include group IV (Si/SiGe/Ge/GeSn) CVD epitaxy, GAA/3D FETs, thermal modeling, MRAM, photonics, and IGZO TFT.