Received 17 May 2019; revised 28 June 2019; accepted 16 July 2019.
Date of publication 22 July 2019; date of current version 3 February 2020.

Digital Object Identifier 10.1109/JXCDC.2019.2930284

Design and Analysis of an Ultra-Dense, Low-Leakage, and Fast FeFET-Based Random Access Memory Array

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This work was supported in part by Applications and Systems-Driven Center for Energy-Efficient Integrated NanoTechnologies, one of six centers in the Joint University Microelectronics Program, a Semiconductor Research Corporation (SRC) program sponsored by the Defense Advanced Research Projects Agency.

ABSTRACT High static power associated with static random access memory (SRAM) represents a bottleneck in increasing the amount of on-chip memory. Novel, emerging nonvolatile memories such as spin-transfer torque magnetic random access memory (STT-RAM), resistive random access memory (RRAM), and ferroelectric field effect transistor-based random access memory (FeFET-RAM) are alternatives for replacing hardware kernels such as SRAM-based last level caches (LLC) due to their fast access times and lower leakage. In this paper, we study an ultra-dense FeFET-RAM based on 1-FeFET memory cells, and address potential disturbance issues at the array level. Disturbances are studied experimentally and via simulation. Experimental measurements are well correlated with modeling results suggesting that we have a good understanding of how disturbance issues will manifest themselves. That said, previous WRITE schemes for 1-FeFET arrays may: 1) exacerbate disturbances and 2) significantly degrade figures of merit (FoM) such as WRITE power. To address these issues, we propose the use of columnwise body connections to simultaneously overcome disturbances and reduce leakage currents during WRITES. We present detailed studies on how 1-FeFET memory cells and arrays (with columnwise body bias) fare when compared to traditional SRAM approaches and other emerging technologies. Notably, we benchmark the 1-FeFET memory against 1T + 1FeFET and 2T + 1FeFET designs proposed in early works, as well as SRAM, STT-RAM, and RRAM. Our evaluation of a 64×64 FeFET-RAM array shows that the area, READ delay, and static power are reduced by $\sim$5.3×, $\sim$1.5×, and $\sim$74×, respectively, when compared to an SRAM equivalent. Also, the 1-FeFET memory cell design shows $\sim$50× improvements in terms of WRITE energy with respect to STT-RAM and RRAM counterparts.

INDEX TERMS Emerging technologies, FeFETs, memory.

I. INTRODUCTION

In state-of-the-art processors, cache structures are typically comprised of complementary metal–oxide–semiconductor (CMOS) static random access memory (SRAM) cells. While transistor scaling has helped to reduce memory cost and improve cache capacity, low density and high leakage power associated with MOSFET SRAMs make it challenging to satisfy the growing memory demands from data intensive programs via 2-D CMOS-based SRAMs. The aforementioned challenges with SRAM have led to the search for alternative on-chip memory structures. Nonvolatile memories based on emerging technologies such as spin-transfer torque magnetic random access memory (STT-RAM), resistive random access memory (RRAM), and phase-change memory (PCM) have

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been exploited to build prototypes that could ultimately lead to the development of dense and power efficient on-chip memories [1]–[3]. That said, WRITES to memory cells based on resistive devices could be slow and demand significant energy, as long set/reset pulses with currents in the range of tens or even hundreds of micro Amperes are required. Furthermore, the low I_{ON}/I_{OFF} ratios for READ currents of resistive devices (on the order of 10^1–10^3) combined with process variations may result in degraded sensing margins.

Alternatively, ferroelectric field effect transistors (FeFETs) are emerging devices that offer unique possibilities for the design of ultra-dense, low-leakage, and fast RAMs. 32-MBit AND-type memory arrays comprised of single FeFET memory cells (1-FeFET) have been fabricated [4]. Although [4] seems to suggest that inhibition bias (IB) might be used to assist with the writing of different logic states in the cells in a 1-FeFET array, formal descriptions of WRITE schemes were not discussed. More recently, $(V_W/2)$ and $(V_W/3)$ IB WRITE schemes [5] for writing arrays based on 1-FeFET memory cells were considered [6]. However, [6] only includes the experimental results for a single 1-FeFET cell, and array writing is not evaluated. Even more importantly, the WRITE schemes as described do not consider the body voltage as an active part of the memory cell writing. As noted in [7], the body potential is critical for the correct operation of 1-FeFET memory arrays. An always-grounded body [6] may result in severe WRITE disturbance issues. In addition, high leakage currents due to forward bias between body-(source/drain) terminals are likely to arise during WRITE operations, leading to high WRITE power (as we will describe in Section III-C).

To combat these challenges, we propose a columnwise body connection that: 1) can solve the aforementioned (and severe) disturbance problems associated with previous $\pm(V_W/2)$ and $\pm(V_W/3)$ WRITE schemes and 2) reduce leakage currents during the WRITE operation by ensuring $V_b = V_s = V_d$ in all unselected cells in every column. Furthermore, we propose and evaluate a WRITE scheme ($(V_W/2)$ GS/B) that splits the $V_{g(s/b)}$ WRITE bias into two $V_g - V_{(s/b)}$ voltage components. We further leverage experimental results from a GLOBALFOUNDRIES prototype fabricated with bulk CMOS at the 28-nm technology node to analyze the effects of variations and disturbance on the sensing margin of 1-FeFET memory cells. We also employ a multi-domain Preisach-based model for FeFETs [8] to conduct a simulation-based case study of WRITE disturbances on a 2×2 array assuming the aforementioned WRITE schemes. Our results show a good correlation between experiments and simulations for the three WRITE schemes evaluated.

After addressing impediments to array functionality, i.e., disturbance issues, we perform SPICE simulations using the aforementioned model to compare the energy and latency of the 1-FeFET memory cells with two other FeFET-based memory cells. We compare FeFET-based designs with designs based on SRAM, STT-RAM, and RRAM through simulations with SPICE models [9]–[11]. This design space exploration suggests that the READ energy of the FeFET-based memory cells is comparable with other technologies. Moreover, even when we consider columnwise body connections (proposed to alleviate disturbance issues), the area of a 1-FeFET memory array is only ~19% of the area of a conventional 6T-SRAM array. In addition, WRITE energy and leakage power is reduced by ~50× and ~74× when compared to STT-RAM/RRAM and SRAM, which makes 1-FeFET-based FeFET-RAMs promising candidates for the design of last level caches (LLCs) that demand high speed, high density, and low leakage.

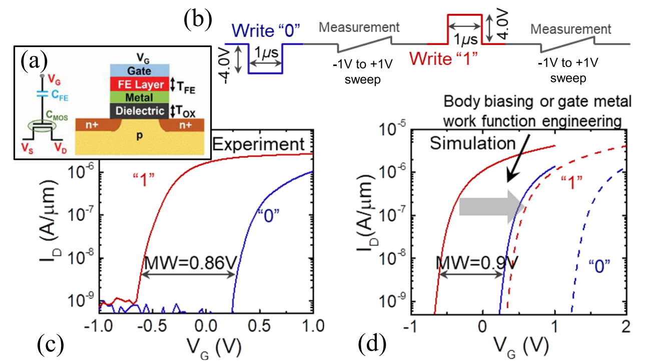


FIGURE 1. (a) Equivalent circuit and physical structure of a FeFET. (b) Applied gate waveform for FeFET characterization. (c) Experimentally measured and (d) simulated *I–V* characteristics of a FeFET device. Hysteresis shift by body biasing or gate metal work function engineering is possible.

II. BACKGROUND AND RELATED WORK

Here, we discuss FeFET device structures and device models. We also review related work on emerging dense and low-leakage memories that could replace SRAM caches.

A. A FeFET DEVICE

Structurally, a FeFET resembles a MOSFET, except a layer of FE oxide is deposited in the gate-stack. The equivalent circuit for a FeFET appears in Fig. 1(a), where we represent the FE and CMOS capacitances as C_{FE} and C_{CMOS}. The coupling between these capacitances can lead to a hysteretic effect, and hence nonvolatility. Fig. 1(b) illustrates −4 V/+4 V and −1 V/+1 V pulses that can be used to WRITE and READ FeFET state (respectively). Fig. 1(c) depicts the I_D versus V_{GS} characteristic of a FeFET device measured via experiments [8]. The information stored in a FeFET corresponds to one of two possible states—logic "0" (high V_{TH}) and logic "1" (low V_{TH}). A sufficiently wide memory window (MW) of ~0.86 V separates the two states, and I_{ON}/I_{OFF} ratios on the order of 10^4 are observed.

B. FeFET MODELS

A model based on the time-dependent Landau Khalatnikov (LK) equations [12] has been used to describe the switching behavior of FeFETs [13]–[15]. However, actual FE switching dynamics are not easily modeled by the LK equation, which

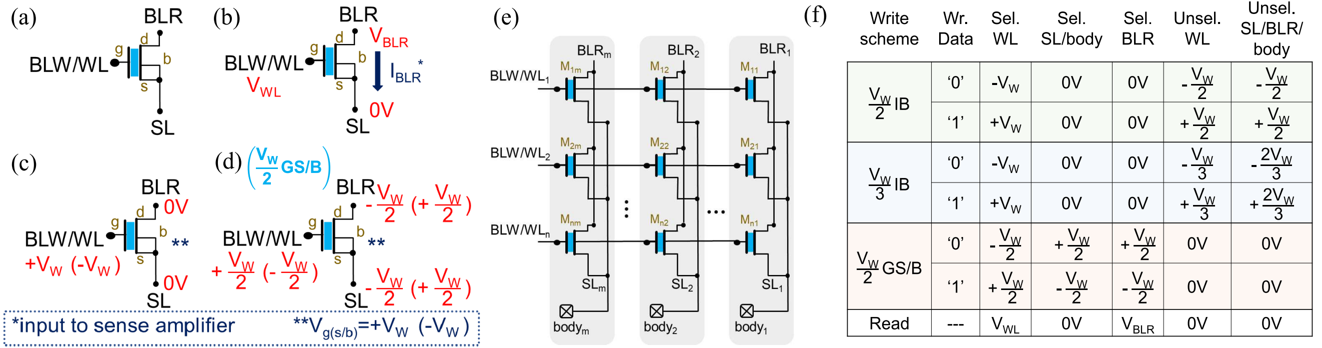


FIGURE 2. (a) 1-FeFET memory cell with its three-terminal connections, along with (b) READ scheme, as well as (c) conventional and (d) ($V_W/2$) GS/B WRITE schemes. (e) AND-type FeFET-RAM array with *n* rows and *m* columns based on 1-FeFET memory cells is also shown. (f) Three array WRITE schemes (($V_W/2$) IB, ($V_W/3$) IB, and ($V_W/2$) GS/B) are described in detail. The columnwise body and source connections allow the writing of individual target cells while avoiding source-body forward bias that may cause leakage and damage to the content of neighbor memory cells.

assumes a single-domain ferroelectric (FE) material with a single coercive field for the whole FE thin film. More specifically, phenomena such as nonsaturated hysteresis loops, history effects, and polarization switching dynamics cannot be captured by the LK model.

These issues are addressed by an FeFET compact model [8] based on the Preisach theory. A Preisach-based multi-domain model was derived from the experimental data and is employed in this work. Unlike the single-domain LK model, the Preisach model can reproduce characteristics of fabricated FE devices. It assumes an FE film with multiple-independent single crystal domains with a distribution of coercive fields. Thus, the model captures the behavior of saturated and nonsaturated hysteresis loops. It also tracks FE history by employing an efficient turning-point tracking algorithm [16]. The model successfully reproduces the FE behavior by combining the aforementioned characteristics with a delay unit that can model the polarization switching dynamics. The Preisach-based model was employed in recent work with FeFETs, for logic-in-memory designs, e.g., in [17]. Fig. 1(d) depicts the I_D versus V_{GS} characteristic of a FeFET device simulated with the Preisach model. The threshold voltage (V_{TH}) could be shifted through body biasing or gate metal work function engineering to meet requirements of particular designs. (We assume that V_{TH} has been shifted to enable a READ voltage in the range of 0.5–1.0 V.) Simulation results are aligned to those from experiments, which are depicted in Fig. 1(c).

C. RELATED WORK: DENSE ON-CHIP MEMORIES

Leakage currents and large area footprints of SRAM present a challenge for designing large size LLC. Some works have proposed replacing SRAM LLC by emerging (volatile or nonvolatile) memories. Recently, IBM released its POWER9 processor chip [18], which offers a 120-MB fast-access embedded dynamic random-access memory (eDRAM) LLC. Despite high density, the volatile nature of eDRAM requires periodic data refreshing, which might incur a significant amount of energy overhead.

Alternatively, nonvolatile memories based on emerging devices are promising candidates for improving CMOS-based on-chip memories. RRAM, STT-RAM, and FeFET-RAM memory designs have been proposed [1], [2], [4], [19]–[26]. Although resistive devices such as memristors and magnetic tunnel junction (MTJs) can be used to design structures such as LLCs, high currents, and long latency pulses are required for writing—and the WRITE energy of 1T + 1R ReRAM or 1T+1MTJ STT-RAM cells can be ∼100× greater than a 6T-SRAM [27].

FeFET-RAM memories could combine attractive features of resistive memories (fast access, low leakage, and high density), with lower WRITE energies due to their inherent MOSFET-like switching mechanism. Related work has employed the single-domain LK model to design 2T + 1FeFET and 1T+1FeFET memory cells that are used to build AND-type arrays [28], [25]. Although these memory designs provide advantages over STT-RAM/ RRAM/ CMOS-based SRAM, their density can be further improved. A higher density FeFET-based NOR-type memory comprised of 1-FeFET memory cells was proposed in [26]. However, the FeFETs employed there are very scaled devices (at 10 nm) that have significant less FE domains to be flipped during WRITES compared to FeFETs employed here (at 22 nm). Ultimately, different FeFET models may be required to describe both devices.

D. 1-FeFET MEMORY CELL

A higher density FeFET-based NOR-type memory comprised of 1-FeFET memory cells was proposed in [26]. However, there is no evaluation of possible disturbs caused by WRITE and READ mechanisms. In addition, AND-type arrays based on 1-FeFET memory cells have been proposed and fabricated [4]. The latter work has no discussion on WRITE schemes and benchmarking results, which are the focus of this paper.

A typical 1-FeFET memory cell (used in both NOR-type and AND-type arrays) is depicted in Fig. 2(a). The drain (d) of the FeFET is associated with the READ bitline (BLR) of

a memory cell, while the source (s) and body (b) terminals of the FeFET are both connected to the sourceline (SL). The FeFET gate (g) serves as both WRITE bitline (BLW, when writing) and wordline (WL, when reading). The READ operation for a 1-FeFET memory cell is depicted in Fig. 2(b). A suitable bitline READ voltage V_{BLR} is provided by a precharge circuit. The resulting current (I_{ON} or I_{OFF}) depends on the logic state previously stored in the FeFET device and can be sensed by a sense amplifier (SA). The memory cell can be selected for reading through the application of a wordline READ voltage V_{WL} within the MW of the FeFET. Both simulation and experimental results (to be presented in Section IV) suggest I_{ON}/I_{OFF} ratios on the order of 10^4. A writing scheme for a single 1-FeFET memory cell is shown in Fig. 2(c). The scheme assumes the application of the full value of V_W (typically, $\pm 4V$ [8]) to the gate of the FeFET. Source, drain, and body must be grounded at all times during the WRITE operation, so $V_{g(s/b)} = \pm V_W$.

Finally, endurance and retention time of 1-FeFET memory cells are discussed in [4] and [29]. At present, up to 10^5 endurance cycles and 7 days retention can be realized for a 1-FeFET memory cell [4]. However, the experimental data from [29] suggests that as many as 10^{12} endurance cycles may be possible.

III. 1-FeFET MEMORY DESIGN

Ultradense 1-FeFET memories have to deal with disturbance issues due to the absence of access transistors. Hence, efficient WRITE schemes represent a necessary step toward advancing the state-of-the-art of FeFET memories. In this section, we introduce a new $(V_W/2)$ GS/B WRITE scheme for 1-FeFET AND-type arrays that could alleviate disturbance issues without compromising scalability. Furthermore, we propose the use of columnwise body connections in $(V_W/2)$ IB and $(V_W/3)$ IB WRITE schemes that can also address the disturbance problem. Finally, we analyze the implication of WRITE disturbs and variations on the sensing margin of FeFET-RAMs.

A. $(V_W/2)$ GS/B WRITE SCHEME

We propose a new WRITE scheme which supports simplified 1-FeFET memory array design. Specifically, the proposed $(V_W/2)$ GS/B WRITE scheme [Fig. 2(d)] requires us to set $V_{g(s/b)} = \pm V_W$ by simultaneously applying half of V_W ($\pm(V_W/2)$) to BLW, and an opposite voltage to SL and body in order to WRITE the memory cell. Different from the WRITE scheme in Fig. 2(c), the $(V_W/2)$ GS/B WRITE scheme does not require modifications in order to work in arrays, as demonstrated in Section III-C. Routing and peripheral circuitry design could be simplified when we employ the $(V_W/2)$ GS/B WRITE scheme, as additional voltage levels for IB are not necessary.

B. WRITE DISTURBANCES

WRITE disturbances—where a bit stored in a memory cell is changed as other bits are written—are a well-studied issue that could occur in memory arrays comprised of many different technologies, including SRAM, STT-RAM, and RRAM. As FeFET devices can enable the design of memory cells with decoupled READ and WRITE paths, WRITE disturbances could be less prevalent compared with other memory technologies. In more detail, disturbances do not occur in previous 1T + 1FeFET [25] and 2T + 1FeFET [28] memories as there is always a WRITE access transistor that is turned off to avoid accidental changes in data as other cells in the memory array are written. That said, 1-FeFET memories are subject to WRITE disturbances due to the absence of access transistors. We elaborate this point in the detailed studies based on both experimental results and simulations (see Section IV).

C. ARRAYS BASED ON 1-FeFET MEMORY CELLS

Body bias has a significant impact on the writing of 1-FeFET memory cells, with consequences to the design of FeFET-RAM arrays. We describe the body bias issue in more detail in the following. We then discuss modifications to the $(V_W/2)$ IB and $(V_W/3)$ IB WRITE schemes [6], [7] and demonstrate how the $(V_W/2)$ GS/B scheme can be used in FeFET-RAM arrays.

Prior work with 1-FeFET arrays does not consider the body as an active part of writing. The work in [26] does not discuss the role of body voltage when writing an FeFET. IB WRITE schemes for AND-type arrays with structures similar to Fig. 2(e), but with a body potential fixed at 0 V is described in [6]. A writing voltage of $\pm V_W$ is applied to the BLW of the target cell, along with an IB of either $\pm(V_W/2)$ or $\pm(V_W/3)$ at the BLWs, SLs, and BLRs of all unselected 1-FeFET cells. Identical WRITE schemes are also employed in [7]. In [7], the writing schemes discussed either assume a body fixed at 0 V or that is connected to a common a common substrate bias.

Correct biasing of the body is crucial to guarantee the correct writing of 1-FeFET memory cells in the FeFET-RAM array, as gate-body potential mainly determines the voltage drop across the FE layer [7]. Fixing the body potential at 0 V may lead to two critical issues. First, due to the nature of a shared BLW in AND-type arrays, unselected memory cells in the same row as the target cell share a common gate-body potential V_{gb} of $\pm V_W$. Therefore, writing a target cell could change the state of unselected cells in the same row. Second, the WRITE schemes discussed in [6] and [7] adopt IBs of either $\pm(V_W/2)$ or $\pm(V_W/3)$ applied to the SLs and BLRs of all unselected 1-FeFET cells. As a result, when IBs are negative, there could be forward biases between body to drain and source—i.e., either $V_{b-(s/d)} = (V_W/2)$ or $V_{b-(s/d)} = (V_W/3)$, leading to high currents during the WRITE operation. Ultimately, the power consumption of 1-FeFET arrays may be adversely impacted.

We modify the $(V_W/2)$ IB and $(V_W/3)$ IB WRITE schemes from [6], [7] as presented in Fig. 2(e) and (f). Essentially, we propose connecting source and body terminals in every column to ensure $V_b = V_s = V_d$ in all cells. To WRITE logic "1"("0") in the selected cells, we apply V_W $(-V_W)$

to the BLW while grounding the SLs (and bodies). To avoid data loss due to WRITE disturbances, we set the voltage at the BLWs, SLs, and bodies of unselected cells to $\pm(V_W/2)$ and $\pm(V_W/2)$ for $(V_W/2)$ IB, or $\pm(V_W/3)$ and $\pm(2V_W/3)$ for $(V_W/3)$ IB. A third WRITE scheme suitable for arrays is also possible. The scheme is a direct application of the $(V_W/2)$ GS/B WRITE scheme (presented in Section III-A) to FeFET-RAM arrays. We apply opposite $\pm(V_W/2)$ voltages to the BLW, SL, and body of selected cells while grounding the corresponding terminals of unselected cells. We note that while the $(V_W/2)$ GS/B and $(V_W/2)$ IB schemes produce the same level of WRITE disturbance for unselected cells in an array (details in Section IV-C), the proposed $(V_W/2)$ GS/B WRITE scheme requires less complicated peripheral circuitry as dedicated voltage levels for IB are not required.

Our proposed columnwise body could solve the aforementioned issues associated with $(V_W/2)$ and $(V_W/3)$ schemes [6], [7]. In this work, the column body potentials are always equivalent to the voltages applied to SLs, which has two significant implications. First, by separating the body in every column, we are able to individually control V_{gb} of unselected cells that share a common BLW with target cells during writing. The IB applied to SLs are also equivalent to the body potential, leading to gate-body potentials V_{gb} of $\pm(V_W/2)$ $(\pm(V_W/3))$ as opposed to $\pm V_W$. Our evaluation results (Section IV) suggest that $V_{\text{gb}} = \pm(V_W/2)$ $(V_{\text{gb}} = \pm(V_W/3))$ do not result in the destruction of logic states in unselected cells. A second implication is that forward biases between body and source/drain of the FeFETs are eliminated, as this approach ensures $V_b = V_{s/d}$. High leakage currents that lead to high WRITE energy no longer exist in $(V_W/2)$ IB, $(V_W/3)$ IB, and $(V_W/2)$ GS/B WRITE schemes, resulting in low WRITE power as suggested by our simulation-based case study for a 64×64 1-FeFET array (Section IV-C).

We note that selective body bias techniques have been successfully applied to control leakage and improve margins of SRAM memories [30]. In addition, previous work on 1-FeFET arrays has proposed to use a fixed body bias to alleviate WRITE disturbance issues [7]. However, to the best of our knowledge, this is the first work that proposes columnwise, dynamic control of body potential to enable WRITE operations in 1-FeFET arrays.

D. VARIABILITY

FeFET-RAMs based on 1-FeFET memory cells may also contend with variability. While the analysis in [4] considers device-to-device process variations, we focus on cycle-to-cycle variations, *i.e., changes in V_{TH} for one device, when programmed or erased under the same conditions, and in different cycles*. Cycle-to-cycle variations could lead to nonuniform lengths of the MW that might ultimately cause degradation of $I_{\text{ON}}/I_{\text{OFF}}$ ratios, especially at the boundaries of the low and high V_{TH} states. Implications of cycle-to-cycle variations in the design of 1-FeFET memories are presented in Section IV-B.

IV. EXPERIMENTAL AND SIMULATION-BASED VALIDATION

We leverage experiments with a GLOBALFOUNDRIES and-type array prototype fabricated with bulk CMOS at the 28-nm technology node. The memory cell dimensions are $W/L = 500/500$ *nm*. Here, we analyze the effects of $\pm(V_W/2)$ and $\pm(V_W/3)$ disturbs, as well as cycle-to-cycle variations on the sensing margin of 1-FeFET memory cells. Furthermore, we perform SPICE simulations in order to evaluate the WRITE disturbance resulting from $(V_W/2)$ IB, $(V_W/3)$ IB, and $(V_W/2)$ GS/B WRITE schemes in 2×2 memory arrays.

A. WRITE DISTURBANCE IN 1-FeFET MEMORY CELLS

We performed experiments with the aforementioned prototype to investigate the effects of disturbs in 1-FeFET memory cells. In our experiments, logic "0"("1") is written to a 1-FeFET memory cell through a −4.5 V(+4.5 V) pulse of 500-ns duration applied to the gate of the FeFET. Disturb pulses of the same length with $\pm(V_W/2)$ and $\pm(V_W/3)$ amplitudes are applied to the gate of the memory cell for 10^6 consecutive cycles. Source, drain, and body are grounded. The value of V_{TH} is periodically measured. Fig. 3(a) shows V_{TH} versus disturb cycles for $\pm(V_W/2)$ and $\pm(V_W/3)$ biases. There are little changes to V_{TH} of the FeFET for $\pm(V_W/3)$ bias for the first ten disturb cycles. Regarding the experiment with $\pm(V_W/2)$ biases, there is degradation of logic "0" and "1" states in the initial disturb cycles (the more pronounced degradation is for the logic "1" state). We note that the effect of charge trapping [31] is responsible for the nonmonotonic behavior of V_{TH} when logic "1" is disturbed with negative pulses, which may be observed from cycle 10^3 (10^5) in the experiments with $\pm(V_W/2)$ $(\pm(V_W/3))$ biases. Fig. 3(b) shows the effect of $(-V_W/2)$ $(+V_W/2)$ disturbs on I_D versus V_G of the FeFET for logic "1" (logic "0") states. Note that the most significant degradation of the sensing margin occurs after 10^2 (10^4) disturb cycles for $\pm(V_W/2)$ $(\pm(V_W/3))$ biases, suggesting that the use of $\pm(V_W/3)$ WRITE scheme (with columnwise body connections) makes 1-FeFET memory cells quite tolerant to disturbs.

B. CYCLE-TO-CYCLE VARIATIONS

We studied cycle-to-cycle variations experimentally in the aforementioned prototype. We monitor the I_D current of high and low V_{TH} states, i.e., logic "0" and "1," of the same device for 50 program/erase cycles. Variations must be considered when designing 1-FeFET-based memory arrays, as they might cause the MW of FeFET devices to shrink, ultimately degrading their sensing margins. Our results [depicted in Fig. 3(c)] show that although the MW of 1-FeFET memory cell becomes slightly narrower, there is no overlap between the boundaries of high and low V_{TH} regions. For the device tested, a suitable value for V_{WL} is 0.8 V, which is the middle of the MW.

*measurements use a -1V to 1V pulse sweep

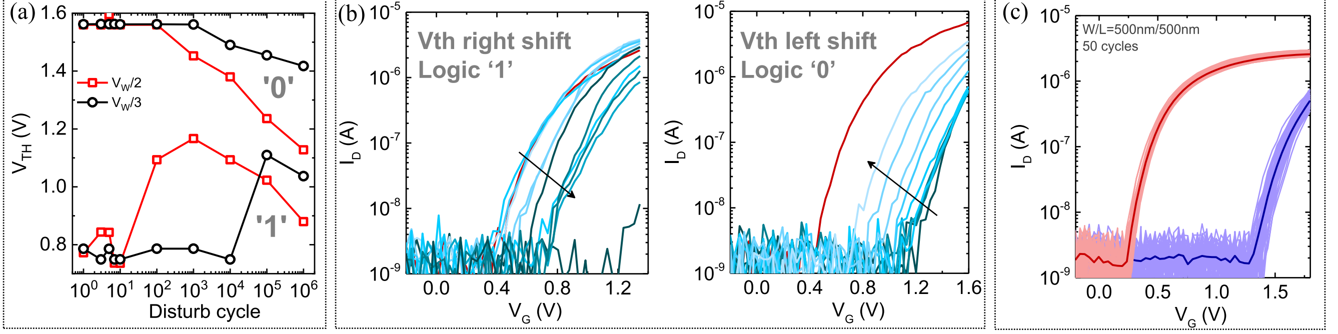


FIGURE 3. (a) Experimental results for 10^6 cycles of $\pm V_W/2$ and $\pm V_W/3$ disturbances in logic state "1" ("0"). (b) Graphs of I_D versus V_G show logic states "1" and "0" (blue curves) that are shifted to the right and left, respectively, with $\pm V_W/2$ disturbances (memory cells always get disturbed by logic states that are opposite to what is stored in the memories). Red line: low V_{TH} reference. (c) Experiments* demonstrate that the MW of a 1-FeFET memory cell may shrink due to cycle-to-cycle variations. Therefore, a suitable READ voltage needs to be chosen carefully.

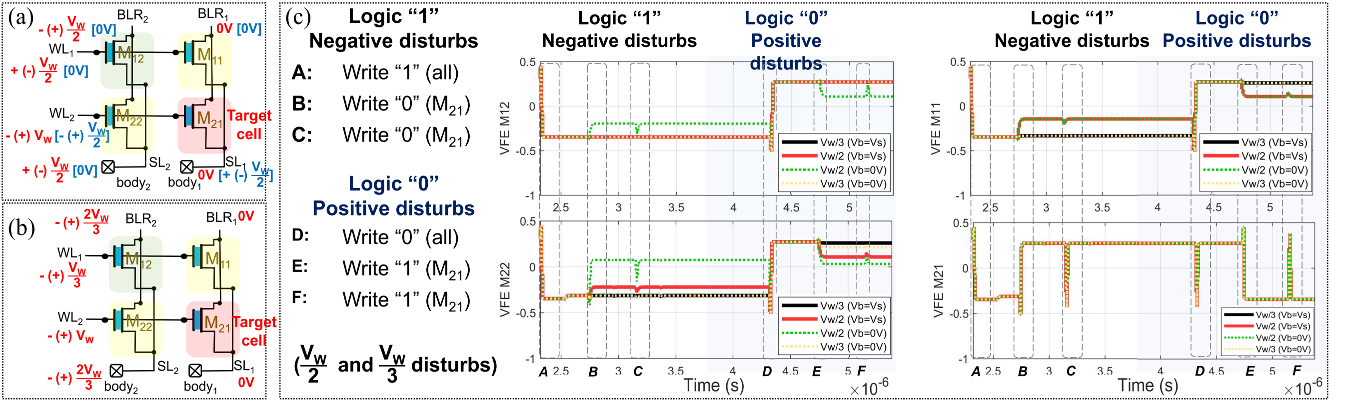


FIGURE 4. WRITE disturbance simulation-based case study for (a) ($V_W/2$) IB, [($V_W/2$) GS/B] and (b) ($V_W/3$) IB WRITE schemes. (c) Steps are listed from "A" to "F." Initially, all cells store "1" ("0"), then "0" ("1") is written to the target cell (M_{21}) twice. The waveforms depict voltage across FE (V_{FE}) versus time for each memory cell. When $V_b = V_s$, disturbances are expected in M_{11} and M_{22}. M_{12} is disturb-free due to its position in the array. When $V_b = 0V$, severe disturbance is expected for M_{22}, as its WL is shared with the target cell (M_{21}).

C. WRITE DISTURBANCE IN 1-FeFET MEMORY ARRAYS

To evaluate the impact of WRITE disturbance on the sensing margins of arrays, we perform SPICE simulations of ($V_W/2$) IB, ($V_W/3$) IB, and ($V_W/2$) GS/B WRITE schemes assuming a 2 × 2 array based on 1-FeFET memory cells (see Fig. 4). Specifically, M_{21} is the target cell to be written and we study the disturbances on the rest of the three cells. We employ the multi-domain FeFET model described in Section II and use a 22-nm PTM as our underlying MOSFET model [9]. Note that experimental evaluations of disturbance and variations (described in Sections IV-A and IV-B) were performed on a 28-nm GLOBALFOUNDRIES prototype, therefore in a different technology node than used in simulations. Although this fact might lead to some differences between the results of experiments and simulations, we do not expect major mismatches in the behavior of 1-FeFET memories that are based on these two different technology nodes. The choice of 22-nm PTM as underlying MOSFET model for simulations was due to its open-access feature.

We simulate ($V_W/2$) IB, ($V_W/3$) IB, and ($V_W/2$) GS/B WRITE schemes employing the columnwise body with a potential equal to SL, which ensures that the contents of unselected cells are not accidentally changed by undesirable V_{gb} biases. As a sanity check, we also simulate ($V_W/2$) IB and ($V_W/3$) IB WRITE schemes *without* columnwise body connections as proposed in [6] and [7], i.e., with body potential fixed at 0 V.

We show the results of WRITE disturbance evaluation for ($V_W/2$) IB,[($V_W/2$) GS/B] and ($V_W/3$) IB disturbs in Fig. 4(c). The two cases evaluated are: 1) negative disturbances in state "1" (produced by ($-V_W/2$) and ($-V_W/3$) biases) and 2) positive disturbances in state "0" (produced by ($+V_W/2$) and ($+V_W/3$) biases), as explained in Fig. 4(c). We verify in our tests that the disturbance caused by ($V_W/2$) IB and ($V_W/2$) GS/B with columnwise body are identical, since both WRITE schemes lead to the $V_{g(s/b)}$ bias of $\pm(V_W/2)$ in the same unselected cells of the array.

The graphs in Fig. 4(c) show the voltage across the FE (V_{FE}) versus time for M_{11}, M_{12}, M_{21}, M_{22} memory cells in a sequence from "A" through "F" of the simulation-based case study. Logic "1" is written in all cells ("A"), then a logic "0" is written to the target cell twice ("B," "C"). The process is

repeated with inverted logic values from "D" to "F." V_{FE} is directly related to the FE polarization that encodes logic states "0" and "1," therefore an excessive degradation of V_{FE} due to the writing of neighbor memory cells may result in data destruction. The cells could be subject to $\pm(V_W/2)$ (red solid/green dotted line) or $\pm(V_W/3)$ (black solid/ yellow dotted lines) $V_{g(s/b)}$ biases due to the writing of the target cell (M_{21}).

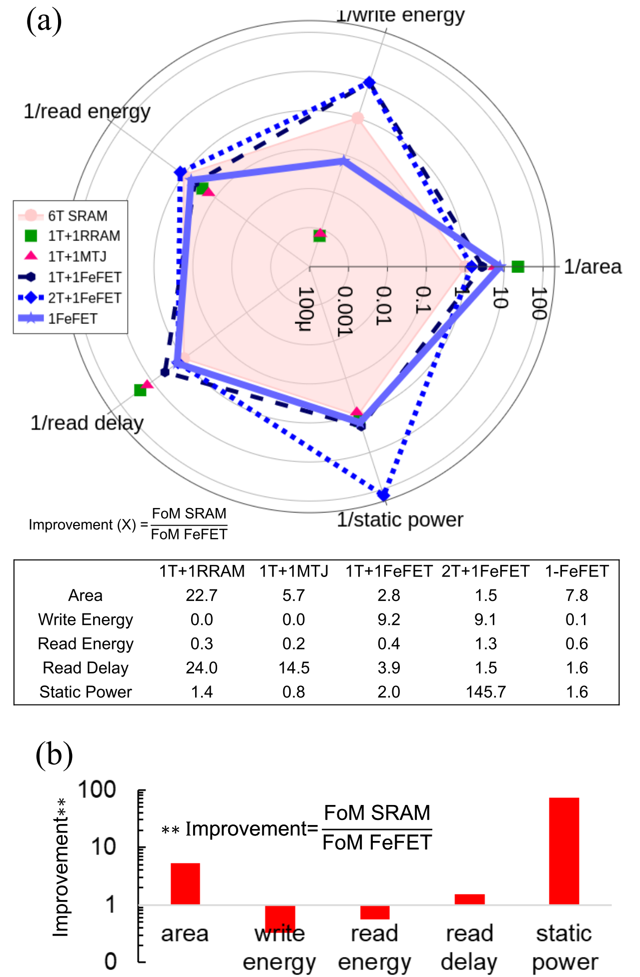
When considering the case of $V_b = 0V$, we note a degradation of V_{FE} in M_{12} and M_{22} memory cells for $(-V_W/2)$ disturbs (see green dotted line in Fig. 4, at "B"). A severe V_{FE} degradation that could potentially lead to loss of the data occurs in M_{22}. This cell share its BLW with M_{21} (target cell). When analyzing the results with $V_b = V_s$ (columnwise body), we observe that a $\pm(V_W/3)$ $V_{g(s/b)}$ bias does not lead to changes in the V_{FE} of unselected cells (M_{11} and M_{22}) during the WRITE of the target cell (M_{21}) in steps "B," "C," "E," or "F." However, when the same cells have $V_{g(s/b)} = \pm(V_W/2)$, there are significant changes in the V_{FE} levels of their FeFETs during steps "B" or "E," which correspond to the first writing of the M_{21} memory cell. During the second WRITE of M_{21} (steps "C" or "F"), the V_{FE} disturb is less severe, although still present. We note that the observed degradation of READ margins when $V_{g(s/b)} = \pm(V_W/2)$ do not lead to loss of the data stored in unselected cells, i.e., there is still a minimum margin of 30% for two distinguishable logic states (without an overlap) even given disturbances. *Notably, array-based simulation studies with columnwise body are well-aligned to the experimental data presented in Section IV-A.*

V. BENCHMARKING

After demonstrating that 1-FeFET memories can tolerate WRITE disturbances in an efficient manner (i.e., via a column bias)—as we must ensure a memory array functions correctly—we then evaluated 1-FeFET memories at the cell and array levels. We compare the energy, latency, and area of FeFET-based memory cells to 6T-SRAM, 1T + 1MTJ STT-RAM, and 1T + 1R RRAM cells, as well as 1T + 1FeFET [25] and 2T + 1FeFET [28] memory cell designs. We employ SPICE simulations with the multi-domain FeFET model described in Section II, and PTM models per Table 1, which summarizes simulation setups for different memory cells considered in our evaluation. We also extend our cell-level comparison to 64 × 64 arrays based on 1-FeFET and 6T-SRAM memory cells. We are aware that FeFETs require a high voltage for writing, which may inccur in overheads in the design of periphery circuits. Similarly, RRAM and STT-RAM would also require special writing circuits to generate high WRITE currents. Nonetheless, our evaluation includes only energy from memory cells for all technologies and excludes the impact of peripherals, which will be studied in future work.

A. MEMORY CELLS OF VARIOUS TECHNOLOGIES

The radar plot depicted in Fig. 5(a) shows the comparison of a 1-FeFET memory cell to other memory cells that may be



	1T+1RRAM	1T+1MTJ	1T+1FeFET	2T+1FeFET	1-FeFET
Area	22.7	5.7	2.8	1.5	7.8
Write Energy	0.0	0.0	9.2	9.1	0.1
Read Energy	0.3	0.2	0.4	1.3	0.6
Read Delay	24.0	14.5	3.9	1.5	1.6
Static Power	1.4	0.8	2.0	145.7	1.6

FIGURE 5. (a) Benchmarking of the 1-FeFET memory cell against 6T-SRAM (baseline, gray-shaded), 1T + 1R RRAM, 1T + 1MTJ STT-RAM, 1T + 1FeFET [25], and 2T + 1FeFET [28]. (b) Figures of merit (FoMs) for a 64 × 64 arrays of 1-FeFET and SRAM.

employed to build high-density arrays. We use a 6T-SRAM memory cell [36] as the baseline for our comparison. When comparing across FeFET-based memory cells, we note that access transistors increase the series resistance at WRITE/READ bitlines, resulting in considerably lower WRITE energy. When compared to memory cells based on other emerging technologies such as STT-RAM and RRAM, 1-FeFET and other FeFET-based cells enable WRITE energy reductions of up to 50× with comparable latency and with similar (and often better) areas. Indeed, one obvious advantage of 1-FeFET memories compared to 6T-SRAM and previous FeFET-based memories is lower area. Fig. 6 depicts the layout of 1-FeFET memory cells and arrays, as well as the layout of a baseline 6T-SRAM [36]. Note that when accounting for area, we include routing overhead for bitlines and wordlines in both 1-FeFET and 6T-SRAM memory cells. When considering a single memory cell, a 1-FeFET cell is 8.7× denser than a 6T-SRAM. Notably, 1-FeFET arrays that adopt columnwise body connections to alleviate disturbance issues need to ensure independent body potentials in each column. Hence,

TABLE 1. Simulation setups for memory cells of various technologies used in our benchmarking.

	6T-SRAM	1T-1R	1T-1MTJ	2T+1-FeFET	1T+1FeFET	1-FeFET
Model	CMOS ASU PTM 22 nm [9]	RRAM ASU [11] w/ PTM 22 nm	MTJ ASU [10] w/ PTM 22 nm	Multi-domain [8] PTM 22 nm	Multi-domain [8] PTM 22 nm	Multi-domain [8] PTM 22 nm
Cell area	$2000\lambda^2$	$88\lambda^2$	$350\lambda^2$	$1366\lambda^2$	$720\lambda^2$	$256\lambda^2$
Write voltage and time[a]	1V @1ns	2V @10ns	1.8V @10ns	±4V @10ns	±4V @10ns	±4V @10ns
Read voltage and time[a]	1V @1ns	1V @1ns	1V @1ns	1V @1ns	1V @1ns	1V @1ns
I_{ON}/I_{OFF} ratio	$> 10^4$	10^2	1.8	10^4	10^4	10^4
Endurance	∞	10^6[32] – 10^{10}[33]	up to 10^{12}[34]	10^7[35] – 10^{12}[29]	10^7[35] – 10^{12}[29]	10^7[35] – 10^{12}[29]

[a] In this context, the terms write and read time refer to duration of the pulse applied to memory wordlines.

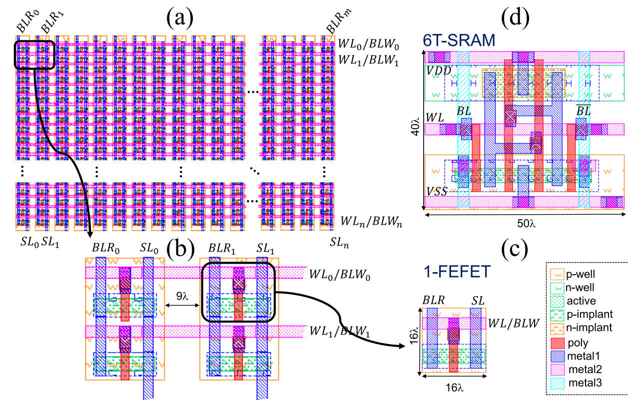


FIGURE 6. (a) *n* x *m* 1-FeFET array, where (b) 2 x 2 array section is highlighted. Columnwise body bias requires separate P-wells with minimum spacing between columns. (c) 1-FeFET memory cell area is 256λ^2, in contrast to 2000λ^2 of (d) layout of baseline 6T-SRAM adapted from [36].

a minimum spacing of 9λ between separate P-wells has to be respected. This leads to a slight reduction in density improvements (from 8.7× to 5.3×).

B. 64 x 64 ARRAYS

We also designed and simulated 64 × 64 memory arrays based on 6T-SRAM and 1-FeFET memory cells. We measure leakage power, dynamic energy, and latency for READ and WRITE operations. Per the results reported in Fig. 5(b), we note that READ delay and energy of 1-FeFET arrays are comparable to an SRAM equivalent. The impact of biased bodies was considered in the simulation results presented. Toggling the body in different columns potentially leads to an increase in dynamic energy, which accounts for the READ energy overhead of 1-FeFET arrays when compared to SRAM. Finally, although SRAM outperforms 1-FeFETs for WRITE energy, arrays based on 1-FeFET could reduce static power consumption by ∼74× when compared to SRAM, due to FeFET nonvolatility. These results make FeFET-based memories an attractive option for low-leakage LLCs where WRITES are not as frequent as in higher level caches.

VI. CONCLUSION

In this paper, we presented a columnwise body connection that enables three distinct WRITE schemes suitable for arrays based on 1-FeFET memory cells. We showed a detailed simulation-based case study of the WRITE disturbance of a 2 × 2 array, validating our observations with experimental results from a GLOBALFOUNDRIES prototype fabricated with bulk CMOS at the 28-nm technology node. We also discussed and evaluated cycle-to-cycle variations in 1-FeFET memory cells. Our results for a 64 × 64 array show area reductions of at least 5.3× when comparing the 1-FeFET to a conventional SRAM that employs 6T memory cells. READ delay and leakage are also reduced by 1.5× and 74×, respectively. Finally, the 1-FeFET memory cell design shows ∼50× of improvement in terms of WRITE energy with respect to STT-RAM and RRAM due to the voltage-based nature of FeFET writing mechanism.

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