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Complementary Logic Implementation for Antiferromagnet Field-Effect Transistors

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ABSTRACT In this paper, a compact and complementary logic implementation is proposed for antiferromagnet field-effect transistor (AFMFET) devices. The implementation enables a complete set of Boolean operations based on complementary logic as well as majority-gate logic. The impacts of several key device-level design parameters are investigated, such as the channel resistance and critical switching voltage, and their optimal values that minimize the overall energy-delay product (EDP) of a 32-bit arithmetic logic unit are quantified. In addition, it is shown that one can potentially take advantage of the large domain size of some AFM materials such as chromium and build a compact majority-gate-based logic. The potential performance benefits of the majority-gate-based logic are also quantified. Compared to the conventional CMOS logic circuit, the one with AFMFET devices using majority gates can potentially achieve 10× improvement in terms of the EDP.

INDEX TERMS Antiferromagnet field-effect transistor (AFMFET), complementary logic, majority-gate logic, performance analysis.

I. INTRODUCTION

Thereis a global search for beyond-CMOS logic devices that can complement or even replace CMOS technology to alleviate the scaling challenges and sustain the exponential growth in chip throughput [1]–[4]. Magnetic devices have been at the center of this search as they provide new features, such as nonvolatility and low-voltage operation [5], [6]. One set of the spintronic devices are current driven, and some of the well-studied device concepts in this category include all-spin logic (ASL), charge-coupled spin logic, and domain wall logic devices [7]–[9]. However, the high current densities in current-driven devices increase the power dissipation, cause the reliability issues, and lead to large static power dissipation.

To improve the computing energy efficiency, voltage-controlled spintronic devices have been proposed. Some promising candidates include magnetoelectric magnetic tunnel junction (MEMTJ) devices, spin wave device (SWD), and composite-input magnetoelectric-based logic technology (CoMET) [10]–[12]. From a recent beyond-CMOS device benchmarking research, voltage-controlled spintronic devices are expected to dissipate the orders of magnitude less energy per binary switching operation compared to current-controlled magnetic devices [13]. However, the most magnetic device concepts proposed so far are based on the switching of the magnetization of ferromagnets. The ferromagnet switching time is in the order of nanoseconds [14], [15], which is orders of magnitude slower compared to the conventional charge-based FETs. This large switching delay also leads to the increased energy dissipation due to the leakage power in the readout circuitry [7]–[9].

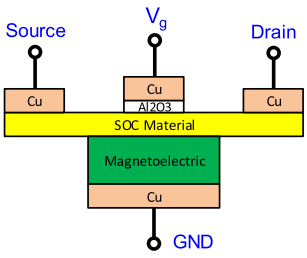

FIGURE 1. Schematic of AFMFET device [16].

To further improve the performance in terms of the switching speed, a recent study proposed an antiferromagnet field-effect transistor (AFMFET) device [16] whose schematic is shown in Fig. 1. By applying an input voltage on the gate, the magnetic order of the AFM layer is switched by the generated electrical field. The uncompensated

surface magnetization of the AFM is tied to the magnetic order, polarizes the spins of carriers in the spin–orbital coupling (SOC) channel, and induces a preferred direction for conduction, i.e., either from source to drain or drain to source. This way, the polarity of the voltage applied to the gate determines which way current flows more easily. This operational characteristic differs significantly from the traditional spintronic devices that require the switching of a ferromagnet or movement of a ferromagnetic domain wall, whose switching speed is normally in the order of hundreds of picoseconds to nanoseconds [14], [17]. The switching speed of AFM layers has been reported to be at the sub-10-ps range [16], [18], which is much faster and creates unique opportunities for fast and energy-efficient logic implementations. Thanks to the low electrical field required to switch the AFM [19], the proposed device concept may potentially lead to energy-efficient ultralow voltage circuits. This nonvolatile and voltage-controlled device is expected to provide the room temperature operation with on/off ratios well beyond what can be achieved using magnetic tunnel junctions (MTJs) [16].

There are several experiments indicating that the magnetic order in chromium can be switched back and forth via an applied electric field in the presence of a static magnetic field [20], [21]. The creation of a preferred direction via SOC has only been predicted based on first principle calculations and is yet to be confirmed experimentally [16]. Although research on the experimental demonstration of the device is ongoing, it is helpful to evaluate the potential performance of the proposed device, determine whether or not a flexible and complete logic family can be implemented with this device, and identify the desired material and device-level parameters to maximize the overall circuit-level performance. The results can provide important motivation and guidance for device researchers and experimentalists working in this area.

Regarding the logic implementation, only a multiplexer-based logic has been proposed in the original proposal [16]. However, such logic lacks gain, and a more generic and robust logic implementation is needed for a wider range of applications. In this paper, a novel logic implementation is proposed for AFMFET devices to achieve complementary logic similar to what can be achieved in CMOS logic. However, to further increase the density and improve the energy and delay, a majority-gate-based logic is proposed taking advantage of the large domain size in some antiferromagnetic materials such as chromium. The proposed logic implementation does not need any dedicated MOSFETs to drive the next stage or special clocking scheme. It satisfies all five essential requirements for general logic applications, including nonlinearity, gain, concatenability, feedback prevention, and a complete set of Boolean operations. The proposed logic implementation also has a compact layout that is comparable to the CMOS technology.

The rest of this paper is organized as follows. Section II proposes two logic implementations for AFMFET devices, including complementary and majority-gate logic gates. Section III describes the device-level performance modeling approach to estimate the intrinsic delay, energy, and footprint area of the proposed AFMFET logic. The circuit-level performance analyses and benchmarking results and discussions are presented in Section IV. Finally, conclusions are made in Section V.

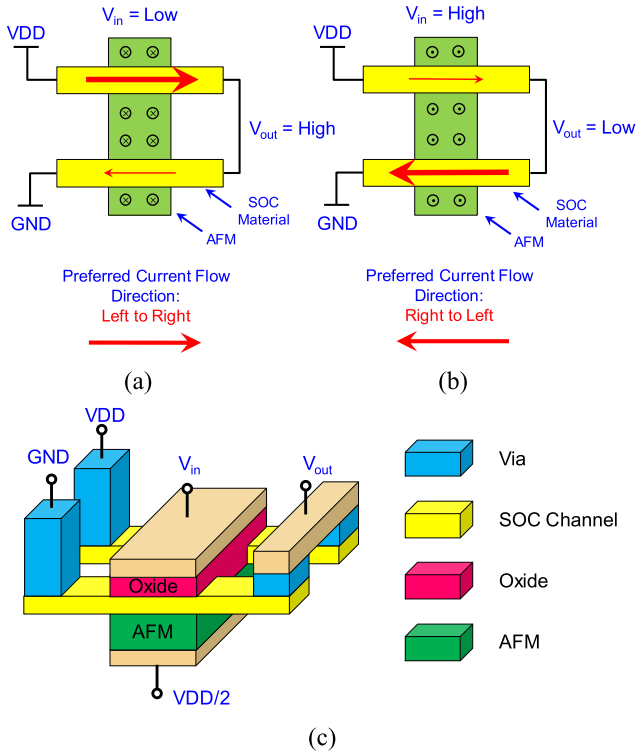

FIGURE 2. (a) and (b) Top-down view for an AFMFET-based inverter when the input is GND and VDD, respectively. (c) 3-D structure view of the proposed AFMFET-based inverter implementation.

II. PROPOSED LOGIC IMPLEMENTATION

To utilize the unique feature of the directionality of conduction present in AFMFET devices, we propose a complementary logic implementation. The top-down and 3-D views of the proposed logic gate are shown in Fig. 2. For an inverter, the direction of the currents flowing through the SOC materials in the pull-up and pull-down networks are right to left and left to right, respectively. Depending on the input voltage, the boundary magnetization of the AFM layer switches, leading to an asymmetry of the current flow in the two SOC channels. For instance, when the input voltage is low as shown in Fig. 2(a), the preferred current direction is from left to right. Therefore, the output voltage is pulled close to VDD, achieving the inversion operation. The voltage transfer characteristic (VTC) of the inverter is illustrated in Fig. 3. The device is considered active and has a large gain when the input voltage is above or below half of the supply voltage by the threshold voltage of the AFM V_{crit}.

The same technique is applicable to all complementary logic gates, such as a NAND2 gate, as shown in Fig. 4. When multiple current paths are connected in series/parallel,

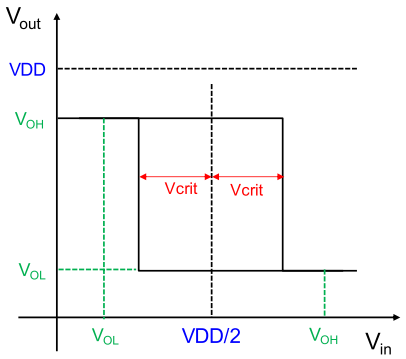

FIGURE 3. Illustration of the VTC of an inverter.

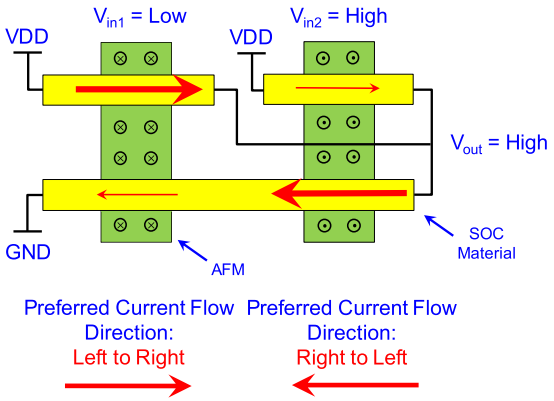

FIGURE 4. Proposed AFMFET-based two-input nand logic implementation.

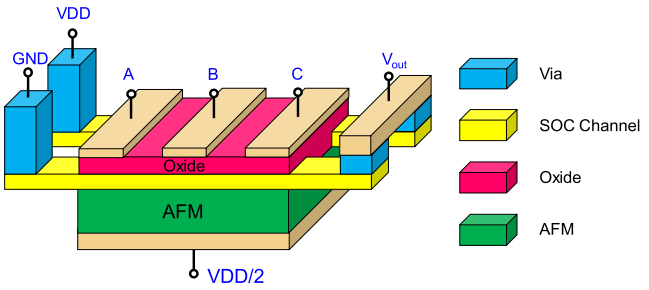

FIGURE 5. 3-D device structure view of a majority gate using AFMFET devices.

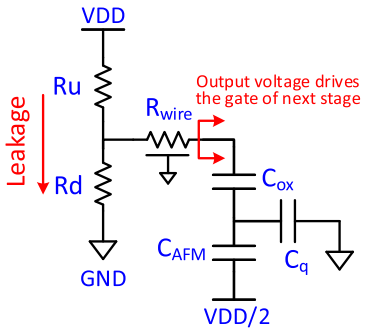

FIGURE 6. Equivalent circuit model for AFMFET-based logic implementation.

the overall current is dominated by the least/most conductive path. This is quite similar to what happens in CMOS logic, with the difference being that p- and n-channel devices are replaced with devices with left-to-right and right-to-left current paths, respectively. By connecting AFMFET devices in the pull-up and pull-down networks properly, all complementary logic functions can be achieved. The voltage generated at the output is static, which can directly drive the input of the next stage without using auxiliary field-effect transistors or any special clocking schemes as needed in prior magnetoelectric-based device proposals [12].

Another option to implement a complete logic set is by creating a majority gate. From the experimental results in [22], the typical domain size in chromium is about 5 μm, which is more than 10$\times$ larger compared to the AFM layer used in this paper. Therefore, a single-domain assumption is expected to be valid, and this property has been used in the past proposals to implement a majority gate based on the MEMTJ device [12], [23]. In these proposals, three input gates are used and the surface magnetization of chromium is controlled by the majority of the inputs. Here, we adopt the majority-gate concept and incorporate it with the complementary AFMFET logic, as shown in Fig. 5. Compared to the prior magnetoelectric majority logic gate proposals [12], [23] that use a dynamic logic style to implement Boolean logic, the proposed majority gate does not need a dedicated preset clocking and is more compatible with the CMOS static circuits and standard cell design.

III. MODELING APPROACH

In this section, the intrinsic delay and energy of the proposed logic gates are modeled to enable the circuit-level performance analysis in Section IV. Instead of using spin-transfer torque as the switching mechanism, the AFMFET device relies on the voltage-controlled magnetoelectric (exchange bias) effect [24].

The intrinsic delay of an AFMFET logic gate is modeled as

$$t_{\text{int}} = t_{\text{AFM}} + t_{\text{RC}} \tag{1}$$

where t_{AFM} is the intrinsic switching delay of AFM, which is assumed to be 10 ps, and t_{RC} is the electrical RC delay based on the equivalent circuit model illustrated in Fig. 6, where R_u and R_d are the pull-up and pull-down network resistances, respectively, and C_{AFM}, C_{ox}, and C_q are the AFM capacitance, oxide capacitance, and quantum capacitance. The dielectric constants for AFM and oxide are 12 and 3.9 [25], respectively, and the thickness of AFM and oxide layers are 10 and 1 nm, respectively. The quantum capacitance is assumed to be 50% of the gate oxide capacitance. The values of the pull-up and pull-down resistances are determined by the SOC channel resistance that depends on the direction of magnetoelectric polarization of the AFM. The relation between the current and gate voltage, shown in Fig. 7, is obtained by using nonequilibrium Green's function transport simulations in a 2-D ribbon with a width

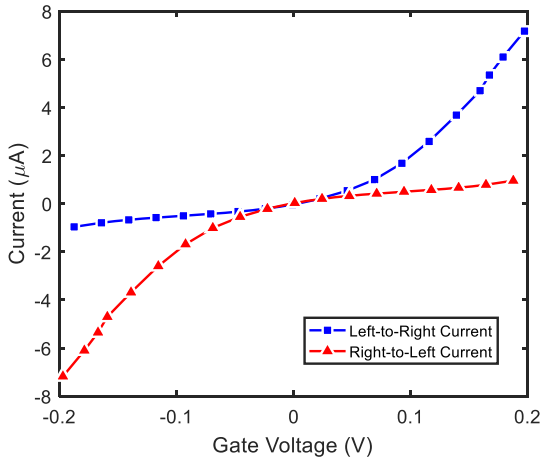

FIGURE 7. ***IV*** **characteristics of the AFMFET device [16].**

of 20 nm and a band mass of $0.1m_e$ [16]. A conservative value of exchange splitting of 0.1 eV at 300 K is assumed.

To model the energy dissipation of the AFMFET logic, the dynamic switching energy during charging and discharging the gate capacitance is written as

$$E_{\text{dyn}} = \frac{1}{2} C_g \Delta V^2 \tag{2}$$

where ΔV is the voltage swing at the output. To drive the next stage without additional transistors, the minimum value of ΔV is determined by the critical switching voltage of the AFM V_{AFM}, which is written as $\Delta V = V_{\text{AFM}}(C_{\text{AFM}} + C_{\text{ox}})/C_{\text{ox}}$. Note that both the electric field E and a small symmetry breaking magnetic field H are needed simultaneously to perform isothermal switching of chromium, where the product of E and H needs to overcome a critical threshold [19], [26]. In Section V, we will investigate the performance of AFMFETs with three V_{AFM} assumptions under different external magnetic fields.

For the leakage energy calculation, if the on–off ratio is small, a supply clocking scheme can be employed such that the device only consumes leakage power during the logic operation [27]. The corresponding leakage energy is written as

$$E_{\text{leak}} = \frac{\text{VDD}^2}{R_u + R_d + R_{\text{clk}}} t_{\text{clk}} \tag{3}$$

where t_{clk} is the half of the clock period, R_{clk} is the equivalent on-resistance of the clocking transistor per AFMFET logic gate, and VDD is the supply voltage. For a given V_{AFM}, the voltage swing at the output can be calculated, which determines the supply voltage according to the following equation

$$\text{VDD} = \frac{2\Delta V(R_u + R_d + R_{\text{clk}})}{|R_u - R_d|}. \tag{4}$$

In this paper, the clock speed is limited to 5 GHz, and the transistor resistance follows the 15-nm CMOS high-performance device used in the previous benchmarking work [2], assuming that the width of the transistor is 150 nm.

The switching energy associated with the supply clocking is written as

$$E_{\text{clk}} = \frac{1}{2} (\text{C}_{\text{wire}} + C_{\text{clk}}) \, \text{VDD}^2 \tag{5}$$

where C_{wire} and C_{clk} are the interconnect capacitance and gate capacitance of the clocking transistors. Interconnect parasitic capacitance is 0.15 fF/μm, which is estimated based on a validated capacitance model [28], [29], and the input capacitance of clocking transistors is 0.2 fF [2]. The number of logic gates shared by a clocking transistor is set as 10 to achieve the proper balance between footprint area and dynamic and leakage energy overheads of the supply clocking.

The total intrinsic energy of an AFMFET logic gate is the summation of all energy components

$$E_{\text{int}} = E_{\text{dyn}} + E_{\text{leak}} + E_{\text{clk}}. \tag{6}$$

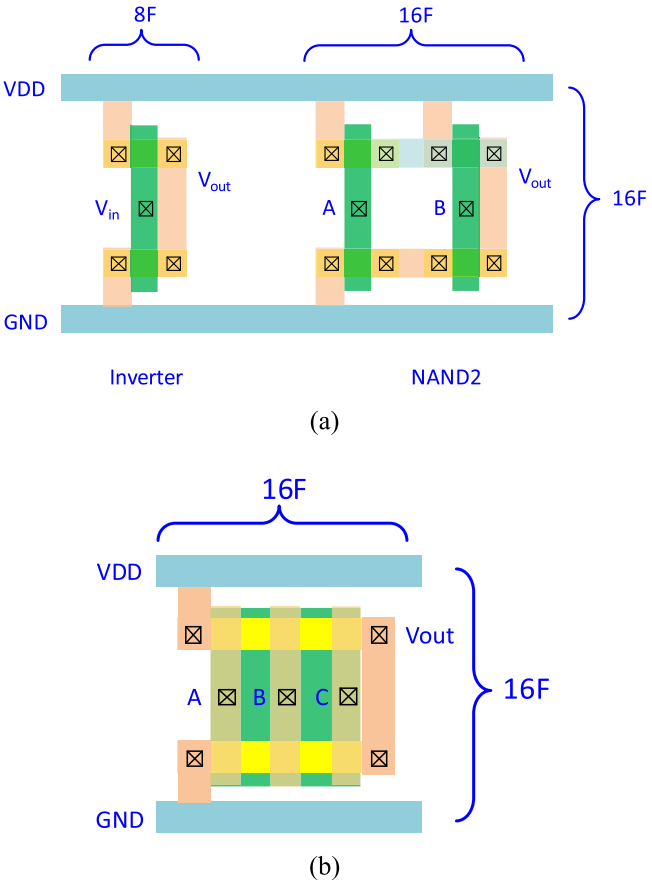

FIGURE 8. Proposed layout views for (a) inverter and two-input NAND gate and (b) majority gate using AFMFET devices.

Fig. 8 illustrates the layout of the proposed AFMFET logic using complementary and majority-gate-based implementations. The design rule follows the previous benchmarking methodology [2], [13], where the minimum distance between the two contacts is 4F. The footprint area of the proposed AFMFET logic is comparable to its CMOS counterpart for a basic inverter. For a two-input nand gate, 33% of the footprint

area overhead is observed. This is mainly due to the fact that to achieve opposite current flow directions in the pull-up or pull-down networks, the source and drain of the AFMFET devices cannot be shared. For a majority gate, the AFMFET device provides a large area saving thanks to the compact design and layout.

IV. PERFORMANCE ANALYSES

In this section, the circuit-level performance of the proposed AFMFET logic implementations is analyzed and benchmarked against various beyond-CMOS technologies. The benchmarking circuit is a 32-bit arithmetic logic unit (ALU), which is adapted from a uniform benchmarking tool [2]. Based on the modeling approach described in Section III, the delay, energy dissipation, and footprint area per logic gate are evaluated and used as the basic building block in the benchmarking tool.

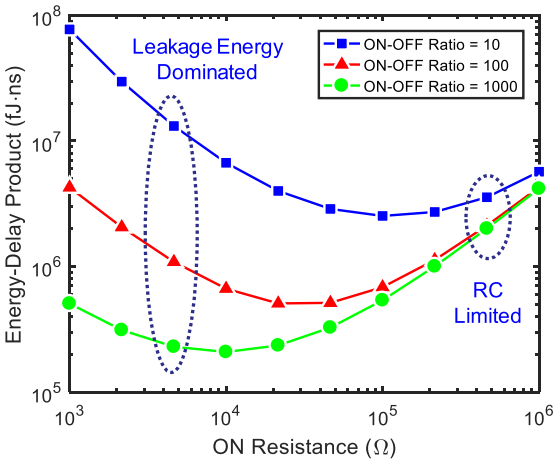

FIGURE 9. EDP as a function of ON-resistance of the AFMFET channel at different ON–OFF ratio assumptions.

A. CHANNEL RESISTANCE OPTIMIZATION

To properly design and optimize the device and circuit performance, one key parameter investigated in this paper is the channel resistance. The choice of material and doping level for the channel can result in vastly different channel resistance values. Fig. 9 shows the energy-delay product (EDP) per ALU operation by sweeping the channel resistance at three hypothetical on–off ratios under a given critical switching voltage of 100 mV. For a small channel resistance, the leakage energy dominates the overall energy dissipation because of the large current flowing from VDD to GND. As the channel resistance increases beyond a certain point, the delay keeps increasing due to the significantly larger *RC* delay values. The energy dissipation becomes dominated by the switching energy associated with charging and discharging the AFM. As a result, optimal channel resistances exist to minimize the overall EDP.

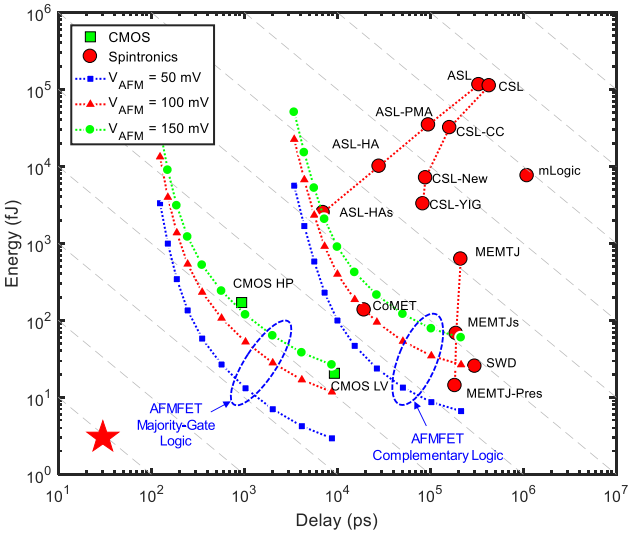

FIGURE 10. Comparison of energy and delay of a 32-bit adder among various charge- and spin-based devices.

B. CIRCUIT-LEVEL ANALYSIS AND BENCHMARKING

To compare the AFMFET devices with other spintronic devices and the conventional CMOS devices, we use a uniform benchmarking methodology with a 32-bit ALU as the benchmarking circuits [2]. The energy versus delay per ALU operation for AFMFET devices at three different critical switching voltages is shown in Fig. 10. Since the product of the applied electrical and magnetic fields needs to overcome a critical threshold [19], [26], a smaller supply voltage requires a larger static magnetic field. In this paper, three critical switching voltages of 50, 100, and 150 mV are considered. The corresponding and magnetic fields are 628, 314, and 214 Oe, respectively [19].

In general, spintronic devices are slower due to the limitation of the magnet switching delay. The voltage-controlled devices, including the SWD, CoMET, and MEMTJ, consume much less energy compared to the current-driven devices, such as the ASL and charge spin logic devices. For the proposed AFMFET logic, both complementary and majority-gate-based implementations perform better compared to their spintronic counterparts. The main advantage is the fast switching time of the AFM without the need of switching an entire ferromagnet or moving a domain wall inside a ferromagnet. At the optimal channel resistance with a small critical switching voltage of 50 mV, the AFMFET with the complementary logic implementation provides an EDP comparable with its CMOS counterpart. However, the majority-gate-based AFMFET logic implementation can potentially provide up to 30× EDP reduction. This is because a variety of the logic functions can be implemented quite efficiently with majority gates. For example, only one majority operation is needed to generate the carry out in a full adder. This reduces the number of logic gates in the critical path significantly and saves the energy due to fewer logic gates required to achieve the same functionality.

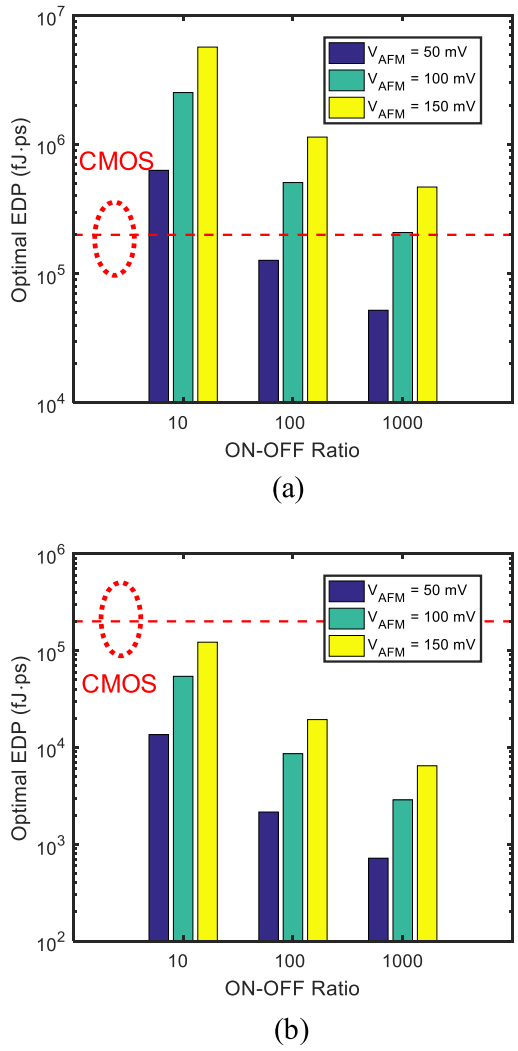

FIGURE 11. Comparison of optimal EDP of a 32-bit adder using CMOS and AFMFET devices with (a) complementary and (b) majority-gate logic implementation.

The results shown in Fig. 10 are based on an on–off ratio of 10 [16]. To quantify the benefits of the proposed AFMFET logic with an improved on–off ratio, Fig. 11 shows the EDP of a 32-bit adder at various on–off ratios up to 10^3 with the optimal channel resistance. For both complementary and majority-gate logic implementations, the performance of AFMFET improves as the on–off ratio increases. For a small AFM critical switching voltage of 50 mV with a relatively large on–off ratio of 10^3, the majority-gate-based AFMFET logic implementation can potentially reduce the EDP by two orders of magnitude compared to the CMOS counterparts. The main advantage comes from the ultralow operation voltage as well as the fast AFM switching delay. In addition, the majority-gate based logic is more efficient compared to its complementary logic implementation.

V. CONCLUSION

This paper proposes two novel logic implementations for AFMFET devices with complementary logic and majority-gate logic. The proposed logic gates satisfy five essential properties, allowing AFMFETs to be used as fast and energy-efficient stand-alone logic devices. Optimal channel resistance is found to minimize the overall EDP under different critical switching voltages and ON–OFF ratios. At the circuit-level analysis, AFMFET devices based on majority-gate implementations are projected to be more energy efficient compared to their CMOS counterparts thanks to their low operating voltages and the need for fewer devices needed for implementing adders.

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