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MagCAD: Tool for the Design of 3-D Magnetic Circuits

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ABSTRACT The post-CMOS scenario poses many challenges to researchers. Innovative solutions must be found to further improve electronic circuits. Exploiting the potential offered by the third dimension is clearly one of the best possibilities available. However, due to the lack of a simple and straightforward methodology, it is difficult to analyze and compare beyond-CMOS technologies. We tackle this challenge by presenting a framework that enables the design of 3-D circuits based on field-coupled technologies. The tool is called MagCAD and is part of the ToPoliNano design suite, created to design and simulate circuits based on emerging technologies by applying a top–down methodology. Right now, MagCAD supports the two main implementations of nanomagnetic logic (NML), the in-plane NML, and the perpendicular NML (pNML). However, it is designed to be easily extended to other beyond-CMOS technologies. Researchers can design pNML circuits by using MagCAD, which embeds design rules, physical models, and technological parameters. The compact model and the physical properties of these cells are based on experimental results. After the design phase, a register-transfer-level model of the circuit is automatically extracted by MagCAD. The model is written in VHSIC Hardware Description Language and has been validated through experiments. The extracted model can be simulated with fast HDL-simulators; this makes it possible to verify the behavior and extract the performance of the designed circuit. With MagCAD, designers have the possibility to easily design, simulate, and compare 3-D NML circuits, exploring the advantages provided by the third dimension freely.

INDEX TERMS 3-D architectures, design tools, emerging technologies, MagCAD, nanomagnetic logic (NML), perpendicular NML (pNML).

I. INTRODUCTION

IN RECENT years, the interest in emerging technologies has been consistently growing. Limits related to CMOS technology, predicted by the Roadmap [1], are becoming real. Alternative technologies are currently under investigation. Both academia and electronic industry's needs are looking for new materials to replace or support CMOS technology. The benchmarking of emerging technologies represents a key point to permit the identification and the focusing of resources on the most promising devices. The nanoelectronics research initiative proposed a uniform methodology in [2] and updated in [3] for their benchmarking. Benchmarking environments represents a key resource for the study and the development of these technologies; with our tool MagCAD, we are working toward noncharge-based devices, which make use of novel materials to enable logic operations. Among all candidates belonging to this category, nanomagnetic logic (NML) is considered a promising option [4]. Our work falls within the scope of the benchmarking methodology proposed by Nikonov *et al.* [2], [3]. Indeed, although our goal is to present MagCAD, what is interesting is that this tool has been demonstrated by analyzing one of the test circuit considered in their studies, the 32-bit ripple carry adder. In Section IV, the performance offered by this target technology is presented. Therefore, not only basic layouts are considered, but also a 32-bit ripple carry adder.

The main features of this technology include the possibility to store binary information, the nonvolatility of the information, the absence of wired interconnections, and the possibility of being integrated with CMOS.

However, the biggest disadvantage of NML technology lies in its limited clock speed, compared with the state-of-the-art

CMOS circuits. The real value of a technology cannot be simply measured by its clock speed. Particularly, all the features provided by a technology should be considered in order to obtain a precise evaluation of it. What makes the NML technology really shine is the range of additional features it has compared with CMOS circuits. For example, the basic magnetic element can be seen both as a logic element and a memory device. Moreover, NML technology, particularly perpendicular NML (pNML) circuits, intrinsically enables the fabrication of 3-D circuits. In CMOS technology, 3-D circuits can be implemented with VIAs, at the cost of greatly increased fabrication complexity. pNML enables the design circuits organized in different layers, freely mixing logic and interconnection elements.

The study of this technology must be enabled by CAD tools and other software, which make it possible to design, simulate, and test NML circuits. Nowadays, different low level simulators are available, such as NMAG [5], OOMMF [6], or mumax^3 [7]. They offer the possibility to perform micromagnetic simulations on size-limited problems. They are valuable for that purpose, but being CPU/GPU intensive they are not affordable to analyze large and complex circuits. Compact models instead should be used to make architectural exploration of a technology. In digital electronics, register-transfer-level (RTL) design is a typical practice. As happens with CMOS technology, the RTL design implements the functional models in a hardware description language like Verilog or VHSIC Hardware Description Language (VHDL).

We recently presented our CAD Software called ToPoliNano [8], [9]. This tool reproduces the same top–down approach established for the standard CMOS technology. Indeed, the design of NML circuits is automatically performed by ToPoliNano considering a VHDL file as entry point. Specifically, tailored place and route algorithms and simulation engines enable the design of the final circuit, which can be simulated and tested. This complete flow has been presented for the in-plane NML (iNML) [10], a particular NML implementation [see Fig. 1(a)], where rectangular shaped nanomagnets are placed on a planar substrate [see Fig. 1(b) and (c)]. Besides ToPoliNano, another tool called MagCAD has been developed. This software is conceived as a layout editor, where users can manually compose their custom circuits by simply dragging and dropping a list of library devices. The tool is enriched with customizable layout rules compliant with the target technology. With MagCAD, we have enabled an easy way to design any kind of circuit starting from a few elements present within a library. The tool can automatically export the VHDL netlist associated with the custom circuits. The extracted VHDL includes the compact model of each cell, the physical equations describing the technology, and the technological parameters. All the models have been previously validated through experiment and presented in [11].

The flexibility of this organization is particularly suited for the study of field-coupled and other beyond-CMOS technologies. At first, we developed a library of the main elements,

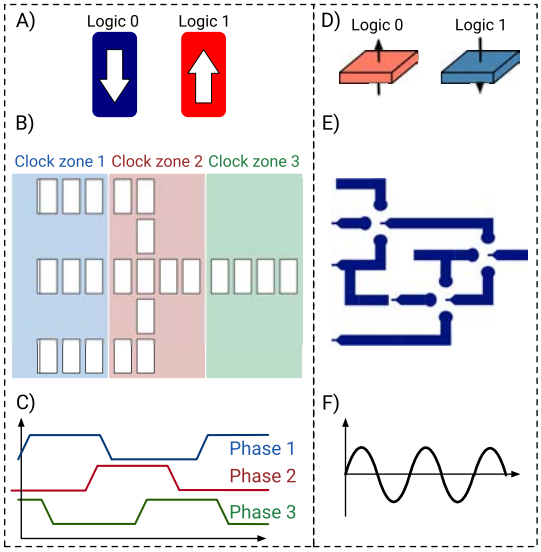


FIGURE 1. Comparison between iNML and pNML technologies. (a) iNML basic elements. (b) iNML circuit sample. Clock zones are highlighted with different colors. (c) To each of them, a specific clock phase is applied. (d) pNML basic elements. (e) pNML circuit sample and (f) related clock signal.

which can be used for the composition of iNML circuits. With this paper, we present how we have extended our framework to another NML implementation: the pNML [12] [see Fig. 1(d)]. While MagCAD supports NML technologies for now, in the future, it can be easily extended to other beyond-CMOS devices by means of plugins. Compared with iNML, pNML features many peculiarities: the complexity of the clocking system affecting iNML is overcome by the use of a unique, global, and perpendicular clock field, which is applied uniformly to the entire circuit [13] [see Fig. 1(e) and (f)]. This not only entails a reduction of the occupied area, but it has also a remarkable impact in terms of power consumption. In addition, the monolithic 3-D integration of pNML circuits has been experimentally demonstrated in [14]–[16]. This characteristic makes it possible to design compact low-power circuits. MagCAD enables the design of 3-D architectures making it possible, for example, to separate interconnections, logic, and memory in different levels. Threshold gates are particularly suitable to exploit both the logic-in-memory (LIM) [17], [18] concept and the peculiarities of programmable gates. Memory elements have been experimentally demonstrated in [19]. MagCAD allows pNML designers to conceive stacked architectures significantly limiting the amount of area occupied by interconnections.

In this paper, we present and describe MagCAD and the methodology adopted, focusing on the newly implemented pNML technology. With the introduction of this technology, we have also added the possibility of designing circuits on different layers. Circuits designed with MagCAD can be simulated with an RTL model written with VHDL language. The model and the pNML technology

are described in Section II. The structure of MagCAD, how it works and how it handles objects and 3-D circuits, is presented here for the first time and described in Section III. Several circuits, from simple logic gates to a 4-bit Ripple Carry Adder, all designed with MagCAD, are proposed and simulated. MagCAD is able to automatically extract information about occupied area, power consumption, and latency. Results are presented in Section IV. MagCAD is indeed a powerful instrument for researchers. It gives them the opportunity to create custom circuits based on all types of NML technologies. No other tools presented since now allow to reach this goal. MagCAD is also designed with the clear objective of supporting as many different technologies as possible, further extending its utility.

II. BACKGROUND

The MagCAD Graphical Editor is conceived around the idea of being flexible in order to be used for the exploration of emerging technologies. It is distributed under free license and can be downloaded at the following url: *https://topolinano.polito.it*.

In this paper, we introduce the new library and features specifically tailored for pNML technology. In this technology, the basic elements are characterized by a perpendicular magnetic-anisotropy. pNML circuits are typically etched from Co/Pt multilayer films, then the focused ion beam is used to irradiate specific spots [20]. These Artificial Nucleation Centers (ANCs) are created to control the switching process of nanomagnets. An accurate positioning of ANCs guarantees a correct signal propagation. Indeed, information flows through the circuit mainly according to two factors: 1) the ferromagnetic/antiferromagnetic interaction among neighboring devices and 2) the clocking signal.

In this case, the clock is a sinusoidal perpendicular signal applied to the entire circuit. This field, which oscillates in the order of hundred MHz, is generated by the on-chip coils. As for the iNML implementation, the clocking mechanism is adopted with the purpose of lowering the energy barrier required to switch magnets. The need of a clock can be an issue for the overall circuit power consumption. However, pNML gets energy efficient when is very dense and possibly when presents multiple functional layers [16].

A. pNML ARCHITECTURES

Logic functions are achieved by the use of a set of logic gates [see Fig. 2(a)–(c)]. The simplest one is the inverter, and this function is obtained by simply using an odd number of devices. It is worth noting that when the magnetic structure of the first device surrounds the ANC of the second one, this design aims to increase the coupling field acting among them. VIA components are obtained by placing two devices onto two different layers, where the two nanomagnets are partially overlapped in order to increase the ferromagnetic interaction. Thanks to the use of this principle, interconnections, memory elements, and so on can be organized into different layers, increasing the circuit compactness. Threshold gates, and in particular the Minority Voter, can be programmed to act both as nand and nor gates [21]. Moreover, one of the inputs can be placed on a different layer making it possible to design 3-D programmable gates. The combination of all these gates enables the design of any kind of logic architectures. For this reason, in our systems, these basic elements must be considered as library components.

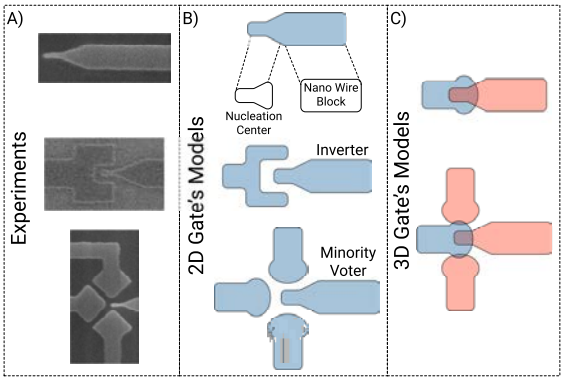


FIGURE 2. **Each circuit can be composed by using a few basic components. (a) Each element has been fabricated and characterized. Physical equations and quantities have been extracted and modeled. (b) List of the 2-D gates developed in the components library. In order to increase the flexibility of the model, the simple wire is divided into two subblocks: the nucleation center and the nanowire. (c) List of the 3-D gates developed in the components library.**

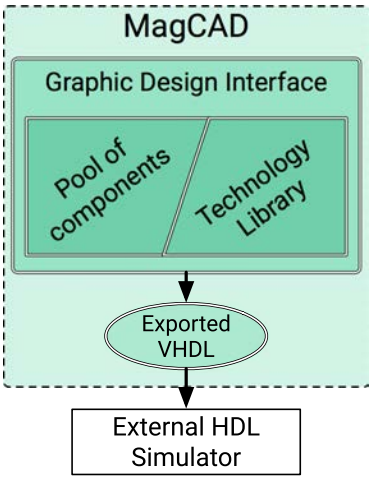
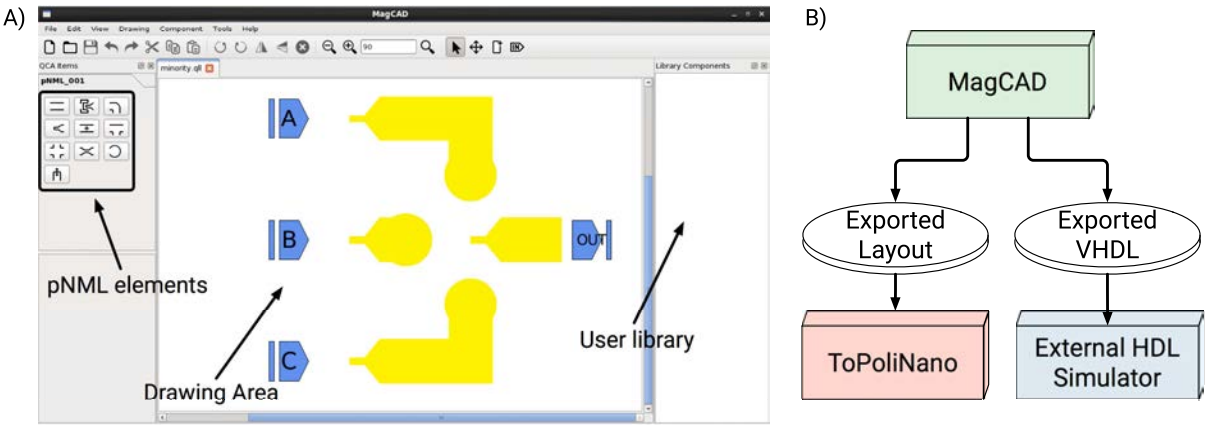


FIGURE 3. **MagCAD organization.**

B. METHODOLOGY

Fig. 3 shows the methodology adopted to implement MagCAD. The bottom level is represented by the model of each library component. As shown in Fig. 2(a), this model is based on physical quantities and equations finely fitted through experiments. The idea behind this is also to split each device into a few sub-basic elements. As shown in Fig. 2(a) for example, a simple device can be obtained by the composition of a nucleation center and a domain wall (DW).

FIGURE 4. (a) MagCAD main window. (b) Design flowchart of the MagCAD tool.



Moreover, the DW can be again split into smaller pieces of DWs. In this way, circuits can be designed in a matrix-like organization where basic elements occupy the nodes.

The model is entirely developed in VHDL and, besides this, includes also a technological library containing all the quantities and functions needed to describe the properties of this technology. Thanks to the graphical user interface (GUI), users can create circuits by simply dragging and dropping components from the library. Once the design is completed, cells are automatically interconnected. The complete VHDL description of the architecture is given as an output; files can be imported into standard software like Modelsim and then simulated.

C. COMPACT MODEL

The equation, which drives the dynamic behavior of nanomagnets, is the well-known Landau–Lifshitz–Gilbert equation. Since the aim of our tool is to analyze complex circuits at an RTL level, a simplified model is preferable. The model presented in the following has been validated via experiments [22], [23]. It is entirely developed in VHDL; here, each component represents an independent entity, which contains the equations needed to describe the related physical behavior. The implemented entities are shown in Fig. 2(b) and (c):

1) nucleation center (ANC);
2) DW;
3) inverter;
4) via (3-D);
5) minority gate (2-D and 3-D).

A detailed description of the implementation of each component can be found in [11]. Concerning the ANC, the most important parameter that must be considered is the time required to nucleate the DW. t_{prop} depends on τ and the probability of nucleation P_{nuc}

$$t_{\text{nuc}} = -\tau(H_{\text{eff}}) \cdot \ln(1 - P_{\text{nuc}}). \tag{1}$$

In this formula, τ is evaluated by the following equation:

$$\tau(H_{\text{eff}}) = f_0^{-1} \cdot \exp\left(\frac{E_{0,\text{ANC}}\left(1 - \frac{H_{\text{eff}}}{H_{0,\text{ANC}}}\right)^2}{K_B T}\right). \tag{2}$$

Instead, the probability of nucleation P_{nuc} is

$$P_{\text{nuc}}(t_{\text{clock}}, H_{\text{eff}}) = 1 - \exp\left(-\frac{t_{\text{clock}}}{\tau(H_{\text{eff}})}\right). \tag{3}$$

The evaluation of P_{nuc} and τ is influenced by the effective field H_{eff}

$$H_{\text{eff}} = H_{\text{clock}} - C_{\text{eff}}, \quad C_{\text{eff}} = \sum_{i=1}^{N} C_i M_i. \tag{4}$$

The delay introduced by DWs can be evaluated as

$$t_{\text{prop}} = \frac{l_{\text{mag}}}{v_{\text{DW}}(H_{\text{clock}})} \tag{5}$$

where v_{DW} is the velocity of propagation and this is influenced by the relation of the external field H_z and the intrinsic pinning field H_{int}. In the creep regime, $H_z \ll H_{\text{int}}$, while in the depinning regime ($H_z \approx H_{\text{int}}$) the velocity increases exponentially. In these two regimes, the domain velocity can be evaluated as

$$v_{\text{DW}}(H_z \ll H_{\text{int}}) \approx v_0 \cdot e^{-\frac{E_{\text{pin}}}{k_B T}\left(\frac{H_{\text{int}}}{H_z}\right)^{\frac{1}{4}}}. \tag{6}$$

When $H_z \gg H_{\text{int}}$ (flow regime), there is a linear dependence on the applied field

$$v_{\text{DW}}(H_z \gg H_{\text{int}}) = v_0 + \mu_w(H_z - H_i nt). \tag{7}$$

III. MagCAD

The idea behind this tool is to provide a design framework that can be used to investigate and compare emerging technologies from an architectural point of view by means of standard VHDL simulations. At the time of writing, the iNML and the pNML were fully supported; however, MagCAD is developed to be easily extended to any emerging device. The tool is cross platform, thus can be run on Linux, Windows, and Mac OS X, and it is entirely developed in C++.

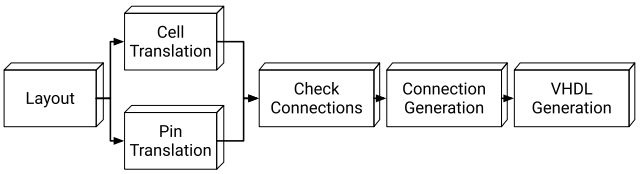
The aim is to simplify the design of custom digital circuits by exploiting a straightforward GUI with a tool palette of basic blocks [see Fig. 4(a)]. The user can draw the custom circuit by simply dragging and dropping these basic elements. Once the design is completed, the user can export the

layout in the ToPoliNano-compatible format or can export the VHDL model associated with the drawn circuit [see Fig. 4(b)]. The VHDL code is automatically generated by MagCAD according to the selected technology and the circuit layout. The exported VHDL embeds a compact model of the investigated technology. In particular, the model includes the technological parameters and physical equations that characterize the device.

The generated VHDL can be simulated by using standard tools like Modelsim from Mentor Graphics [24]. During the simulation, physical equations are solved to obtain circuit information like switching probability, nucleation time, and propagation time.

In this paper, we present the pNML extension of MagCAD. This plugin enables the design and analysis of 3-D pNML circuits. When a new layout is created, the user defines the geometrical parameters of the magnetic nanowires. After that, the tool palette provides, as basic pNML blocks, the magnetic nanowire, nucleation center, inverter, notch, via, fan-out, and pad [see Fig. 4(a) (left)]. These elements combined together can be used to describe any kind of pNML circuit. By simply dragging and dropping this finite number of blocks, it is possible to create a custom pNML layout. When the design of a pNML circuit is completed, the user can save the layout in the user library to reuse it in another design or export its associated VHDL description. In both cases, the user should define the circuit inputs and outputs. To achieve the automatic generation of the associated VHDL code, we developed a specific algorithm for the pNML technology (see Fig. 5). It starts from the graphical representation of the circuit, which can be 2-D or 3-D, and extracts the associated netlist. During the translation from drawing to VHDL model, connections among basic elements need to be identified. This is done by using a matrix-like data structure as support.

FIGURE 5. VHDL Algorithm flowchart used to generate the associated pNML circuit model.



First of all, the layout drawn by the user is translated into a 3-D matrix that represents the circuit connectivity. According to the kind of pNML block translated, the proper number of input/output pins is created and introduced into the matrix. At this point, the algorithm does not yet know the signal flow directionality. Thus, it might occur that redundant pins are created; this is done to have a general connectivity interface among pNML elements.

A second step is required to define the actual connections. During this procedure, the algorithm starts from the circuit inputs and follows the information flow directionality defined by the layout. Once the elements are connected, the useless pins are removed. A recursive approach has been implemented to follow the natural flow path of the information.

Once the actual connections are defined, the algorithm starts the VHDL generation, which represents the last step of this process. All the elements in the layout are scanned and the corresponding VHDL instances are written in a .vhdl file. As described in Section II, a VHDL model is associated with each basic block. VHDL *signals* are also declared and *portmaps* are generated according to connectivity information coming from the previous phase. Connectivity errors are thrown during the algorithm execution. In particular, the algorithm checks whether or not there are floating connections or if pNML blocks are placed in the wrong way. Once the VHDL netlist is generated, the circuit behavior can be verified through Modelsim simulations, providing a proper VHDL testbench.

TABLE 1. Geometrical and physical parameters set according to [25] and [26].

Parameters	Value
Nanowire width	$200 \cdot 10^{-9} m$
Grid size	$350 \cdot 10^{-9} m$
Inter-magnet space	$150 \cdot 10^{-9} m$
Co thickness	$3.2 \cdot 10^{-9} m$
Stack thickness	$6.2 \cdot 10^{-9} m$
ANC volume	$1.68 \cdot 10^{-23} m^3$
Activation volume	$1.26 \cdot 10^{-23} m^3$
Clock field amplitude	560 Oe
Intrinsic pinning field	190 Oe
Coupling field strength for the inverter	153 Oe
Coupling field strength for the minority gate	48 Oe
Coupling field strength for the magnetic via	75 Oe
Effective anistropy	$2.0 \cdot 10^5 J/m^3$
Saturation magnetization of Co	$1.4 \cdot 10^6 A/m$
Depinning field	736.6 Oe
Nucleation probability	95 %

IV. RESULTS

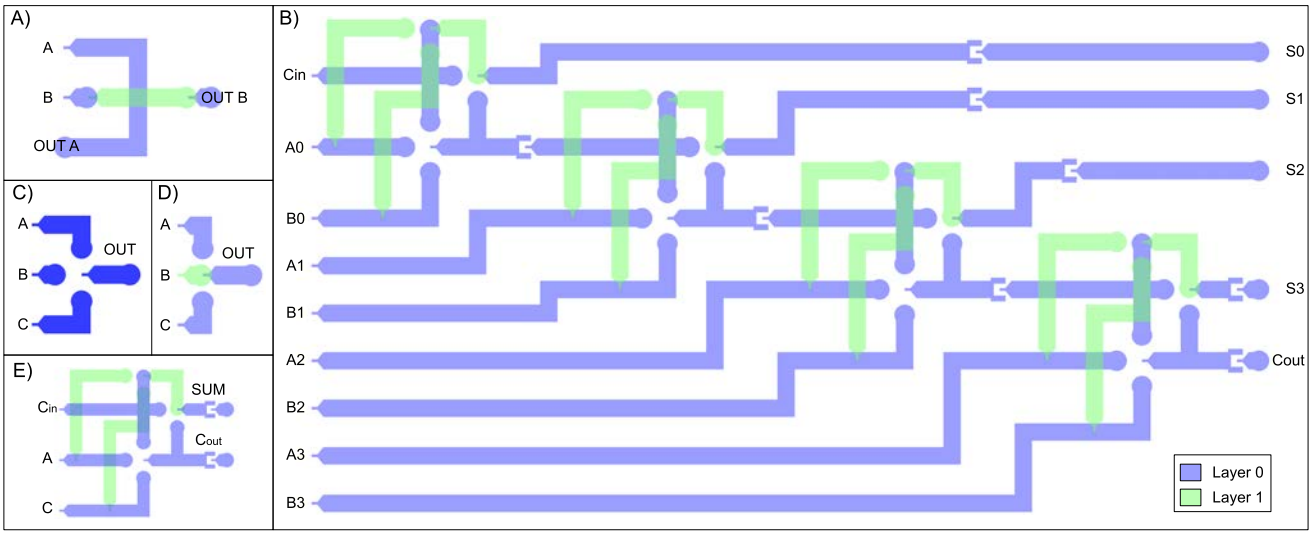
In this section, we verify our tool MagCAD with some sample test circuits to demonstrate the features available in it. Flat and 3-D layouts are shown. In particular, for each circuit, we report information about bounding box area, latency, maximum frequency, and nucleation time considering the set of technological and physical parameters reported in Table 1. These parameters come from experiments and measurements made in our labs. All the data are inputs for our model and make it possible to extract circuits' performance via VHDL simulations. The analyzed circuits are as follows:

1) Crosswire;
2) Minority Voter 2-D;
3) Minority Voter 3-D
4) Full Adder 3-D;
5) 4-bit Ripple Carry Adder 3-D;
6) 32-bit Ripple Carry Adder 3-D.

In the following, the complete design and simulation flow for a 2-D minority voter is reported to better clarify how data are extracted.

At first, the grid size and the nanowire width need to be defined by the user. In this paper, we considered a nanowire

FIGURE 6. Layouts of the analyzed circuits. (a) 3-D Crosswire. (b) 3-D 4-bit RCA. (c) 1-D Minority Voter. (d) 3-D Minority Voter. (e) 3-D Full-Adder.



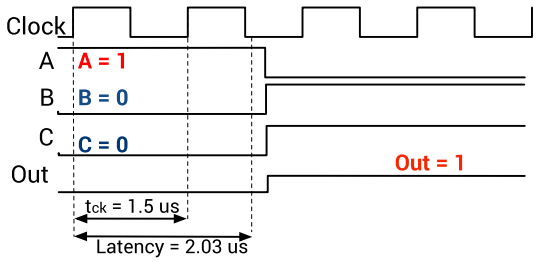


FIGURE 7. Simulation waveform of the 2-D minority gate when the input patter 110 is applied.

TABLE 2. Performance analysis for a 2-D Minority Voter.

Minority Voter 2D		
Critical path = 5.82E-7 s		
Bounding Box Area = 1.32 μm^2		
Input pattern ABC	Output O	Latency $[s]$
000	1	2.03E-6
001	1	2.03E-6
010	1	2.03E-6
011	0	1.29E-6
100	1	2.03E-6
101	0	1.29E-6
110	0	1.29E-6
111	0	1.29E-6

width of 200 nm and a grid size of 350 nm. This implies that the space between two subsequent parallel nanowires is 150 nm. The size of the nanowire should be considered as an example, comparable with the nanowire width that we usually use for our samples [15]. At this point, it is possible to draw the flat implementation of the minority gate by simply dragging and dropping the basic pNML elements available in the tool palette. The final layout is shown in Fig. 6(c). Once the layout is completed, input and output pins have to be defined by inserting special elements indicating an input or an output. During this phase, it is mandatory to specify the pin name. Without pins, it is not possible to extract the VHDL model associated with the drawn circuit. The 2-D implementation of the minority gate shown in Fig. 6(c) shows three inputs (A,B,C) and one output (OUT).

The next step concerns the VHDL extraction. Here, many physical and technological parameters are shown to the user with default values. These parameters are used to write down the pNML technology library required during the VHDL simulation. The user can decide to keep the default values or change them to explore, for example, the effect of technological parameters at the architectural level. In this paper, we considered the parameters reported in Table 1.

At this point, the circuit behavior can be verified via simulations. The propagation time related to the longest nanowire and the nucleation time are automatically extracted by MagCAD and are saved within the technology definition file. These two parameters are necessary to define the minimum clock period. A template VHDL testbench is also generated along with the circuit netlist. However, the input stimuli should be provided by the user. In addition, a file containing the compact model is added to the user folder. All these four files are required to perform the simulation.

Fig. 7 shows the latency and the maximum frequency taking into account the DW propagation speed in the longest nanowire and nucleation time considering the 2-D minority gate with the input pattern 100. Table 2 summarizes the circuit performance considering all input patterns. As expected, the latency changes according to the input pattern. This is due to the effective coupling on the minority ANC. On the other hand, the maximum frequency is equal to 0.69 MHz. The maximum clocking frequency is limited by the DW nucleation time, the clock rise time, and the propagation time given by the longest nanowire. In particular, the pulse time (t_{pulse}) is evaluated as the sum of t_{prop} and t_{nuc} plus the rise time (t_{rise}), which is approximately 25% of $t_{\text{prop}} + t_{\text{nuc}}$.

The 3-D implementation of the minority gate is shown in Fig. 6(d). This layout, drawn with MagCAD, reproduces

FIGURE 8. 3-D layout of the 32-bit Ripple Carry Adder.

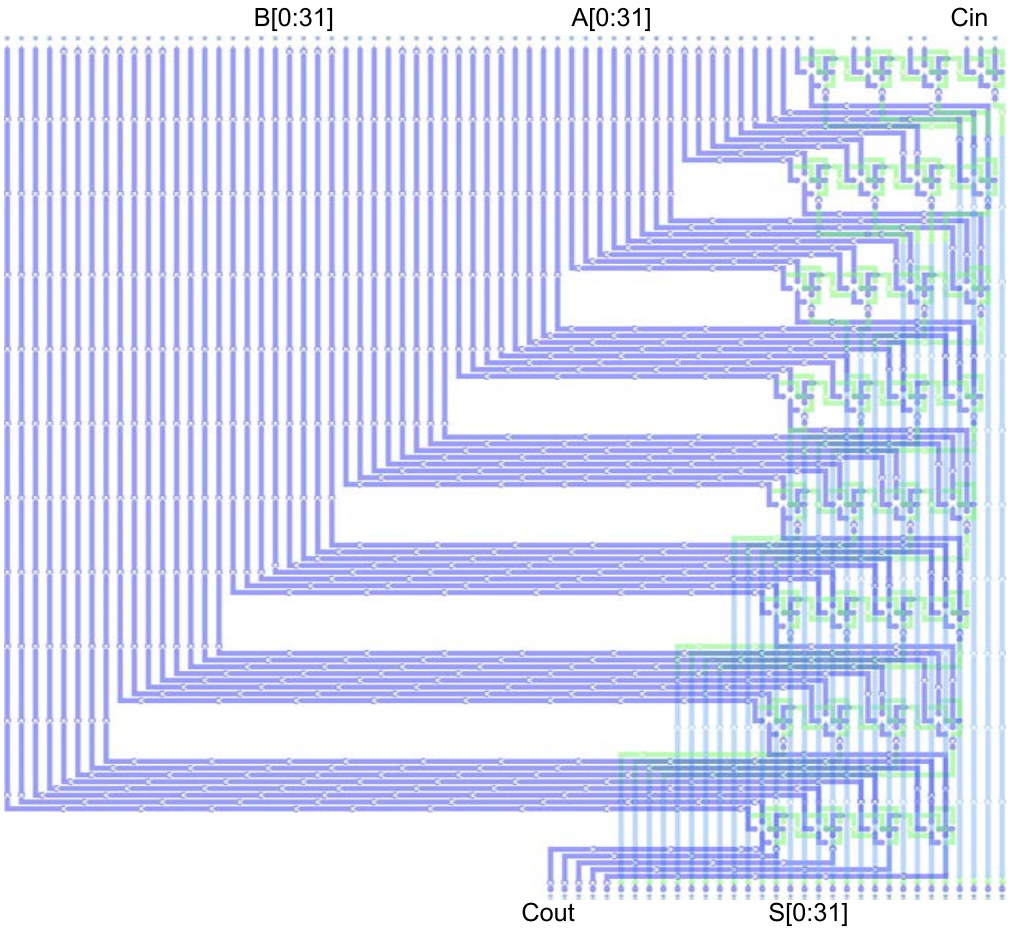


TABLE 3. Performance analysis for a 3-D Minority Voter.

Minority voter 3D		
Critical path = 5.75E-7 s		
Bounding Box Area = 1.03 μm^2		
Input pattern ABC	Output O	Latency $[s]$
000	1	2.01E-6
001	0	2.73E-6
010	1	2.01E-6
011	1	2.01E-6
100	0	2.73E-6
101	0	1.29E-6
110	1	2.01E-6
111	0	1.29E-6

the physical 3-D minority gate experimentally demonstrated in [27]. By looking at Table 3, it is possible to observe that the 3-D implementation of the minority gate is faster than the 2-D implementation only for some input patterns. The critical path is lower compared to the 2-D version; this is due to shorter nanowires involved in bringing the input values close to the nucleation center. On the other hand, a higher latency is observed when inputs A and C are different and the final output value is determined by the ferromagnetic coupling of input B, lying on a different plane. However, the 3-D minority is 43% more compact than that of the 2-D implementation.

The next sample circuit analyzed is the Crosswire shown in Fig. 6(a). This layout shows how it is possible to cross two signals by exploiting a second functional layer. The area occupied by the considered Crosswire layout is 1.85 μm^2. In this case, the critical path, due to DW nucleation and subsequent motion, is equal to 0.63 μs. Table 4 reports the latency from input to output considering the worst case, i.e., the least favorable path. Fig. 6(e) shows a possible 3-D implementation of a Full Adder. This 3-D layout is around 29% more compact than the 2-D implementation experimentally demonstrated in [26]. Here, the critical path is in the range of 629 ns. On the other hand, the latency is increased due to the higher number of ANCs to be crossed by the signals when compared to the previous tested circuits.

The next circuit considered in this paper is the 4-bit Ripple Carry Adder. The layout is shown in Fig. 6(b). Here, four 3-D Full Adders have been instantiated and properly connected. The time required by the nucleated DW to propagate in the longest wire is 300 ns, while the critical path is equal to 0.86 μs. As expected, the higher critical path is due to the longer interconnection wire present in this layout. Therefore,

TABLE 4. Performance analysis for a 3-D Crosswire.

Crosswire 3D		
Critical path = 8.52E-7 s		
Bounding Box Area = 1.85 μm^2		
Input pattern AB	Output OUTA OUTB	Latency $[s]$
00	00	4.52E-6
01	01	3.73E-6
10	10	4.52E-6
11	11	3.73E-6

TABLE 5. Performance analysis for a 3-D Full Adder.

Full Adder 3D		
Critical path = 6.26E-7 s		
Bounding Box Area = 5.24 μm^2		
Input pattern ABC	Output C_{out} S	Latency $[s]$
000	00	6.05E-6
001	01	3.7E-6
010	01	5.27E-6
011	10	6.05E-6
100	01	5.27E-6
101	10	6.05E-6
110	10	2.91E-6
111	11	5.27E-6

the intrinsic pipelining of the information results in a latency of 10.3 μs considering a clock period of 2.15 μs. The area occupied by the 4-bit ripple carry adder is equal to 44.43 μm^2, when considering the nanowire width and grid size reported in Table 5.

The last circuit is a 32-bit Ripple Carry Adder. Its layout is shown in Fig. 8. Here, 32 3-D Full Adders have been placed within the layout and properly connected. Long nanowires have been shortened to reduce the propagation time, which is equal to 89 ns. As a consequence, the latency increases due to the higher number of ANC to be crossed. This approach makes it possible to apply a higher clock frequency. Indeed, this pipelined version of the 32-bit RCA can run at 0.62 MHz. The bounding box is 2176.34 μm^2. The area considers the space required to route input/output signals from the circuit input to its output. However, the circuit compaction could be further improved by exploiting the 3-D dimension for routing the most significant bits.

V. CONCLUSION

With this paper, we have presented our new tool MagCAD, a graphical editor which enables users to design and explore custom circuits based on NML technology. The pNML component library is now integrated in our system making it possible to extract and simulate an RTL description of the designed circuit.

The study of simple logic gates like Crosswires and Minority Voters has been presented. Results include the graphical representation of circuits obtained by MagCAD and the information extracted by the simulation of the produced VHDL architecture. Attention has been given to timing parameters in order to prove the validity of the physical equations developed in our model. Indeed, the core of our system is the model and the VHDL generation algorithm which are behind MagCAD's software. More complex architectures are also proposed; a complete study of a Full Adder and Ripple Carry Adders up to 32-bit is provided. It is worth noting that all results are influenced by the physical parameters set into the technological library. Table 1 lists the values adopted for these preliminary tests, but a refinement of these quantities will lead to significant performance improvements. The accuracy among the model used and the experiments is one of the strengths of our tool and the whole methodology.

With this paper, we have demonstrated how MagCAD enables the design of 3-D architectures, a characteristic particularly suitable for pNML technology. We are now developing the models of pNML memory elements; with this further improvement, the peculiarities of the LIM concept are becoming a reality. As future work, we would like to include the model of a current wire or an STT-device able to generate electrical inputs within the basic pNML blocks. In addition, a model of giant magnetoresistance device could be introduced to perform the electrical read-out of magnetic information. This would enable a powerful way to interface and analyze combined pNML and CMOS architectures. We are also planning to introduce a power model to enable a full comparison with CMOS and beyond-CMOS technologies. Furthermore, we are also working toward the extension of MagCAD to other emerging technologies.

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