IEEE Journal on Exploratory Solid-State Computational Devices and Circuits

Received 6 March 2017; revised 10 April 2017, 2 May 2017, and 12 May 2017; accepted 16 May 2017. Date of publication 23 May 2017; date of current version 6 June 2017.

Digital Object Identifier 10.1109/JXCDC.2017.2706671

Electrical-Spin Transduction for CMOS–Spintronic Interface and Long-Range Interconnects

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This work was supported by Intel MSR under Contract 2011-IN-2198.

ABSTRACT We propose circuits for efficient transduction between electrical and spin signals and compare designs for long-range spintronic interconnects based on transducers and repeaters. This paper analytically analyzes the performance of spintronic all-spin logic (ASL) interconnects in terms of delay, area overhead, and energy dissipation, and validates the analysis by numerical simulations. The results of simulations show that compared to ASL repeaters, the proposed transducer-based interconnect achieves 5× shorter delay, 19× lower energy dissipation per bit per length, and a 9× smaller area-delay-power product for a 4 μm long interconnect. We show that the proposed interconnect can operate under supply voltage values ranging from 300 to 950 mV and tunnel magnetoresistance values ranging from 131% to 450%.

INDEX TERMS All-spin logic (ASL), CMOS, interconnects, modelling, spintronics, transducers.

I. INTRODUCTION

OVER the past half-century, the computational throughput and memory storage of integrated circuits have improved exponentially mainly through the downscaling of the geometrical dimensions of field-effect transistors [1]. Sustaining this trend is becoming more and more challenging as CMOS devices approach their scaling limits [2], [3]. To address this challenge, researchers are investigating novel beyond CMOS devices such as spintronics devices that augment CMOS circuits. Because of the robustness, nonvolatility, and enhanced functionalities of spin-based devices, hybrid CMOS–spintronic circuits are expected to provide new and enhanced memory and computational functionalities [4]–[6]. Hence, passing information back and forth between spintronic and CMOS devices requires efficient transduction.

The data signal of spin-based devices can be transferred by spin-polarized currents through interconnects [7]. An excellent medium for transferring spin signals in short interconnects are metals. Their high conductivity reduces conductivity mismatch problems encountered in spin-based devices composed of graphene and semiconducting channels [8]. Several studies [9]–[11] have analyzed the transmission delay and the energy dissipation of short all-spin logic (ASL) interconnects for metallic, silicon, and graphene interconnects, respectively. The amplitudes of spin signals attenuate exponentially in lengths comparable to spin relaxation length (L_{SRL}), which is generally shorter than 1 μm for metals [12]. This length becomes even shorter in nanoscale wires, which results from sidewall and grain boundary scattering in metallic wires [13]. Thus, spin signals must be amplified multiple times to pass through longer interconnects. These repeaters add to power dissipation and the wafer area, which has led to a demand for novel long interconnect designs that efficiently carry spin signals over long ranges in microchips. In contrast to the amplitude of spin signals, that of the electrical signals does not attenuate exponentially with interconnect length (L_{Int}). Using CMOS–spintronic transducers and electrical interconnects,

we propose a structure that transmits spin signals in long metallic interconnects. The proposed structure outperforms ASL repeaters for interconnects longer than 1.6 μm.

Several studies have examined CMOS–spintronic interface circuits, which write and read from magnetoresistive random access memory and spin-transfer torque magnetic random access memory (STT–RAM) [14], [15], and sense amplifiers that read from these magnetic memories [16], [17]. These interface circuits are suitable for large memory arrays, in which a single large, complicated sense amplifier reads many magnetic tunnel junctions (MTJs). However, in the case of signal transduction, the use of sense amplifiers creates prohibitive energy and circuit area overhead.

This paper proposes compact energy efficient transducers for converting back-and-forth magnetic states in ASL [18] and CMOS binary signals. ASL has been proposed as a potentially low voltage beyond CMOS technology option and has been analyzed for a wide range of applications including image-recognition systems [19], [20], interconnects [7], and various Boolean functions [21]. With existing materials, ASL is not expected to compete with CMOS in terms of energy and delay while performing Boolean functions. However, with advances in magnetic materials ASL is expected to become more competitive and the target material and interface properties for nanomagnets and channels have been presented in [22]. In this paper, we propose two CMOS–spintronic interface circuits with simple structures based on MTJs and ASL gates for the transduction of electrical signals and spin signals. These transducers work under a wide range of supply voltage and tunnel magnetoresistance (TMR) values.

The rest of the paper is organized as follows. Section II describes an electrical-to-spin-signal transducer that converts binary CMOS voltage to the magnetization orientation of a magnet. Then, Section III describes a simple yet efficient interface circuit that converts the magnetization orientation of a magnet to CMOS binary voltage. Section IV presents an analytical study of the delay, area-delay-power product (ADPP), and the per-unit length value of energy-per-bit of spintronic interconnects with ASL repeaters and benchmarks them against the electrical transmission of spin signals. Section V provides the conclusion.

II. CMOS-TO-SPINTRONIC-SIGNAL TRANSDUCTION

The transduction of CMOS data in the form of electrical voltage to spintronic data in the form of the magnetization orientation of magnets can be achieved by using the properties of ASL gates. The polarity of the electrical voltage applied to ASL gates controls copy and invert operations [7]. Employing this property, an ASL-based CMOS-to-spintronic transducer is shown in Fig. 1. In this device, the direction of the electrical current passing through the fixed magnet determines the polarity of the spin accumulation of electrons underneath it. If the electrons are injected by the fixed magnet into the channel, a majority of spins underneath the magnet will have magnetic moments aligned with the magnetic orientation of the fixed magnet. Conversely, if the direction

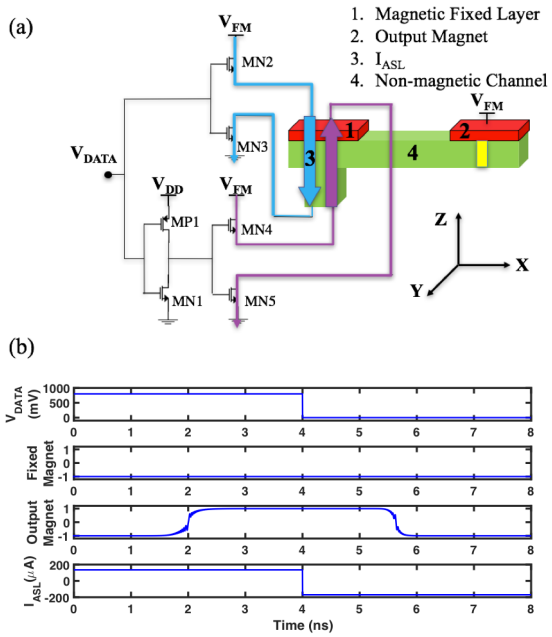

FIGURE 1. Electrical signal to spin signal transducer. (a) Schematics of the transducer. The physical layout is shown in Fig. 6(c). (b) Input signal (V_{DATA}), which switches the polarity of the voltage applied to the fixed magnet, which switches the output magnet accordingly. The orientation of the output magnet follows the input signal with a delay of 1.6 and 2 ns for high-to-low and low-to-high switching.

of the current is reversed and the electrons are extracted by the fixed magnet, most of the electrons will have magnetic moments antiparallel to that of the fixed magnet. In both cases, the accumulated spins diffuse inside the nonmagnetic channel toward the output magnet and apply a torque on the output magnet, based on the STT phenomenon, changing the orientation of the output magnetization [7], [23]. In summary, the direction of the electrical current passing through the fixed magnet determines whether the orientation of the output magnet becomes parallel or antiparallel to that of the fixed magnet. In Fig. 1(a), when the input signal (V_{DATA}) is 1, then transistors MN2 and MN3 are ON, but when V_{DATA} is 0, then transistors MN1, MP1, MN4, and MN5 are ON. The direction of the electrical current passing through the fixed magnet is designated by either a blue arrow for 1 or purple arrow for 0.

The transducer either inverts or copies the magnetization orientation of the fixed magnet to the output magnet according to whether V_{DATA} is high or low. Hence, the gate converts electrical voltage (V_{DATA}) to the magnetization orientation of the output magnet. The proposed circuit is simulated using SPICE models, which account for magnetization dynamics and spin transport mechanisms and are calibrated with experimental results, presented in [24]. The simulation results in Fig. 1(b) show that the switching of V_{DATA} from 800 mV (bit "1") to 0 mV (bit "0"), changes the magnetization orientation of the output magnet to the $+x$-direction (bit "1") and then to the $-x$-direction (bit "0"). This transducer copies the logic value of the V_{DATA} into the output magnet with

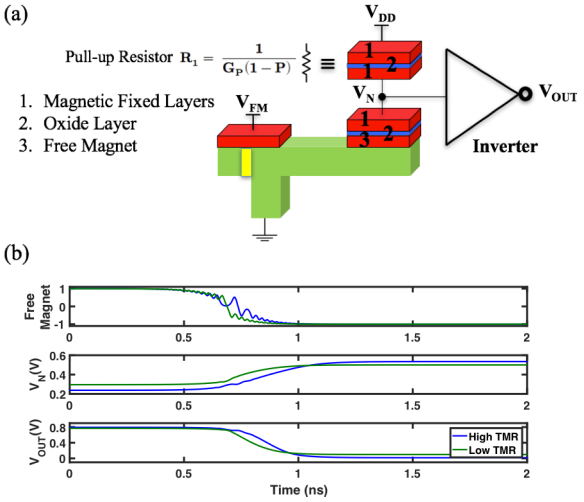

FIGURE 2. Spin signal to electrical signal transducer. (a) Schematics of the transducer. The physical layout is shown in Fig. 6(c). The resistor R_1 with the fixed resistance value of $(1/(G_P(1-P)))$ is implemented using an MTJ consisting of two magnetic fixed layers and is referred to as the resistor R_1 in this paper. The magnetic fixed layer, the oxide layer and the free magnet shown at the output of the ASL gate, labeled by 1, 2, and 3 in the figure, form an MTJ referred to as the MTJ in this paper, which the orientation of its free magnetic layer is changing due to the torque applied by the spin current, diffused from the input magnet. (b) Changes in the orientation of the free magnet are translated into changes in electrical voltage on the node V_N. The inverter provides a full swing between the ground and supply voltages at V_{OUT} accordingly. Simulations are done for two TMR values of 131% (low TMR) and 355% (high TMR).

a delay of 1.6 ns for high-to-low switching and a delay of 2 ns for low-to-high switching. The delay decreases as V_{FM} increases, but to ensure that the current density is safely below the breakdown value [25], we choose 150 mV as the largest simulated V_{FM} value. For the maximum V_{FM} value, the current density in the copper channel from the input magnet to the ground node is less than 10^7 A/cm^2, where the breakdown current density of the channel, determined by its length and width, is close to 10^8 A/cm^2 [25]. As Fig. 1(b) shows, the current passing through the fixed magnet (I_{ASL}) does not exceed 200 μA, which is less than the conventional write currents of MTJs [26].

III. SPINTRONIC TO CMOS SIGNAL TRANSDUCTION

To implement a spintronic to CMOS signal transducer, Fig. 2(a) employs a MTJ-based circuit that relies on the STT mechanism for switching. An MTJ consists of two magnets encompassing an oxide layer in which the electrical conductance across the gate is determined by the relative difference between the magnetization orientations of the two magnets [23] as

$$G_{MTJ} = \frac{G}{2} + \frac{\Delta G}{2}\hat{m}_1 \cdot \hat{m}_2 \tag{1}$$

where $G = G_p + G_{AP}$, $\Delta G = G_p - G_{AP}$, and $\hat{m}_1$ and $\hat{m}_2$ represent the magnetization orientation of the two magnets [23]. Under an assumption that magnet 2 ($\hat{m}_2$) is a fixed magnet in the $+x$-direction, the resistance across the MTJ is

$$R_{MTJ} = \frac{1+P}{G_P(1+P\hat{m}_{1,X})} \tag{2}$$

in which polarization factor P is defined as $P = \Delta G/G = \text{TMR}/(\text{TMR}+2)$ [23].

While the top layer of the MTJ of Fig. 2(a) is a magnetic fixed layer oriented along the $+x$-direction, the bottom layer is a free magnet receiving spin currents from the input magnet through a metallic channel. Through the STT mechanism, initiated by receiving spin currents, the magnetization orientation of the free magnet switches from antiparallel to parallel with the direction of the magnetic fixed layer. As the change in direction alters the resistance across the MTJ, the voltage at node V_N also changes. In Fig. 2(a), resistor R_1, composed of an MTJ consisting of two fixed magnets, has a fixed resistance value of $(1/(G_P(1-P)))$. The resistances across both R_1 and the MTJ depend on the thickness of their oxide layers. In the simulations of the paper, the TMR and resistance per-area values are based on the values, reported in [27]–[30]. Furthermore, the inverter captures the voltage changes at V_N and provides a full voltage swing between 0 and V_{DD} at the output.

It is important to note that in an STT–RAM, an electrical current must pass through MTJs for both read and write operations. Thus, the oxide thickness has to be sufficiently small so that the required write voltage does not become too large. As a result, a voltage swing across the low-resistance of an MTJ is too small to drive a CMOS inverter, requiring a more complicated sense amplifier. However, in the case of the proposed transducer, the write operation takes place via the spin current provided by the driving ASL gate. Hence, we can choose a large enough oxide thickness of the MTJ, which produces a large enough voltage swing to directly drive a CMOS inverter.

The large thickness of the oxide layer offers four more advantages: 1) lowers the read current, reducing the dissipated power; 2) drastically decreases the read disturb rate of the MTJ; 3) increases the TMR [27]–[30]; and 4) lowers the magnitude of the parasitic spin current injected from the fixed to the free magnet. Hence, the transducer can employ MTJs with TMR values as large as 300% to 400% and resistances as large as a few hundred kilohms while STT–RAM read/write circuits rely on MTJs with TMR values of 100% to 200% and resistances of one to two kilohms [31]. Simulation results of the transducer with two TMR values of 355% and 131% are presented in Fig. 2(b) [26]. Results show that by increasing the TMR, the voltage swing increases at V_N; in the case of the TMR value of 355%, the inverter is able to provide a full voltage swing (0 to V_{DD}) at its output. The negligible parasitic spin flux from the fixed to the free magnet, 1000$\times$ smaller than the spin current injected from the input to the free magnet, is accounted for in the simulations.

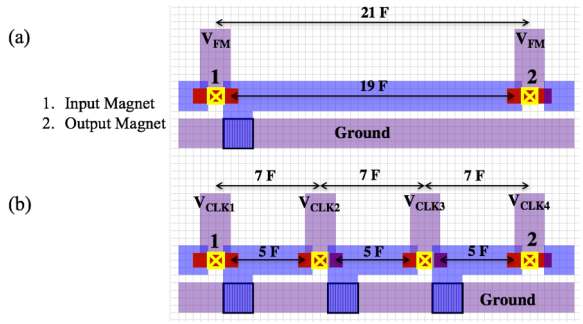

FIGURE 3. **(a) Layout of an ASL gate that transfers spin signals through a metallic interconnect. (b) Layout of ASL gates in a cascaded structure, which is a solution to transfer spin signals in long interconnects. The meaning of colors is defined in [33].**

IV. ASL TRANSDUCER FOR LONG-SPINTRONIC INTERCONNECTS

Spin signals in metallic interconnects attenuate exponentially with L_{Int} [7], so propagating signals along ASL interconnects longer than 1 μm is impossible. One potential solution is to use multiple ASL repeaters [32] that amplify a spin signal along the interconnect, illustrated in Fig. 3(b). We analytically study ASL gates as the building blocks for short metallic ASL interconnects and repeaters and present an approximate solution describing their switching delay and energy dissipation in Section IV-A. Then, we introduce a new transducer-based interconnect in Section IV-B and compare the potential performance of the two approaches.

A. PERFORMANCE ANALYSIS OF ASL REPEATERS

An ASL repeater consists of a cascade of ASL gates, shown in Fig. 3(b). Fig. 3(a) illustrates an ASL gate in which the electrical current passing through the input magnet becomes spin polarized at the interface of the magnet with the interconnect. We define the polarization factor (η) as $=(I_{SX}/I_C)$; I_C denotes the electrical current passing through the magnet, and I_{SX} denotes the spin-polarized current at the interface.

Generalized Ohm's law, including spin currents for the interface, is [34]

$$\begin{bmatrix} I_C \\ I_{SX} \\ I_{SY} \\ I_{SZ} \end{bmatrix} = \begin{bmatrix} G_{\uparrow\uparrow}+G_{\downarrow\downarrow} & G_{\uparrow\uparrow}-G_{\downarrow\downarrow} & 0 & 0 \\ G_{\uparrow\uparrow}-G_{\downarrow\downarrow} & G_{\uparrow\uparrow}+G_{\downarrow\downarrow} & 0 & 0 \\ 0 & 0 & 2\text{Re}G_{\uparrow\downarrow} & 2\text{Im}G_{\uparrow\downarrow} \\ 0 & 0 & -2\text{Im}G_{\uparrow\downarrow} & 2\text{Re}G_{\uparrow\downarrow} \end{bmatrix} \times \begin{bmatrix} V_N - V_F \\ V_{SX} \\ V_{SY} \\ V_{SZ} \end{bmatrix} \quad (3)$$

where $G_{\uparrow\uparrow}$, $G_{\downarrow\downarrow}$, and $G_{\uparrow\downarrow}$ are matrix elements derived from spin scattering at the magnet-interconnect interface [34]. Thus, by defining $G_u = G_{\uparrow\uparrow} + G_{\downarrow\downarrow}$ and $G_d = G_{\uparrow\uparrow} - G_{\downarrow\downarrow}$, the polarization factor is

$$\eta = G_d + \frac{G_u}{G_d}(1 - R_1 G_u). \quad (4)$$

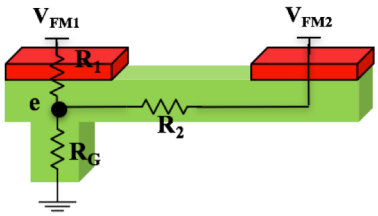

FIGURE 4. **ASL gate modeled by a star network of resistors for calculating the electrical current passing through the input magnet.**

The resistances R_1, R_2, and R_G are shown in Fig. 4, where R_1 is predominantly the interface resistance between the metallic channel and the input magnet, R_2 is the interface resistance between the metallic channel and the output magnet plus the resistance of the metallic channel between the input and the output magnets, and R_G is the resistance to ground. To ensure nonreciprocity (i.e., the magnetization of the input magnet determines that of the output magnet and not the other way around), R_1 must be smaller than R_2. For an ASL device with a short channel (interconnect) length of $\sim$150 nm, $R_1 = 2.6\ \Omega$ and $R_2 = 8.2\ \Omega$. However, for an ASL with a longer interconnect length of 600 nm, $R_1 = 2.6\ \Omega$ and $R_2 = 16\ \Omega$. By applying Kirchhoff's current law to the star network of Fig. 4 and connecting both magnets to the same supply voltage levels, $V_{\text{FM1}} = V_{\text{FM2}} = V_{\text{FM}}$, the voltage of node e becomes $V_{\text{FM}}(R_1R_G + R_2R_G)/(R_1R_2+R_2R_G+R_GR_1)$. Thus, we derive the electrical current passing through the input magnet as $I_{\text{In}} = (V_{\text{FM}} - V_e)/R_1 = V_{FM}R_2/\Delta$, in which $\Delta = R_1R_2+R_2R_G+R_GR_1$; hence, the spin-polarized current at the interface of the interconnect and the input magnet ($I_{S,\text{In}}$) is derived as

$$I_{S,\text{In}} = \eta I_{\text{In}} = \eta \frac{V_{\text{FM}}R_2}{\Delta}. \quad (5)$$

The spin current diffuses along the interconnect and experiences exponential attenuation because of the spin relaxation mechanisms [12]. Hence, the spin-polarized current at the interfaces of the interconnect with the output magnet ($I_{S,\text{Out}}$) will be

$$I_{S,\text{Out}} = I_{S,\text{In}} e^{-\frac{L_{\text{Int}}}{L_{\text{SRL}}}} = \eta \frac{V_{\text{FM}}R_2}{\Delta} e^{-\frac{L_{\text{Int}}}{L_{\text{SRL}}}}. \quad (6)$$

The spin current applied to a magnet exerts a torque on the magnet, which, if strong enough, switches the magnetization orientation of the magnet. The minimum current needed to switch a magnet, that is, the critical current (I_{Critical}), is defined as [10]

$$I_{\text{Critical}} = \frac{4e\alpha E_b}{\eta\hbar}\left(1 + \frac{\overline{H_S}}{2\overline{H_U}}\right) \quad (7)$$

where $\overline{H_S}$ and $\overline{H_U}$ represent the z-projections of the demagnetization field and the uniaxial anisotropy field, respectively. In CGS units, $\overline{H_S} = 4\pi M_S N_Z$, where the demagnetization tensor N is a tensor determined by the geometrical shape of

the magnets and M_S is the saturation magnetization of the magnets. The perpendicular uniaxial anisotropy field resulting from the crystal structure of the magnets is specified as $H_U = H_k m_z \hat{z}$, in which H_k is the Stoner–Wohlfarth field, which is related to the energy density K of the magnets [10]; thus, the magnitude of the z-projection of the anisotropy field is $(2K/(\mu_0 M_S))$. As the spin-polarized current reaching the output magnet increases, the magnet switches faster, we define an overdrive factor (σ) as

$$\sigma = \frac{I_{S,\text{Out}}}{I_{\text{Critical}}} = \frac{\eta V_{\text{FM}} R_2}{\Delta \cdot I_{\text{Critical}}} e^{-\frac{L_{\text{Int}}}{L_{\text{SRL}}}}. \tag{8}$$

The spin-polarized current applied to a magnet determines the switching delay of the magnet as [10], [35]

$$\tau = \frac{\tau_0 \ln\left(\frac{\pi}{\sqrt{\langle \phi_0^2 \rangle}}\right)}{\frac{I_{S,\text{Out}}}{I_{\text{Critical}}} - 1} \tag{9}$$

where ϕ_0 is the initial angle of switching and τ_0 is a fitting parameter. The stochastic thermal motion of electrons of a magnet generates thermal noise modeled as white Gaussian noise. In the presence of the uniaxial anisotropy field, the demagnetization field, and thermal noise, thermal fluctuations obey [10]

$$\begin{aligned}\langle \phi_0^2 \rangle &= \frac{k_b T}{\mu_0 M_S V\,(H_U - M_S(N_X - N_Y))} = \frac{k_b T}{\mu_0 M_S \text{VH}} \\ &= \frac{1}{\mu_0 M_S \text{VH} \beta}\end{aligned} \tag{10}$$

in which V is the volume of the magnet, $\beta = (1/k_b T)$ is the thermodynamic beta, and H is $H_U - M_S(N_X - N_Y)$. Thus, the switching delay of ASL gates is derived as

$$\tau_{\text{SW}} = \frac{\tau_0}{2} \frac{\ln(\pi^2 \mu_0 M_S \text{VH} \beta)}{\sigma - 1}. \tag{11}$$

The equation is simplified when $\sigma \gg 1$, in which

$$\begin{aligned}\tau_{\text{SW}} &= \frac{\tau_0 \ln(\pi^2 \mu_0 M_S \text{VH} \beta)}{2\sigma} \\ &= \frac{\tau_0 \Delta \cdot I_{\text{Critical}} \ln(\pi^2 \mu_0 M_S \text{VH} \beta)}{2\eta V_{\text{FM}} R_2} e^{\frac{L_{\text{Int}}}{L_{\text{SRL}}}}.\end{aligned} \tag{12}$$

For the magnet described in [7], we require $V_{\text{FM}} \gg 30\ \mu\text{V}$, which yields $\sigma \gg 1$. Moreover, (12) shows that τ_{SW} is exponentially dependent on L_{Int}, and τ_{SW} sharply increases for $L_{\text{Int}} > L_{\text{SRL}}$ [7]. The delay calculated from (12) is compared to the results from rigorous SPICE simulations [24] (Fig. 5). The SPICE models presented in [24] capture the magnet dynamics, spin mixing at the interfaces of magnets and normal metal, spin transport in metallic channels, and the thermal noise in magnets. Simulations are repeated 100 times for each data point to capture the effect of thermal noise in which error bars represent the $+/-\sigma$ along the mean value of data points. Furthermore, the switching delay, τ_{SW}, is inversely proportional to V_{FM}. Hence, to transfer bits at a faster rate, V_{DD} must increase proportionally.

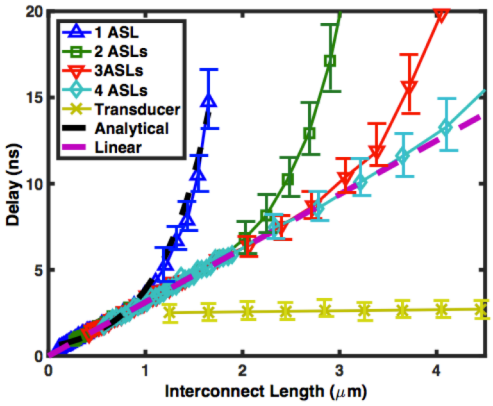

FIGURE 5. Delay of ASL repeaters is compared to that of electrical communication of spin information through transduction. For long lengths, the delay of ASL gates increases exponentially with length as predicted by the analytical equation. Meanwhile, for short lengths, the delay increases linearly because the linear terms of the Taylor expansion of delay are dominant. Similarly, the delay of ASL repeaters increases linearly with L_{Int} for short lengths and exponentially for long lengths. Although with multiple ASLs, the linear region is extended, the delay of the electrical interconnect is still shorter than that of the repeaters even for L_{Int} as small as 1.25 μm.

By taking the calculated delay and the power dissipation into account, we can derive the energy dissipation of ASL gates. The power dissipation of the ASLs is $P = \Sigma R_i I_i^2$, in which I_1, I_2, and I_G, the electrical currents passing through the resistors R_1, R_2, and R_G, are $(V_{\text{FM}} - V_e)/R_1$, $(V_{\text{FM}} - V_e)/R_2$, and V_e/R_G, respectively. Thus, the power dissipation of ASLs is $P = V_{\text{DD}}^2 \frac{R_1 + R_2}{\Delta}$. Hence, the energy dissipation per transferred bit is

$$\begin{aligned}E &= P\tau_{\text{SW}} \\ &= V_{\text{FM}} \frac{\tau_0 (R_1 + R_2) I_{\text{Critical}} \ln(\pi^2 \mu_0 M_S \text{VH} \beta)}{2R_2} e^{\frac{L_{\text{Int}}}{L_{\text{SRL}}}}.\end{aligned} \tag{13}$$

Energy dissipation E shows the same dependence on L_{Int} as τ_{SW}. Moreover, E is linearly proportional to V_{FM}, which confirms the tradeoff between the bit transfer rate and V_{FM}, which was discussed before. The power dissipation further increases because of the nonideal ground contact and supply voltage wires, which are accounted for in simulations under an assumption that 300 Ω of resistance has been added to the supply path [33]; that is, R_1 and R_2 are replaced by $R_1' = R_1 + 300\ \Omega$ and $R_2' = R_2 + 300\ \Omega$ in (13). For a repeater composed of N ASLs, we can approximate the delay by $\tau_{\text{Repeater}} = N\tau_{\text{SW}}$ and the fabrication area by the layout shown in Fig. 3.

B. PROPOSED LONG-RANGE SPINTRONIC INTERCONNECT

Fast transfer of spin signals in long-range interconnects requires an increase in the number of cascaded ASLs, N; however, the power dissipation of ASL repeaters increases proportionally with N. Fig. 6(a) shows the proposed

TABLE 1. Simulation parameters.

Interface Parameters (Co/Cu) [38]		
Majority Spin Conductance	$G_{\uparrow}$	0.375 1/Ω
Minority Spin Conductance	$G_{\downarrow}$	0.125 1/Ω
Real Spin-Mixing Conductance	Re $G_{\uparrow\downarrow}$	3.43751 1/Ω
Imaginary Spin-Mixing Conductance	Im $G_{\uparrow\downarrow}$	9.37×10^{-3} 1/Ω
Magnets (Co) [22] [24] [39] [40]		
Magnet Length	L_X	66 nm
Magnet Width	L_Y	22 nm
Magnet Height	L_Z	3 nm
Gilbert Damping Coefficient	α	0.005
Saturation Magnetization	M_S	1.45×10^6 A/M
Demagnetization Tensor Coefficient	N_X	0.0443
Demagnetization Tensor Coefficient	N_Y	0.1390
Demagnetization Tensor Coefficient	N_z	0.8166
Magnet Barrier	Δ/K_BT	40
Channels (Cu) [12]		
Channel Length	L_{Int}	142 nm
Channel Width	W_{Int}	44 nm
Aspect Ratio	AR	1
Transistors [41]		
Half Pitch Size	F	22 nm
Length	L_X/F	1
Width (Inverters)	W_X/F	5
Width (Drivers)	W_X/F	30

transducer-based interconnect for the electrical transmission of spin information. The interconnect converts the spin signals into electrical signals, which transfer along an electrical interconnect, a more efficient way to communicate signals over long distances. Then, the electrical signals are converted back into spin signals. Fig. 6(b) shows the simulation results of the interconnect. The delay of the proposed interconnect is compared to that of the ASL repeaters in Fig. 5. As shown in Fig. 5, the switching delay of ASL gates can be approximated as a linear function of L_{Int} for lengths shorter than L_{SRL}, but it exhibits an exponential dependence on L_{Int} for $L_{\text{Int}} \gg L_{\text{SRL}}$. The slope of the delay in the linear region is $((\tau_0\Delta \cdot I_{\text{Critical}}\ln(\pi^2\mu_0 M_S \text{VH}\beta))/(2\eta V_{\text{FM}}R_2L_{\text{SRL}}))$. For a repeater composed of N-cascaded ASLs, the linear region extends proportional to N, which is consistent with the simulation results of Fig. 5. Fig. 5 shows that the switching delay of the proposed interconnect is lower than that of the ASL repeaters even for a length of 1.25 μm, the shortest possible length of the interconnect using transducers. As illustrated in the layout in Fig. 6(c), the length of the interconnect is longer than 57 F (half-pitch size), in which the shortest possible length is 1.25 μm for $F = 22$ nm, shown in Table 1.

The delay of the transducer-based interconnect increases with L_{Int} because the parasitic resistances and capacitances of electrical interconnects increase with L_{Int}; however, the rate of the increase in the delay is far smaller than that of the linear region of ASL repeaters. In these devices, the supply voltage is turned on only when the signals are passing through the gate. Thus, the supply voltage clocking, shown in Fig. 7, reduces energy dissipation with turning OFF the device once data has transmitted along the interconnect [21]. We account for the energy dissipation in the driving transistors, which comes in two forms: 1) the energy dissipation due to the drain–source current ($I_D V_{\text{DS}}\tau$) and 2) the energy dissipation due to charging and discharging the transistor capacitance (CV^2). Because of the relatively large current amplitude

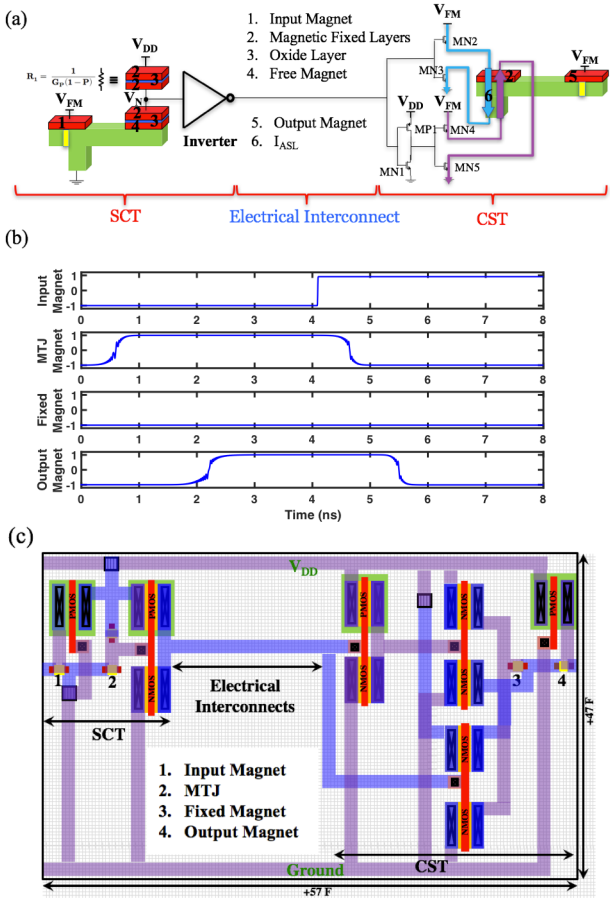

FIGURE 6. Proposed long spintronic interconnect. (a) First, the spin signals are converted to electrical signals using a spin to CMOS signal transducer (SCT); then, the electrical signal is transmitted through a long electrical interconnect and converted back to spin signals using a CMOS to the spin signal transducer (CST). (b) Magnetization orientation of the output magnet is the inverse of the magnetization orientation of the input magnet with a delay of 1.6 ns. (c) Layout consists of two transducers with minimum feature sizes connected to an electrical interconnect.

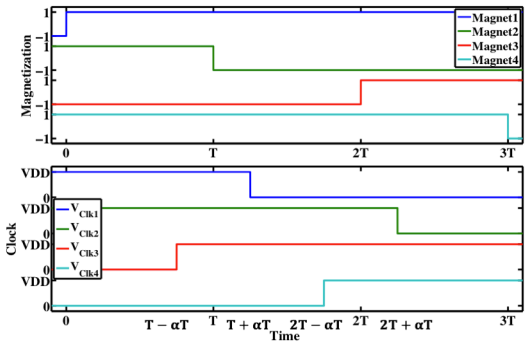

FIGURE 7. Clocking schemes used to minimize the energy dissipation of the ASL repeaters. Clocks are on αT before and after the mean switching time to cancel the potential impact of thermal noise. α is assumed to be 25% in the simulations.

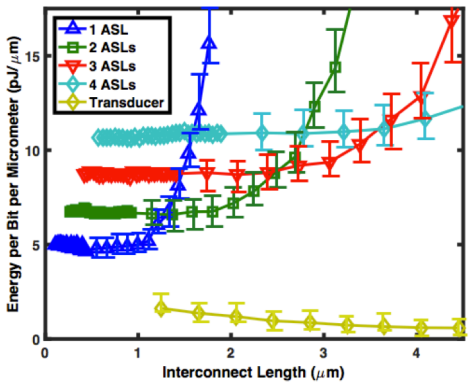

FIGURE 8. **Energy dissipation per unit length of the ASL repeaters is compared to that of the proposed spintronic interconnect. The dissipated energy of the proposed interconnect is lower than that of repeaters even for L_{Int} as small as 1.25 μm. Although the energy dissipation of repeaters increases as the number of cascaded ASLs for short interconnects increases, but the repeaters with more cascaded ASLs dissipate lower power for long interconnects.**

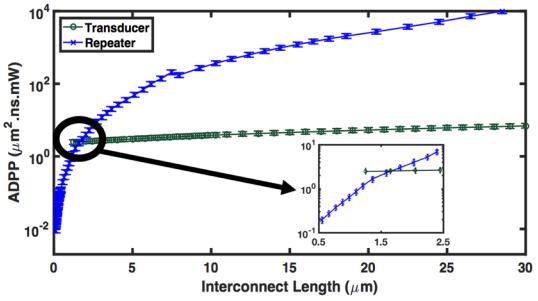

FIGURE 9. **ADPP is a measure that takes delay, power dissipation, and area into account. Although the proposed interconnect has larger area overhead, its advantage in terms of energy enables it to outperform ASL repeaters for lengths longer than 1.6 μm.**

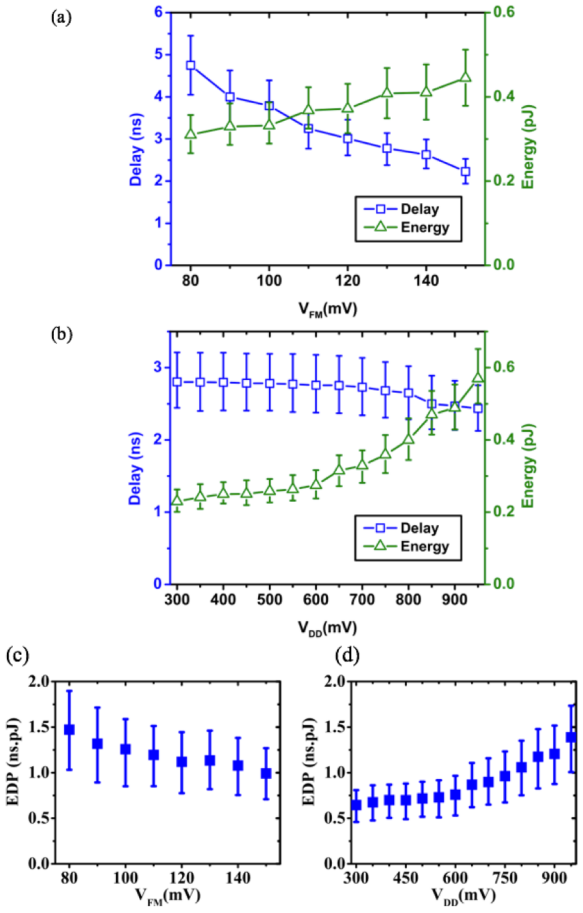

FIGURE 10. **Delay and energy dissipation variations versus (a) voltage applied to the magnets (V_{FM}) and (b) supply voltage (V_{DD}). EDP variations versus (c) V_{FM} and (d) V_{DD}. The interconnect must operate at the lowest V_{DD} and the highest V_{FM} voltage values without reaching its breakdown current density to minimize the EDP. The error bars represent variations in the delay and energy dissipation generated by the stochastic thermal noise of magnets.**

and the pulsewidth needed to switch a magnet, the second component is more than 100× smaller than the first one and can be ignored. The power dissipation associated with clock generation and distribution has not been incorporated in this paper. While the proposed interconnect scheme requires only two transistors for supply clocking, the ASL repeater requires $N+1$ transistors where N is the number of ASL stages in the repeater. Hence, having a simpler clocking circuit, is another advantage of the proposed transducer-based interconnect. In Fig. 7, to counter the impact of thermal noise, clocks are on αT before and after the mean switching time. The energy dissipated by the supply voltages is shown in Fig. 8. As L_{Int} increases, the energy per-unit length remains constant in the linear region and increases exponentially afterwards. Hence, repeaters composed of two, three, and four ASLs minimize the energy dissipation of interconnects longer than 1.3, 2.5, and 3.7 μm, respectively. The transducer-based interconnect dissipates less energy than ASL repeaters, even for interconnects as short as 1.25 μm. Compared to energy per-unit length of the ASL repeaters, that of the electrical interconnect decreases as the length of the interconnect increases since energy dissipation, which mostly takes place in the transduction of signals, experiences a far smaller increase. Despite the advantage of the transmission of signals using transducers over that of ASL repeaters in terms of switching delay and energy dissipation, ASL repeaters have an advantage in terms of a smaller footprint area. Taking all these factors into account, we show the ADPP metric [36], [37] for both interconnect schemes in Fig. 9, which shows that the proposed transduction-based scheme, utilizing electrical transmission, has an advantage in terms of the ADPP for interconnects as short as 1.6 μm. Although the proposed scheme compared to the ASL repeater scheme shows a significant improvement in terms of delay, energy, and ADPP, the proposed structure cannot compete with electrical interconnects used in purely CMOS circuits.

Fig. 10 depicts the delay and energy dissipation of signal transduction and transmission under various supply

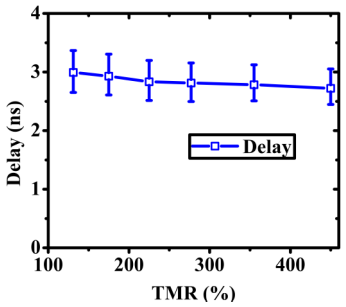

FIGURE 11. As TMR increases, the voltage swing at node V_N of Fig. 5 becomes larger; hence, the delay becomes smaller. However, the voltage swing is relatively large even for TMR values as low as 125%, and the improvement in switching delay by increasing TMR is limited to less than 10%.

voltage (V_{DD}) and magnet voltage (V_{FM}) values. In Fig. 10(a), V_{DD} is fixed at 650 mV while V_{FM} changes from 80 to 150 mV. In Fig. 10(b), V_{FM} remains fixed at 120 mV while V_{DD} changes from 300 to 950 mV. Fig. 10(c) exhibits the energy-delay product (EDP), which decreases 49% by increasing V_{DD} from 300 to 950 mV; Fig. 10(d) shows that the EDP decreases 31% by decreasing V_{FM} from 80 to 150 mV. Hence, we minimize EDP by operating the proposed device under lower V_{DD} and higher V_{FM} voltage values. The thickness of the oxide layer potentially changes the delay and the energy dissipation of the proposed interconnect. The oxide thickness, subject to variations by various fabrication processes, changes both the TMR and the resistance of MTJs. To capture potential variations, Fig. 11 illustrates changes in the switching delay by changing TMR values. The simulations use the relationship between the TMR and the oxide thickness from [30]. Fig. 11 shows that the increase of the TMR from 125% to 450% decreases the switching delay by less than 10%. Although by increasing TMR, voltage sweep $(2P/(4-P^2))V_{DD}$ becomes larger at V_N, but the voltage sweep is already large enough for the inverter, even for TMR values as low as 125%. In these simulations, the TMR and resistance per-area values are based on the values mentioned in [27] and [30].

V. CONCLUSION

Studies have examined spintronic devices to augment CMOS circuits and systems in memory and data processing applications, owing to their inherent nonvolatility, low voltage operation, and introduced new and enhanced functionalities. This paper proposes two simple, yet efficient CMOS–spintronic transducer circuits that convert back and forth between spin signals and electrical signals in hybrid CMOS–spintronic circuits, which must efficiently transmit spin signals in both short and long ranges. Unlike electrical signals, spin signals, however, suffer from exponential decay of their amplitudes as their interconnect lengths increase. Amplifying spin signals through long-range interconnects using repeaters is an inefficient method of transmitting spin signals. Thus, using the proposed transducer circuits, we propose a new scheme for long-range spintronic interconnects. Although the transducers add to circuitry and area overhead, the proposed spintronic interconnect outperforms all-spin-based repeaters in terms of transmission delay, energy dissipation per bit per unit length, and ADPP for interconnects longer than 1.6 μm.

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