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Uniform Benchmarking of Low-Voltage van der Waals FETs

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ABSTRACT Monolayer MoS_2, $MoSe_2$, $MoTe_2$, WS_2, WSe_2, and black phosphorous field-effect transistors (FETs) operating in the low-voltage (LV) regime (0.3 V) with geometries from the 2019 and 2028 nodes of the 2013 International Technology Roadmap for Semiconductors are benchmarked along with an ultrathin-body Si FET. Current can increase or decrease with scaling, and the trend is strongly correlated with the effective mass. For LV operation at the 2028 node, an effective mass of $\sim 0.4\ m_0$, corresponding to that of WSe_2, gives the maximum drive current. The short 6-nm gate length combined with LV operation is forgiving in its requirements for material quality and contact resistances. In this LV regime, device and circuit performances are competitive using currently measured values for mobilities and contact resistances for the monolayer 2-D materials.

INDEX TERMS 2-D materials, benchmarking, black phosphorous (BP), field-effect transistor (FET), transition metal dichalcogenide (TMD), ultrathin body (UTB) Si, van der Waals (vdW) materials.

I. INTRODUCTION

THERE is significant interest in understanding how 2-D semiconductors compare with traditional semiconductors for use as the channel material in ultrascaled field-effect transistors (FETs). The FET also serves as a baseline device for determining targets for material parameters. For example, given a set of FET performance specifications, such as drive current, switching energy, switching delay, etc., one can then ask, ''what material parameters, such as, for example, mobility, effective mass, bandgap, or contact resistance, are sufficient to achieve these device performance metrics?'' One can also inquire, ''what material parameters optimize the device performance?'' Thus, benchmarking of a baseline device provides top–down targets for materials benchmarking [1].

Promising 2-D semiconductors include the transition metal dichalcogenides (TMDs) with the chemical form MX_2, where M = Mo or W and X = S, Se or Te [2]–[9], and bandgaps in the range of 1–2 eV [3], [6]. A more recent addition to the van der Waals (vdW) class of materials for FET applications is black phosphorus (BP) [10]–[12]. BP's large field-effect mobility and highly anisotropic bandstructure make it a promising material for FET applications [10], [11], [13]–[16].

A number of articles in the literature have theoretically predicted the performance of these alternate materials for future device applications. While the majority of the performance predictions are for MoS_2 FETs [17]–[24] and BP [14], some of them focus on device comparisons within the TMD group for conventional FETs [25]–[27] and for tunnel FETs [28], [29]. The BP FET was compared against the MoS_2 FET in [30]. A BP-based TFET was proposed in [31].

There are two different operation regimes denoted as high performance (HP) and low power (LP) defined in the 2013 International Technology Roadmap for Semiconductors (ITRS) [32]. There is also a low-voltage (LV) regime considered in [33] and benchmarked in [34] and [35]. It is this LV regime that we consider in this paper with a supply voltage of 0.3 V. As of today, there are a large number of material candidates for future CMOS devices. But little is known about their relative performance in the LV regime, since, to the best of our knowledge, they have never been compared in a single

systematic study. In general, LV has been given less attention than HP or LP operation.

Inspired by the device benchmarking of the Nanoelectronics Research Initiative [34], [35] and the materials benchmarking of STARnet centers [1], in this paper, we present and compare BP and five different TMD-based FETs. For a baseline comparison, we also simulate an ultrathin body (UTB) Si FET using the same model and code. The vdW materials that we chose to compare are MoS_2, $MoSe_2$, $MoTe_2$, WS_2, WSe_2, and BP. Performance metrics are compared for individual devices as well as for a standard integrated circuit of a 32 bit adder using the beyond CMOS benchmarking (BCB) scheme 3.0 [35].

II. SIMULATION METHOD

The structural parameters for the devices were taken from columns 2019 and 2028 of the LP technology requirement tables, ITRS 2013 [32]. The values are summarized in Table 1. The devices are assumed LV with $V_{DD} = 0.3$ V [35]. Two different production years were selected to examine the effect of scaling on the devices of interest. We primarily considered single gate (SG) FETs, and a few exemplary simulations were performed for double gate (DG) structures as well.

TABLE 1. Device dimensions according to ITRS 2013 [32].

Structural Parameters	Year of production	
	2019	2028
Metal 1 1/2 pitch, F (nm)	20	7.1
Physical gate length, L_g (nm)	13.3	5.9
Effective channel length, L_{ch} (nm)	10.6	4.7
Dielectric constant of top gate oxide, ϵ_r	15.5	20
Physical gate oxide thickness, t_{ox} (nm)	2.42	2.10
Equivalent oxide thickness, EOT (nm)	0.6089	0.4095

Fig. 1 shows the device structures used for the simulations in this paper [36]. The buried oxide and extended oxide regions are SiO_2 with a dielectric constant of 3.9. The gate oxide is composed of both high-K (according to Table 1) oxide under the gate and SiO_2 [37] in the source–drain extensions for improved gate control. For the Si FET, transport from source to drain is in the (100) direction. For the BP FET, transport is in the X-direction, the direction of the light mass. For the circuit metrics, the default width of four times the pitch is used for the FETs [35].

For the TMD and Si FETs, electron conduction is considered, while for the BP FET, both electron and hole conduction are considered, since most recent experimental work focuses on hole transport [38]. For the vdW materials, the source and drain doping densities were swept from 1×10^{19} to 1×10^{20} cm^{-3} ($\sim 5.7 \times 10^{11} - \sim 7.3 \times 10^{12}$ cm^{-2}). For each node and geometry, two results are recorded. One result is for the doping density that results in the maximum drive current. The second result is for the maximum doping density

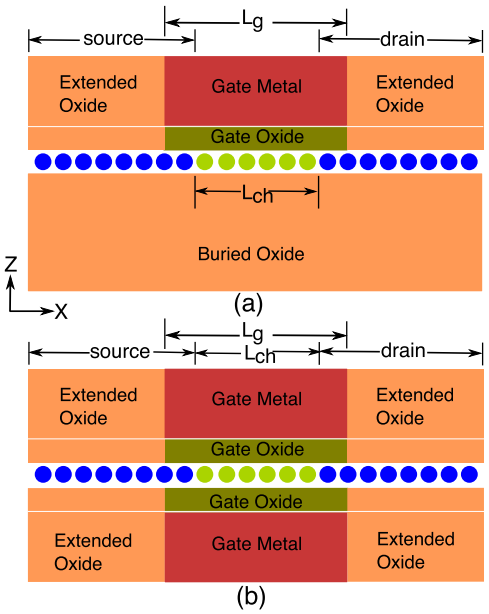

FIGURE 1. Cross section of the device used for simulation. (a) SG FET. (b) DG FET. The central line of dots indicates the monolayer device region.

of 1×10^{20} cm^{-3}. The drive currents versus source doping are shown in Fig. S1 of the Supplementary Information. This optimization is performed with the contact resistance set to zero. For the 3-nm Si UTB FETs, a source and drain doping density of 1×10^{19} cm^{-3} (3×10^{12} cm^{-2}) is used [19].

Material properties for all of the materials considered in this paper are summarized in Table S1 of the Supplementary Information. The UTB Si has a finite thickness of 3 nm, and all of the vdW materials are monolayers. It has been shown that adding multiple layers on top of a single layer cannot boost the ON-current [24]. Listed mobilities for monolayer vdW materials are experimentally measured values obtained from the literature [7], [39]–[43] except for $MoTe_2$. Mobility in monolayer $MoTe_2$ was unknown at the time of this work; hence, it was approximated from $MoSe_2$ using both materials' electron effective masses (see footnote of Table S1).

As evident from the conduction band Λ-valley to K-valley energy separation, $\Delta_{K\Lambda}$, listed in Table S1, all values of $\Delta_{K\Lambda}$ are less than V_{DD}, and therefore, they will have an effect on the electron transport in the TMD FETs. In addition, there is considerable spin-splitting in many of the conduction band K and Λ valleys. Therefore, we have taken the different spins and valleys into account by using a multiple single-band approach, as shown in Fig. 2. In this approach, each spin and valley is treated as an independent band with its own effective mass.

For each band, the discretized effective mass Schrödinger equation is solved for the charge density using a nonequilibrium Green function approach similar to that described in [19]. The heavily doped source and drain regions are treated as contacts in equilibrium with their respective Fermi levels [44]. The total charge at each site is the sum of

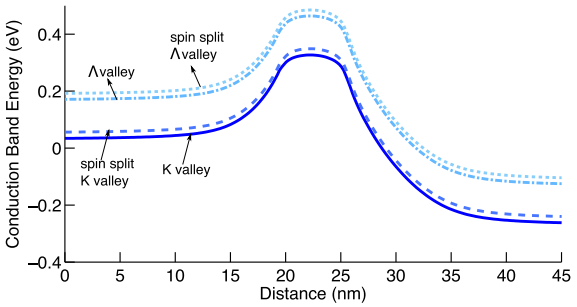

FIGURE 2. Illustration of the multiple single-band approach used in this paper. Potential profile for four valleys in the conduction band for a typical TMD FET is shown.

the charge calculated for each band. The charge is self-consistently solved with Poisson's equation. The electrostatic potential within the device is calculated using a 2-D finite difference solution of Poisson's equation discretized on a 0.2-nm grid within the channel and a 0.5-nm grid within the oxide. Dirichlet boundary conditions are set at the metal gate and Von Neumann boundary conditions are used at all other exterior boundaries.

Once the charge calculation has converged, current is calculated for each band. The contribution from all bands is summed to give the total current. The effect of scattering in the channel is included with a reflection coefficient determined from a mean free path related to the mobility and an effective channel length [45], [46]. Details are provided in the Supplementary Information.

The OFF-current is set at 1.5 nA/μm for all devices. The drain bias V_{DS} and ON-state gate voltage V_{GS} are 0.3 V. The maximum allowable source–drain total contact resistances (R_{SD}) are estimated following the methodology used by the ITRS [32], [36]. For this, a reference value of current was first calculated with scattering included but R_{SD} set to 0. A set of simulations, including scattering, were then performed for a range of R_{SD} values. R_{SD} was divided equally between the source and the drain. In the self-consistent loop, the internal gate and drain potentials with respect to the source, V'_{GS} and V'_{DS}, were updated at each iteration according to $V'_{GS} = V_G - I_D R_{SD}/2$ and $V'_{DS} = V_{DD} - I_D R_{SD}$, where V_G is the applied gate voltage with respect to ground. The series resistance raises the source potential by $I_D R_{SD}/2$, which lowers the gate to source voltage by the same amount. The particular value of R_{SD} that resulted in a 33.3% reduction of current compared with the reference current was then chosen as the maximum allowable contact resistance for the LV devices.

Two performance metrics are the switching delay and the switching energy defined as

$$t = CV_{DD}/I_{ON} \text{ and } E = CV_{DD}^2 \tag{1}$$

where I_{ON} is the ON-current, C is the total capacitance that includes the oxide capacitance, the semiconductor capacitance (also known as quantum capacitance), and any parasitic capacitance that might be present. The capacitance is determined as follows. The total capacitance $C = \partial Q/\partial V_G$, where Q is the total charge in the entire semiconductor region that includes the source, channel, and drain. In this manner, the gate and fringing capacitances are taken into account all at the same time. In doing so, one has to make sure that no other external inputs are changing except the applied gate bias. Therefore, the total charge Q is calculated with $R_{SD} = 0$, since R_{SD} alters the effective gate voltage V'_{GS}.

The calculated drive currents and capacitances are input into the BCB 3.0 scripts [35]. The BCB 3.0 scripts use the input for one type of transistor and approximate the ON-current of the pFET, which is equal to that of the nFET. Delay times and switching energies are calculated using empirical rules chosen to match SPICE simulations. For circuits, a per unit length interconnect capacitance of 126 aF/μm is used, and the interconnect length associated with each transistor is $20F$, where F is the DRAM half pitch corresponding to the technology node. Full details of the BCB 3.0 method are given in [35].

III. RESULTS

The ON-current, optimum doping, and series resistance for each material, node, and geometry are tabulated in Table 2. I_{ball} refers to the ballistic ON-current calculated with both the contact resistance R_{SD} and the backscattering coefficient r_c set to 0. R_{SD} is the maximum allowable total contact resistance (source plus drain) that degrades the current calculated in the presence of scattering by 33.3%. I_{scatt} is the ON-current, where both r_c and the maximum allowable R_{SD} are included. For the rest of our discussion, unless otherwise noted, the ON-current will refer to the scattering limited current, I_{scatt}. For the SG vdW materials, the drive currents at optimum doping are shown in Fig. 3 plotted versus the bandedge effective mass of the material for both the 2019 and 2028 nodes. The inset is the same plot but for a fixed doping of 1×10^{20} cm^{-3}. Each data point is labeled with its material.

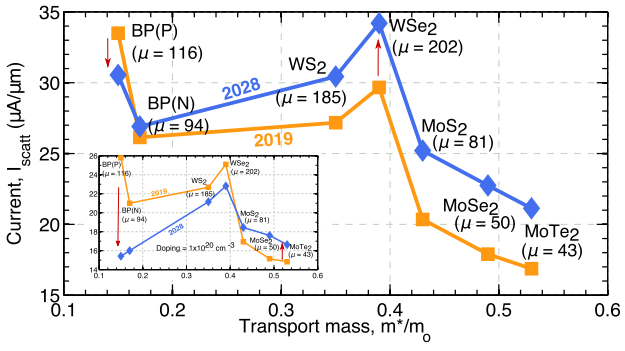

FIGURE 3. I_{scatt} versus effective mass for the SG vdW FETs at the 2019 and 2028 nodes with optimized source and drain doping. Each data point is labeled with its material and mobility. The red arrows indicate the current trends when scaling the gate lengths from the 2019 node to the 2028 node. Inset: same plot for a fixed doping density of 1 × 10^{20} cm^{-3}.

TABLE 2. Ballistic on currents, I_{ball} (μA/μm) and scattering limited on currents, I_{scatt} (μA/μm) for both 2019 and 2028 nodes. Source–drain doping, N_{SD} (cm^{-3}) is the optimum doping at which I_{scatt} maximizes for the vdW FETs. For Si, current maximizes at a doping even lower than 1 × 10^{19} cm^{-3}, and hence, this value was chosen as a compromise between current and screening length. I_{ball} was calculated at the listed N_{SD}'s, where contact resistance, R_{SD} (k$\Omega\mu$m), and backscattering coefficient, r_c, were both set to 0. I_{scatt} is the ON-current, where both R_{SD} and r_c are included. BP(n) and BP(p) refer to n-type and p-type BP FETs, respectively.

		13.3 nm				5.9 nm			
		$I_{\rm ball}$	$I_{\rm scatt}$	$N_{SD}(\times 10^{19})$	R_{SD}	$I_{\rm ball}$	$I_{\rm scatt}$	$N_{SD}(\times 10^{19})$	$R_{\rm SD}$
MoS_2	SG	63.14	20.35	3	1.68	56.86	25.21	3	1.2
	DG	107.1	33.6	6	0.9	110.2	48.06	5	0.6
$MoSe_2$		61.81	17.89	4	1.8	56.8	22.75	3	1.28
$MoTe_2$		61.7	16.9	4	1.9	55	21.16	3	1.57
WS_2	SG	64.6	27.18	3	1.1	62	30.44	2	1.03
	DG	109.8	45.18	4	0.63	113.2	56.9	4	0.5
WSe_2	SG	67.6	29.67	3	1.02	64.85	34.2	2	0.83
	DG	116	50.23	4	0.53	116.56	62.5	5	0.43
BP(N)	SG	70.65	26.14	3	1.18	58.94	26.91	2.1	1.11
	DG	121.6	42.08	4	0.76	111.15	50.95	4	0.6
BP(P)	SG	75.8	33.45	2.55	0.95	59.2	30.55	2	0.95
	DG	123.4	53.26	4	0.54	113.5	58.4	4	0.53
Si	SG	19.7	9.73	1	2.9	6.22	3.73	1	6.5
	DG	77.25	36	1	0.87	45.46	25.07	1	1.1

The physical mechanisms governing FET performance are the same as those analyzed in [47] for III–V FETs, the balance between source exhaustion and tunneling leakage. The range of transport effective masses, from 0.15 m_0 for p-type BP to 0.53 m_0 for $MoTe_2$, makes this balance different for the different materials. The optimum source doping is lower for the lighter mass materials. The lower doping results in longer screening lengths of the channel potential into the source and drain regions increasing the effective channel length and decreasing the OFF-state direct tunneling.

For the X-directed transport in p-type BP, the low mass in the transport direction provides a high velocity, and the large transverse effective mass provides many modes for transport. Because of the low transport mass, the optimum source doping of 2 × 10^{19} cm^{-3} is the lowest among the vdW FETs. As shown in Fig. 4, in the OFF-state, the low doping results in long screening lengths of the channel potential into the source and drain regions increasing the effective OFF-state channel length and decreasing the OFF-state direct tunneling. The OFF-state channel potential decays approximately 10 nm into the source and 15 nm into the drain giving an OFF-state total effective source to drain length of 30 nm at the 2028 node. In the ON-state, the small channel potential decays within a few nanometers into the source, and the high field region extends approximately 10 nm into the drain. Thus, the effective source to drain region in the ON-state is approximately 15 nm. One advantage is that the longer depletion lengths in the source and drain reduce the fringing capacitance between the source and drain, and therefore reduce the *RC* delay time. A disadvantage is that the transit time increases. A saturation velocity of 10^7 cm/s gives a transit time that is ten times less than the *RC* delay time. At 10^6 cm/s, the two times are comparable.

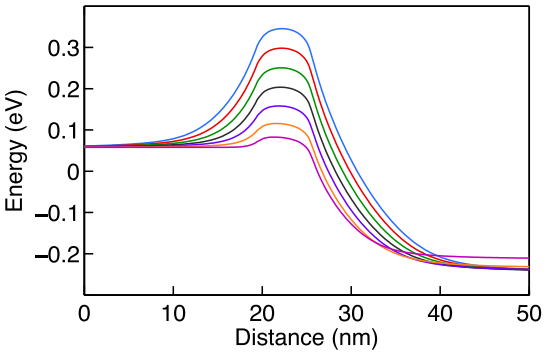

FIGURE 4. Energy band diagrams for different gate biases of the p-type BP FET at the 2028 node with doping density of 2 × 10^{19} cm^{-3}. Kinetic energy for the holes is taken to be positive. The source Fermi energy is 0 eV.

As the gate length is scaled from 13 to 6 nm, with optimized doping, the ON-current of BP drops slightly, and the ON-currents of all of the TMD FETs increase. The TMD FETs with the heavier effective masses benefit from scaling, while the BP FET with the lightest transport mass is degraded by the scaling. In every case, the ballistic current decreases as the channel length decreases from 13 to 6 nm, in agreement with the previous work [36], and the ballistic current of p-type BP with the lightest transport mass decreases the most. For BP, the large decrease in the ballistic current dominates, and the total current including scattering decreases. For the heavier mass TMDs, the ballistic current is only slightly reduced.

As the channel length becomes comparable with the mean free path, reflection is reduced. This process dominates for the TMDs with heavier effective masses, and their ON-current increases as the gate length is scaled down to 6 nm.

The effective mass affects two processes that determine if the current will increase or decrease with scaling, and the trends become very clear with a fixed source and drain doping of 1×10^{20} cm^{-3}, as shown in Fig. 3 (inset). The first process is direct tunneling through the channel, and the second process is scattering in the channel. The process of direct tunneling is governed by the effective mass of the channel material. A heavier mass minimizes the OFF-state leakage, which enhances the drive current for a fixed V_{DD}, because a smaller percentage of V_{DD} is required to shut the device OFF. This effect is shown in Fig. 5. The background color indicates the current spectrum (on a log scale) with the brightest yellow indicating the highest current. A comparison of Fig. 5(a) and (b) shows that, in the OFF-state, tunneling is significant through the BP barrier but is suppressed in the $MoTe_2$ barrier. For BP with the lightest transport mass, the barrier height required to attain the OFF-state current of 1.5 nA/μm is 365 meV. For $MoTe_2$ with the heaviest transport mass, the barrier height required to attain the same OFF-state current is 307 meV, approximately 60 meV lower than that for BP. Applying 0.3 V to the gate reduces the potential in the channels by 254 meV for BP and 247 meV for $MoTe_2$, so that the barrier height in the ON-state is 111 meV for BP and 60 meV for $MoTe_2$. Thus, the barrier height of the channel in the ON-state for BP is almost twice that for $MoTe_2$. This effect is responsible for the reduction in I_{ball} as the gate length is scaled from 13 to 6 nm.

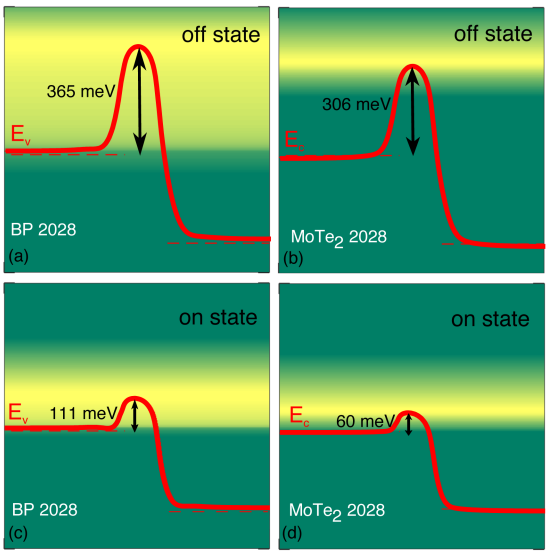

FIGURE 5. (a) Valence band edge for p-type BP (with the hole energy taken as positive) and (b) conduction band edge of $MoTe_2$ (with the electron energy taken as positive) in the OFF-state. (c) BP and (d) $MoTe_2$ in the ON-state for the 2028 node with fixed source and drain doping of 1×10^{20} cm^{-3}. The source Fermi energy is the reference energy at $E = 0$. The background color indicates the current density per unit energy on a log scale. Yellow is the highest current (color online).

The second process of scattering in the channel is also strongly correlated with the effective mass. A heavy mass is associated with a short mean free path, so that as the channel is scaled down to 6 nm, the device becomes more ballistic, r_c decreases, and the current increases with scaling. The Mo compounds have the highest effective masses, the lowest measured electron mobilities, and the shortest mean free paths, as shown in Table S1. Therefore, these materials benefit most from scaling, since direct leakage through the channel is not a problem, and they become more ballistic as the channel length is scaled. For BP with the lightest mass in the transport direction, the first process of tunneling dominates the performance, and there is significant reduction in I_{scatt} going from the 2019 node to the 2028 node when the doping is fixed at 1×10^{20} cm^{-3}. Even at the optimum doping condition, BP is the only 2-D material that suffers from a reduction in current after scaling.

Adding a second gate to create a DG structure increases the magnitude of the current, and the increase in the magnitude of the current is qualitatively different for the vdW channels and the UTB Si channel. At the 2019 node, adding a second gate increases I_{ball} by a factor of 1.7 for the TMD FETs and 1.63 for p-type BP. The increase in I_{scatt} is slightly less. For 2028 TMDs, adding the second gate increases I_{ball} by the factors of 1.8–1.94 for TMDs and 1.9 for both BP. The increase in I_{scatt} is identical to the increase in I_{ball} within numerical error. The larger increases in current due to doubling the gates in the 2028 2-D FETs indicate that the SG is losing some control of the channel when the gate is scaled down to 5.9 nm. In the DG geometry, the second gate provides greater electrostatic control of the channel. The increased gate control moves the position, where $\Delta V_{ch} = k_B T/q$, further toward the drain which increases L_{eff} and, consequently, r_c, and is the reason why the increase in I_{scatt} resulting from a second gate may not be quite as large as the increase in I_{ball}.

The maximum allowable projected total contact resistance (source plus drain) R_{SD} for each node and material are also included in Table 2. For the SG devices, the current is small, and one can get away with relatively high contact resistances on the order of 0.48–0.95 k$\Omega\mu$m per contact at the 2019 node, and 0.42–0.52 k$\Omega\mu$m per contact at the 2028 node. To achieve the higher current densities of the DG TMD devices, lower contact resistances are required, on the order of 265–450 $\Omega\mu$m per contact at 2019 node and 215–300 $\Omega\mu$m per contact at 2028 node. Contact resistances of 240 $\Omega\mu$m have already been reported in the literature [48].

From Eq. (1), the product of device capacitance and resistance gives the switching delay of each individual device. Fig. 6 shows the capacitance versus resistance for each material, node, and geometry. The arrows show the effect of going from an SG geometry to a DG geometry. First, we discuss the SG geometry at each node. At the 2019 node, among the SG vdW FETs, $MoSe_2$ and $MoTe_2$ have both the most resistance and capacitance and BP has the least. At the 2028 node,

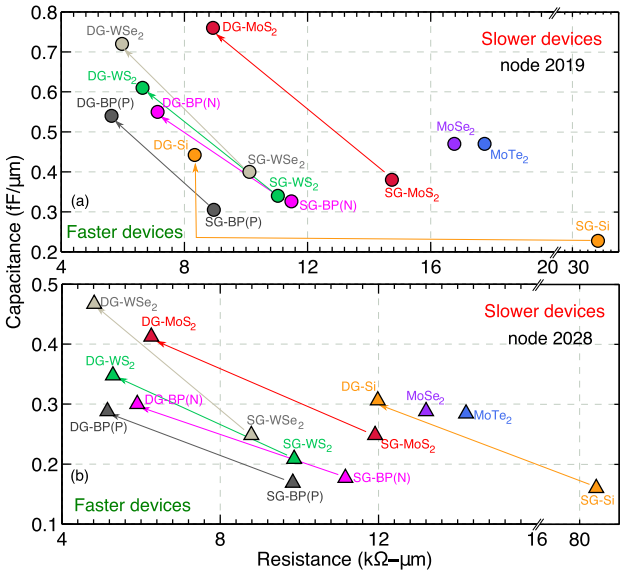

FIGURE 6. Capacitance versus ON resistance for individual FETs. (a) Node 2019. (b) Node 2028. Data points marked with DG represent DG structures. Circles represent the 2019 node and triangles represent the 2028 node. Arrows show the effect of adding a second gate.

among the SG vdW FETs, WSe_2 has the smallest resistance among all the vdW materials, since it has the highest drive current, and BP has the lowest capacitance. To understand the low capacitance, recall that the "device" capacitance is determined by $C = \partial Q/\partial V_G$. Therefore, if the device is only weakly turned ON, there is little charge in the channel, and C is small, irrespective of the actual geometrical gate capacitance. Considering the band diagram of BP at the 2028 node in Fig. 4, it is weakly turned ON, since the top of the barrier is 83 meV above the source Fermi level. In comparison, $MoTe_2$ with the heaviest mass is more strongly turned ON, and its capacitance is the highest even though its current is the lowest among the vdW FETs. Its low current or high resistance result from the low mobility and short mean free paths.

Both the 2028 SG and DG Si FETs stand out in Fig. 6. Applying a DG to 2028 UTB Si gives a capacitance that is slightly below the DG vdW FET using p-type BP. There are several reasons for the low capacitance of the Si DG FET. The 3-nm-thick channel requires a DG to accumulate significant charge in the channel and turn the device ON. Even when charge is accumulated in the channel, the relatively lower effective mass of the lowest quantized state in the channel of 0.22 m_0 results in a lower quantum capacitance [19]. Finally, the lower doping of the source and drain of 10^{19} cm^{-3} compared with the doping of the DG vdW FETs of 4×10^{19} cm^{-3}–5×10^{19} cm^{-3} results in longer depletion regions in the source and drain that reduce the fringing capacitance for the sidewalls of the gates. The UTB Si band diagrams shown in Fig. S3 illustrate these points.

The intrinsic switching energies versus switching delay times are shown in Fig. 7. At node 2019, the SG WS_2 and WSe_2 FETs and DG-Si have very similar switching energies

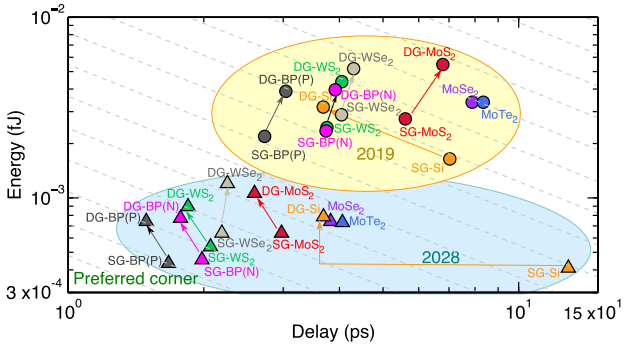

FIGURE 7. Intrinsic switching energy versus delay for individual FETs. Circles and triangles stand for the 2019 and 2028 nodes, respectively. Diagonal dashed lines are constant energy-delay product lines. Each successive line represents an increase of 1.5. An enlarged version of this figure is provided in the Supplementary Information.

and delay times. Adding a second gate to the 2-D materials is detrimental in all cases causing both the energy and delay to increase. At the 2028 node, adding a second gate still moves all of the 2-D materials to a higher energy-delay product. Only Si is moved to a lower energy-delay product by the addition of a second gate.

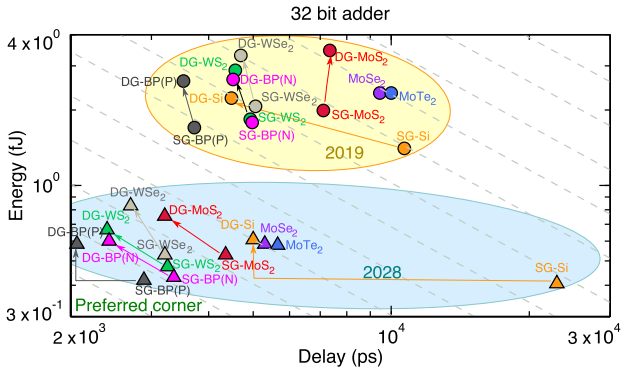

FIGURE 8. Switching energy versus delay for 32-b adder. An enlarged version of this figure is provided in the Supplementary Information.

Energy-delay benchmarks for a 32 bit adder are shown in Fig. 8. Now, the added capacitance of the interconnects is included. For a per unit length capacitance of 126 aF/μm, the interconnect capacitance per transistor (c_i) is 50 aF at the 2019 node and 18 aF at the 2028 node. The default widths used for the FETs are four times the pitches, and they are 80 nm at the 2019 node and 28.4 nm at the 2028 node. Multiplying these widths times the capacitance values in Fig. 6 gives the actual FET capacitances. For the vdW FETs, at the 2019 node, c_i ranges between 1.33 and 2.05 times the SG-FET capacitances and between 0.82 and 1.16 times the DG-FET capacitances. At the 2028 node, c_i ranges between 2.18 and 3.73 times the SG-FET capacitances and between 1.35 and 2.18 times the DG-FET capacitances. The interconnect contribution to the delay depends on the current that flows through the interconnect, and this current is the same

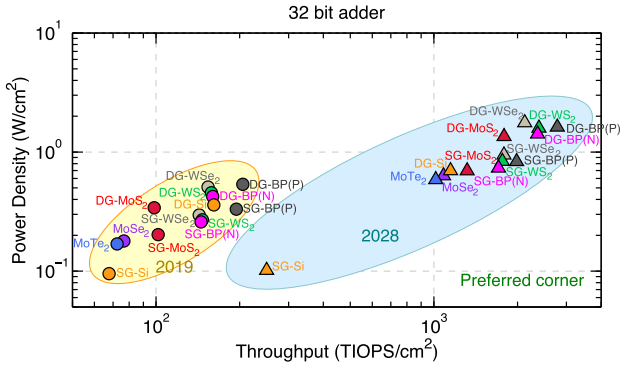

FIGURE 9. Dissipated power versus computational throughput in terainteger operations per sec per cm^2. An enlarged version of this figure is provided in the Supplementary Information.

as the device current. As a result, the drive current becomes more important for the performance of circuits. For an SG-TMD FET at either the 2019 or 2028 node, adding a second gate increases the intrinsic device switching energy more than it decreases the delay, so that the device energy-delay product increases. This same trend applies to the 2019 circuit. However, for the 2028 circuit, adding a second gate leaves the energy-delay product almost unchanged for BP, WS_2 and MoS_2 and slightly increased for WSe_2.

The power density as a function of computational throughput is shown in Fig. 9. Computational throughput is defined as number of integer operations per second per unit area (32 bit additions in the case of 32 bit adder) [34]. The throughput is the inverse of the circuit delay time in Fig. 8 divided by the circuit area. Since the areas for all adders at a given node are taken to be the same, the throughput is proportional to the inverse of the adder delay time. At the 2028 node, SG WSe_2, WS_2, and BP all have significantly higher throughputs than DG-Si with slightly higher power density. Following [34] and [35], we set the power density limit to 10 W/cm^2. All of the FETs lie within the power density constraints, since they all operate at LV (0.3 V).

IV. CONCLUSION

We performed quantum mechanical simulations for vdW FETs with monolayer MoS_2, $MoSe_2$, $MoTe_2$, WS_2, WSe_2, and BP channels operating in the LV regime for geometries corresponding to those of the 2019 node and the 2028 node of the 2013 ITRS. A UTB Si FET was simulated using the same approach to provide a comparison. The FET serves as a baseline device for determining targets for material parameters. As the gate length is scaled from 13.3 to 5.9 nm, blocking the leakage current becomes more critical, and the TMD materials with the heavier effective masses benefit most from extreme scaling. For all materials, the ballistic current always reduces with scaling in agreement with the previous work [36]. However, the full current that includes the effect of scattering can either increase or decrease, and the increase or decrease is governed by two competing processes that are both closely tied to the effective mass, direct tunneling through the channel and backscattering from the channel. There is an optimum effective mass of $\sim$0.4 m_0 corresponding to that of WSe_2 that provides a maximum drive current for LV operation with $V_{DD} = 0.3$ V. The short 6-nm gate length combined with LV operation is forgiving in its requirements for material quality and contact resistances. LV results in low current and thus low IR drop across the contact resistances, and the short 6-nm gate length becomes less than the mean free path of the low-mobility material. At the 2028 node, the SG vdW FETs show competitive performance in terms of drive current and power density. These performance metrics are obtained using currently measured values for mobilities shown in Table S1 and contact resistances shown in Table 2 that are comparable with the best measured contact resistances [48].

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