IEEE Journal on Exploratory Solid-State Computational Devices and Circuits

Received 10 December 2014; revised 5 April 2015 and 5 February 2015; accepted 1 June 2015.
Date of publication 22 June 2015; date of current version 21 September 2015.

Digital Object Identifier 10.1109/JXCDC.2015.2448415

Interconnects for All-Spin Logic Using Automotion of Domain Walls

SOU-CHI CHANG[1], SOURAV DUTTA[1], (Student Member, IEEE), SASIKANTH MANIPATRUNI[2] (Member, IEEE), DMITRI E. NIKONOV[2] (Senior Member, IEEE), IAN A. YOUNG[2] (Fellow, IEEE), AND AZAD NAEEMI[1] (Senior Member, IEEE)

[1]School of Electrical and Computer Engineering, Georgia Institute of Technology, Atlanta, GA 30332 USA
[2]Components Research, Intel Corporation, Hillsboro, OR 97124 USA

CORRESPONDING AUTHOR: S.-C. CHANG (souchi@gatech.edu)

This work was supported by Intel Corporation, Hillsboro, OR, USA, through Intel MSR under Contract 2011-IN-2198.
This paper has supplementary downloadable material available at http://ieeexplore.ieee.org., provided by the author.

ABSTRACT In this paper, an interconnect scheme based on automotion of domain walls (DWs) for all-spin logic (ASL) has been proposed. The proposed interconnect is analyzed using a comprehensive numerical model including an equivalent circuit for ASL operations, the 1-D Landau–Lifshitz–Gilbert equation for DW creation, reflection, and disappearance at the boundaries. Analytical expressions for DW transport along the wire are also presented. From the model, it is found that the reflection of the DW can be eliminated using a material with a high Gilbert damping coefficient at the end, the energy dissipation can be independent of the interconnect length, and DW displacement and energy dissipation can be further improved using a material with a low damping factor and saturation magnetization. Furthermore, the interconnect reliability is also studied by applying the thermal random noise analysis on the dynamics of DWs, and it is found that thermal fluctuations can have a significant impact on the interconnect performance; thus, the interconnect with a low Gilbert damping factor is desired to suppress the thermal noise effects.

INDEX TERMS All-spin logic (ASL), domain walls (DWs), interconnects.

I. INTRODUCTION

RECENTLY, active research has been focused on computational devices using electron spin for the beyond-complementary metal–oxide–semiconductor technology [5]. In particular, a lateral nonlocal spin valve combined with spin-transfer-torque switching, also known as all-spin logic (ASL) [6], has drawn a lot of attention since it provides a complete set of Boolean functions with an extremely low operation voltage due to the full metallic structure. In general, any emerging logic device needs to have a compatible fast and low-power interconnect technology; otherwise, the intrinsic advantage of the device may be shadowed by the wiring network since the delay and energy of interconnects dominate the entire system performance [7].

For ASL, interconnects have been studied using a lateral conventional spin valve with spin-transfer-torque switching using copper, aluminum, and silicon as channel materials [8], [9]. It is shown that the energy of the interconnect is significantly reduced by eliminating the shunt path in ASL. Also, depending on the length of the interconnect, the energy can be minimized by choosing a metallic or semiconducting channel due to different spin relaxation lengths [10], [11] and the electric field effect [12]. However, no matter what structure or material is used, spin tunneling injection is still required to create spin polarization in the nonmagnetic semiconducting channel or maintain the reciprocity of the metallic interconnect. To avoid this charge-to-spin conversion, it is intuitive to use ferromagnetic wires as interconnects, where the spin information can be stored and propagate directly. A magnetic domain wall (DW) is the transition region between magnetic domains in the ferromagnetic material; therefore, it is of interest to explore the possibility of DWs as interconnects for ASL.

Despite the fact that the DW can be moved over a significant distance by an external magnetic field [2], in-plane spin current [13]–[16], or out-of-plane spin current [17], it requires an additional energy to create a magnetic field or electrical current associated with a spin torque on the interconnect. Recently, automotion of DWs has been demonstrated [18], and it is shown that due to intrinsic transverse

anisotropy, which is mainly due to demagnetization inside the wire, the DW can travel a long distance with a high velocity (∼1 km/s) by simply transforming its shape. The concept of spintronic interconnects using automotion of DWs has been proposed in [19], and in general, the DW velocity in a wire is less than that in a plane due to fewer degrees of freedom for DW shape transformations. However, in terms of energy, it has an obvious advantage over the existing proposed interconnects [8], [9], where the charge current flowing through the channel is always required to carry spin information. Therefore, this paper aims at clarifying the potential of DW automotion as interconnects for ASL.

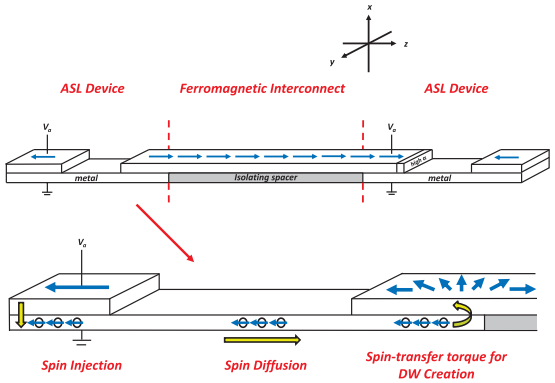

FIGURE 1. Schematics of ASL interconnects using automotion of DWs and creation of DWs using ASL. The Cartesian coordinate used for the calculations of interconnects is also defined.

In this paper, an interconnect for ASL using DW automotion has been proposed and analyzed. The structure is shown in Fig. 1, where the logic stages are connected by a ferromagnetic interconnect which is uniformly magnetized initially. The DW is created and propagates automatically once the previous logic stage finishes the computation. The energy for the interconnect is simply that required for DW creation, which is exactly the same as that used in logic computation in the previous device stage; therefore, this configuration is particularly interesting compared with those based on spin-transfer-torque switching since there is no extra power consumption for data transmission in the interconnect as illustrated in Fig. 2. Note that a leakage current path through the interconnect exists, and the resulting spin-transfer torque may either improve or degrade the DW transport depending on the functionality of ASL. However, this leakage current is typically negligible because of the relatively high resistance of the very thin (∼2 nm) ferromagnetic interconnect compared with nonmagnetic metallic wires in ASL. For simplicity, in this paper, a single inverter or buffer is used for the device stage, which in general can be a more complex function such as a majority gate [20], [21].

The rest of this paper is organized as follows. In Section II, the general formalism including the circuit representation for ASL, the 1-D Landau–Lifshitz–Gilbert (LLG) equation for DW creation, reflection, and disappearance, and analytical

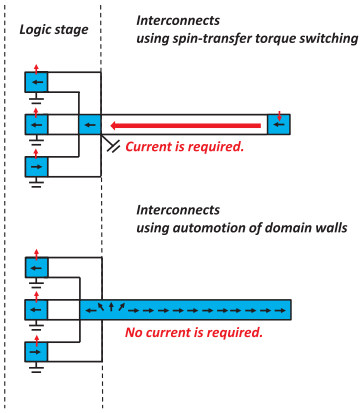

FIGURE 2. Schematics illustrating the difference between interconnects based on spin-transfer-torque switching and automotion of DWs. The ferromagnetic metals are represented by blue rectangles with black arrows. The red arrows represent the direction of electrical current.

equations of motion for DW transport are presented. More details can be found in the supplementary materials. In Section III, using this hybrid numerical model, the interconnects for ASL using DW automotion are analyzed and discussed. Section IV concludes this paper.

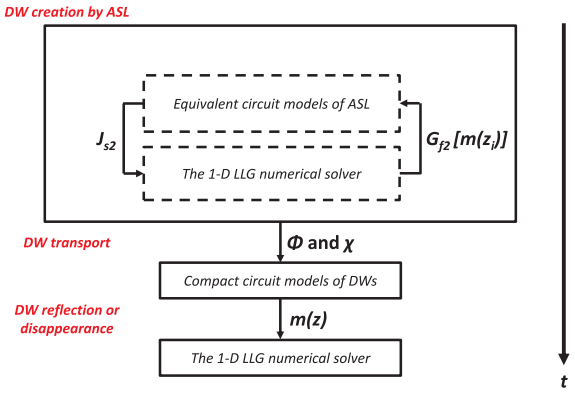

FIGURE 3. Numerical procedure for modeling DW interconnects for ASL.

II. MATHEMATICAL MODELS

To analyze the proposed interconnect scheme shown in Fig. 1, it is necessary to appropriately describe the operation of ASL, DW creation, reflection, and disappearance at the edges, and DW displacement in the channel. Fig. 3 shows the numerical procedure for modeling the DW interconnect for ASL. Since, at each time step, spin currents for creating the DW depend on the ASL/interconnect interface resistance, which is determined by the magnetization of the wire, simultaneously solving the ASL equivalent circuit and the 1-D LLG equation is required to model the creation of the DW. Once the DW is created at the beginning of the interconnect, it can be well described by two important parameters in the Walker's trial form [2] as we will show later,

the displacement (χ) and phase (ϕ) of the DW. The analytical expression for DW transport is used to estimate how far the DW can move automatically in the channel. Finally, as the DW approaches the end of the wire, the magnetization distribution of the interconnect is plugged back into the 1-D LLG equation to see whether the DW is either reflected or destroyed. Note that analytical DW transport equations only work in the absence of random noise fluctuations. Hence, when discussing the thermal noise effects on DW dynamics, the LLG equation is required to be solved throughout the interconnect.

In this section, the mathematical formalism of the ASL, 1-D LLG equation, and DW transport models are presented, and the comparison in DW transport between the analytical expressions and numerical simulations can be found in the supplementary materials.

A. ALL-SPIN LOGIC

The ASL structure is shown in the device part of Fig. 1. In ASL, the spin-polarized electrons, injected by local charge currents, diffuse through the channel and insert a spin torque onto the ferromagnetic interconnect. If the torque is strong enough, the magnetization in the region where spin current is present will be reversed, and the DW is created. To model the operation of ASL, the circuit representations of spin transport in the nonmagnetic channel [1] and ferromagnet/normal metal interface [22] are used, and the equivalent circuit of ASL with the interconnect on which spin currents are applied is shown in Fig. 4. The corresponding circuit conduction matrix $\mathbf{G}$ is obtained by applying the nodal analysis on the circuit (see the supplementary materials) and defined as

$$\{V\} = \mathbf{G}^{-1}\{I\} \tag{1}$$

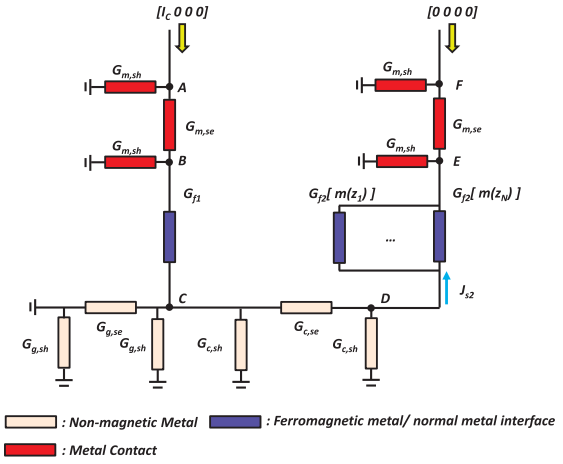

FIGURE 4. Circuit representation of ASL connected by ferromagnetic wires for modeling DW creation. The red, blue, and light yellow bars represent the conductance of the contact, ferromagnetic metal/normal metal interface, and nonmagnetic transport channel, respectively.

where $\{V\}$ and $\{I\}$ are the voltage and current vectors representing charge and spin components at each node, respectively. The current vector has only one nonzero component representing the source of charge currents. Note that parallel interface conduction matrices are used to describe multiple domains in the ferromagnetic interconnect, where the exchange effect is accounted for by the 1-D LLG equation. The magnitude of spin currents at the end of ASL is also affected by the magnetization profile of the wire; therefore, at each time step, once the magnetization of the wire is updated, the corresponding voltage vector at each node can be calculated from (1), and the spin currents responsible for creating the DW are also known using the following:

$$I_{ij} = G(V_i - V_j) \tag{2}$$

where I_{ij} is the 4×1 current vector flowing from the node i to the node j; therefore, the current density used in the 1-D LLG equation for DW creation is given as

$$J_s = \frac{1}{A_{\text{in}}}\left[\sum_{k=1}^{N} I_{ij}(\vec{m}_k)\right] \tag{3}$$

with A_{in} being the cross-sectional area at the ASL/wire interface and k is the index for each domain. Note that J_s changes with time during the DW creation because of the magnetization reversal in the beginning of the channel.

B. 1-D LANDAU-LIFSHITZ-GILBERT EQUATION

The magnetization dynamics of the wire is governed by the LLG equation. Since here the structure we are interested in is a wire, where typically the width and thickness are much smaller than the length, the magnetization in the cross-sectional area is assumed to be uniform; therefore, instead of 3-D micromagnetic simulations [19], the 1-D LLG equation is used to capture the essential physics of DWs in a ferromagnetic interconnect [3].

The 1-D LLG equation under the effects of an external magnetic field and spin-torques from in-plane and out-of-plane spin currents is given as

$$\begin{aligned}\frac{\partial \vec{m}}{\partial t} &= -\gamma\mu_0(\vec{m}\times\vec{H_{eff}}) + \alpha\left(\vec{m}\times\frac{\partial\vec{m}}{\partial t}\right)\\ &\quad -\gamma a_J[\vec{m}\times(\vec{m}\times\vec{p})] - u_J\left(\frac{\partial\vec{m}}{\partial z}\right)\\ &\quad +\beta u_J\left(\vec{m}\times\frac{\partial\vec{m}}{\partial z}\right)\end{aligned} \tag{4}$$

where γ is the gyromagnetic coefficient, α is the Gilbert damping coefficient, μ_0 is the free space permeability, $\vec{m}$ represents the unit vector of the magnetization of each domain, and $\vec{H_{\text{eff}}}$ is the effective magnetic field including the uniaxial anisotropy field $\vec{H}_u$, demagnetization field $\vec{H}_d$, exchange interaction, external magnetic field $\vec{H_{\text{ex}}}$, and thermal random field $\vec{H}_{\text{th}}$, defined as

$$\vec{H}_{\text{eff}} = \vec{H}_u + \vec{H}_d + \frac{2A}{\mu_0 M_s}\frac{\partial^2\vec{m}}{\partial z^2} + \vec{H}_{\text{ex}} + \vec{H}_{\text{th}} \tag{5}$$

where M_s is the saturation magnetization, A is the exchange constant, and $\vec{H}_u$, $\vec{H}_d$, $\vec{H}_{\text{ex}}$, and $\vec{H}_{\text{th}}$ are given as

$$\vec{H}_u = \frac{2K_{u,x}}{\mu_0 M_s} m_x \hat{x} + \frac{2K_{u,y}}{\mu_0 M_s} m_y \hat{y} + \frac{2K_{u,z}}{\mu_0 M_s} m_z \hat{z} \tag{6}$$

$$\vec{H}_d(z_i) = -M_s \left[\sum_j N_{x,ij} m_x(z_j)\hat{x} + \sum_j N_{y,ij} m_y(z_j)\hat{y} + \sum_j N_{z,ij} m_z(z_j)\hat{z} \right] \tag{7}$$

$$\vec{H}_{\text{ex}} = H_{\text{ex},x}\hat{x} + H_{\text{ex},y}\hat{y} + H_{\text{ex},z}\hat{z} \tag{8}$$

$$\vec{H}_{\text{th}}(z_i) = \sqrt{\frac{2\alpha k_B T}{\mu_0^2 \gamma M_s V_D}} \left[\frac{\partial W_x(z_i)}{\partial t}\hat{x} + \frac{\partial W_y(z_i)}{\partial t}\hat{y} + \frac{\partial W_z(z_i)}{\partial t}\hat{z} \right] \tag{9}$$

where k_B is the Boltzmann constant, T is the temperature, V_D is the volume of each domain, and W is the Weiner process. The thermal random fields are assumed to be isotropic, spatially and temporally uncorrelated, and satisfy the following relations [23]:

$$\langle H_{\text{th}}(z_i, t)\rangle = 0 \tag{10}$$

$$\langle H_{\text{th},a}(z_i, t)\, H_{\text{th},b}(z_j, t')\rangle = \frac{2\alpha k_B T}{\mu_0^2 \gamma M_s V_D} \delta_{ab}\delta(z_i - z_j)\,\delta(t - t') \tag{11}$$

with $\langle\cdot\rangle$ denoting the ensemble average, and a, b being indices labeling Cartesian components. Note that the demagnetization field at each time step has spatial dependence and is calculated using the entire magnetization profile along the wire with the demagnetization tensor including magnetostatic interactions between magnetic domains [24], [25]. In (4), a_J is the coefficient for the Slonczewski torque defined as

$$a_J = \frac{\hbar J_{s,\text{out-of-plane}}}{2etM_s} \tag{12}$$

where $J_{s,\text{out-of-plane}}$ is the magnitude of the out-of-plane spin current density, t is the thickness of the wire, and e is the elementary charge. Note that the field-like torque is incorporated into the imaginary part of the mixing conductance in the interface conductance matrix, which is negligible at the normal metal/ferromagnet interface [22]. For the torques due to in-plane spin currents, μ_J and βu_J represent the strengths of the adiabatic and nonadiabatic processes, respectively, where β is typically in the range between 0.01 and 0.1 for different types of the DW [26], and u_J is given as

$$u_J = -\frac{\mu_B J_{s,\text{in-plane}}}{eM_s} \tag{13}$$

where μ_B is the Bohr magneton and $J_{s,\text{in-plane}}$ is the magnitude of in-plane spin current density. In this paper, a perfect ferromagnetic strip with no specific pinning site is assumed. In practice, extrinsic pinning may exist along the interconnect due to local defects or line-edge roughness that may impair the DW automotion. However, these extrinsic factors could be significantly reduced or even completely eliminated as the technology advances; thus, this paper is aimed at the intrinsic properties of an ASL interconnect using DW automotion. The numerical procedure of solving (4) is provided in the supplementary materials.

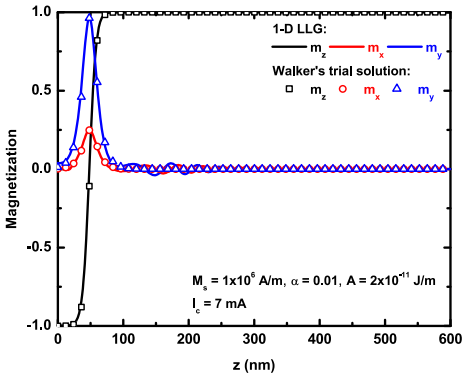

FIGURE 5. Comparison between the DW created by ASL/1-D LLG in a 600-nm interconnect and Walker's trial solutions [2]. Walker's trial parameters: $\phi = 1.32$ rad and $\chi = 50$ nm.

C. DOMAIN WALL TRANSPORT

Fig. 5 shows that Walker's trial form [2] can fit the DW created by ASL quite well in the absence of thermal fluctuations; therefore, instead of solving the 1-D LLG equation for the entire wire, the analytical expressions based on Walker's trial solutions are used to capture the DW transport in the interconnect. The standard approach [2]–[4] is followed to derive the analytical expressions for DW transport, and the detailed derivation can be found in the supplementary materials. Note that the derived expressions here include not only transverse anisotropy (automotion) but also an external magnetic field and in-plane and out-of-plane spin currents to be consistent with (4).

The equations of motion for DW transport in the channel are given as

$$(1+\alpha^2)\frac{\partial \chi}{\partial t} = \frac{-\gamma\Delta(K_x - K_y)\sin 2\phi}{QM_s} + (1+\alpha\beta)\mu_J + \frac{\gamma\Delta p a_J}{Q} + \frac{\gamma\Delta\alpha\mu_0 H_{\text{ex}}}{Q} \tag{14}$$

$$(1+\alpha^2)\frac{\partial \phi}{\partial t} = \frac{\alpha\gamma(K_x - K_y)\sin 2\phi}{M_s} + \frac{(\beta-\alpha)Q}{\Delta}\mu_J - \gamma p\alpha a_J + \gamma\mu_0 H_{\text{ex}} \tag{15}$$

where Q is the topological charge distinguishing the type of the DW ($+1$: head-to-head and -1: tail-to-tail), H_{ex} is the magnitude of an applied magnetic field in the z-direction, p is either 1 or -1, representing z or $-z$ spin polarization, respectively, Δ is the DW thickness, and K_i includes uniaxial and shape anisotropy with the form given as $(1/2)\mu_0 M_s^2 N_i - K_{u,i}$. An important assumption here is that the demagnetization tensor N_i is independent of the space and determined

only by the geometry [27]; therefore, the approximate demagnetization field $\vec{H'}_d$ is simply given as

$$\vec{H'}_d = -M_s(N_x m_x \hat{x} + N_y m_y \hat{y} + N_z m_z \hat{z}). \quad (16)$$

The justification of using (16) in the equations of motion for DW transport is provided in the supplementary materials. In the following section, these analytical equations are used to study DW transport along the interconnect after the DW is created.

III. RESULTS AND DISCUSSION

In this section, the comprehensive numerical model we mentioned above will be used to study ASL interconnects based on the automotion of the DW. First, we focus on how to avoid DW reflection at the end of the interconnect, which is an undesired feature in transmitting information. Next, the delay and energy of DW automotion interconnects in the ASL configuration are quantified. The performance of DW automotion interconnects can be optimized by adjusting the strength of transverse anisotropy and Gilbert damping coefficient. Finally, the effects of thermal noise on interconnect reliability are discussed. Note that all the interconnects simulated in this section are initially in-plane magnetized since a higher wall velocity can be obtained from in-plane DWs [19]. A perpendicularly magnetized wire is interesting as well since ASL using perpendicular magnetization anisotropy (PMA) magnets potentially has higher thermal stability and lower switching current [28]. However, the design aspects discussed in this section for an in-plane wire is general and thus also adaptable to the PMA one. The performance comparison between in-plane and PMA interconnects is beyond the scope of this paper and left as future work.

A. DOMAIN WALLS AT BOUNDARIES

After the DW is created by ASL, it moves toward the end of the interconnect automatically due to transverse anisotropy. For the purposes of the interconnect, the magnetization of the wire has to be completely reversed when the DW reaches the end, which is possible if the DW is destroyed as it is close to the boundary; however, in some cases, instead of being destroyed at the edge, the DW is reflected and the magnetization of the wire is recovered as the DW moves backward. This is an undesired feature for the use of the interconnect since the transmitting signal is coming back; therefore, it is of interest to understand the DW reflection so that a proper structure can be designed to make the DW disappear at the end of the interconnect.

Fig. 6 shows the time evolution of the magnetization at the end of the interconnect for the cases that the DW is reflected and destroyed. For the reflection, the DW with an opposite phase, which is responsible for a negative velocity, is recreated at the end of the channel as the DW reaches the boundary. On the other hand, if there is no enough energy for the DW to reform, through the damping mechanism, the DW will gradually disappear at the end of the channel.

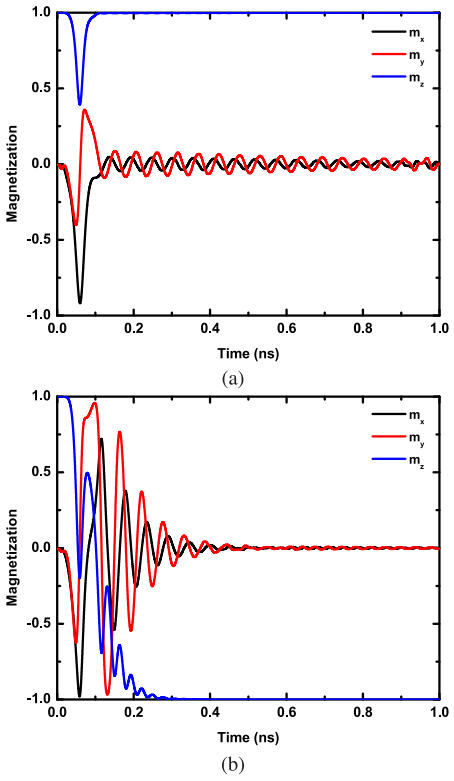

FIGURE 6. Time evolution of the magnetization at the end of the interconnect for (a) DW reflection ($\alpha = 0.01$) and (b) DW disappearance ($\alpha = 0.1$). The DW is located near the boundary initially and moves toward the edge due to automotion.

Fig. 7(a) shows that the DW energy is a key parameter to determine the transient behavior of the DW at the end of the interconnect. In Fig. 7(a), a DW with a given phase is initially located near the boundary and it moves toward the end automatically due to transverse anisotropy. It is found that with a higher damping coefficient, the DW tends to disappear at the end since most of energy is dissipated during the transport. Also, with a constant damping coefficient, the DW in a lower energy configuration [see Fig. 7(b)] prefers to disappear at the end. However, the control of the DW phase reaching the end is difficult since it depends on both injected spin currents from ASL and DW transport in the channel; hence, high damping materials [29] incorporated at the end of the interconnect as shown in Fig. 1 are recommended to prevent DWs from being reflected.

B. DELAY, ENERGY, AND MATERIAL TARGETS

After knowing that the DW will disappear at the end using high damping materials, the delay of the interconnect can be defined as

$$\text{DELAY} = \tau_c + \tau_t \quad (17)$$

where τ_c is the time for ASL creating the DW in the interconnect, and τ_t is the time for the DW traveling to the end of the channel. The energy of the entire structure is given as

$$\text{ENERGY} = I_c V \tau_p \quad (18)$$

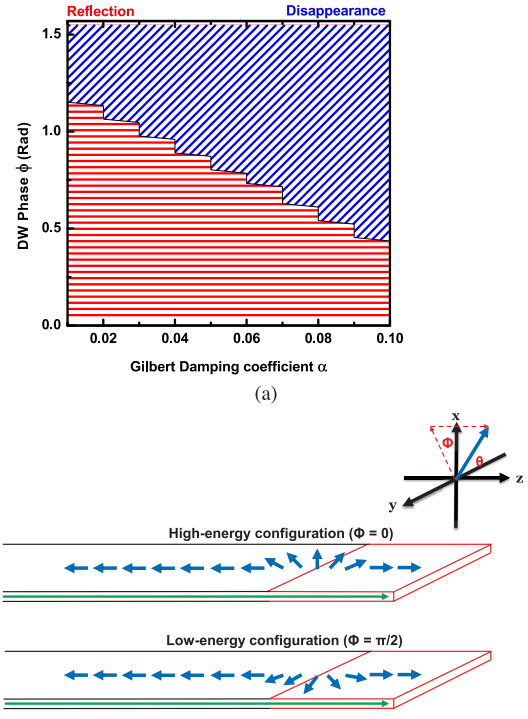

FIGURE 7. (a) Effects of phase and Gilbert damping coefficient at the end of the interconnect on the DW reflection and disappearance. Red lines show that the DW is reflected, and blue lines show that the DW is destroyed at the end. The interconnect length is 400 nm and the DW is located initially at $z = 360$ nm. The Gilbert damping coefficient changes from 0.01 to 0.1 for $z = 360$–400 nm, and is set to be 0.01 for the rest of the wire. Note that if ϕ is exactly $\pi/2$ or 0, the DWs have zero speed. (b) Schematics for illustrating high- and low-energy DW configurations in the in-plane ferromagnetic interconnect. The green arrow represents the direction of uniaxial anisotropy. The red region is where the damping coefficient is changed in Fig. 7(a).

where I_c is the charge current supply on ASL, V is the voltage on the transmitting magnet of ASL, and τ_p is the pulse duration of the current supply. Note that the current source can be turned off once the DW is formed in the interconnect; thus, for the lowest energy operation, τ_p would be equal to τ_c, which will vary due to different current sources; however, for simplicity, here the pulse duration is set to be 1 ns in all the simulations. The simulation parameters are summarized in the supplementary materials.

Fig. 8 shows that the energies needed for different interconnect lengths are the same. This is because the required energy for the interconnect is simply to create the DW, instead of driving the DW. Due to shape anisotropy, the DW is able to move automatically along the interconnect without consuming any energy. Note that the delay does not linearly increase with the interconnect length since due to the damping process, the DW velocity becomes lower as the DW travels through the wire. Therefore, if the interconnect is too long for a DW to reach the end, the delay becomes infinite.

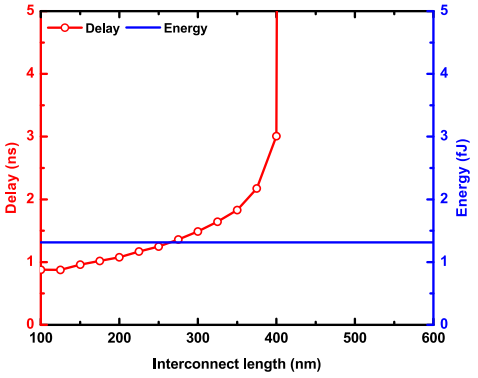

FIGURE 8. Delay and energy versus the interconnect length. The current source for ASL is 0.5 mA. For the ferromagnetic interconnect, the saturation magnetization is 1 x 10^6 A/m and damping coefficient is 0.01. The infinite delay represents no DW reaching the end of the interconnect.

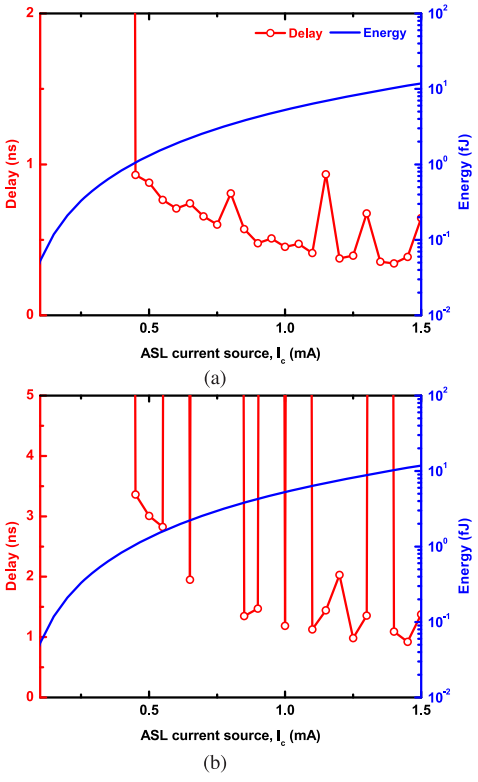

FIGURE 9. Delay and energy versus the magnitude of the ASL current supply for (a) 100-and (b) 400-nm interconnects. The parameters for the interconnects are the same as those shown in Fig. 8.

The current source in ASL plays an important role in determining the interconnect performance. Fig. 9(a) shows that with different magnitudes of the current supply, the delay changes in an oscillating fashion. This can be explained by the fact that the initial phase of the DW depends on the injected spin current in a similar fashion, which is also observed in 3-D micromagnetic simulations [19]. Since the DW velocity has the sinusoidal dependence on the phase, a higher velocity is not necessarily obtained from a stronger current.

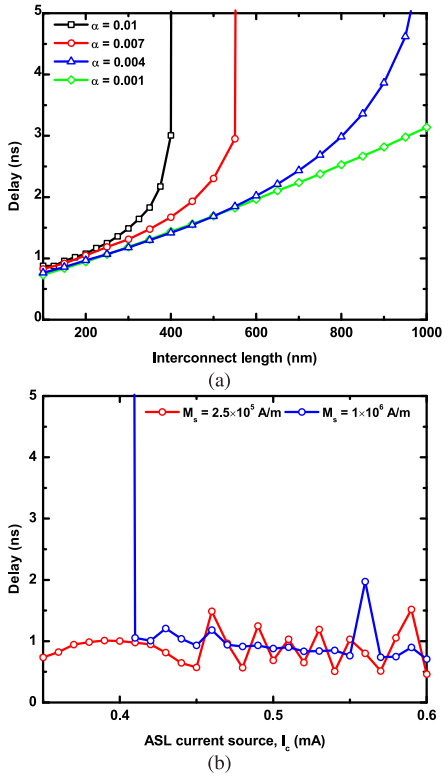

FIGURE 10. Effects of (a) Gilbert damping coefficient (I_C = 0.5 mA) and (b) saturation magnetization on the delay (the interconnect length is 100 nm).

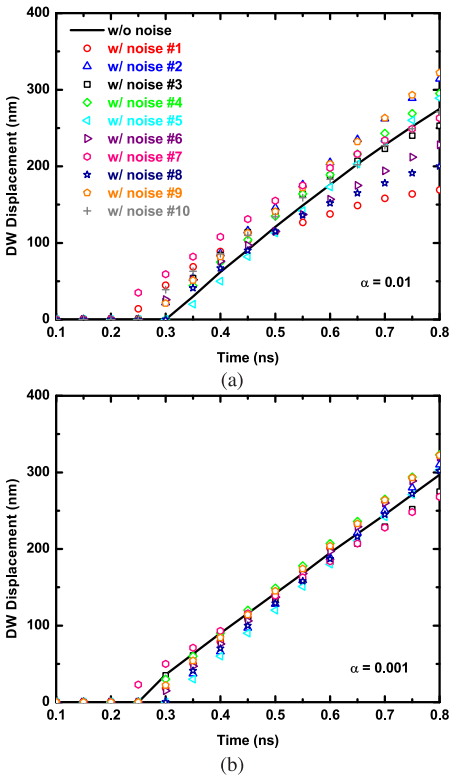

FIGURE 11. Thermal noise effects (T = 300 K) on the DW displacement using automotion with different damping coefficients (a) α = 0.01 and (b) α = 0.001. The interconnect length is 400 nm with saturation magnetization being equal to 1 × 10^6 A/m (I_C = 1 mA).

Therefore, even though the time for DW creation increases as the current magnitude is reduced, there is no guarantee for obtaining a shorter delay using a stronger current. Furthermore, in Fig. 9(a), we can see that when the current is low enough, the delay becomes infinite since within the current pulse, the spin torque from ASL is not strong enough to create the DW that moves properly. Thus, there exists a minimum energy for operating the interconnect. However, in Fig. 9(b), in the case of longer interconnects, the delay also becomes infinite as the current increases. This is because the initial DW phase created by ASL fails to provide enough velocity that drives the DW to the end of the interconnect. In such a case, the DW stops in the middle of the interconnect and the delay becomes infinite. As a result, choosing a proper biasing current working for different interconnect lengths is critically important for interconnects using automotion of DWs.

To mitigate the DW-stopping issue in longer interconnects, as shown in Fig. 10(a), a ferromagnetic material with a lower Gilbert damping coefficient [30], [31] is suggested since in such a case, the DW can preserve its velocity longer and travel over a reasonable distance for the use of interconnects. On the other hand, in Fig. 10(b), the energy of the interconnect can be further reduced by using a material with a lower saturation magnetization since the DW can be created with the lower current. However, the delay does not necessarily increase with saturation magnetization since both DW creation time and initial DW velocity depend on the magnitude of the spin torque. Furthermore, saturation magnetization also affects how DW velocity changes in the channel. Therefore, instead of saturation magnetization, reducing damping mechanisms in the interconnect will be a more efficient way to improve the displacement. Moreover, the energy performance can be further improved by using a metallic channel in ASL with a longer spin relaxation length, e.g., a channel with smaller grain boundary reflectivity and larger surface specularity, since the minimum charge current in ASL required to create a DW can be reduced.

C. THERMAL FLUCTUATIONS

At room temperature, thermal fluctuations on magnetization dynamics inside the interconnect is inevitable; therefore, it is of interest to study how DW automotion is influenced by the thermal noise. Fig. 11(a) shows that the DW automotion is strongly dependent on the thermal noise. This is mainly because the fluctuating DW phase due to the noise changes the velocity as the DW travels through the interconnect; thus, the trajectory of the DW displacement in time can largely deviate from that without the noise. This large deviation can significantly impair the reliability of the interconnect since the DW can reach the end of the wire with quite different delays. The similar constraint can also be observed in

interconnects based on spin-transfer-torque switching [8], [9], where the delay distribution becomes wider as the interconnect length increases or the applied voltage is reduced. As a result, to reduce the noise effect on DW automotion, an interconnect with low Gilbert damping is recommended since the magnitude of the thermal field can be reduced, and the deviation from the noiseless situation is largely suppressed using a low damping channel as shown in Fig. 11(b).

IV. CONCLUSION

In this paper, interconnects for ASL using automotion of DWs are proposed to make ASL circuits more energy-efficient, and are analyzed using a hybrid physical solver including ASL equivalent circuits, 1-D LLG equation, and equations of motion for DW transport. Through the model, the reflection of the DW is eliminated by adding a layer with a high damping coefficient at the end of the ferromagnetic interconnect. The energy and delay are also studied. It is found that the delay of the interconnect using DW automotion can be independent of the length; furthermore, the interconnect performance can be improved by reducing both saturation magnetization and damping coefficient along the channel, and the reliability can also be enhanced by a low damping channel.

REFERENCES

[1] S. Manipatruni, D. E. Nikonov, and I. A. Young, "Modeling and design of spintronic integrated circuits," *IEEE Trans. Circuits Syst. I, Reg. Papers*, vol. 59, no. 12, pp. 2801–2814, Dec. 2012.

[2] N. L. Schryer and L. R. Walker, "The motion of 180° domain walls in uniform dc magnetic fields," *J. Appl. Phys.*, vol. 45, no. 12, pp. 5406–5421, 1974.

[3] A. Thiaville, J. M. Garcia, and J. Miltat, "Domain wall dynamics in nanowires," *J. Magn. Magn. Mater.*, vols. 242–245, pp. 1061–1063, Apr. 2002.

[4] A. P. Malozemoff and J. C. Slonczewski, *Magnetic Domain Walls in Bubble Materials*. New York, NY, USA: Academic Press, 1979.

[5] D. E. Nikonov and I. A. Young, "Overview of beyond-CMOS devices and a uniform methodology for their benchmarking," *Proc. IEEE*, vol. 101, no. 12, pp. 2498–2533, Dec. 2013.

[6] B. Behin-Aein, D. Datta, S. Salahuddin, and S. Datta, "Proposal for an all-spin logic device with built-in memory," *Nature Nanotechnol.*, vol. 5, pp. 266–270, Feb. 2010.

[7] N. Magen, A. Kolodny, U. Weiser, and N. Shamir, "Interconnect-power dissipation in a microprocessor," in *Proc. Int. Workshop Syst. Level Interconnect Predict. (SLIP)*, 2004, pp. 7–13.

[8] S.-C. Chang, S. Manipatruni, D. E. Nikonov, I. A. Young, and A. Naeemi, "Design and analysis of Si interconnects for all-spin logic," *IEEE Trans. Magn.*, vol. 50, no. 9, Sep. 2014, Art. ID 3400513.

[9] S.-C. Chang, R. M. Iraei, S. Manipatruni, D. E. Nikonov, I. A. Young, and A. Naeemi, "Design and analysis of copper and aluminum interconnects for all-spin logic," *IEEE Trans. Electron Devices*, vol. 61, no. 8, pp. 2905–2911, Aug. 2014.

[10] S. Rakheja, S.-C. Chang, and A. Naeemi, "Impact of dimensional scaling and size effects on spin transport in copper and aluminum interconnects," *IEEE Trans. Electron Devices*, vol. 60, no. 11, pp. 3913–3919, Nov. 2013.

[11] S. Rakheja and A. Naeemi, "Roles of doping, temperature, and electric field on spin transport through semiconducting channels in spin valves," *IEEE Trans. Nanotechnol.*, vol. 12, no. 5, pp. 796–805, Sep. 2013.

[12] Z. G. Yu and M. E. Flatté, "Electric-field dependent spin diffusion and spin injection into semiconductors," *Phys. Rev. B*, vol. 66, p. 201202, Nov. 2002.

[13] L. Berger, "Exchange interaction between ferromagnetic domain wall and electric current in very thin metallic films," *J. Appl. Phys.*, vol. 55, no. 6, pp. 1954–1956, 1984.

[14] Z. Li and S. Zhang, "Domain-wall dynamics and spin-wave excitations with spin-transfer torques," *Phys. Rev. Lett.*, vol. 92, p. 207203, May 2004.

[15] S. Zhang and Z. Li, "Roles of nonequilibrium conduction electrons on the magnetization dynamics of ferromagnets," *Phys. Rev. Lett.*, vol. 93, p. 127204, Sep. 2004.

[16] A. Yamaguchi, T. Ono, S. Nasu, K. Miyake, K. Mibu, and T. Shinjo, "Real-space observation of current-driven domain wall motion in submicron magnetic wires," *Phys. Rev. Lett.*, vol. 92, p. 077205, Feb. 2004.

[17] A. V. Khvalkovskiy *et al.*, "High domain wall velocities due to spin currents perpendicular to the plane," *Phys. Rev. Lett.*, vol. 102, p. 067206, Feb. 2009.

[18] J.-Y. Chauleau, R. Weil, A. Thiaville, and J. Miltat, "Magnetic domain walls displacement: Automotion versus spin-transfer torque," *Phys. Rev. B*, vol. 82, p. 214414, Dec. 2010.

[19] D. E. Nikonov, S. Manipatruni, and I. A. Young, "Automotion of domain walls for spintronic interconnects," *J. Appl. Phys.*, vol. 115, no. 21, p. 213902, 2014.

[20] D. E. Nikonov, G. I. Bourianoff, and T. Ghani, "Proposal of a spin torque majority gate logic," *IEEE Electron Device Lett.*, vol. 32, no. 8, pp. 1128–1130, Aug. 2011.

[21] V. Calayir, D. E. Nikonov, S. Manipatruni, and I. A. Young, "Static and clocked spintronic circuit design and simulation with performance analysis relative to CMOS," *IEEE Trans. Circuits Syst. I, Reg. Papers*, vol. 61, no. 2, pp. 393–406, Feb. 2014.

[22] A. Brataas, G. E. W. Bauer, and P. J. Kelly, "Non-collinear magnetoelectronics," *Phys. Rep.*, vol. 427, no. 4, pp. 157–255, 2006.

[23] C. Ragusa *et al.*, "Full micromagnetic numerical simulations of thermal fluctuations," *IEEE Trans. Magn.*, vol. 45, no. 10, pp. 3919–3922, Oct. 2009.

[24] A. J. Newell, W. Williams, and D. J. Dunlop, "A generalization of the demagnetizing tensor for nonuniform magnetization," *J. Geophys. Res., Solid Earth*, vol. 98, no. B6, pp. 9551–9555, 1993.

[25] J. E. Miltat and M. J. Donahue, *Numerical Micromagnetics: Finite Difference Methods*. New York, NY, USA: Wiley, 2007.

[26] M. Eltschka *et al.*, "Nonadiabatic spin torque investigated using thermally activated magnetic domain wall dynamics," *Phys. Rev. Lett.*, vol. 105, p. 056601, Jul. 2010.

[27] M. Beleggia, M. De Graef, and Y. T. Millev, "The equivalent ellipsoid of a magnetized body," *J. Phys. D, Appl. Phys.*, vol. 39, no. 5, pp. 891–899, 2006.

[28] D. C. Worledge *et al.*, "Spin torque switching of perpendicular Ta|CoFeB|MgO-based magnetic tunnel junctions," *Appl. Phys. Lett.*, vol. 98, no. 2, p. 022501, 2011.

[29] C. Luo *et al.*, "Enhancement of magnetization damping coefficient of permalloy thin films with dilute Nd dopants," *Phys. Rev. B*, vol. 89, p. 184412, May 2014.

[30] T. Graf, S. S. P. Parkin, and C. Felser, "Heusler compounds—A material class with exceptional properties," *IEEE Trans. Magn.*, vol. 47, no. 2, pp. 367–373, Feb. 2011.

[31] V. Alijani, J. Winterlik, G. H. Fecher, and C. Felser, "Tuning the magnetism of the Heusler alloys Mn_{3-x} Co_x Ga from soft and half-metallic to hard-magnetic for spin-transfer torque applications," *Appl. Phys. Lett.*, vol. 99, no. 22, p. 222510, 2011.

SOU-CHI CHANG received the B.S. degree in electrical engineering from National Chiao Tung University, Hsinchu, Taiwan, in 2008, and the M.S. degree in electrical engineering and computer science from the University of Michigan, Ann Arbor, MI, USA, in 2011. He is currently pursuing the Ph.D. degree in electrical and computer engineering with the Georgia Institute of Technology, Atlanta, GA, USA.

SOURAV DUTTA (S'13) received the B.E. degree in electrical engineering from Jadavpur University, Kolkata, India, in 2012. He is currently pursuing the Ph.D. degree in electrical and computer engineering with the Georgia Institute of Technology, Atlanta, GA, USA, with a focus on modeling and simulation of post-CMOS spintronic devices and interconnects.

SASIKANTH MANIPATRUNI (M'07) received the (Hons.) degree in electrical engineering from IIT Delhi, Delhi, India. He received the Ph.D. degree in silicon photonics and opto-mechanics from Cornell University, Ithaca, NY, USA, under the supervision of Prof. M. Lipson.

During his PhD, he was a co-inventor of several silicon photonic devices, including the first 18 Gb/s microring modulator, first GHz poly-silicon modulator, hitless broadband EO switches, and integrated silicon nanophotonic link. He was a KVPY National Science Fellow with the Indian Institute of Sciences, Bengaluru, India, from 1999 to 2001. He was with the Swiss Federal Institute of Technology, Zurich, Switzerland, in 2004, and the Inter University Center for Astronomy and Astrophysics in 2001. His business plan for fab-less photonics received the first place in Asia-Pacific at Asia Moot Corporation in 2008, and was selected as an outstanding product at World Moot Corporation in 2009. He was with the General Electric Global Research Center, Munich, Germany, where he was involved in nanophotonic interconnects for massively parallel magnetic resonance imaging (MRI) and demonstrated the first analog-RF optical MRI system at 3T magnetic fields. He joined Intel Corporation, Santa Clara, CA, USA, in 2011. He is currently a Research Scientist with the Exploratory Integrated Devices and Circuits Group, Intel Components Research, Technology and Manufacturing Group, Intel Corporation. He is involved in emerging novel devices to identify technology options for beyond CMOS logic technologies. He holds 50 patent applications in nanophotonics and MRI, and 40 peer-reviewed journal and conference papers.

Dr. Manipatruni serves as a Peer-Reviewer for the Optical Society, the IEEE, and Nature Photonics.

DMITRI E. NIKONOV (M'99–SM'06) received the M.S. degree in aeromechanical engineering from the Moscow Institute of Physics and Technology, Moscow, Russia, in 1992, and the Ph.D. degree in physics from Texas A&M University, College Station, TX, USA, in 1996.

He joined Intel, Santa Clara, CA, USA, in 1998. He is currently a Principal Engineer with the Components Research Group, Hillsboro, OR, USA, doing simulation and benchmarking of beyond-CMOS logic devices and managing research programs with universities on nanotechnology. He has authored 79 publications, and holds 48 issued patents.

IAN A. YOUNG (M'78–SM'96–F'99) was born in Melbourne, VIC, Australia. He received the bachelor's and master's degrees in electrical engineering from the University of Melbourne, Melbourne, and the Ph.D. degree in electrical engineering from the University of California at Berkeley, Berkeley, CA, USA, in 1978.

He was involved in the pioneering research on MOSFET switched-capacitor filters with the University of California at Berkeley. He was involved in analog/digital integrated circuits for telecommunications products with Mostek Corporation, Carrollton, TX, USA. He joined Intel, Santa Clara, CA, USA, in 1983. Starting with the development of circuits for the world's first 1 Mb CMOS DRAM, and first 1 μm 64 K SRAM, he led the design of three generations of SRAM products and manufacturing test vehicles, and developed the original phase locked loop (PLL)-based clocking circuit in a microprocessor, while involves in the 50 MHz Intel 486 processor design. He subsequently developed the core PLL clocking circuit building blocks used in each generation of Intel microprocessors through the 0.13 μm 3.2 GHz Pentium 4. From 2001 to 2010, he led a circuit design team doing research and development of analog mixed-signal high-speed serial I/O circuits for microprocessors and wireless RF CMOS synthesizers and transceiver circuits, in conjunction with the development of Intel's 90 to 22 nm process technology. He has also led research to enable optical I/O for microprocessors. He is currently a Senior Fellow with the Technology and Manufacturing Group, Intel Corporation, Hillsboro, OR, USA. He holds 57 issued patents in integrated circuits and has authored or co-authored over 50 technical papers.

Dr. Young has received three Intel Achievement Awards. He served as the Technical Program Committee Chairman of the 2005 International Solid-State Circuits Conference and the Chairman of the 1998 Symposium on VLSI Circuits. He is thrice a Guest Editor of the IEEE Journal of Solid-State Circuits. He received the 2009 International Solid-State Circuits Conference's Jack Raper Award for outstanding technology directions paper.

AZAD NAEEMI (S'99–M'04–SM'04) received the B.S. degree in electrical engineering from Sharif University, Tehran, Iran, in 1994, and the M.S. and Ph.D. degrees in electrical and computer engineering from the Georgia Institute of Technology (Georgia Tech), Atlanta, GA, USA, in 2001 and 2003, respectively.

He was a Research Engineer with the Microelectronics Research Center, Georgia Tech, from 2003 to 2008, and joined the School of Electrical and Computer Engineering Faculty, Georgia Tech, where he is currently an Associate Professor. His current research interests include the boundaries of materials, devices, circuits and systems, investigating integrated circuits based on conventional and emerging nanoelectronic and spintronic devices and interconnects.

Dr. Naeemi was a recipient of the IEEE Electron Devices Society Paul Rappaport Award for the best paper that has appeared in the IEEE TRANSACTIONS ON ELECTRON DEVICES in 2007. He has also received an NSF CAREER Award, an SRC Inventor Recognition Award, and four best paper awards at international conferences. He is a recipient of the ECE Outstanding Junior Faculty Member Award and the Richard M. Bass/Eta Kappa Nu Outstanding Teacher Awar (Determined by the vote of the ECE senior class).