

Tunnel Field-Effect Transistors in 2-D Transition Metal Dichalcogenide Materials

HESAMEDDIN ILATIKHAMENEH¹, YAOHUA TAN¹, BOZIDAR NOVAKOVIC¹,
GERHARD KLIMECK¹, RAJIB RAHMAN¹, AND JOERG APPENZELLER²

¹Department of Electrical and Computer Engineering, Network for Computational Nanotechnology, Purdue University, West Lafayette, IN 47907 USA

²Birk Nanotechnology Center, Department of Electrical and Computer Engineering, Purdue University, West Lafayette, IN 47907 USA
CORRESPONDING AUTHOR: H. ILATIKHAMENEH (hesam.ilati2@gmail.com)

This work was supported in part by the Center for Low Energy Systems Technology (LEAST), one of six centers of STARnet, a Semiconductor Research Corporation program sponsored by MARCO and DARPA. The use of nanoHUB.org computational resources operated by the Network for Computational Nanotechnology funded by the US National Science Foundation under grant EEC-1227110, EEC-0228390, EEC-0634750, OCI-0438246, and OCI-0721680 is gratefully acknowledged.

ABSTRACT In this paper, the performance of tunnel field-effect transistors (TFETs) based on 2-D transition metal dichalcogenide (TMD) materials is investigated by atomistic quantum transport simulations. One of the major challenges of TFETs is their low ON-currents. 2-D material-based TFETs can have tight gate control and high electric fields at the tunnel junction, and can, in principle, generate high ON-currents along with a subthreshold swing (SS) smaller than 60 mV/decade. Our simulations reveal that high-performance TMD TFETs not only require good gate control, but also rely on the choice of the right channel material with optimum bandgap, effective mass, and source/drain doping level. Unlike previous works, a full-band atomistic tight-binding method is used self-consistently with 3-D Poisson equation to simulate ballistic quantum transport in these devices. The effect of the choice of the TMD material on the performance of the device and its transfer characteristics are discussed. Moreover, the criteria for high ON-currents are explained with a simple analytic model, showing the related fundamental factors. Finally, the SS and energy delay of these TFETs are compared with conventional CMOS devices.

INDEX TERMS MoS₂, MoTe₂, Nonequilibrium Green's Function (NEGF), Scaling theory, Transition Metal Dichalcogenide (TMD), Tunnel Field-Effect Transistor (TFET), WSe₂, WTe₂.

I. INTRODUCTION

POWER consumption is one of the main challenges for future electronics. In this regard, tunnel field-effect transistors (TFETs) are among the most promising candidates for future integrated circuits (ICs) due to their small subthreshold swing (SS) and low OFF-current [1], [2]. Having small SS and OFF-current reduces both the static power consumption and the dynamic power consumption of the ICs [3].

One of the major drawbacks of the TFETs is their low ON-current. The current in the TFETs is the result of band-to-band tunneling (BTBT) of the carriers. The tunneling probability is usually much smaller than 1, and as a result, the ON-currents of the TFETs are much smaller than those of the conventional FETs. However, the tunneling probability

can increase significantly if the electric field at the tunneling region is high enough. Atomically thin 2-D devices are very interesting in this context for TFET applications, analogous to nanotubes [1], [2], due to the tight gate control over the channel that results in high electric fields at the tunnel junction. Since the BTBT transmission probability depends on the electric field exponentially, high ON-currents are expected in 2-D TFETs. However, tight gate control is not the only player in determining the ON-currents and there are other critical factors, such as bandgap, effective mass (m^*), and doping concentration.

The well-known scaling length theory [6] can be used to quantify the effect of gate control on the electric field at the tunnel junction [7]. This theory provides a simple ana-

lytic way to understand how various device parameters affect the spatial variation of the potential along the channel [6] described by a modified 1-D Poisson equation

$$\frac{d^2V}{dx^2} - \frac{V}{\lambda^2} = 0 \quad (1)$$

where V and λ are the electrostatic potential and the natural scaling/decay length of the potential, respectively. In double-gated FETs, λ is given by [8]

$$\lambda = \sqrt{\frac{\epsilon_{\text{ch}}}{2\epsilon_{\text{ox}}} \left(1 + \frac{\epsilon_{\text{ox}} t_{\text{ch}}}{4\epsilon_{\text{ch}} t_{\text{ox}}} \right) t_{\text{ch}} t_{\text{ox}}} \quad (2)$$

where ϵ_{ch} and ϵ_{ox} are the dielectric constants of the channel and oxide, respectively, while t_{ch} and t_{ox} are their thicknesses. According to (2), reducing the channel thickness reduces the natural scaling length of the potential, which results in higher electric fields and ON-currents.

Besides advantageous 2-D electrostatics, there are other incentives for using 2-D materials for future electronics [9]. For example, thinning the 3-D material-based FETs (which is required in transistor scaling) increases the effect of surface roughness on carrier transport, which leads to lower mobility [10]. However, 2-D materials have relatively weak interlayer bonds and can be exfoliated easily without surface roughness [11], [12], [16], [17]. Moreover, there are no dangling bonds in 2-D transition metal dichalcogenides (TMDs) unlike thinned 3-D materials [13]–[15]. Another advantage of the 2-D materials is that thinning the material does not increase the bandgap of the material as much as it does in the 3-D materials [16]. This is again due to the weaker coupling between the stacked layers in the 2-D materials. For example, thinning InAs nanowires to achieve better gate control can increase the bandgap more than 100% [18], while the increase in bandgap from bulk to monolayer is much smaller in the 2-D materials [16]. This is useful in the TFETs as a larger bandgap results in a lower ON-current. Moreover, monolayer 2-D materials usually have small dielectric constants [19], which can also increase the ON-current and reduce the drain-induced barrier lowering (DIBL) in TFETs.

Previously, TMD TFETs have been simulated without solving the Poisson and the transport equations self-consistently [4], [5]. In these works, the electric field at the source-channel junction has been approximated assuming that the 1-D Poisson equation (1) is accurate throughout the entire source-to-channel junction. Although λ is a critical factor in determining the electric field, it is not the only factor. Other factors, such as the depletion width in the source region, are important too. The non-self-consistent results predict very large ON-currents for all TMD TFETs irrespective of the channel material. In this paper, the correctness of these assumptions for the TMD TFETs has been investigated by solving the 3-D Poisson equation self-consistently with full-band quantum transport, and the factors limiting the ON-currents are elucidated.

The band structure and electronic properties, such as bandgap, m^* , and dielectric constant of TMD materials, depend on the number of layers. Consequently, devices with different number of layers show different characteristics. Although increasing the thickness reduces the bandgap, it increases λ and decreases the electric field at the source-to-channel junction. Moreover, multilayer TMDs usually exhibit indirect bandgaps, which imply that phonons need to be involved in the BTBT process. As a result, it is favorable to use the monolayer TMDs and instead explore different materials to obtain small values of λ , direct bandgap, and m^* simultaneously. Since TMDs form a general class of materials of the form MX_2 , where M is a transition metal (Mo, W, and so on) and X is a chalcogenide (Te, Se, and S), a variety of material parameters can be accessed by the correct choice of material. The field of the 2-D materials is still at its infancy as novel materials are being discovered [22], [23], which opens up opportunities for TFET designs. Accordingly, in this paper, only monolayers of a set of more common TMDs, whose critical parameters span the design space of TFETs, are studied.

II. SIMULATION METHOD

The TMD Hamiltonian is represented by an sp^3d^5 second nearest neighbor tight-binding (TB) model with spin-orbit interaction. The Slater–Koster TB [24] parameters are optimized based on the first principle band structures obtained from density functional theory (DFT) with the generalized gradient approximation (GGA). DFT-GGA has been shown to provide bandgaps and effective masses in TMDs comparable with the experimental measurements [25]. The motivation for using a DFT-guided TB model is that a realistically extended device size can be simulated at ease compared with computationally expensive and size limited *ab initio* methods [26]. Bandgaps and effective masses of monolayer MoS_2 , WSe_2 , MoTe_2 , and WTe_2 obtained from our TB model are listed in Table 1. The TB parameters are general and capture the band structure of both the bulk and monolayer TMDs. As an example, the TB band structure of monolayer WTe_2 is shown in Fig. 1.

TABLE 1. Bandgap (Eg), electron and hole effective masses (m_e^* and m_h^*), and in-plane and out-of-plane relative dielectric constants (ϵ_r^{in} and ϵ_r^{out}) of TMD materials. All the parameters are obtained from TB band structure of TMD monolayers with the exception of the dielectric constants, which are taken from *ab initio* studies [19], [20].

Parameters	MoS_2	WSe_2	MoTe_2	WTe_2
Eg [eV]	1.68	1.56	1.085	0.75
m_e^* [m_0]	0.52	0.36	0.57	0.37
m_h^* [m_0]	0.64	0.5	0.75	0.3
ϵ_r^{in}	4.2	4.5	8	5.7
ϵ_r^{out}	2.8	2.9	4.4	3.3

In this paper, a self-consistent Poisson-quantum transmitting boundary method (QTBM) [27] methodology has been used within the TB description. The QTBM method

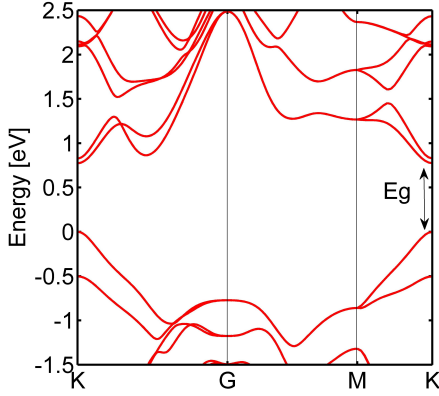


FIGURE 1. Band structure of a monolayer WTe_2 .

is equivalent to the well-known nonequilibrium Green's function approach without scattering, but is a more computationally efficient implementation [28]. In this method, the Schrödinger equation with open boundaries is solved using the following equation:

$$(EI - H - \Sigma)\psi_{S/D} = S_{S/D} \quad (3)$$

where E , I , H , and Σ are energy, identity matrix, device Hamiltonian, and total self-energy due to open boundaries and ψ and S are the wave function and a carrier injection term from either source (subscript S) or drain (subscript D) [28]. The electron and hole carrier density and current can be obtained from the wave function ψ [28]. Since the in-plane and out-of-plane dielectric constants (ϵ^{in} and ϵ^{out}) of the TMD materials are different, the Poisson equation reads as follows if considering the z -direction to be along the out-of-plane direction (or c -axis) of the TMDs:

$$\frac{d}{dx} \left(\epsilon^{\text{in}} \frac{dV}{dx} \right) + \frac{d}{dy} \left(\epsilon^{\text{in}} \frac{dV}{dy} \right) + \frac{d}{dz} \left(\epsilon^{\text{out}} \frac{dV}{dz} \right) = -\rho \quad (4)$$

where V and ρ are the electrostatic potential and total charge, respectively. The dielectric constant values (ϵ^{in} and ϵ^{out}) for the TMD materials are taken from *ab initio* studies [19], [20] and are listed in Table 1. In this paper, transport simulations have been performed with the nanodevice simulation tool NEMO5 [29], [30].

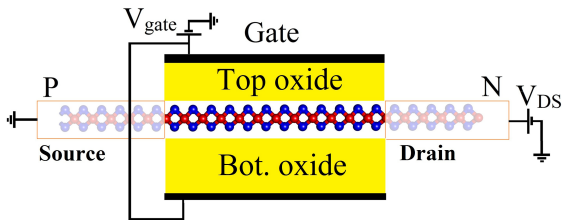


FIGURE 2. Physical structure of a monolayer TMD TFET with channel and source/drain lengths of 15 and 10 nm, respectively. Source and drain regions have a doping level of $1e20 \text{ cm}^{-3}$ and EOT is fixed to 0.43 nm.

III. RESULTS AND DISCUSSION

All the simulated TMD TFET devices assume a structure, as shown in Fig. 2, and have channel and source/drain lengths of 15 and 10 nm, respectively. A doping level of $1e20 \text{ cm}^{-3}$ is assumed in the source and drain regions, which seems feasible by molecular doping of the source and drain contact regions [31]. A source–drain voltage V_{DS} of 0.5 V is used unless mentioned otherwise. Equivalent oxide thickness (EOT) of top and bottom oxides is set to 0.43 nm to be consistent with International Technology Roadmap for Semiconductors (ITRS) projections for 2027 [32].

A. TRANSFER CHARACTERISTICS OF TMD TFETs

Fig. 3 shows the transfer characteristics of the TMD TFETs with OFF-current fixed to $1 \text{ nA}/\mu\text{m}$ at 0 gate voltage. It is worthwhile to notice that in TFETs, lower OFF-currents can be readily achieved without losing too much ON-current. This is because the slope of the $I_{\text{DS}}-V_{\text{Gate}}$ curve is very steep in the low current regime. As a result, a much lower OFF-current can be obtained with a very small reduction of V_{Gate} . For example, an OFF-current of $0.1 \text{ nA}/\mu\text{m}$ (ten times smaller than before) can be obtained with the ON-current just being approximately 5%–10% smaller.

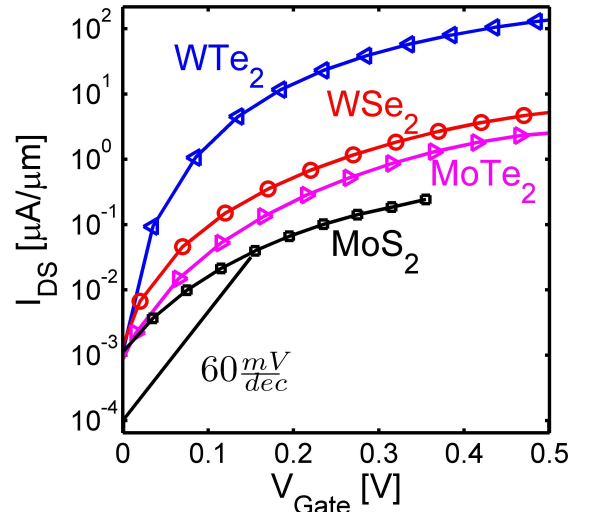


FIGURE 3. Transfer characteristics of TMD TFETs with $I_{\text{OFF}} = 1 \text{ nA}/\mu\text{m}$.

The simulation results show that WTe_2 TFETs can provide the highest performance in terms of ON-current and SS in comparison with the other TFETs. Since WTe_2 has the smallest bandgap and effective mass compared with the other TMDs, its ON-current is significantly higher. Notice that despite the fact that MoTe_2 has a smaller bandgap than WSe_2 , it shows a smaller current. The values of ON-current (the current at $V_{\text{GS}} = V_{\text{DS}} = V_{\text{DD}} = 0.5 \text{ V}$), bandgap, and reduced effective masses ($1/m_r^* = 1/m_e^* + 1/m_h^*$) of these TMDs are listed in Table 2. Although MoS_2 has a high effective mass for tunneling applications, it is ideal for ultrascaled MOSFET applications where a high effective mass can suppress the

source-to-drain tunneling [33], [34]. To understand the origin of the difference between ON-currents of these devices, one needs to consider several factors: 1) electron and hole effective masses; 2) bandgap; 3) body thickness; 4) EOT of oxide; 5) source-to-channel potential difference; and 6) source and drain doping level. These factors are considered in the analytic equation for the current in the ON-state of a TFET [35]

$$I \propto \exp\left(\frac{-4\sqrt{2m_r^*}E_g^{3/2}}{3q\hbar E}\right) \quad (5)$$

where q , \hbar , and m_r^* are the charge of an electron, the reduced Plank constant, and the reduced effective mass, respectively. E is the electric field at the source-channel junction and can be approximated by $(\phi_S - \phi_{ch})/\Lambda$, where Λ is the effective natural scaling length of the potential at the source-channel junction and $q(\phi_S - \phi_{ch})$ is the source-channel potential difference. At threshold voltage, $q(\phi_S - \phi_{ch})$ equals E_g . For small overdrive voltages ($V_{GS} - V_{Th}$), the current can be simplified using $q(\phi_S - \phi_{ch}) \approx E_g$ to

$$I \propto \exp\left(\frac{-4\Lambda\sqrt{2m_r^*}E_g}{3\hbar}\right). \quad (6)$$

Equation (6) shows that the fundamental factor in determining the current in TFETs is

$$\eta = \frac{\Lambda\sqrt{m_r^*}E_g}{\hbar}. \quad (7)$$

The factor η depends on the device design (EOT, body thickness, and doping) through Λ and band structure of channel through m_r^* and E_g . Note that for small overdrive voltages, the bandgap and the effective mass have an equal impact on the current. For example, despite the fact that MoTe₂ has a smaller bandgap compared with WSe₂, it has a larger reduced effective mass, which can partly compensate for the reduction in the bandgap.

The parameter Λ is composed of two components: 1) the depletion width in the source region (W_D) and 2) the natural scaling length (λ) in the gated region. The difference between this analysis and [4], [5], and [36] is that the effective natural scaling length Λ is calculated from a self-consistent potential profile, which includes the effect of both W_D and λ accurately. Ideally, the dielectric constant of the channel should be small to make Λ as small as possible. W_D and λ depend on the in-plane and out-of-plane dielectric constants, respectively.

TABLE 2. ON-current I_{ON} [$\mu\text{A}/\mu\text{m}$], bandgap E_g [eV], reduced effective masses m_r^* [m_0], natural scaling length λ [nm], effective natural scaling length Λ [nm] from simulation, and η values [unitless] of TMD TFETs.

Material	I_{ON}	E_g	m_r^*	λ	Λ	η
WTe ₂	127	0.75	0.17	0.45	2.45	3.15
WSe ₂	4.6	1.56	0.21	0.41	2.5	5.2
MoTe ₂	2.3	1.08	0.32	0.5	2.7	5.8
MoS ₂	0.3	1.68	0.29	0.38	2.5	6.3

The difference between the values of Λ and λ , listed in Table 2, shows the importance of W_D . According to the DFT simulations, MoTe₂ has the higher dielectric constant if compared with WSe₂ [19], which further lowers its ON-current. The factor η for these materials is shown in Table 2. The larger the η , the smaller the current. By comparing the η values, it can be seen that WSe₂ provides higher currents close to the threshold voltage compared with MoTe₂ TFETs in spite of its higher bandgap. Moreover, it is expected that WTe₂ TFET produces the highest ON-current. Note that by employing (6), the ON-current ratios between the TMD FETs from different materials can be reproduced within reasonable accuracy when using the η values from Table 2.

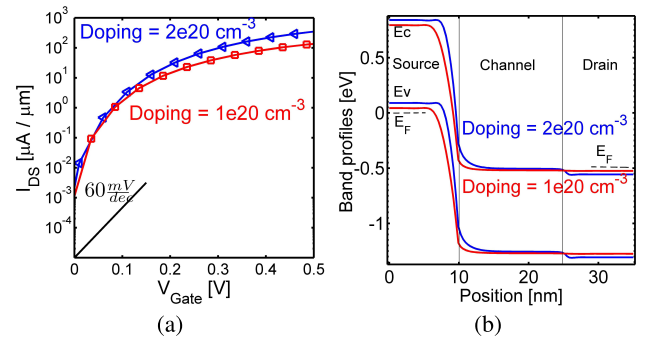


FIGURE 4. (a) Transfer characteristics and (b) band diagrams of WTe₂ with doping levels of 1e20 and 2e20 cm⁻³.

From Fig. 3, one can conclude that WTe₂ TFETs show promising ON-currents and a steep SS compared with other TMD TFETs. It is possible to further increase the ON-current of WTe₂ TFET by increasing the doping concentration at the source and drain regions. Increasing the doping decreases the depletion width of the source-to-channel interface, which also decreases η according to (7). Consequently, the ON-current increases. Fig. 4(a) shows a comparison between the ON-currents of WTe₂ TFETs with source/drain doping levels of 1e20 and 2e20 cm⁻³. In the case of 2e20 cm⁻³ doping level, the ON-current increases to 350 $\mu\text{A}/\mu\text{m}$, which is a very high ON-current if compared with other TFETs. It is important to notice that the electric field at the source-to-channel interface depends on both the natural scaling length λ and the depletion width W_D . As a result, reduction of λ is not sufficient for high ON-currents. A smaller W_D is also needed. In this regard, the doping of the source and drain regions should be designed carefully, whether this doping is chemically or electrically induced. Fig. 4(b) shows the band profiles for these two different doping concentrations. It is apparent that the higher doping concentration shows higher electric field due to the smaller W_D . Notice that the drain region is usually doped less than the source region to suppress the p-branch in the I - V characteristics and improve the OFF-state performance of the TFET [38]. However, due to a relatively large bandgap and effective mass of the TMD materials, the minimum achievable current in the TMD TFETs is always very small and below 1 nA/ μm even for a drain doping level

of $2e20 \text{ cm}^{-3}$. Consequently, lowering the drain doping does not have any significant impact on the transfer characteristics of the TMD TFETs.

B. C-V AND DIBL

Fig. 5 shows the total gate capacitance versus the gate voltage ($C-V$) for the TMD TFETs under investigation. There are two major factors that determine the $C-V$ characteristics: 1) the quantum capacitance and 2) the threshold voltage. The total gate capacitance (C_G) can be modeled as a series of oxide capacitance (C_{ox}) and quantum capacitance (C_Q). The quantum capacitance is proportional to the density of states and m^* of the material [39], [40]. Materials with larger m^* have larger C_Q , which translates into larger C_G . On the other hand, the threshold voltage determines the voltage where the charge starts to appear in the channel. Since the OFF-currents of the TFETs have been fixed here, the threshold voltage of one material is different from the other. Clearly, WTe_2 is showing the lowest C_G values, another benefit when it comes to benchmarking of various TMD devices is discussed below.

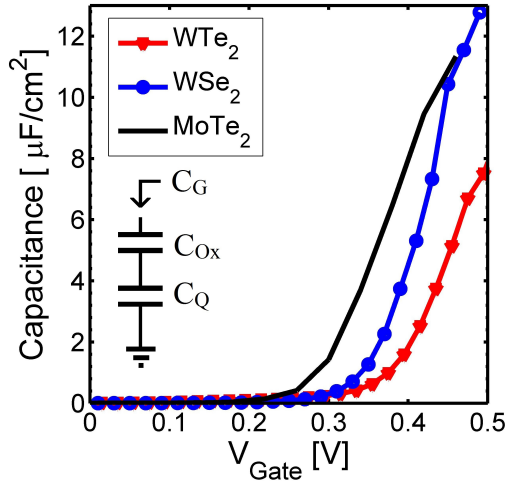


FIGURE 5. $C-V_{\text{Gate}}$ of WTe_2 , WSe_2 , and MoTe_2 TFETs.

DIBL is one of the most important short-channel effects for ultrascaled transistors. DIBL causes a reduction of the threshold voltage by the drain voltage, and it is one of the commonly used criteria for indicating short-channel behavior [37]. In TFETs, the active region in which tunneling occurs is right at the source-to-channel interface, far from the drain contact. Moreover, in 2-D TFETs, gate control is stronger due to a thin channel that suppresses short-channel effects. Consequently, short-channel effects are less significant in comparison with conventional FETs (n-i-n or p-i-p doped transistors). The numerical values of DIBL for the TMD TFETs obtained in

TABLE 3. DIBL values for TMD TFETs.

Material	WTe_2	WSe_2	MoTe_2
DIBL [mV/V]	25	20	67

this paper are listed in Table 3. Note that the DIBL values of WSe_2 and WTe_2 TFETs are substantially smaller than the reported 80 mV/V DIBL of ultrascaled MOSFETs [32], [41]. DIBL is calculated at the current level of $1 \text{ nA}/\mu\text{m}$ from the change in the threshold voltage caused by varying V_{DS} from 0.1 to 0.5 V

$$\text{DIBL} = -\frac{V_{\text{Th}}(V_{\text{DS}} = 0.5) - V_{\text{Th}}(V_{\text{DS}} = 0.1)}{0.5 - 0.1}. \quad (8)$$

Among these TMD TFETs, WSe_2 and WTe_2 show a smaller DIBL compared with MoTe_2 . This is because WSe_2 and WTe_2 have a smaller in-plane dielectric constant compared with MoTe_2 , which reduces the electric field penetration from drain, and hence suppresses the short-channel effects.

C. SUBTHRESHOLD SWING AND ENERGY-DELAY PRODUCT

The main idea behind a TFET is to achieve a steep SS below the Boltzmann limit of 60 mV/decade. It is important to compare the steep devices in a generic way. For example, the average SS does not provide information about the current range in which the $I-V$ is steep. Recently, a method for benchmarking steep devices has been proposed, which gives insight into the local steepness of the $I-V$ curve [42]. In this method, the SS is plotted against the drain-to-source current density of the device. Fig. 6(a) shows how monolayer TMD TFETs fit in this picture. Notice that the current on the horizontal axis is not the ON-current but the current where the SS has been calculated. The devices with the best performance will ideally be placed on the lower right corner of the figure, where the SS is small and the drain-to-source current is large.

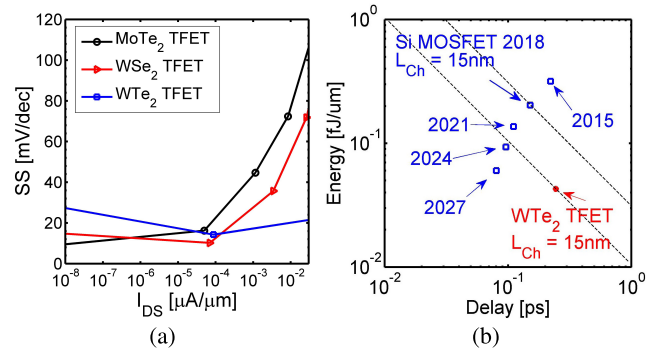


FIGURE 6. (a) $SS-I_{\text{DS}}$ for different TMD TFETs. (b) Energy delay of WTe_2 TFET with a doping level of $2e20 \text{ cm}^{-3}$ versus Si MOSFETs from ITRS [32], [41]. Dashed lines: constant energy-delay products.

Fig. 6(a) shows again that monolayer WTe_2 is the most promising candidate for TFET applications among the TMD materials considered in this paper. Fig. 6(b) shows the energy ($C_{\text{Gate}} V_{\text{DD}}^2$) versus the intrinsic delay ($C_{\text{Gate}} V_{\text{DD}} / I_{\text{ON}}$) of a WTe_2 TFET versus ultrascaled silicon MOSFETs. The WTe_2 TFET shows a smaller intrinsic energy-delay product

value when compared with MOSFETs with the same channel length. In terms of the anticipated circuit performance of a 32-bit adder based on TMD TFETs, the performance specs discussed in this paper for WTe₂ devices for $V_{DD} = 0.5$ V result in the similar energy-delay product as reported in [43] for $V_{DD} = 0.25$ V. The actual energy and delay values were calculated to be 13 fJ and 2450 ps, respectively, using the same code as in [43].

IV. CONCLUSION

In this paper, the performance of various TMD materials (MoS₂, WSe₂, MoTe₂, and WTe₂) TFETs has been investigated through self-consistent atomistic simulations. It has been shown that an atomically thin channel alone is not sufficient for high-performance TFETs; in particular, to achieve high ON-currents, the choice of channel material and device design are critical as well. According to our analysis, WTe₂ is the most promising TMD in this paper for TFET applications with high ON-currents of 350 $\mu\text{A}/\mu\text{m}$. TMD TFETs exhibit reduced short-channel effects: DIBL and SS values are significantly lower than for Si MOSFETs (by a factor of $\sim 1/3$). Moreover, the energy-delay product of the optimized WTe₂ TFET is lower than that of an ultrascaled Si MOSFET. Our simulations show that 2-D materials with lower bandgaps (0.5–0.7 eV) and effective masses are more suitable for high-performance TFETs.

ACKNOWLEDGMENT

The authors would like to thank J. Nahas and R. Perricone for the 32-bit adder energy-delay calculations and T. Ameen for his help with the simulations. The use of nanoHUB.org computational resources operated by the Network for Computational Nanotechnology is gratefully acknowledged.

REFERENCES

- [1] J. Appenzeller, Y.-M. Lin, J. Knoch, and P. Avouris, "Band-to-band tunneling in carbon nanotube field-effect transistors," *Phys. Rev. Lett.*, vol. 93, no. 19, p. 196805, 2004.
- [2] J. Appenzeller, Y.-M. Lin, J. Knoch, and P. Avouris, "Comparing carbon nanotube transistors—The ideal choice: A novel tunneling device design," *IEEE Trans. Electron Devices*, vol. 52, no. 12, pp. 2568–2576, Dec. 2005.
- [3] A. M. Ionescu and H. Riel, "Tunnel field-effect transistors as energy-efficient electronic switches," *Nature*, vol. 479, pp. 329–337, Nov. 2011.
- [4] R. K. Ghosh and S. Mahapatra, "Monolayer transition metal dichalcogenide channel-based tunnel transistor," *IEEE J. Electron Devices Soc.*, vol. 1, no. 10, pp. 175–180, Oct. 2013.
- [5] X.-W. Jiang and S.-S. Li, "Performance limits of tunnel transistors based on mono-layer transition-metal dichalcogenides," *Appl. Phys. Lett.*, vol. 104, no. 19, p. 193510, 2014.
- [6] R.-H. Yan, A. Ourmazd, and K. F. Lee, "Scaling the Si MOSFET: From bulk to SOI to bulk," *IEEE Trans. Electron Devices*, vol. 39, no. 7, pp. 1704–1710, Jul. 1992.
- [7] L. Liu, D. Mohata, and S. Datta, "Scaling length theory of double-gate interband tunnel field-effect transistors," *IEEE Trans. Electron Devices*, vol. 59, no. 4, pp. 902–908, Apr. 2012.
- [8] K. Suzuki, T. Tanaka, Y. Tosaka, H. Horie, and Y. Arimoto, "Scaling theory for double-gate SOI MOSFET's," *IEEE Trans. Electron Devices*, vol. 40, no. 12, pp. 2326–2329, Dec. 1993.
- [9] D. Jena, "Tunneling transistors based on graphene and 2-D crystals," *Proc. IEEE*, vol. 101, no. 7, pp. 1585–1602, Jul. 2013.
- [10] T. Low et al., "Modeling study of the impact of surface roughness on silicon and germanium UTB MOSFETs," *IEEE Trans. Electron Devices*, vol. 52, no. 11, pp. 2430–2439, Nov. 2005.

- [11] L. F. Mattheiss, "Band structures of transition-metal-dichalcogenide layer compounds," *Phys. Rev. B*, vol. 8, no. 8, pp. 3719–3740, 1973.
- [12] M. Chhowalla, H. S. Shin, G. Eda, L.-J. Li, K. P. Loh, and H. Zhang, "The chemistry of two-dimensional layered transition metal dichalcogenide nanosheets," *Nature Chem.*, vol. 5, no. 4, pp. 263–275, 2013.
- [13] Q. H. Wang, K. Kalantar-Zadeh, A. Kis, J. N. Coleman, and M. S. Strano, "Electronics and optoelectronics of two-dimensional transition metal dichalcogenides," *Nature Nanotechnol.*, vol. 7, no. 11, pp. 699–712, 2012.
- [14] J. Kang, W. Cao, X. Xie, D. Sarkar, W. Liu, and K. Banerjee, "Graphene and beyond-graphene 2D crystals for next-generation green electronics," in *Proc. SPIE*, Jun. 2014, p. 908305.
- [15] S. Vishwanath et al., "Atomic structure of thin MoSe₂ films grown by molecular beam epitaxy," *Microsc. Microanal.*, vol. 20, no. S3, pp. 164–165, 2014.
- [16] K. F. Mak, C. Lee, J. Hone, J. Shan, and T. F. Heinz, "Atomically thin MoS₂: A new direct-gap semiconductor," *Phys. Rev. Lett.*, vol. 105, no. 13, p. 136805, 2010.
- [17] B. Radisavljevic, A. Radenovic, J. Brivio, V. Giacometti, and A. Kis, "Single-layer MoS₂ transistors," *Nature Nanotechnol.*, vol. 6, pp. 147–150, Jan. 2011.
- [18] C. L. dos Santos and P. Piquini, "Diameter dependence of mechanical, electronic, and structural properties of InAs and InP nanowires: A first-principles study," *Phys. Rev. B*, vol. 81, no. 7, p. 075408, 2010.
- [19] A. Kumar and P. K. Ahluwalia, "Tunable dielectric response of transition metals dichalcogenides MX₂ (M=Mo, W; X=S, Se, Te): Effect of quantum confinement," *Phys. B*, vol. 407, no. 24, pp. 4627–4634, 2012.
- [20] T. Cheiwchanchamnangij and W. R. L. Lambrecht, "Quasiparticle band structure calculation of monolayer, bilayer, and bulk MoS₂," *Phys. Rev. B*, vol. 85, no. 20, p. 205302, 2012.
- [21] E. S. Kadantsev and P. Hawrylak, "Electronic structure of a single MoS₂ monolayer," *Solid State Commun.*, vol. 152, no. 10, pp. 909–913, 2012.
- [22] H. Liu et al., "Phosphorene: An unexplored 2D semiconductor with a high hole mobility," *ACS Nano*, vol. 8, no. 4, pp. 4033–4041, 2014.
- [23] P. Vogt et al., "Silicene: Compelling experimental evidence for graphene-like two-dimensional silicon," *Phys. Rev. Lett.*, vol. 108, no. 15, p. 155501, 2012.
- [24] J. C. Slater and G. F. Koster, "Simplified LCAO method for the periodic potential problem," *Phys. Rev.*, vol. 94, no. 6, pp. 1498–1524, Jun. 1954.
- [25] C. Gong, H. Zhang, W. Wang, L. Colombo, R. M. Wallace, and K. Cho, "Band alignment of two-dimensional transition metal dichalcogenides: Application in tunnel field effect transistors," *Appl. Phys. Lett.*, vol. 103, no. 5, p. 053513, 2013.
- [26] Y. Tan et al., "Empirical tight binding parameters for GaAs and MgO with explicit basis through DFT mapping," *J. Comput. Electron.*, vol. 12, no. 1, pp. 56–60, 2013.
- [27] C. S. Lent and D. J. Kirkner, "The quantum transmitting boundary method," *J. Appl. Phys.*, vol. 67, no. 10, pp. 6353–6359, 1990.
- [28] M. Luisier, A. Schenk, W. Fichtner, and G. Klimeck, "Atomistic simulation of nanowires in the $sp^3d^5s^*$ tight-binding formalism: From boundary conditions to strain calculations," *Phys. Rev. B, Condens. Matter*, vol. 74, no. 20, p. 205323, 2006.
- [29] S. Steiger, M. Povolotskiy, H.-H. Park, T. Kubis, and G. Klimeck, "NEMO5: A parallel multiscale nanoelectronics modeling tool," *IEEE Trans. Nanotechnol.*, vol. 10, no. 6, pp. 1464–1474, Nov. 2011.
- [30] J. E. Fonseca et al., "Efficient and realistic device modeling from atomic detail to the nanoscale," *J. Comput. Electron.*, vol. 12, no. 4, pp. 592–600, 2013.
- [31] L. Yang et al., "Chloride molecular doping technique on 2D materials: WS₂ and MoS₂," *Nano Lett.*, vol. 14, no. 11, pp. 6275–6280, 2014.
- [32] (2013). *International Technology Roadmap for Semiconductors (ITRS)*. [Online]. Available: <http://www.itrs.net>
- [33] M. Salmani-Jelodar, S. Mehrotra, H. Ilatikhameneh, and G. Klimeck, "Design guidelines for sub-12 nm nanowire MOSFETs," *IEEE Trans. Nanotechnol.*, vol. 14, no. 2, pp. 210–213, Mar. 2015.
- [34] K. Alam and R. K. Lake, "Monolayer MoS₂ transistors beyond the technology road map," *IEEE Trans. Electron Devices*, vol. 59, no. 12, pp. 3250–3254, Dec. 2012.
- [35] A. C. Seabaugh and Q. Zhang, "Low-voltage tunnel transistors for beyond CMOS logic," *Proc. IEEE*, vol. 98, no. 12, pp. 2095–2110, Dec. 2010.
- [36] S. Das, A. Prakash, R. Salazar, and J. Appenzeller, "Toward low-power electronics: Tunneling phenomena in transition metal dichalcogenides," *ACS Nano*, vol. 8, no. 2, pp. 1681–1689, 2014.
- [37] W. Zhao et al., "Origin of indirect optical transitions in few-layer MoS₂, WS₂, and WSe₂," *Nano Lett.*, vol. 13, no. 11, pp. 5627–5634, 2013.

- [38] V. Vijayvargiya and S. K. Vishvakarma, "Effect of drain doping profile on double-gate tunnel field-effect transistor and its influence on device RF performance," *IEEE Trans. Nanotechnol.*, vol. 13, no. 5, pp. 974–981, Sep. 2014.
- [39] S. Luryi, "Quantum capacitance devices," *Appl. Phys. Lett.*, vol. 52, no. 6, pp. 501–503, 1988.
- [40] Z. Chen and J. Appenzeller, "Mobility extraction and quantum capacitance impact in high performance graphene field-effect transistor devices," in *Proc. IEEE IEDM*, Dec. 2008, pp. 1–4.
- [41] M. Salmani-Jelodar, S. Kim, K. Ng, and G. Klimeck, "Transistor roadmap projection using predictive full-band atomistic modeling," *Appl. Phys. Lett.*, vol. 105, no. 8, p. 083508, 2014.
- [42] H. Lu and A. Seabaugh, "Tunnel field-effect transistors: State-of-the-art," *IEEE J. Electron Devices Soc.*, vol. 2, no. 4, pp. 44–49, Jul. 2014.
- [43] D. E. Nikonov, and I. A. Young, "Benchmarking of beyond-CMOS exploratory devices for logic integrated circuits," *IEEE J. Exploratory Solid-State Comput. Devices Circuits*, to be published.



HESAMEDDIN ILATIKHAMEH received the M.S. degree in electrical engineering from Sharif University, Tehran, Iran, in 2007. He is currently pursuing the Ph.D. degree with Purdue University, West Lafayette, IN, USA.

He conducts research on the novel electronic, thermoelectric, and optoelectronic devices to predict the performance and understand the underlying physics of these devices. He has also been an Active Member of LEAST Project with the

purpose of realizing steep subthreshold devices. He is currently a member of NEMO5 development team and has been involved in the development of quantum transport, strain, mode-space, and phonon solvers for this tool. His current research interests include ultrascaled Si, III–V, and 2-D materials FETs and tunnel FETs, Nitride hetero-structures, quantum dots, quantum transport, and scaling theories.



YAOHUA TAN received the B.S. and M.S. degrees from Tsinghua University, Beijing, China, in 2006 and 2008, respectively. He is currently pursuing the Ph.D. degree with the School of Electrical and Computer Engineering, Purdue University, West Lafayette, IN, USA.



BOZIDAR NOVAKOVIC (M'13) received the B.S. degree in electrical and computer engineering from the University of Novi Sad, Novi Sad, Serbia, in 2005, the M.S. degree in electrical engineering from the University of Belgrade, Belgrade, Serbia, in 2007, and the M.A. degree in physics and Ph.D. degree in electrical and computer engineering from the University of Wisconsin—Madison, Madison, WI, USA, in 2011 and 2012, respectively.

He has been a Post-Doctoral Research Associate with the Network for Computational Nanotechnology, Purdue University, West Lafayette, IN, USA, since 2012. His current research interests include time-resolved quantum transport, steep subthreshold electronic devices, and nanoelectronic simulation software development.



GERHARD KLIMECK (S'91–M'95–SM'04–F'13) received the Ph.D. degree from Purdue University, West Lafayette, IN, USA, in 1994, and the German Electrical Engineering degree from Ruhr-University Bochum, Bochum, Germany, in 1990.

He is currently the Reilly Director of the Center for Predictive Materials and Devices and the Network for Computational Nanotechnology, and a Professor of Electrical and Computer Engineering with Purdue University, West Lafayette, IN, USA.

He leads the development and deployment of web-based simulation tools, research seminars, tutorials, and classes that are hosted on <http://nanohub.org> a National Nanotechnology Resource and Infrastructure community website that is utilized by over 330 000 users annually. He co-authored 35 tools on nanoHUB that have been used by over 36 000 users. Over 11 000 students used these tools in formalized educational settings such as homework or project assignments in over 776 courses at 64 institutions. His lectures and tutorials have been viewed by over 200,000 nanoHUB users. He was the Technical Group Supervisor for the Applied Cluster Computing Technologies Group and continues to hold his appointment as a Principal Member with the NASA Jet Propulsion Laboratory on a faculty part-time basis. He was a member of Technical Staff with the Central Research Laboratory, Texas Instruments. His current research interests include the modeling of nanoelectronic devices, parallel cluster computing, and genetic algorithms. He has been the lead on the development of NEMO 3-D, a tool that enables the simulation of tens-of-million atom quantum dot systems, and NEMO 1-D, the first nanoelectronic CAD tool. His work is documented in over 350 peer-reviewed publications and over 580 conference presentations.

Dr. Klimeck is also a fellow of the Institute of Physics and the American Physical Society.



RAJIB RAHMAN received the bachelor's degree in physics from Gettysburg College, Gettysburg, PA, USA, in 2002, and the master's and Ph.D. degrees in electrical engineering from Purdue University, West Lafayette, IN, USA, in 2005 and 2009, respectively.

He was a Post-Doctoral Fellow with Sandia National Laboratories, Albuquerque, NM, USA, from 2009 to 2012, where he investigated quantum computing architectures in silicon. He is currently a Research Assistant Professor with Purdue University, working on atomistic modeling of electronic structure and transport properties of nanoscale devices. His current research interests include spin relaxation and many-body interactions in semiconductor qubits, and device applications of two-dimensional materials. He is one of the developers of the NEMO3D tool.



JOERG APPENZELLER received the M.S. and Ph.D. degrees in physics from the Technical University of Aachen, Aachen, Germany, in 1991 and 1995. His Ph.D. dissertation investigated quantum transport phenomena in low-dimensional systems based on III/V heterostructures.

He spent one year as a Research Scientist with the Research Center, Juelich, Germany, before he became an Assistant Professor with the Technical University of Aachen in 1996. During his professorship, he explored mesoscopic electron transport in different materials, including carbon nanotubes and superconductor-semiconductor-hybrid devices. From 1998 to 1999, he was with the Massachusetts Institute of Technology, Cambridge, MA, USA, as a Visiting Scientist, exploring the ultimate scaling limits of silicon MOSFET devices. From 2001 to 2007, he had been with the IBM T. J. Watson Research Center, Yorktown, NY, USA, as a Research Staff Member, mainly involved in the investigation of the potential of carbon nanotubes and silicon nanowires for a future nanoelectronics. Since 2007, he has been a Professor of Electrical and Computer Engineering with Purdue University, West Lafayette, IN, USA, and a Scientific Director of Nanoelectronics with the Birck Nanotechnology Center. In 2014, he became the Barry M. and Patricia L. Epstein Professor of Electrical and Computer Engineering. His current research interests include novel devices based on low-dimensional nano-materials as nanowires, nanotubes, graphene, and di-chalcogenides.