Benchmarking of Beyond-CMOS Exploratory Devices for Logic Integrated Circuits

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ABSTRACT   A new benchmarking of beyond-CMOS exploratory devices for logic integrated circuits is presented. It includes new devices with ferroelectric, straintronic, and orbitronic computational state variables. Standby power treatment and memory circuits are included. The set of circuits is extended to sequential logic, including arithmetic logic units. The conclusion that tunneling field-effect transistors are the leading low-power option is reinforced. Ferroelectric transistors may present an attractive option with faster switching delay. Magnetoelectric effects are more energy efficient than spin transfer torque, but the switching speed of magnetization is a limitation. This article enables a better focus on promising beyond-CMOS exploratory devices.

INDEX TERMS   Adder, arithmetic logic unit (ALU), beyond-CMOS, computational throughput, electronics, ferroelectric, integrated circuits, logic, magnetoelectric, power dissipation, spintronics.

I. INTRODUCTION

SUCCESSFUL scaling of CMOS field-effect transistors (FETs) has occurred over more than four decades according to the cadence of Moore's law [1] and has now reached gate lengths of 20 nm in [2]. The projection of scaling limits and quantum limits on the size of electronic transistors [3] has increased the urgency of research for finding beyond-CMOS device options. Various research centers, including the Nanoelectronics Research Initiative (NRI), were therefore organized [4].

Benchmarking devices became an important effort within the NRI. It not only provided a comparison between various device options, but also demanded a clear articulation of how each device performs digital computation with an integrated circuit. The first pass at beyond-CMOS benchmarking [5] (which we call BCB 1.0) was performed based on estimates done by each device group that were neither reviewed by others nor validated through an audit process. The next release (BCB 2.0) [6], [7] applied a simple, transparent, and uniform methodology to all the beyond-CMOS devices to derive an estimate of logic circuit performance—area, switching delay, and energy. It took a few device parameters from device groups as inputs and calculated the performance estimates using consistent equations and assumptions. BCB 2.0

received positive feedback and assurances of usefulness from the research community. Since then, the thrust of NRI has been renewed and a new program, STARnet was added with a common mission. Their exploratory research scope included a wider range of exploratory materials, switching mechanisms, and devices. In general, the understanding of important aspects of beyond-CMOS circuit operation and requirements improved. Several review papers [8], [9] focused on different classes of beyond-CMOS devices. We decided to prepare a new release of benchmarking (BCB 3.0) to reflect the improved understanding and to update it with the current input parameters and to add the additional new beyond-CMOS devices. Several changes were made compared with the previous BCB 2.0 release [7]. We have included 11 additional devices. New switching mechanisms are included: 1) spin Hall effect; 2) ferroelectric switching; and 3) piezoelectric switching. A better understanding of the role of the power supply and clocking of spintronic devices by charge currents is achieved. We now include not only active power, but also standby power in circuits. Most importantly, we drastically extended the functionality of benchmarking circuits, which now comprises sequential logic up to arithmetic logic units (ALUs). Also a number of minor improvements were made throughout the benchmarking methodology. One can follow all the changes and utilize

BCB 3.0 by downloading the new version of the MATLAB code [10]. We maintain the approach of 2.0, preferring simpler analytical estimates of performance and recognizing that the performance estimates can only be approximate at this stage of the research into of beyond-CMOS devices. The goal of this paper is to capture the changes made and the new insights gained since the previous BCB release.

II. NEW DEVICES

The concept of computational variables for devices was described in [7] and [11]. In BCB 3.0 we include additional computational variables (Table 1). Ferroelectric devices rely on electric polarization. Piezoelectronic devices utilize stress and strain mechanisms to be switched. Metal–insulator transition devices are switched between states with different orbital states of electrons within the crystal lattice cell. Based on their approach to the circuit architecture, we divide beyond-CMOS circuits into two major groups—transistor circuits (TCs) and majority-gate circuits (MGCs). The first mostly includes electronic, ferroelectric, straintronic, and orbitronic devices, while the second is mostly composed of spintronic devices. However, there are exceptions: even though a spinFET is a spintronic device, we use only its transistor-like operation in making circuits. Also the spintronic device STT/DW has electrical interconnects and is connected into circuit topologies reminiscent of CMOS. The reason why the majority gates are used for most of spintronic devices is that there is no analog of a transistor for magnetization. A transistor uses charge on a gate to control current which can switch another gate. However, the magnetization cannot directly control a flux of any physical quantity that can switch magnetization (e.g., spin current). Instead one can use the vector property of magnetization where the addition of three input magnetizations gives a vector with a definite direction. Note that majority-gate logic is a subclass of threshold logic [12]. Below we relate many estimates back to an intrinsic switching element. For TC, the intrinsic element is a transistor. For MGC, the intrinsic element is a single nanomagnet, rather than a whole majority gate.

TABLE 1. Computational variables and corresponding devices.

Class	VARIABLES	Example
Charge	Q, I, V	CMOS, TFET
Electric Dipole	P	FeFET
Magnetic Dipole	M, I_{spin}	ASL, SWD, NML
Orbital State	Orb, Bose condensate	BisFET
Strain	σ	PiezoFET

Q=charge, I=current, V=voltage, P=electric polarization, M=magnetization, I_{spin}=spin current, Orb=orbital state, σ=stress.

The list of considered devices changed compared with [7]. One device, STTtriad, has been removed due to generally worse performance estimates and a lack of continued research on it. Several devices currently under study at NRI and STARnet centers have been added: ITFET [13] aka SymFET [14], FEFET [15], NCFET [16],

PiezoFET [17], MITFET [18], CSL [19], ExFET [5], ThinTFET [20], GaNTFET [21], TMDTFET [22], and van der Wall FET (vdwFET) [23]. Also the mLogic [24] device concept has been merged with that of the STT/DW [25] due to the similarity of the essential elements of the devices. We do not include semiconductor spintronic devices, such as the spin gain transistor [26]. The physical principles of the operation of the devices are discussed in [27]. In addition, a list summarizing the devices under consideration and their attributes is in Table 2. The cells are colored according to their computational variables with a coloring scheme consistently used in this paper. The newly included devices involve a larger variety of switching mechanisms and provide more options for beyond-CMOS logic.

TABLE 2. List of devices under consideration with their employed computational variables and classification.

Device name	acronym	input(s)	control	int. state	output	material
Si MOSFET high perf.	CMOS HP	V	Vg	Q	V	silicon
Si MOSFET low voltage	CMOS LV	V	Vg	Q	V	InAs
van der Walls FET	vdWFET	V	Vg	Q	V	MoS₂
Homojunction III-V TFET	HomJTFET	V	Vg	R	V	InAs
Heterojunction III-V TFET	HetJTFET	V	Vg	R	V	GaSb/InAs
Graphene nanoribbon TFET	gnrFTET	V	Vg	R	V	graphene
Interlayer tunneling FET	ITFET	V	Vg	R	V	graphene
Two D Heterojunction Interlayer TFET	ThinFET	V	Vg	R	V	WTe₂/SnSe₂
GaN TFET	GaNFET	V	Vg	R	V	GaN
Transition Metal Dichalchogenide TFET	TMDTFET	V	Vg	R	V	WTe₂
Graphene pn-junction	GpnJ	V	Vg	R	V	graphene
Ferroelectric FET	FEFET	V	Vg	P	V	PZT
Negative capacitance FET	NCFET	V	Vg	P	V	PZT
Piezoelectric FET	PiezoFET	V	V	σ	V	AlN
Bilayer pseudospin FET	BisFET	V	Vg	BC	V	graphene
Excitonic FET	ExFET	V	Vg	BC	V	MoS₂/MoSe₂
Metal-insulator transistor	MITFET	V	Vg	Orb	V	NdNiO₃
SpinFET (Sughara-Tanaka)	SpinFET	V	Vg, Vm	Q, M	V	CoFeB
All-spin logic	ASL	M	V	M	M	CoPtCrB
Charge-spin logic	CSL	V	V	M	I	CoPtCrB
Spin torque domain wall	STT/DW	I	V	M	I	CoFeB
Spin majority gate	SMG	M	V	M	M	PMN-PT
Spin torque oscillator	STO	I	V	M	I	CoPtCrB
Spin wave device	SWD	M	I or V	M	M	PMN-PT
Nanomagnetic logic	NML	M	B or V	M	M	PMN-PT

B=magnetic field, Vg=gate voltage, Vm=magnetic switching voltage, BC=Bose condensate. The cell color designates the computational variable: blue=electronic, orange=ferroelectric, yellow=straintronic, purple=orbitronic, red=spintronic devices. Key materials are also listed.

III. SWITCHING MECHANISMS AND MATERIAL PARAMETERS

Devices with various computational variables require appropriate physical effects for their switching. We distinguish four switching mechanisms: 1) electronic—charging of a gate capacitor by current; 2) ferroelectric—similar to electronic, but accompanied by switching of electric polarization; 3) current-driven magnetization switching; and 4) voltage-driven magnetization switching. The first two are employed in TC; the second two underpin MGC. Models for these switching mechanisms employ material parameters collected in [27]. Several parameters were kept the same as in BCB 2.0 (refer to [7] for their definition and values). Here we focus on the models that are new or updated in BCB 3.0.

Models for switching mechanisms are built to obtain the switching delay and energy for intrinsic elements (transistors or nanomagnets). While beyond-CMOS devices are very diverse, we reduce their operation to a few
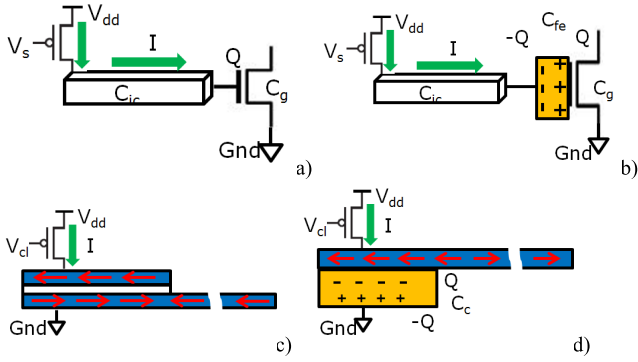
FIGURE 1. Scheme of driving switching of (a) electric device, (b) ferroelectric device, (c) ferromagnetic device, and (d) magnetoelectric device.

cases based on fundamental principles and switching mechanisms.

In electronic switching [Fig. 1(a)] current generated by a transistor is used to charge a gate of a transistor in the next logic state. The characteristic switching delay (determined by charging of the gate) and energy are obtained via well-known expressions [28]

$$t_{el} \approx CV_{dd}/I, \quad E_{el} \approx CV_{dd}^2 \quad (1)$$

where V_{dd} is the power supply voltage, I is the ON-current in a transistor, and C is the capacitance that is driven in switching. This capacitance includes the capacitance of the gate dielectric, the semiconductor capacitance, and the parasitic capacitance (such as fringing) for one transistor. The nontrivial aspect of applying this model is the need for a thorough accounting of the capacitances of the gates, and interconnects, and parasitic capacitances.

Ferroelectric switching [Fig. 1(b)] is treated similarly to the electronic one. The difference is that the total transfer charge includes a term proportional to the saturation polarization of the ferroelectric P_{fe}

$$Q = P_{fe}A + CV_{dd}, \quad t_{ch} \approx Q/I, \quad E_{el} \approx QV_{dd}. \quad (2)$$

Also, the switching delay is limited by the intrinsic response time of a ferroelectric τ_{fe} rather than the charging time t_{ch}. Experiments [29] provide a value of ~70 ps for large area samples. We adopt optimistic estimates of the material parameters of nanoscale ferroelectric materials [27]. We also treat piezoelectric switching using this ferroelectric switching model, though we assume that polarization is only partially switched.

Current-driven magnetization switching [Fig. 1(c)] is primarily based on the spin transfer torque effect. In such a case, the current is spin polarized in a pinned magnet and the polarized spin is used to switch a free magnet. It can be modeled as in the previous BCB 2.0 release [30], [31]. The spin-polarized current $I_s = PI$ needs to exceed the critical value

$$I_{cs} = e\alpha\mu_0 M_s^2 v_{nm}/\hbar \quad (3)$$

where v_{nm} is the volume of a nanomagnet. Material parameters are defined in [27]. The switching time and energy are

$$t_{stt} \approx \frac{eM_s v_{nm}}{g\mu_B(I_s - I_{cs})} \log\left(\frac{2\sqrt{2}\pi}{\sqrt{\Delta}}\right), \quad E_{stt} = IV_{dd}t_{stt}. \quad (4)$$

The spin torque is zero when there is zero angle between the injected spin polarization and the magnetization in the nanomagnet. Thermal fluctuations provide an initial angle difference to start the switching, which is thus a stochastic process. The above switching delay calculation corresponds to a 50% probability of switching. To account for the thermal spread, we introduce an additional factor of three into the delay estimate. Once magnetization is switched in one part of a ferromagnetic wire, it can propagate as a domain wall or a spin wave to the next logic stage. Switching by the spin Hall effect is described similarly. In this case, the spin-polarized current is generated by and flows perpendicular to the charge current in a material with strong spin-orbit coupling (such as Pt, W, or Ta). The spin current injected in the nanomagnet of width w_{nm} is approximately

$$I_s = \theta_{she}w_{nm}I/d_{she}. \quad (5)$$

Voltage-driven magnetization switching [Fig. 1(d)] is performed by a magnetoelectric effect [32]. When a capacitor is charged, and electric polarization of the material is switched, bulk or surface magnetoelectric coupling causes switching of the magnetization. We consider four cases of the magnetoelectric effect in various material combinations and treat each of them in a similar manner.

Material parameters, including the measured electric field and the corresponding effective magnetic field, are provided in [27] and are distinguished with corresponding subscripts. The cases are: mf = exchange bias exerted by a multiferroic material effect (such as in bismuth-iron-oxide) [33], me = exchange bias in a linear magnetoelectric effect (such as in chromia, Cr_2O_3) [34], ms = piezoelectric material (such as lead magnesium niobate-lead titanate) exerts strain on a ferromagnet with a high magnetostrictive coupling effect [35], su = electrically switchable surface anisotropy effect between a ferromagnet and a dielectric (such as MgO) [36]. The required electric field, switching delay of a nanomagnet, charge, and magnetoelectric charging energy, and the charging time are

$$E_r = E_{mf}B_c/B_{mf}, \quad t_{mag} = \pi/(\gamma B_c) \quad (6)$$
$$Q = A_{me}(\varepsilon_0\varepsilon_{mf}E_r + P_{mf}) \quad (7)$$
$$t_{mf} \approx Q/I, \quad E_{me} \approx QE_r t_{mf}. \quad (8)$$

Here the area of the magnetoelectric surface is A_{me}, and the critical magnetic field $B_c \approx 0.1$ T for switching the nanomagnets is obtained from micromagnetic simulations.

Note that all of these switching mechanisms involve a short pulse of charge current. However, the current plays a different role in each. In electronic and ferroelectric devices, current carries the computational variable from one logic stage

to the next. In spintronic devices, magnetization is the computational variable passed to the next stage. The current pulse serves both as the power supply to perform the switching and as a clock to time the operation. This realization is a major change compared with the initial intent of NRI. It was believed that beyond-CMOS devices needed to avoid charge current in order to be energy efficient. Since then, charge current has turned out to be an indispensable aspect of beyond-CMOS devices. Note that therefore the energy of clocking separate circuits is included, but not the contribution of the clock distribution on the whole chip.

IV. DEVICE PARAMETERS

In BCB 3.0, we keep the values for physical geometry parameters consistent with those presented in the 2011 edition of the International Technology Roadmap for Semiconductors, and its 2018 node ($F = 15$ nm) [37]. CMOS HP parameters are taken directly from [37] for high-performance transistors. CMOS LV is an InAs device [38] of the same geometry simulated [39], [40] with the supply voltage scaled down to 0.3 V. Other parameters (summarized in [27]) are specific to each device and come from the simulations of these devices (with methods ranging from drift-diffusion to quantum transport) performed by university groups participating in NRI and STARnet. The geometries of these devices are not necessarily the same as that of CMOS. For example, the gate length of tunneling FET (TFETs) is chosen to be longer than that of CMOS. We determine the capacitance of the gates from the common intrinsic gate capacitance and by using device-specific adjustment factors [27, Tables 1 and 5]

$$C_{\text{tot}} = C_g(M_{\text{cpar}} + M_{\text{cadj}}). \quad (9)$$

The contact resistance is accounted for by a simple rescaling [41]. The resistance of the ON-state of a transistor and the rescaled ON-current with contact resistance R_{cont} are

$$R_{\text{ON}} = V_{\text{dd}}/I_{\text{ON}}, \quad \tilde{I}_{\text{ON}} = I_{\text{ON}}/(1 + R_{\text{cont}}/R_{\text{ON}}). \quad (10)$$

Note that we denote the total current through the devices by I, while $\tilde{I}_{\text{ON}}$ is current per unit width. For spintronic devices, CMOS transistors are needed for controlling the power supply of current. They can operate with voltage bias between the source and the drain much smaller than 1 V. We approximate the resistance per unit width of a CMOS transistor in the linear portion of the $I-V$ characteristic by

$$R_L = (R_{\text{ON}} + R_{\text{cont}})/3. \quad (11)$$

The resistance of this CMOS transistor channel can be larger than the resistance of both the ferromagnetic to normal metal junction (with the resistance-area product, RA) and the short interconnect wires R_{wir}. Therefore, it is the power supply transistor (and its width w_X) that determines the current available for switching. For a magnet with area a_{mag}, the resistance of the total current path in current-driven spintronics devices is

$$R_{\text{stt}} = RA \cdot a_{\text{mag}} + R_{\text{wir}} + R_L w_X. \quad (12)$$

We also design the width of the transistors such that the second and third terms are approximately equal. We start with the minimum acceptable voltage for spintronic devices $V_{\text{dd}} = V_{\text{st}}$. If the resistance proves to be too high to ensure sufficient switching current I_{dev}, we choose a higher voltage to maintain the required current $V_{\text{dd}} = R_{\text{stt}}I_{\text{dev}}$.

V. AREA ESTIMATES

Consistent with the analysis in BCB 2.0, the layout pitch is $p_m = 4F$, where F is the metal-1 half-pitch [37]. We set $F = 15$ nm, corresponding to the 2018 node. We start with areas of simpler circuits and build up to estimates of more complicated circuits. For details, see [27].

VI. TREATMENT OF STANDBY POWER

One aspect missing in previous BCB 2.0 releases was the treatment of standby power. In logic circuits, standby power is dissipated due to leakage current in transistors which flows between the power and ground networks even when no input voltages are switched in circuits. In this leakage analysis of power, we leave the clocking circuit power out, though it too can contribute to standby power. In transistors there are two components of the leakage current in the OFF state: current from source to drain and leakage current through the gate dielectric. They are quantified by the drain current (per unit width) in the OFF state I_{OFF} and by the gate leakage per unit area, J_g, respectively. Therefore, the two components are

$$S_{\text{sd}} = I_{\text{OFF}}V_{\text{dd}}w_X, \quad S_g = J_g L_{\text{ch}} w_X V_{\text{dd}}. \quad (13)$$

The situation becomes more complex in the context of a circuit, in which various voltages are applied to the terminals of transistors and thus, they can be in ON or OFF states.

In an inverter [Fig. 2(a)] depending on the input, one transistor is in a low-resistance, R_L, ON state, while the other is in a high-resistance, R_H, OFF state. The voltage drop is insignificant across the ON transistor, and thus, the overall leakage current is limited by the high-resistance
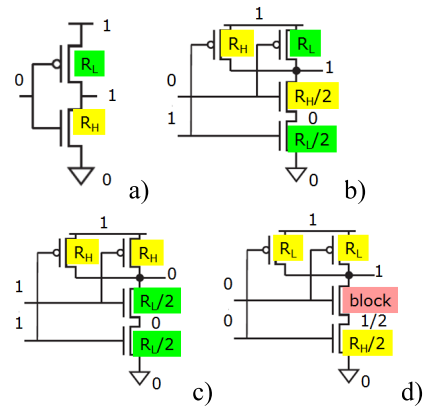

FIGURE 2. Schemes of an inverter (a) and a NAND gate with various inputs (b)–(d). Resistances of the transistors are shown for the purposes of standby power calculation: R_L = low resistance in the ON state, R_H = high resistance in the OFF state, and 'block' = extremely high resistance due to this transistor's negative gate-source bias.

OFF transistor. The standby power for the inverter is the same as for a single transistor and is given by the sum of the two leakage components

$$S_{int} = S_{sd} + S_g. \tag{14}$$

In multi-input gates, like the NAND in Fig. 2(b)–(d), nFET transistors in the pull-down network have larger widths to compensate for their resistance being in series. The ON and OFF states are determined by combinations of the input conditions. The overall standby power needs to be weighted by the probabilities of these input conditions. For example, the input combinations in Fig. 2(c) and (d) have a probability of 0.25. The input combination in Fig. 2(b) and the equivalent one with inputs exchanged have together a probability of 0.5. Standby powers in the cases shown in Figs. 2(b) and (c) are equal to $2S_{int}$. The combination shown in Fig. 2(b) is a special case. One of the transistors (designated as block) is in a state of negative gate-to-source bias (this is due to the so-called stacking effect [42]) and thus has an even higher resistance OFF state that effectively blocks any leakage current. The standby power in this case is much smaller than with the other input combinations. Instead of analytically summing standby powers for the above combinations, we obtained the adjustment factors from circuit simulations. For CMOS and other non-tunneling transistors, these factors [43] are listed in Table 3. For tunneling transistors, the stacking effect proves to be even more pronounced and the factors are different.

TABLE 3. Circuit parameters.

PARAMETER	SYMBOL	VALUE
Standby factor for 2-input NAND	M_{Snand2}	1.625
Standby factor for 3-input NAND	M_{Snand3}	0.897
Standby factor for 4-input NAND	M_{Snand4}	0.625
Standby factor for tunneling 2-input NAND	M_{Snand2}	1.535
Standby factor for tunneling 3-input NAND	M_{Snand3}	0.837
Standby factor for tunneling 4-input NAND	M_{Snand4}	0.6
Inverter delay factor	M_{tinv}	0.9
Inverter energy factor	M_{Einv}	1.4
NAND delay factor	M_{tnand}	2
NAND energy factor	M_{Enand}	2

Nanomagnets in spintronic circuits are nonvolatile. In the time intervals when they do not need to be switched, power can be turned OFF and thus, no current is flowing through the nanomagnets; the nanomagnets would also still retain their states. So spintronic circuits can in theory have zero standby power. In reality, standby power is dominated by the current driving transistors. Even if the gate voltage is set such that driving transistors do not transmit any current, there will be leakage current. We assume that for current-driven circuits, standby power is equal to S_{int} per nanomagnet. It is slightly different for voltage-driven circuits. Their current does not

flow to the ground, but instead it charges a capacitor with negligible leakage. We assume that only the gate leakage part remains for these circuits.

VII. ESTIMATES FOR TRANSISTOR CIRCUITS

We start with simple combinational logic gates: inverters with fan-out of one or four, NANDs with two, three, and four inputs. Then they are used as building blocks for more complicated circuits. In BCB 3.0 we add sequential logic—a state element and a register bit. Most TCs have the complementary transistor implementation [28]. We make the approximation for the ON-current of pFET to be equal to that of nFET. In multi-input gates, transistors in the pull-up and pull-down networks are sized to have the same ON-current. The estimates for switching delay and energy of simple circuits are proportional to those for intrinsic elements, t_{int}, E_{int}, which are given by (1)–(8) for specific switching mechanisms. In a more complicated circuit, a stage is driven by the previous stage and drives the next stage. First we estimate the delay and energy of circuits being driven by a minimum-size inverter. For an inverter driving an inverter with fan-out (FO)

$$t_{inv}(FO) = (FO + 1) \cdot M_{tinv}t_{int} + L_{inv}t_{ic} \tag{15}$$
$$E_{inv}(FO) = FO \cdot (M_{Einv}E_{int} + L_{inv}E_{ic})$$
$$S_{inv}(FO) = FO \cdot S_{int} \tag{16}$$

see (14) and (31)–(36) [27] for symbols used. For an inverter driving an input of a NAND gate with number of inputs (NI)

$$t_{NAND}(NI) = NI \cdot M_{tNAND}t_{int} + L_{NAND}t_{ic} \tag{17}$$
$$E_{NAND}(NI) = NI \cdot M_{ENAND}E_{int} + L_{NAND}E_{ic} \tag{18}$$
$$S_{NAND}(NI) = M_{SNAND,NI}S_{int}. \tag{19}$$

The empirical factors were chosen to approximately match the results of SPICE simulation with Arizona compact predictive technology models [44], [45] of a 10-nm-high-performance FinFET transistor. This is a change from BCB 2.0, where the PETE circuit simulator [46] was used is missing. The factors are in order-of-magnitude agreement with analytical equations [28]. The numerical values for these constants are in Table 3. We assume the estimates for NOR to be the same as for NAND. Then more complicated circuits are built up from these simple parts. We adopt a straightforward approach—summing delays of all parts on the critical path and summing energies of all parts in the circuit as shown by diagrams in [27]. For an exclusive or (XOR), 1:4 mux and 4:1 demux

$$t_{XOR} = 3t_{NAND2} + L_{XOR}t_{ic} \tag{20}$$
$$E_{XOR} = 4E_{NAND2} + L_{XOR}E_{ic}, \quad S_{XOR} = 4S_{NAND2} \tag{21}$$
$$t_{mux} = t_{NAND4} + t_{NAND3} + t_{inv1} + L_{mux}t_{ic} \tag{22}$$
$$E_{mux} = E_{NAND4} + 4E_{NAND3} + 2E_{inv1} + L_{mux}E_{ic} \tag{23}$$
$$S_{mux} = S_{NAND4} + 4S_{NAND3} + 2S_{inv1} \tag{24}$$
$$t_{dem} = t_{NAND3} + t_{inv1} + L_{dem}t_{ic} \tag{25}$$
$$E_{dem} = 4E_{NAND3} + 2E_{inv1} + 4L_{dem}E_{ic} \tag{26}$$
$$S_{dem} = 4S_{NAND3} + 2S_{inv1}. \tag{27}$$

For the sequential circuits, a memory cell and a state element are treated similarly. With non-TFETs and the 6T-SRAM cell (assuming that access transistors do not contribute to standby power)

$$t_{rb} = 2t_{inv1} + L_{ram}t_{ic} \tag{28}$$

$$E_{rb} = 3E_{inv1} + 2L_{ram}E_{ic}, \quad S_{rb} = 2S_{inv1}. \tag{29}$$

With TFETs and the 8T-SRAM cell, additional transistors contribute to the switching energy and leakage, but do not slow down writing of the cell

$$t_{rb} = 2t_{inv1} + L_{ram}t_{ic} \tag{30}$$

$$E_{rb} = 4E_{inv1} + 2L_{ram}E_{ic}, \quad S_{rb} = 3S_{inv1}. \tag{31}$$

For the state element (gated D-latch) (see [27] for schematics)

$$t_{se} = 2t_{inv1} + 3t_{nan2} + L_{se}t_{ic} \tag{32}$$

$$E_{se} = 3E_{inv1} + 4E_{nan2} + 2L_{ram}E_{ic}, \quad S_{ram} = 3S_{inv1} + 4S_{nan2}. \tag{33}$$

For the 1-bit full adder, using the activity factors from [46]

$$t_{add1} = 3t_{XOR}/2 + 5t_{nan2}/2 + L_{add1}t_{ic} \tag{34}$$

$$E_{add1} = 7E_{XOR}/8 + 351E_{nan2}/512 + 2L_{add1}E_{ic} \tag{35}$$

$$S_{add1} = 2S_{XOR} + 3S_{nan2}. \tag{36}$$

We use the most straightforward circuit implementation for an adder—the ripple carry adder. In FETs, all delays and energies are just multiplied by the number of bits. This implies that every bit dissipates energy only when the carry bit propagates and it is switched. A special case is that for BisFET and ITFET. They belong to negative differential resistance (NDR) logic [47]. This logic needs to be clocked on every cycle, regardless of whether a certain gate is switched or not. This suggests an additional factor of 32 in energy. Here the distinction between the active and standby power is blurred: both are dissipated on every clock cycle. Due to their dynamic nature, such circuits are somewhat reminiscent of dynamic logic [28]. The need to clock NDR logic in order to operate the gate probably makes register files (RFs) impossible to implement with them.

VIII. ESTIMATES FOR MAJORITY GATE CIRCUITS
As stated before, most of spintronic circuits are MGC. They are also mostly nonvolatile. Therefore, every node potentially has the functionality of a latch. An inverter is actually simpler than a majority gate and requires just one intrinsic element—a nanomagnet [27]

$$t_{inv1} = t_{int} + L_{inv1}t_{ic}, \quad E_{inv1} = E_{int} + L_{inv1}E_{ic}, \quad S_{inv1} = S_{int}. \tag{37}$$

The register bit and the state element are equivalent to an inverter, i.e., they contain just an output and an input magnet

$$t_{rb} = t_{se} = t_{inv1}, \quad E_{rb} = E_{se} = E_{inv1}, \quad S_{rb} = S_{se} = S_{inv1}. \tag{38}$$

An inverter with a fan-out of two can be implemented with just one majority gate with one input and three outputs; thus, all its characteristics are the same as those for two-input NAND (below). A fan-out of four required two such MGs cascaded and four output nanomagnets driving the next stages of the circuits

$$t_{inv4} = 2t_{int} + L_{inv4}t_{ic} \tag{39}$$

$$E_{inv4} = 5E_{int} + 4L_{inv4}E_{ic}, \quad S_{inv4} = 5S_{int}. \tag{40}$$

Two input NAND or NOR gates are obtained by fixing one of the inputs of a three-input majority gate to 1 or 0, respectively. Three or four input gates require more majority gates

$$t_{NAND}(NI) = (NI - 1)t_{int} + L_{nan}t_{ic} \tag{41}$$

$$E_{NAND}(NI) = (3NI + 1)E_{int} + L_{nan}E_{ic}$$

$$S_{nan}(NI) = (3NI + 1)S_{int}. \tag{42}$$

For the exclusive OR [27]

$$t_{XOR} = 2t_{NAND2} + t_{inv1} + L_{XOR}t_{ic} \tag{43}$$

$$E_{XOR} = 3E_{NAND2} + 2E_{inv1} + L_{XOR}E_{ic}$$

$$S_{XOR} = 3S_{NAND2} + 2S_{inv1}. \tag{44}$$

Here a majority gate is equivalent to a 2-input NAND. For 1:4 mux and demux

$$t_{mux} = 4t_{NAND2} + 2t_{inv2} + L_{mux}t_{ic} \tag{45}$$

$$E_{mux} = 9E_{NAND2} + 3E_{inv2} + L_{mux}E_{ic}$$

$$S_{mux} = 9S_{nan2} + 3S_{inv2} \tag{46}$$

$$t_{dem} = 2t_{NAND2} + t_{inv2} + L_{dem}t_{ic} \tag{47}$$

$$E_{dem} = 8E_{NAND2} + 2E_{inv2} + 4L_{dem}E_{ic}$$

$$S_{dem} = 8S_{NAND2} + 2S_{inv2}. \tag{48}$$

The one-bit full adder is defined by the number of majority gates: i.e., total M_{mg} on the critical path M_{cmg} [27, Table 3]

$$t_{add1} = M_{cmg}t_{NAND2} + L_{add1}t_{ic} \tag{49}$$

$$E_{add1} = M_{mg}E_{NAND2} + (M_{mg} - 1)E_{inv1} + 2L_{add1}E_{ic} \tag{50}$$

$$S_{add1} = M_{mg}S_{NAND2} + (M_{mg} - 1)S_{inv1}. \tag{51}$$

The adder is still a ripple-carry kind. The values are obtained by multiplying by the number of bits, in the present case, 32.

IX. ARITHMETIC LOGIC UNIT
With the circuits described above, one can construct an ALU, which is an example of a state machine, even a rudimentary processor. For the purposes of this estimate, we consider the structure and operation of the ALU shown in Figs. 3 and 4, which, at this level of description, are common to TC and MGC logic.

At the heart of an ALU is the block performing arithmetic operations (AOs): addition, subtraction, NAND, and NOR, as per Fig. 3. All of the operations are performed on two input 32-bit numbers A and B. NAND and NOR are done in parallel. Addition and subtraction require propagating the carry from one bit to another. Therefore, the delay of propagating the
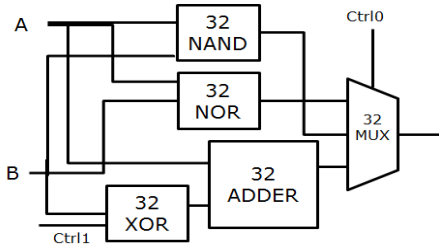
FIGURE 3. Scheme of the circuit block performing the AOs. Ctrl1 inputs enable the XOR blocks to choose between add or subtract operations. Ctrl0 inputs select the result of which AO is directed to the output. Lines represent 32-bit buses.
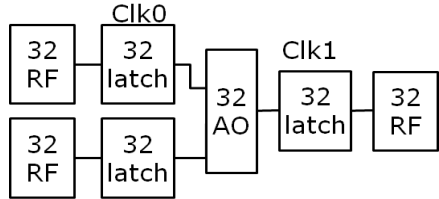

FIGURE 4. Scheme of the whole ALU. Latches are opened on the rising edge of the clocks: Clk0 and Clk1 are offset by half the clock cycle. All blocks contain 32 bits. AO = arithmetic operation unit as in Figure 3. RF = register files.

carry across the adder limits the operational delay of this block. This whole block is based on sequential logic and the operation function options are controlled by two signals Ctrl0 and Ctrl1. The delay, energy, and standby power for this block are

$$t_{ao} = t_{se} + t_{XOR} + t_{add32} + t_{mux} + L_{ao}t_{ic} \qquad (52)$$

$$E_{ao} = E_{add32} + 32(2E_{se} + E_{XOR} + E_{mux} + L_{ao}E_{ic}) \qquad (53)$$

$$S_{ao} = S_{add32} + 32(2S_{se} + S_{XOR} + S_{mux}). \qquad (54)$$

The entire ALU [Fig. 4] performs the following functions: it stores two 32-bit numbers in RFs, retrieves them and passes them to the AO block, receives the result from the AO block, sends it to the output, and writes the result into one of the RFs. Each of the RFs is a 1×32 array of memory cells. Clocking is required to transfer data between the memory and the AO block. We chose a two-phase clock with the signals Clk0 and Clk1 shifted by a half of the clock period relative to each other. On the rising edge of Clk0, the latches transmit the outputs of the RFs to the AO block. On the rising edge of Clk1, the output is transferred to one of the RFs. Simultaneously, on the falling edge of Clk0, the inputs to AO are isolated from the RFs.

On the falling edge of Clk1, the inputs to RFs are isolated from the outputs of AO. The AOs (addition is the limiting one) must fit into the half of the clock cycle between the rise of Clk0 and Clk1 signals. The ALU switches in one complete clock cycle, e.g., period of Clk0

$$t_{alu} = 2(t_{ao} + t_{se} + L_{alu}t_{ic}) \qquad (55)$$

$$E_{alu} = E_{ao} + 32(E_{se} + E_{rb} + L_{alu}E_{ic}) \qquad (56)$$

$$S_{alu} = S_{ao} + 32(S_{se} + S_{rb}). \qquad (57)$$

X. RESULTS AND DISCUSSION

Now we utilize the models described above to obtain the estimates of energy and delay for a selective set of benchmark circuits. The complete set of plots is shown in [27]. A good representation of the performance of combinational circuits is given by the adder (Fig. 5). Consistent with the previous BCB 2.0 release, we note that spintronic devices switch slower than electronic ones. Among these, spin transfer torque (current-driven) spintronic devices require higher energy to switch state. Magnetoelectric (voltage-driven) spintronic devices have lower energies, down by an order of magnitude lower compared with that of CMOS HP. The van der Waals FET is the only device slightly faster than CMOS HP; though a more thorough study may change this assessment. Multiple TFET devices have lower switching energy than CMOS HP, though they switch slower. They still have $2\times$ to $6\times$ lower energy-delay products than CMOS HP. Ferroelectric transistors (such as FEFET and MITFET) are faster than the nonvolatile options—spintronic devices. These qualitative relations remain the same for a sequential logic circuit, such as 32-bit ALU (Fig. 6).
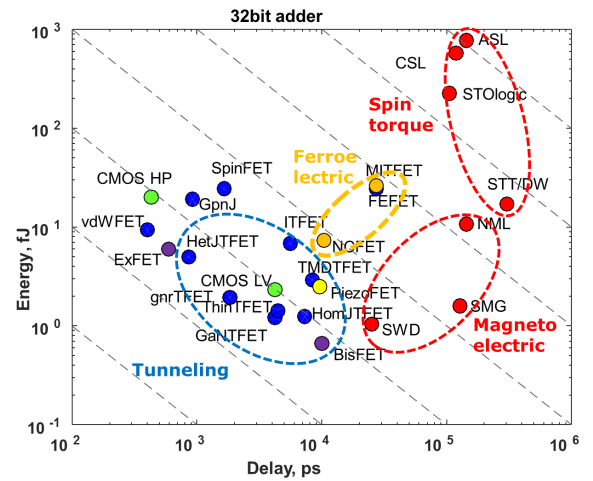

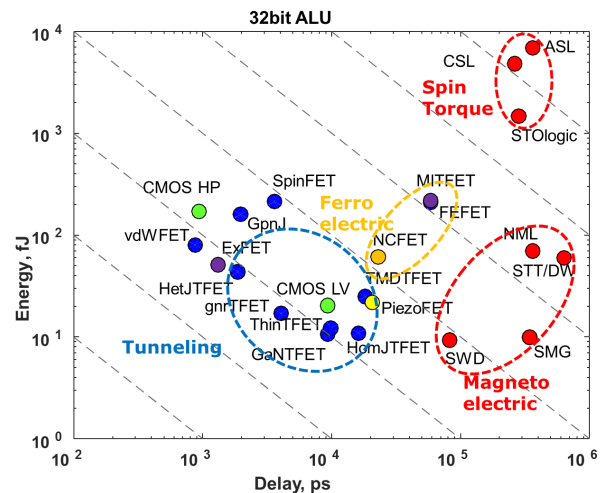**FIGURE 5. Switching energy versus delay of a 32-bit adder.**

FIGURE 6. Switching energy versus delay of a 32-bit ALU.

When we look at active and standby power in Fig. 7, we notice that spintronic devices have lower standby power, especially the magnetoelectric ones. Magnetoelectric devices also have a significantly lower active power. Electronic devices, in general, have both higher active and higher standby power. Among them, TFETs have standby power in the range between nontunneling electronic and spintronic devices. TFETs also have active power between CMOS HP and magnetoelectric devices. We also show the metric introduced in BCB 2.0—computational throughput with capped power (Fig. 8). Under constraints of dissipated power density, CMOS HP cannot achieve its maximal throughput. Other devices, vdWFET, ExFET, and HetJFET, have better energy efficiency and are projected to exceed CMOS in throughput. TFETs enable relatively high throughput with even lower power. Magnetoelectric devices have about an order of magnitude lower throughput than CMOS HP, which is counterbalanced by smaller power dissipation. Ferroelectric devices are predicted to have comparable throughput. Spin torque devices are limited by power dissipation and have low throughput.
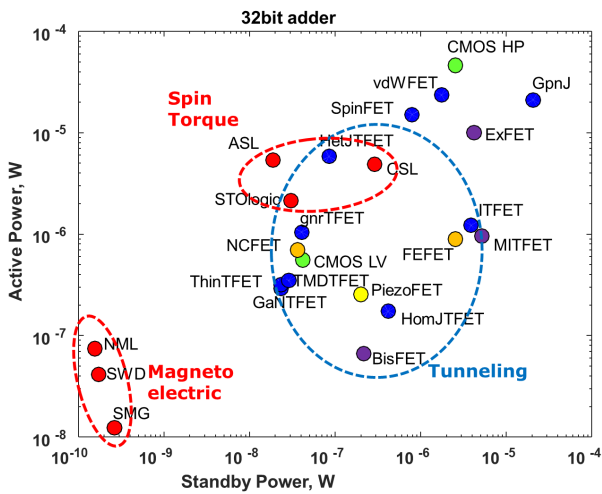
XI. CONCLUSION

A benchmarking methodology has been introduced to compare beyond-CMOS devices which rely on new computational variables with new principles for transduction. A better understanding of electronic power supplies even for non-electronic devices in circuits is laid out. We treated a wide set of benchmarking circuits, including sequential logic and an ALU. We introduced estimates for standby power, which is an extremely important metric, especially for mobile and wearable devices. Ferroelectrics were identified as a promising class of nonvolatile devices, but they have their own switching speed limitation. With our latest, more sophisticated treatment of circuits, we find that interconnects dominate switching energy and delay. Spintronics was found to have simplicity and size advantages for some circuits such as the Register bit-cell, and the state element. Spintronic circuits have a much lower standby power (if they are clocked). With all of the above, we provide an approach for researchers to better focus on promising beyond-CMOS devices and to seek methods of improving their power versus performance.

FIGURE 7. Active power versus standby power of a 32-bit adder.
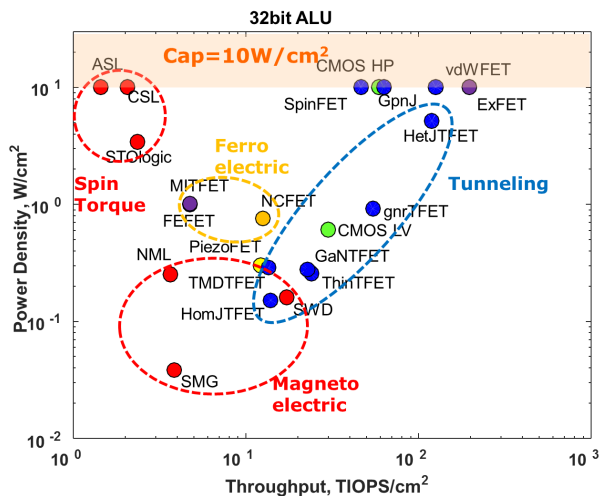
FIGURE 8. Dissipated power versus computational throughput (capped at 10 W/cm^2) related to a 32-bit ALU.

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