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3-D Logic Circuit Design-Oriented Electrothermal Modeling of Vertical Junctionless Nanowire FETs

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ABSTRACT This work presents new insights into 3-D logic circuit design with vertical junctionless nanowire FETs (VNWFET) accounting for underlying electrothermal phenomena. Aided by the understanding of the nanoscale heat transport in VNWFETs through multiphysics simulations, the SPICE-compatible compact model captures temperature and trapping effects principally through a shift of the device threshold voltage. Circuit-level simulations indicate a strong impact of temperature variation on functionality and figures of merits, such as energy-delay products. Subsequent guidelines for design considerations are discussed that are intended to provide feedback for technology improvements.

INDEX TERMS 3-D electronics, compact model, electrothermal modeling, logic circuit design, vertical nanowire (NW) transistor.

I. INTRODUCTION

In the era of emerging computing paradigms and artificial neural networks, hardware and functionality requirements are in the surge. With the deployment of large numbers of sensors and smart devices to form the edge of the Internet of Things to the scale of 50 billion and rising, data are now being generated at the edge rather than in the large-scale data centers that form the cloud. Current estimates put the ratio of data generation at the edge at over 40× that of global data center traffic, today around some 20 ZB. The pure cloud computing model cannot handle this massively distributed, yottabyte (YB)-scale quantity of data—the network infrastructure resources simply do not have the capacity to move the data from the edge to the cloud, the data are vulnerable to attacks, and the transmission delay is prohibitively high. In advanced applications where delay requirements are particularly stringent (e.g., 1 ms in cooperative autonomous driving), the cloud computing model cannot consistently meet the deadlines.

The limits of the cloud computing model have given rise to the emergence of edge computing, where computing tasks are performed as close as possible to data sources to meet the low power and latency criteria [1]. However, resources are constrained at the edge in terms of available computational power, memory capacity, and most importantly energy. Hardware is critical at this level, and there is a clear need to explore the suitability of breakthrough emerging technologies to meet the energy-efficiency, performance, and compactness requirements of edge computing hardware as alternatives to traditional von Neumann machines. International Roadmap for Devices and Systems (IRDS) identifies gate-all-around (GAA) nanowire field-effect transistors (NWFETs) as a future mainstream solution [1], both in lateral and vertical configurations—however, the challenge is to extrapolate analyses beyond the device level to quantify relevant performance metrics [2], [3].

In particular, junctionless vertical NWFETs (VNWFETs), capable of addressing existing process challenges, such as

downscaling, short-channel effects, compactness, and electrostatic control, are difficult to meaningfully compare to existing mainstream technologies due to the additional vertical dimension and opportunities for innovative 3-D logic design [4]. A critical specific issue in this evaluation lies in the correct evaluation of the electrothermal behavior of the device [5]. Indeed, the electrical performances of aggressively scaled transistors are strongly impacted by self-heating, ultrafast thermal transport, and thermal conductivity degradation, all of which link to electron–phonon coupling which is not well understood at the nanoscale. The integration of this technology in the mainstream design flow is thus not straightforward and requires design technology co-optimization (DTCO) at an early stage [6], [7]. This article is an important step to achieve this goal.

In this article, we propose a compact model to enable multiphysics evaluation of intrinsic transistors, considering electrothermal and trapping effects investigated through multiphysics simulations based on non-Fourier heat flow [8]. From the theoretical understanding of these effects in junctionless devices, the proposed compact model [9] captures temperature-induced increase in drain current through temperature dependence of model parameters, including threshold voltage, drain–source Schottky barrier height, and series access resistances. The proposed model also incorporates two additional subcircuits for dynamic self-heating and trapping phenomena for the evaluation of these effects at circuit level. We then project device performance to circuit level by using this compact model to characterize four basic 3-D logic cells (INV, NAND, NOR, and XOR) based on vertical nanowire (NW) transistors in terms of delay and energy consumption, thus proving that this emerging technology can be used as the basic building block for logic gates.

This article is organized as follows. Section II first describes the physical basis and implementation of the compact model [based on the experimental measurements of the devices under test (DUT)]. Section III subsequently describes the logic cells and our characterization methodology in terms of delay and energy consumption and with varying temperature. Section IV discusses the results and perspectives and summarizes possible future work.

II. TRANSISTOR: COMPACT AND NUMERICAL MODELING

A. MULTIPHYSICS MODELING OF INTRINSIC TRANSISTORS

To accurately capture the underlying physics of junctionless FETs, the compact model presented in this work has been specifically developed based on the understanding of carrier transport studied using numerical multiphysics and TCAD simulations. Junctionless FETs offer a much and simpler fabrication process in comparison with classical MOSFETs [10], making them compatible for pursuing scaling beyond the sub 20-nm nodes. Most importantly, along with the absence of metallurgical junctions in these devices, they are heavily doped and the NW diameters are tailored to be quite thin in order to maintain gate electrostatic control over the channel. In order to ensure design compatibility between the junctionless VNWFET technology [10] and associated circuit simulations, the transistor compact model developed based on charge transport in gate-all-around junctionless transistors [9] is used first to calibrate the model parameters against the experimental data of a wide range of transistor geometries (22- and 34-nm NW diameter with 16–81 NWs in parallel) at room temperature.

Key physical parameters include doping, gate work function, mobility, drain–source Schottky barrier, and threshold voltage. Once a good accordance between the model and the data is obtained, the compact model is then modified to take into account electrothermal and trapping effects, two critical issues in nanoscale junctionless transistors that can potentially impact dynamic circuit performance. To do so, we leveraged on-wafer dc measurements over a wide temperature range (15 °C–100 °C) and pulsed conditions with varying pulse widths (1 μs–10 ms) to dissociate temperature and trap-induced effects. From the experimental observations, it could be understood that increasing the temperature leads to a monotonically increasing drain current conforming to prior observations in junctionless transistors [11]. This is explained by the strong temperature dependence of the threshold voltage in junctionless devices that leads to an increase in drain current along with a degradation of the on–off current ratio. This effect is further pronounced by the weak temperature dependence of the mobility due to competing lattice and impurity scattering mechanisms [11]. From the pulsed I–V measurements, it could similarly be observed that the drain current showed a continuous increase with increasing gate pulsewidth, allowing for an increasing number of traps to activate, while the device temperature increases simultaneously. For very large pulses, the transistor current saturated to the measured dc current. This phenomenon can also be considered to impact the threshold voltage as confirmed by the V_{TH}-shift with pulsewidth. This further affirmed that the threshold voltage in junctionless transistors is an important parameter to model both electrothermal and trapping effects. In the following, Section II-A.1 details in-depth physical understanding of these effects obtained through multiphysics simulations, whereas in Section II-A.2 the compact modeling approach is presented.

1) ELECTROTHERMAL AND TRAPPING EFFECTS

Thermal management is one of the most challenging design criteria in nanoscale transistors owing to a lack of understanding of the heat conduction governed by phonon transport in sub-10-nm devices that include: 1) ballistic; 2) boundary scattering; and 3) confinement regimes [12]. Junctionless transistors are fabricated with a very thin channel along with a chosen gate work-function to ensure that the transistors switch to off state at zero gate bias, switching to full depletion mode. In addition, the NWs are required to be strongly doped to ensure a higher drive current in order to compensate for the Schottky barriers at the source and drain sides. Phonons

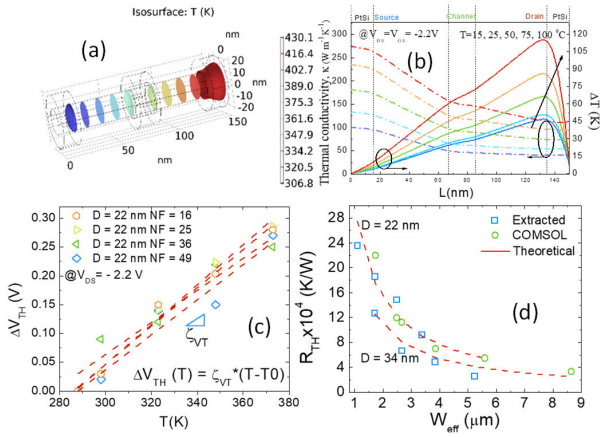

FIGURE 1. Electrothermal simulations using COMSOL. (a) Temperature contours along the NW. (b) Temperature and thermal conductivity at different measurement temperatures. Extracted (c) temperature dependence of the threshold voltage and (d) thermal resistance of the VNWFETs.

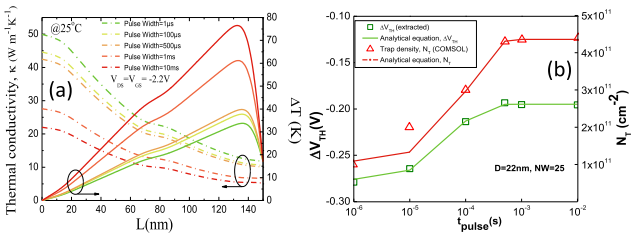

FIGURE 2. Electrothermal simulations using COMSOL. (a) Temperature and thermal conductivity distribution inside the NW obtained at room temperature under different pulse conditions along the NW. (b) Extracted threshold voltage (measurement) and trap density (COMSOL) showing similar dependence on the pulsewidth.

can be considered as a quasiparticle originating due to lattice vibration and can be confined in the Si/SiO_2 interface similar to trapping, leading to a reduction of the thermal conductivity. In addition, due to electron–phonon coupling and phonon confinement, carriers (electron or hole) can be trapped in the lattice distortion leading to the well-known self-trapped electron phenomena [13]. Moreover, in the nanoscale regime, explaining ultrafast heat flow using the classical hydrodynamic formalism based on Fourier's law no longer remains valid. The Guyer and Krumhansl equation (GKE) has recently been demonstrated to capture nondiffusive heat transport in the nanoscale regime beyond classical Fourier's law, offering understanding of nonlocal thermal effects [14].

To understand the electron–phonon coupling behind the electrothermal behavior and trapping effects for nonequilibrium states in both steady and transient conditions in junctionless transistors, we leveraged finite element method (FEM)-based COMSOL multiphysics simulations [15] based on the GKE formulation by solving the non-Fourier heat equation coupled with the drift-diffusion model and interface trapping effects. The material parameters are included in the simulator physics library, whereas the operating conditions and device geometries are defined according to our experimental setups. The governing equation of the GKE for non-Fourier heat dissipation is written as [16]

$$q_x(r) = -\kappa \frac{dT}{dx} + l^2 \frac{d^2 q_x(r)}{dr^2} + l^2 \frac{1}{r} \frac{dq_x(r)}{dr} \tag{1}$$

where q is the heat flux, τ_R is the phonon relaxation time, κ is the thermal conductivity, l is the phonon MFP, c is the heat capacity, and T is the temperature. To consider the electrothermal effect, we use the energy-conservation equation

$$c \frac{dT}{dt} + \nabla . q_x(r) = P \tag{2}$$

where P is the dissipated power defined as $P = V_{DS} I_D$.

The multiphysics simulations reveal that the temperature distribution inside the NW exhibits a steady increase of internal device temperature along the channel [Fig. 1(a)], reaching the peak near the drain [Fig. 1(b)], implying thermal confinement and self-heating at elevated temperatures and bias conditions. This is reflected by an equivalent degradation in thermal conductivity within the channel [Fig. 1(b)]. As highlighted in the previous section, the temperature variation induces a linear threshold voltage shift, which can be extracted from experimental results [Fig. 1(c)]. In addition, the thermal resistances (R_{TH}) of the VNWFETs have been extracted from both measurements and Multiphysics simulations [17], which exhibit an inverse geometry dependence [Fig. 1(d)].

Similarly, under pulse conditions, we studied the thermal conductivity and temperature rise using COMSOL for various pulsewidths that also indicated an increase of the device temperature (along with an equivalent reduction of thermal conductivity) due to phonon accumulation near the drain region at high bias conditions and larger pulse widths [Fig. 2(a)]. The numerical model was then used to extract the trap densities [Fig. 2(b)] that were compared with the V_{TH} variation for different pulse widths, which revealed a clear trend in both cases: the V_{TH} drift observed from the measurements could be described by a similar relation that also governs trap density, $N_T = N_{SS}(1 - \exp(-t_{pulse}/\tau))$. This led us to define the following physical relation for trap-induced V_{TH} shift in our model: $\Delta V_{TH} = \alpha q N_T / C_{ox}$, where α is a constant, q is the electronic charge, and C_{OX} is the gate oxide capacitance. Fig. 3(a) and (b) shows the multiphysics simulation results depicting good agreement with experimental I–V characteristics.

2) COMPACT MODEL IMPLEMENTATION

Following the multiphysics simulations, it could be confirmed that in the junctionless NWs, thermal conductivity reduces significantly with temperature, thus creating temperature hot spots and leading to possible device self-heating. Moreover, the trap density evolves exponentially with applied gate pulsewidth saturating to the dc value, where internal device temperature rises significantly coupled with the presence of traps. To translate these effects for compact modeling, we modify the expression of the threshold voltage to capture the effect of internal device temperature increase and

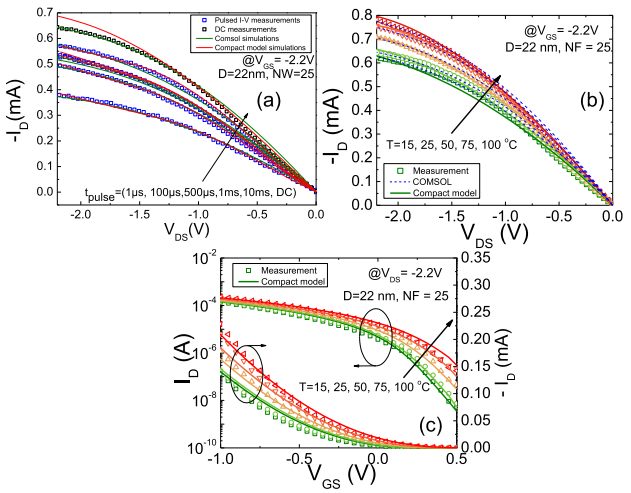

FIGURE 3. Evolution of drain current with (a) different pulse widths and (b) and (c) measurement temperatures comparing experimental results, multiphysics, and compact model simulations for a p-VNWFET with 25 parallel NWs of 22 nm diameter.

trap density fluctuation. To do so, we leverage the equation $\Delta V_{\mathrm{TH}} = \Delta V_{\mathrm{TH}}(T) + \Delta V_{\mathrm{TH}}(N_T)$, where the first term captures a linear temperature dependence through a temperature coefficient, whereas the second term incorporates a trap density-like dynamic exponential formulation activated through a flag parameter, with both parameters extracted from the experimental results. In addition, an equivalent electrical subcircuit consisting of the thermal resistance and capacitance (extracted from low-frequency S-parameter measurements) has been added to the compact model formulation in order to capture the dynamic variation of internal device temperature due to self-heating, which can also be activated through a flag parameter. Lastly, temperature coefficients of additional model parameters, such as the Schottky barrier height, series access resistances, intrinsic carrier concentration, and drain-induced barrier lowering, are also implemented in the model equations. Compact model simulation results are validated against the experimental data for both pulsed [Fig. 3(a)] and temperature [Fig. 3(b) and (c)] measurements.

B. ENHANCED DEVICES THROUGH THE INTEGRATION OF MATERIALS OR ARCHITECTURES

While junctionless VNWFETs already bring significant benefits to transistor performance, additional features can be naturally achieved. This section covers emerging characteristics of such functional enhancements from a prospective viewpoint.

1) FERRO GATE

Adding ferroelectric material to the VNWFET gate-stack [18] enables nonvolatile logic as well as nonvolatile reconfigurability. For example, a nonvolatile full adder [19] is able to store one of the summands in a nonvolatile manner, which is of particular interest in multiplication operations used in digital filters or convolutional neural networks, and where one

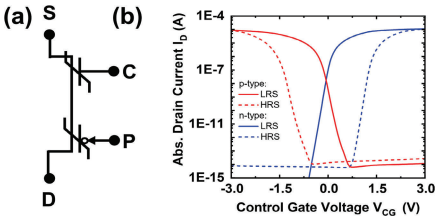

FIGURE 4. Polarity-controllable transistor with Fe gate. While PC-FETs require a constant input to program gates, Fe-gate oxides are programmed by a pulse, reducing the dynamic power consumption.

summand varies constantly (data), while the other one varies rarely (coefficients). Reconfigurable in-memory computing is enabled by the conjunction of ferroelectric VNWFETs with classical lookup table (LUT) circuit structures, such as an LUT2 [20] and where the output depends both on the select inputs (S_0 and S_1) as well as on the stored states (here four states stored in a nonvolatile manner to reflect a two-input truth table), i.e., $Y = A.\bar{S_1}.\bar{S_0} + B.\bar{S_1}.S_0 + C.S_1.\bar{S_0} + D.S_1.S_0$.

2) RECONFIGURABLE FETs

Polarity-controllable transistors (PC-FETs) leverage a multitude of input gates on a single ambipolar channel, to dynamically select both conduction state, as well as carrier type (Fig. 4) [21]. PC-FETs connected to a common body enable inherent X-to-1 multiplexing in a single transistor with X independent drain contacts. Nonvolatile PC-FETs in a 3-D tile also intimately incorporate multibit memory capability within computing elements, thus opening the way for a new concept for computing-in-memory.

C. TOWARD DYNAMIC MODELING

Another design perspective for improved dynamic performance of the logic cells includes optimized test structures. To ensure circuit design involving a 3-D emerging technology, accurate compact models capturing the static and dynamic device behavior are mandatory [7], but on-wafer test structures of such devices also include parasitic elements induced by pads and interconnects that are necessary to probe the DUT. Due to the 3-D nature of interconnects, standard methods to remove these parasitic contributions (de-embedding) become inaccurate owing to the fact that the classical design of passive test structures (open and short) no longer remains sufficient to completely model the extrinsic 3-D parasitic network. Fig. 5 shows the respective sizes of the DUT and its associated test structure illustrating the requirement to reinvent dedicated de-embedding methods for the 3-D VNWFET technology. In [22], a new de-embedding method for this technology was introduced that makes use of electromagnetic (EM) simulations to virtually reconstruct the entire parasitic network, including coupling capacitive, inductive, and resistive parasitic elements.

The values of all these parasitic elements constituting the small-signal equivalent circuit (SSEC) were calculated through: 1) analytical equations from the physical dimensions; 2) the material properties of the device; 3) the standard

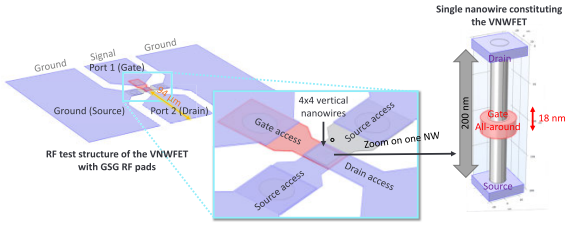

FIGURE 5. Schematic depicting the size of the test structure featuring ground–signal–ground (GSG) pads allowing the use of the RF probe with regard to the size of one single NW featuring the channel of the VNWFET.

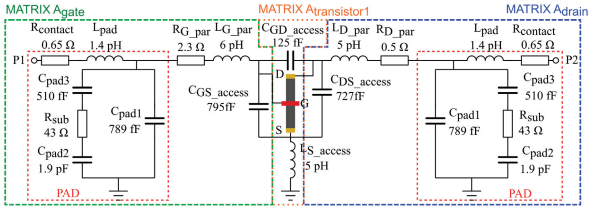

FIGURE 6. Complete SSEC of the passive elements associated with the VNWFET test structure.

calibration techniques, such as short-open-load-thru (SOLT); and 4) from EM simulations. The overall SSEC is shown in Fig. 6 along with the values of the parasitic elements. At this stage, this SSEC can be used to generate the ABCD matrices of the gate and drain parasitic access contributions for successful de-embedding of the intrinsic S-parameter measurements [17], [22]. This allows us to extract the intrinsic transistor S-parameters for device modeling and subsequently continues toward 3-D logic cell design.

III. STANDARD LOGIC CELL MODELING

In this section, we leverage the developed compact model to assess the performance metrics of various 3-D logic cell circuit topologies in the VNWFET technology. The ultimate goal of this study is to enable logic synthesis, which needs a library of characterized basic logic cells as a prerequisite.

A. ENERGY-DELAY CHARACTERIZATION OF STANDARD LOGIC CELLS

The goal of the following simulation-based exploration is to study the impact of using a large range of NWs per transistor on typical static and dynamic logic performance metrics, for several standard logic cell topologies. In the simulation protocol, we assume that the gate capacitance behaves in the same way for both p- and n-type VNWFETs, and that the capacitive load on the output of each structure is equivalent to that of a single inverter of drive strength 1. Since the VNWFET gate capacitance is experimentally determined to be 20 aF per NW, and assuming that its evolution with NW number is linear, we deduce a capacitance contribution for INV1X1 as 160 aF.

In this context, we aimed to study the behavior of four main logic cells: INVX1, NAND2X1, NOR2X1, and XOR2X1. Fig. 7 depicts the transistor-level schematics of these Boolean gates, where the formalism OPnXk indicates the Boolean operation *OP*, the number of inputs n, and the number of outputs k of each gate.

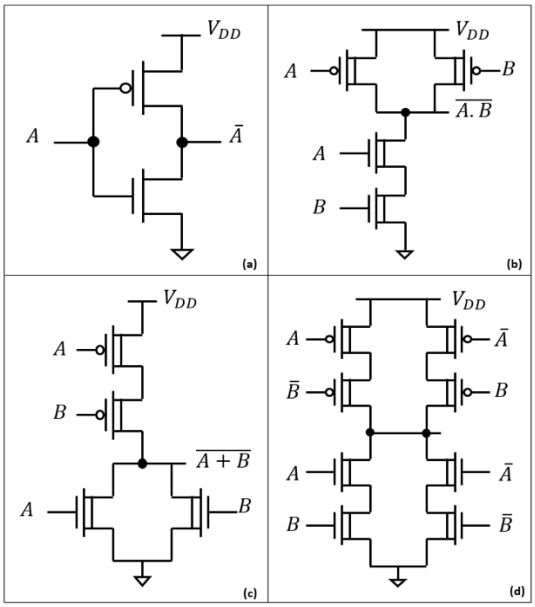

FIGURE 7. Schematics of logic cells studied. (a) INV1X1, (b) NAND2X1, (c) NOR2X1, and (d) XOR2X1.

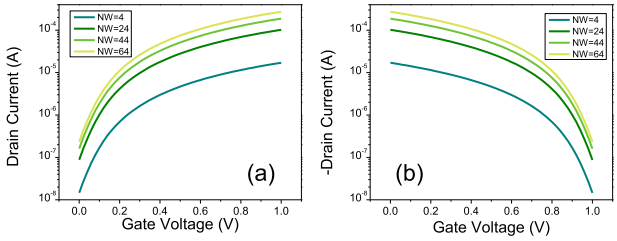

FIGURE 8. Variation of drain–source current I_{DS} with gate–source voltage V_{GS} and number of NWs per VNWFET NW of (a) n-type VNWFET and (b) p-type VNWFET.

The first step was to prove the ability of implementing such cells based on the VNWFET technology. In this context, we carried out simulations using the HSpice[1] commercial simulator, where we used the compact model described in Section II implemented as an executable Verilog-A model for the VNWFET.

Both the gate physical length L_g and the NW diameter d_{nw} are parameters that are determined by the fabrication process. Throughout this work and based on experimental devices, the values of these parameters are set to $L_g = 18$ nm and $d_{\text{nw}} = 22$ nm, respectively. Based on this, as well as the definition of other fixed model parameters, we investigated the number of NWs for p-type and n-type transistors to be used, as the only design parameter remaining to enable the optimization of device and circuit performance. The first essential step in this work is to verify the functionality of the n-type and p-type VNWFET devices themselves through dc-sweep simulation in order to ensure that they have the expected $I_{\text{DS}}/V_{\text{GS}}$ characteristic behavior, as illustrated in Fig. 8.

Subsequent to this verification, we simulate an elementary inverter gate shown in Fig. 7(a) in order to determine the

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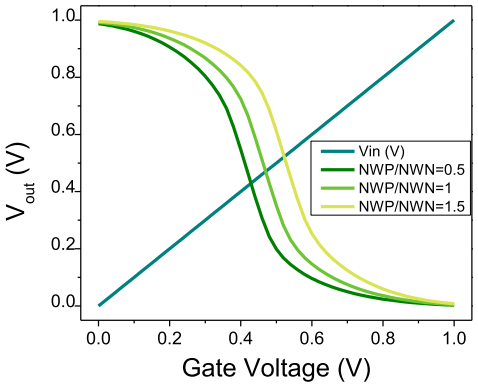

FIGURE 9. Variation of inverter output voltage as a function of the input voltage variation between 0 and V_{DD} (1 V) for different ratios between the number of NWs used for p-type and n-type transistors. It can be clearly seen that a ratio of 1 between NW of p-type and n-type devices achieves optimal midpoint voltage at half V_{DD}.

correct ratio between n-type and p-type NW (number of NWs per VNWFET) values to obtain an optimal midpoint voltage. In this work, we also chose a range of values of NW for n-type transistors that allows us to study the behavior of the device under different drive strengths. For each value, we run dc-sweep simulations while varying the gate voltage from 0 to V_{DD} and assessing the output behavior for varying numbers of NWs for the p-type device. We find that for all the defined NW values, a ratio of 1 between the number of NWs of p-type and n-type will give us an optimal midpoint voltage at half V_{DD}, as shown in Fig. 9, which leads to balanced noise margins and well-matched rise and fall times of the cell.

It is important of course to note that this ratio depends on the set of parameters used in the simulation. For this study, the chosen values for the number of NWs of the n-type device of the inverter were 4, 24, 44, and 64. The corresponding number of NWs for the p-type device is chosen according to the above described methodology. For the other cells, and in order to achieve drive strengths equivalent to that of the inverter, we redefine the number of NWs by doubling the number of NWs in the case of two series transistors.

After defining the sets of NW parameters, we identify the simulation limitations of the executable model and adjust our simulations accordingly. Then, a detailed study of the static and dynamic behavior of all cells was carried out, as detailed in the following subsections.

This study was done by varying the number of NWs used in each logic gate to study their behavior under different drive strengths. The simulations showed that using this technology, we can successfully implement logic NOT, NAND, NOR, and XOR functionalities, as shown in Fig. 10.

To characterize the library of standard logic cells, it is necessary to study the main conventional performance metrics of the targeted logic cells, i.e., propagation delay, rise/fall time, and dynamic power consumption where as follows.

1) The delay corresponds to the time difference between the output voltage and input voltage to reach half V_{DD}.

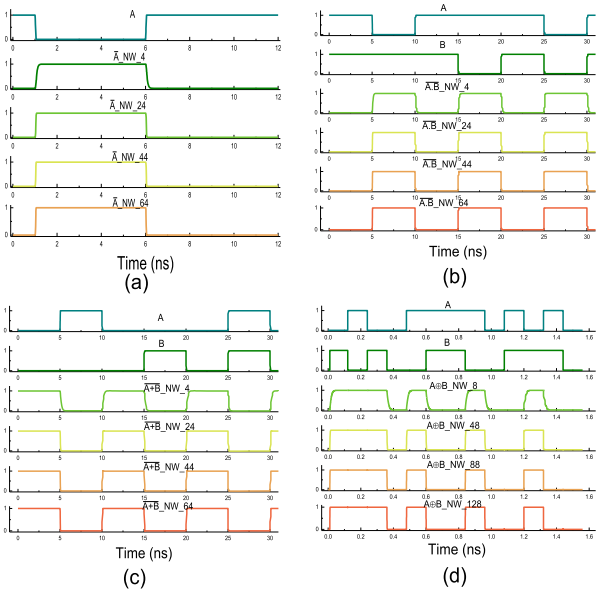

FIGURE 10. All possible output transitions in (a) inverter, (b) NAND, (c) NOR, and (d) XOR affected by input transitions.

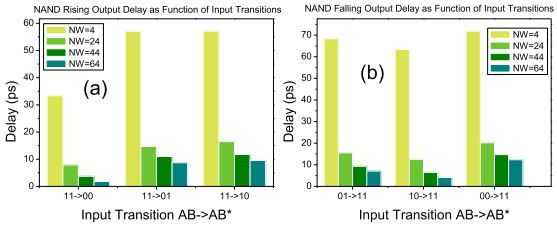

FIGURE 11. Delay in output (a) rising and (b) falling transitions of a NAND gate as affected by different input transitions.

2) Rise (resp. fall) time corresponds to the time needed by the output voltage to rise (resp. fall) from 0.1 V_{DD} (resp. 0.9 V_{DD}) to 0.9 V_{DD} (resp. 0.1 V_{DD}).
3) The dynamic power consumption for a particular transition is calculated by measuring the supply current during the output transition.
4) The leakage power is calculated by measuring the supply current during all static combinations of inputs.

For each cell, all the possible output transitions based on input(s) transitions are defined. Then, for each case, the timing and energy consumption are measured as described above.

Fig. 11 is a detailed example on how we studied the delay behavior of each logic cell. It is clear that the delay is dependent on the input(s) transitions, and that with the increases of NWs used per VNWFET, the delay will decrease. For all the cells under study we found, as expected, that with the increase in the number of NWs used, a decrease in delay (Fig. 12) and rise/fall times is observed as well as an increase in dynamic power consumption (Table 1).

B. PARASITIC-ANNOTATED ASSESSMENT

For devices with such small dimensions and compact footprint, circuit-level parasitics (in particular from coupling capacitance, metal contact, and layout-related issues) can

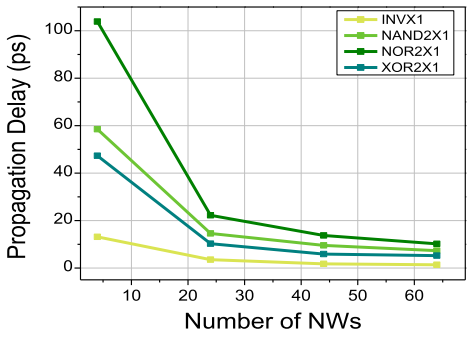

FIGURE 12. Average propagation delay of logic cells under study as a function of the number of NWs used per VNWFET device.

TABLE 1. Dynamic Energy Values (aJ) for the Logic Cells Under Study, for All Possible Input Transitions Leading to Output Rising or Falling Transitions and for Different Number of NWs.

			Nb of nanowires of nmos			
Logic Cell	Output Tran	Input AB	4.0	24.0	44.0	64.0
INV	↑	↓	171	395	645	880
	↓	↑	1.80	232	439	650
NAND	↑	↓1	1151	1374	1490	1736
		1↓	1152	1288	1554	1839
		↓↓	1151	1374	1490	1736
	↓	↑1	2.05	111	326	537
		1↑	2.90	133	385	658
		↑↑	2.05	111	326	537
NOR	↑	↓0	2119	2249	2463	2807
		0↓	2106	2147	2459	2658
		↓↓	2119	2249	2463	2807
	↓	↑0	2.23	82	308	591
		0↑	2.19	203	540	911
		↑↑	2.23	82	308	591
XOR	↑	↓1	742	1289	1934	2533
		↑0	736	1015	1241	1386
		1↓	761	1498	2368	2485
		0↑	750	1402	1235	1370
	↓	↑1	27.5	712	1781	1801
		↓0	66.6	271	495	667
		1↑	19.5	546	1169	1785
		0↓	17.7	244	484	672

significantly limit the benefit in design. In order to assess the impact of parasitics, we designed the layout for a two-input XOR gate (one of the more complex logic functions and including in-cell generation of complemented inputs), as shown in Fig. 13(a), and extracted the associated parasitic network based on the aforementioned geometrical parameters and material coefficients. Metal interconnect layers connect top and bottom NW contacts, as well as gate contacts surrounding the NWs to create GAA devices. Transient simulation results for the resulting parasitic-annotated 2-NW/transistor XOR2 cell are shown in Fig. 13(b). This enabled us to carry out a comparative study in order to quantify the impact of parasitic interconnect networks on key performance metrics. The full dataset is shown in Table 2 . Comparing delay and energy per transition figures, we quantify the average increase in delay as +4% and energy/transition as +19% when considering the parasitic interconnect network.

C. IMPACT OF ELECTROTHERMAL AND TRAPPING EFFECTS

In order to study the electrothermal and trapping effects on the behavior of VNWFET-based logic cells, we first set the

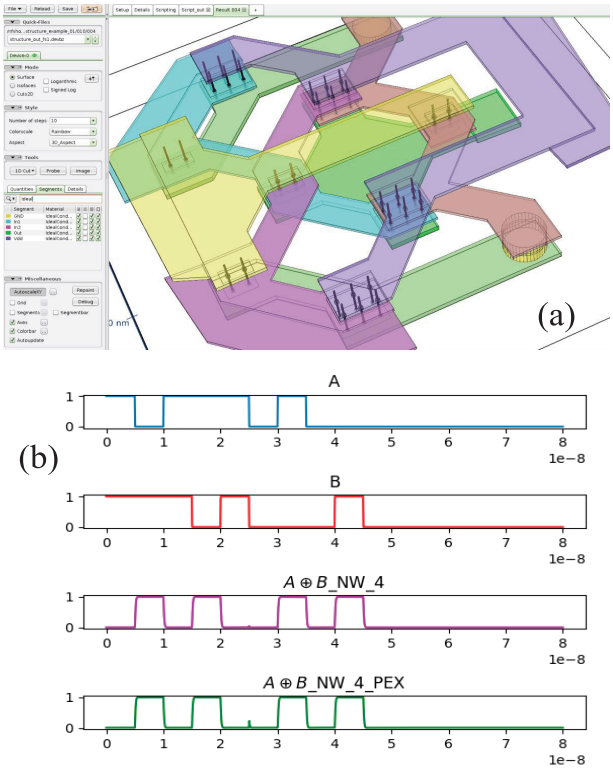

FIGURE 13. Two-input XOR logic cell. (a) Layout used for parasitic extraction. (b) Transient simulation results with and without parasitic annotation.

TABLE 2. Delay (ps) and Energy/Transition Values (aJ) for a 2-NW per Transistor XOR2 With and Without Layout-Extracted Parasitic Annotation.

		Delay (ps)		Energy / transition (aJ)	
Output transition	Input transition A B	Without PEX	With PEX	Without PEX	With PEX
↑	↓1	93.74	83.83	724.81	825.82
	↑0	90.93	111.63	725.42	803.65
	1↓	90.73	83.41	724.91	851.42
	0↑	89.40	100.32	725.77	792.08
↓	↑1	92.12	85.60	5.09	34.69
	↓0	90.75	112.12	5.29	58.59
	1↑	95.57	83.42	4.70	45.04
	0↓	92.73	102.55	5.00	59.05
	Average	92.00	95.36	365.12	433.79
	Increase		+3.65%		+18.81%

related model flag parameters to 1 (described in Section II-A) to activate self-heating and trapping. Next, we vary the temperature (250–400 K), within the range allowed by the technology and model specifications and perform logic circuit simulations.

For all logic cells, we observe that these variations have no effect on the functional behavior. We also observe that while the propagation delay decreases with the increase of temperature, dynamic energy consumption/transition increases. These phenomena result from a reduction of the threshold

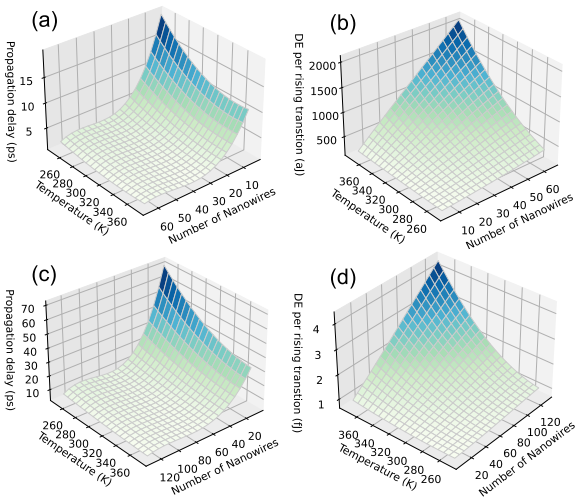

FIGURE 14. Variation of logic cell performance metrics with the number of NWs per VNWFET and temperature while considering self-heating and trapping effects. (a) INV1/propagation delay (ps). (b) INV1/dynamic rising energy consumption (aJ). (c) XOR2/propagation delay (ps). (d) XOR2/dynamic rising energy consumption (fJ).

voltage with temperature, leading to a higher drive current as well as a higher leakage current. Fig. 14 shows these trends using the INV1 and XOR2 cells as examples.

IV. CONCLUSIONS AND PERSPECTIVES

We presented comprehensive insights into 3-D logic circuit design based on junctionless vertical NW transistors leveraging multiphysics simulations and SPICE-compatible compact models. In particular, we studied temperature effects and trap dynamics through dedicated measurements and extracted associated model parameters that couple these effects dynamically to circuit simulations. Cell-level performance of circuits, such as inverter or XOR, studied based on the developed compact model, indicate a strong impact of electrothermal effects in the VNWFET technology. Threshold voltage shift due to increasing temperature leads to an increase in drive current at the detriment of a reduced on–off current ratio, which in turn limits circuit functionality at elevated temperatures especially at the onset of self-heating due to confinement effects for cells with increased complexity. In addition, interface trapping has a major role in determining dynamic performance metrics, such as the delay. Careful consideration is thus required for designing circuits operating under high-temperature conditions using the current state of the VNWFET technology. Work-around solutions such as gate work-function/doping engineering can be envisioned that could be useful as a feedback for fabrication process improvement. Other potential improvements include test structure and cell-level 3-D interconnect design optimization to achieve low-latency and compact 3-D logic circuits.

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