by Alex Lidow

Gallium Nitride Integration: Going Where Silicon Power Can't Go

In the late 1970s, when I was a young research and development engineer working on early power metal–oxide–semiconductor field-effect transistors (MOSFETs), our group was given the challenge of integrating several power devices to form a monolithic half-bridge that could be used in a variable-speed motor drive. We quickly discovered the difficulty of integrating multiple silicon (Si) power devices into a monolithic component because of the migration of minority carriers from one power device to the next. Solving the problem involved expensive technology. The economics did not work, and our group refocused on discrete transistors. Forty years later, and with the fast developments in gallium nitride-on-Si (GaN-on-Si) technology, multiple power devices can now be monolithically integrated economically.

It has been more than eight years since discrete GaN-on-Si power devices hit the off-the-shelf commercial market as replacements for aging Si power MOSFETs. New applications, such as LiDAR and envelope tracking, have benefited from the faster switching speeds and small size of GaN devices. More recently, mainstream applications, such as 48–12-V dc–dc converters, have adopted GaN-on-Si, and their prices have achieved near parity with mature MOSFETs.

But this is just the beginning for GaN-on-Si. Figure 1 shows the relative die size of Si power MOSFETs versus the last two generations of enhancement-mode GaN (eGaN) FETs produced by the Efficient Power Conversion Corporation (EPC). Even with the current superior performance of GaN over Si, the fifth-generation GaN devices, launched in 2017, are still 300 times larger than their theoretical limit. For comparison, in 1978, International Rectifier introduced power MOSFETs that were state of the art yet were still 300 times away from the Si theoretical limit. It took about 20 years for power MOSFETs to hit the theoretical line. GaN technology is on pace to strike the theoretical limit in less time!

GaN-on-Si transistors are lateral devices (the current flow is parallel to the surface of the transistor) as compared with power MOSFETs, which are vertical-conduction devices. Therefore, GaN-on-Si has the advantage of easy integration of multiple power devices that can be electrically isolated from each other. In 2014, EPC demonstrated this capability with a family of monolithic half-bridge products, starting with the EPC2100. Not only was it possible to integrate economically, but the combination of two power devices took less chip area than the individual

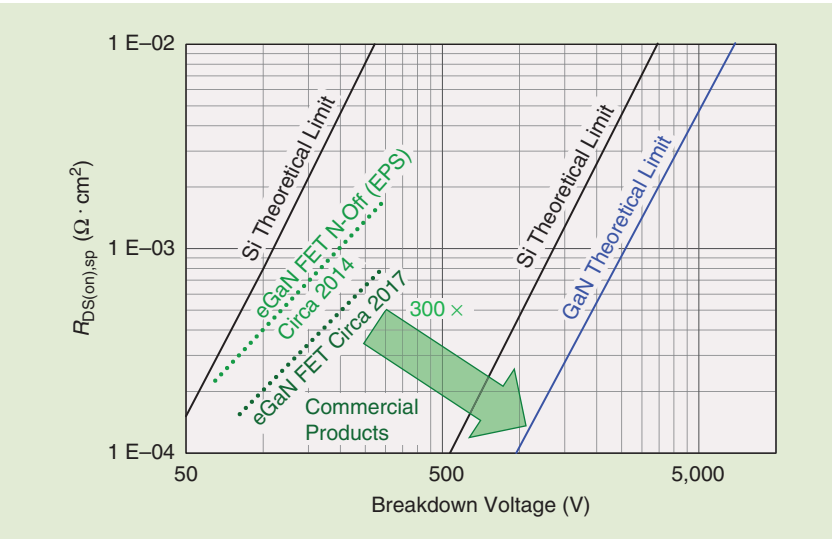

FIG 1 The theoretical on-resistance versus voltage for Si silicon carbide (SiC) and GaN majority carrier devices. (Image used with permission from EPC.)

Digital Object Identifier 10.1109/MPEL.2018.2850738
Date of publication: 10 September 2018

discrete transistors, thus providing additional savings in cost and valuable printed circuit board area. Performance was also improved, largely due to the reduction in power loop inductance by approximately 40%, as shown in Figure 2.

In parallel with the improvement in discrete GaN technology, new devices that incorporate the driver function have been launched by companies such as Navitas Semiconductor, Dialog Semiconductor, and EPC. A good example is the EPC2112, which pairs a 200-V, 40-mΩ FET with a monolithically integrated driver that enables the FET to be switched at multimegahertz frequencies from simple logic gates. The next step, coming in early 2019, is to combine the monolithic half-bridge with drivers and add a level-shift function, such that the entire half-bridge can be controlled by a simple logic gate. A half-bridge with level shift and drivers is the building block for most power conversion applications. This is the dream we had 40 years ago!

Going forward, there are two parallel paths for GaN technology: 1) improving the underlying GaN-on-Si technology to harvest the remaining 300 times in die size reduction theoretically possible and 2) adding more and more useful functionality to integrated circuits (ICs). However, there are several challenges facing integration efforts in GaN.

First and foremost, there needs to be a stable, well-characterized library of passive and active components that can be reliably and predictably integrated monolithically. The first-generation ICs were in a sense handcrafted based on trial and error and highly educated guessing. To achieve the best and most reliable performance, technology platforms need to be translated into a rich set of models that scale; include parasitic interactions; are characterized over all temperature, voltage, and current conditions; and include realistic process variations. This is no small task, and it creates a natural tension with the quickly improving discrete GaN FET performance.

On the one hand, it takes time and effort to fully characterize a technology platform. On the other hand, if the platform is changing faster than the characterization process, then the IC products will lag their discrete counterparts in performance and cost effectiveness. At EPC, this has caused us to put a great deal of engineering talent and resources, including automated device characterization equipment, into the development of a quickly and thoroughly characterized IC platform based on the latest discrete technology.

Our technology road map has the discrete technology evolving from approximately 21 mΩ-mm^2 today, to about 6 mΩ-mm^2 by the year 2021. In addition to monolithic half-bridge ICs, we are planning complete closed-loop buck converters, three-phase motor drives, and multilevel converters complete with a digital interface (and possibly full digital control).

Discrete power transistors are entering their final chapter. With GaN-on-Si technology, the transistor size is making it ever harder to pull enough current out of the tiny discrete chips. We do not see economical metallurgical solutions to extracting 300 Adc out of a 1-mm^2 device. ICs mitigate this to some extent by allowing merged structures that reduce overall metal conduction losses and parasitic inductance. This challenge, however, will require some creativity to enable the achievement of theoretical GaN performance. We did it in Si—and we can do it again in GaN.

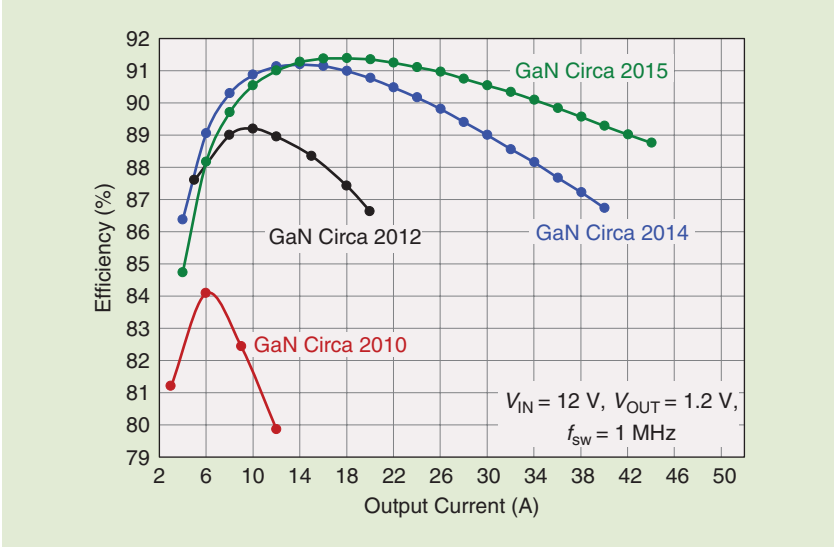

FIG 2 The EPC2100 monolithic half-bridge (green curve) shows improved efficiency in a 12–1.2-V buck converter operating at 1 MHz compared with discrete GaN-on-Si FETs introduced during the five prior years. (Image used with permission from EPC.)

About the Author

Alex Lidow (alex.lidow@epc-co.com) received his B.S. degree from the California Institute of Technology, Pasadena, in 1975 and his Ph.D. degree in applied physics as a Hertz Foundation Fellow from Stanford University, California, in 1977. He was elected to the Engineering Hall of Fame and received the 2015 SEMI Award for North America for innovation in power device technology. He is the chief executive officer (CEO) and cofounder of the Efficient Power Conversion Corporation (EPC). Prior to founding EPC, he was the CEO of the International Rectifier Corporation. A co-inventor of the HEXFET power metal–oxide–semiconductor field-effect transistor (MOSFET), he holds many patents in power semiconductor technology, including basic patents in power MOSFETs and gallium nitride (GaN) FETs. He coauthored the first textbook on GaN transistors, *GaN Transistors for Efficient Power Conversion*.

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