Small-Signal Modeling of Phase-Shifted Digital PWM in Interleaved and Multilevel Converters

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***Abstract*—In this article, small-signal modeling of digital pulsewidth modulators (DPWMs) used in multicell voltage source converters (VSCs) is addressed. In addition to sampling and computation, DPWM introduces delay, which impairs VSC's dynamic performance and robustness. In order to take into account the influence of modulation delay, an accurate small-signal representation of DPWM is necessary. Here, modeling of multisampled bipolar and unipolar phase-shifted DPWMs for single-, double-, and multi-update strategies is presented. The simplest multilevel modulation of single-cell full-bridge VSCs, unipolar DPWM, is also covered by the analysis. The derived operating-point-dependent small-signal DPWM models are verified using simulated and experimental frequency response measurements up to four times the Nyquist frequency. Comparisons are also made with the models conventionally considered in the literature. Additionally, an approximate method is presented to model the influence of dead time on DPWM's small-signal dynamics. For the purposes of showcasing the importance of the proposed DPWM models, high-frequency admittance of a VSC employing multisampled multiupdate unipolar DPWM is modeled and verified in simulations and experiments.**

***Index Terms*—Bipolar, phase-shifted digital pulsewidth modulation (PS-DPWM), small-signal model, unipolar, voltage source converters (VSCs).**

I. Introduction

MULTICELL voltage source converters (MC-VSCs) have recently gained a lot of attention [1], [2], [3], [4], [5], [6]. Besides overcoming current and voltage limitations of individual semiconductor devices, they are crucial for achieving ultrahigh performance conversion, by enabling significant filter reduction and improvement of dynamic response [1], [3], [6], [7], [8]. The cells within MC-VSCs can be connected in series or parallel, resulting in multilevel [1], [2], [3], [4] or interleaved topologies [5], [6], [9].

Phase-shifted digital pulsewidth modulation (PS-DPWM) is the most commonly adopted modulation type for MC-VSCs [2], [3], [4], [5], [10], [11]. In PS-DPWM carriers of adjacent cells are phase-shifted with respect to each other so that harmonic cancelation is achieved [10], [12], [13], [14]. This results in an increased frequency of the output ripple, i.e., frequency multiplication, allowing for the reduction of the output filter and the increase in the control loop bandwidth [2], [3], [5]. For full-bridge-based series stacked topologies, e.g., cascaded H-Bridge (CHB), PS-DPWM can be implemented as bipolar (BPS-DPWM) or unipolar (UPS-DPWM), depending on the modulation chosen for each individual cell [12], [13], [14].

For current-controlled PS-DPWM MC-VSCs, the choice of sampling and controller update rates is not always straightforward [15], [16]. Most often, the multisampled approach is taken, where, due to frequency multiplication [17], the average current is acquired more than twice per switching period of each cell [3], [16]. Ideally, sampling instants are chosen to coincide with the peaks, valleys, and intersections of individual carriers. Regarding the controller update, the first approach, denoted as multisampled single-update (MSSU), assumes that the modulating signal for each cell is updated either at the peaks or at the valleys of the corresponding carrier. If the update is performed both at the peaks and at the valleys, i.e., twice per carrier period, the approach is referred to as multisampled double-update (MSDU) [16], [18]. Another approach, denoted as multisampled multiupdate (MSMU), assumes that the modulating signal, which is the same for all cells, is updated at the peaks, valleys, and intersections of all carriers [3], [7], [19]. With MSMU, some nonlinear characteristics may appear in case of vertical crossings between modulating signals and carriers [7], [19], [20]; on the other hand, MSMU significantly reduces the modulation delay [21], [22].

Modulation delay, together with delays due to sampling and computation, limits the achievable bandwidths and deteriorates the robustness of VSCs employing DPWM [21], [23], [24], [25]. In order to account for the impact of the modulation delay on a system's performance, an adequate small-signal representation of the modulator is essential [21], [26], [27]. Although PS-DPWM is widely used, accurate small-signal models are derived only for two-level modulation strategies [26], [28]. A lack of small-signal modeling is present even for the simplest multilevel modulation of single-cell full-bridge VSCs, unipolar

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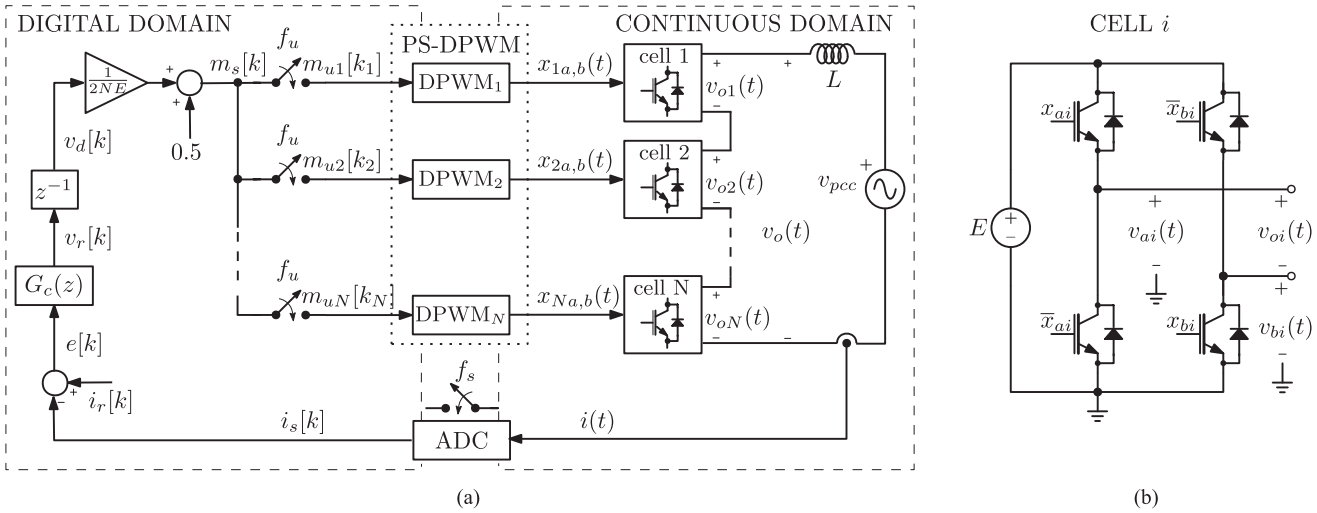

Fig. 1. Digitally controlled, single-phase, grid-following CHB converter employing PS-DPWM. (a) System block diagram. (b) Schematic of a single cell.

DPWM (U-DPWM). Without formal derivations, the authors in [7] assume that the model from [29], derived for two-level DPWM, is directly applicable for MSMU-UPS-DPWM. In this article, we show that the model from [29] accurately represents MSMU-BPS-DPWM, whereas a different model is obtained for MSMU-UPS-DPWM.

To fill in the gaps of previous research, this article addresses modeling of various strategies for multilevel modulation. Small-signal models of U-, BPS-, and UPS-DPWM are derived for the MSMU, MSDU, and MSSU strategies. The presented models are verified using simulated and experimental frequency response measurements (FRMs), up to four times the Nyquist frequency (NF). Benchmarking against models typically considered in the literature is provided to highlight the accuracy achieved. To showcase the importance of an accurate DPWM representation, high-frequency admittance of a full-bridge VSC employing MSMU-U-DPWM is modeled and validated in simulations and experiments.

This article is organized as follows. In Section II, the basic principles of the PS-DPWM are outlined, along with an explanation of the MSMU, MSDU, and MSSU strategies. The mathematical derivation of the U-, BPS-, and UPS-DPWM small-signal models is presented in Section III. The verification and benchmarking of these models is provided in Section IV. As an application example, high-frequency admittance modeling with MSMU-U-DPWM is addressed in Section V. Finally, Section VI concludes this article.

II. Control System of Multicell Converters Employing PS-DPWM

A. System Description

In order to derive small-signal models of U-, BPS-, and UPS-DPWM, a single-phase, digitally controlled, N cell CHB converter is considered in this article. CHB is chosen as an illustrative example because it allows the implementation of the three DPWMs types. Nonetheless, the presented methodology can be directly applied to other MC-VSC topologies, employing PS-DPWM. The dc-link voltage of each cell is assumed to be constant and equal to E. The extension of derived models for unbalanced operation is left for future work.

A block diagram of the considered current-controlled system is shown in Fig. 1(a). An analog-to-digital converter (ADC) performs the transition from the continuous domain to the digital domain. Current sampling is performed at the middle of the applied voltage pulses, so that center-pulse (synchronous) sampling is obtained [21]. The highest possible sampling frequency f_s that ensures removal of the switching ripple from the current i is considered within the article, as explained in Section II-B and II-C.

By subtracting the sampled current i_s from the reference i_r, error signal e is obtained and used as input to the current controller G_c. The controller output update is usually delayed by one sampling period due to the finite execution time [21]. The voltage reference generated by the current controller is scaled to the range [0, 1], resulting in the modulating signal m_s. In order to obtain the digital modulating signal for the ith cell, m_{ui}, a rate transition from f_s to f_u may be required, depending on whether the multi-, double-, or single-update strategy is used. The implementation and differences between these strategies are addressed in Section II-D. It is important to note that this article considers symmetric PS-DPWM, where the same signal m_s is forwarded to all rate transition blocks.

The modulating signal m_{ui} is used by DPWM $_i$ to perform the transition from digital to continuous domain. Its inherent zero-order hold (ZOH) function transforms m_{ui} to m_i. As outlined in the following subsection, switching waveforms for the ith cell, $x_{ia,b}$, are obtained from m_i based on the modulation type. They are used to control the power transistors within the ith cell of the CHB converter. Each cell is realized as an H-Bridge, which consists of two legs, a and b, as shown in Fig. 1(b). The output voltage of the ith cell v_{oi} is determined as a difference between the output voltages of the two legs, $v_{oi} = v_{ai} - v_{bi}$. Since the cells are connected in series, the output voltages of all the cells

are summed up to form the output voltage of the CHB converter

$$v_o(t) = \sum_{i=1}^{N} v_{oi}(t) = \sum_{i=1}^{N} \Big(x_{ai}(t) - \big(1 - x_{bi}(t)\big) \Big) E$$
$$= x_{eq}(t) E \qquad (1)$$

where x_{ai} and x_{bi} are the switching waveforms for legs a and b, respectively, and x_{eq} is the equivalent switching waveform.[1] The difference between v_o and the voltage at the point of common coupling (PCC), v_{pcc}, is applied to an arbitrarily chosen inductive output filter L.

B. Bipolar and Unipolar Modulation of a Single Cell

Control signals for switches within the same leg of an individual H-bridge cell are always complementary to avoid shoot-through. Two widely used strategies to determine switching waveforms for different legs are bipolar (B-DPWM) and unipolar modulation (U-DPWM) [14], [30].

In B-DPWM, the same switching waveform is used to control both legs, i.e., $x_{ai} = x_{bi}$. It is determined by the comparison between $m_i(t)$ and $w_i(t)$, as shown in Fig. 2(a). This results in two possible levels for the cell output voltage, $-E$ and E. In case only one cell is used, the inductor current features a triangular switching ripple with the lowest frequency component at $f_{\text{rip}} = f_{\text{pwm}}$. Thus, for a single cell modulated by B-DPWM, the maximum frequency at which current can be sampled, without introducing switching ripple in the feedback, is equal to $2f_{\text{pwm}}$.

On the other hand, in U-DPWM, $x_{ai} \neq x_{bi}$. The switching waveform for leg a, x_{ai}, is determined in the same way as in B-DPWM. However, x_{bi} is determined by a comparison between the complementary modulating signal $1 - m_i(t)$ and the switching carrier $w_i(t)$, as shown in Fig. 2(b). Alternatively, U-DPWM can be realized so that the two legs use the same modulating signal, but different, 180° phase-shifted carriers. Nevertheless, the former realization is more often used, since it requires fewer carriers. With U-DPWM, three output voltage levels appear: $-E$, 0, and E. In case only one cell is used to supply the filter inductor, its current features a triangular switching ripple with the lowest frequency component at $f_{\text{rip}} = 2f_{\text{pwm}}$. Thus, U-DPWM allows the average current to be sampled four times per switching period. Compared to B-DPWM, U-DPWM offers twice the frequency multiplication [3], [12], [14]; however, it also increases the common-mode noise injection [30].

C. Phase-Shifted Modulation

In PS-DPWM a phase-shift between carriers of the cascaded cells is introduced in order to achieve frequency multiplication effect, i.e., increase of f_{rip}. The value of the phase-shift depends on the number of cells and the modulation type used, i.e., bipolar or unipolar.

In case of BPS-DPWM, in order to achieve the highest possible harmonic cancellation [31], phase-shift between carriers of the adjacent cells should be set to $\Delta\phi_{\text{BPS}} = 360°/N$. In case of balanced cell voltages, this results in $f_{\text{rip}} = N f_{\text{pwm}}$. Thus, BPS-DPWM allows for $f_s = 2N f_{\text{pwm}}$, without introducing a switching ripple in the signal $i_s[k]$. The working principle of BPS-DPWM is illustrated in Fig. 2(c), where $N = 3$ is used as an example.

In case of UPS-DPWM, the highest possible harmonic cancellation is achieved if the phase-shift between carriers of each of the two adjacent cells is set to $\Delta\phi_{\text{UPS}} = 180°/N$. This results in $f_{\text{rip}} = 2N f_{\text{pwm}}$. Thus, UPS-DPWM allows for $f_s = 4N f_{\text{pwm}}$ without introducing a switching ripple in the signal $i_s[k]$. The working principle of UPS-DPWM is illustrated in Fig. 2(d), where $N = 3$ is used as an example.

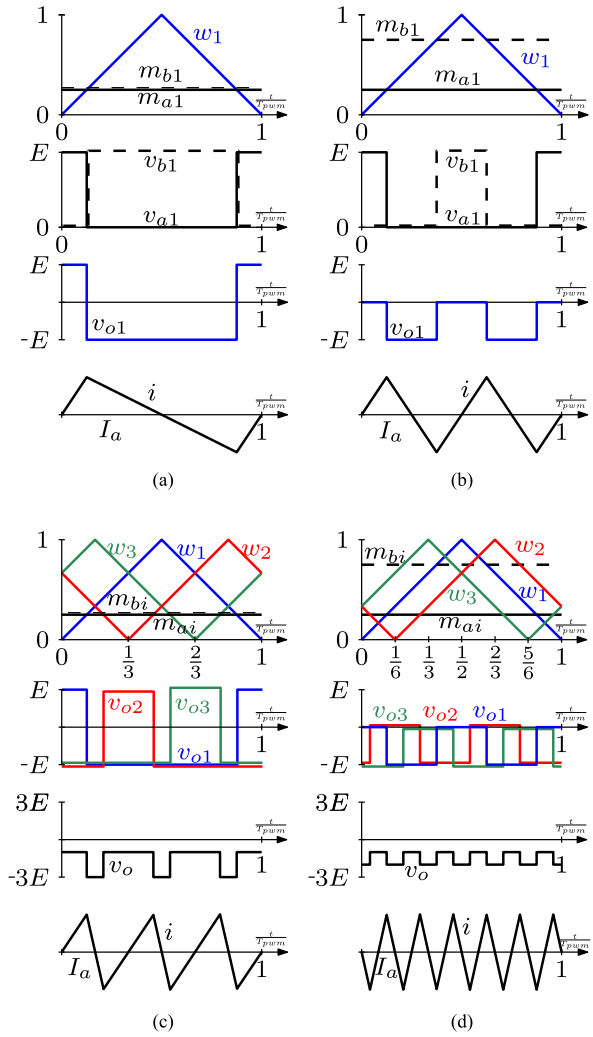

Fig. 2. Illustration of the operating principle, the switching waveforms generation, and the frequency multiplication effect for: (a) B-DPWM ($N = 1$); (b) U-DPWM ($N = 1$); (c) BPS-DPWM ($N = 3$); and (d) UPS-DPWM ($N = 3$). Voltages are vertically offset for visualization, to avoid their overlap.

D. Multisampled Control With Multi-, Double-, and Single Update

In this subsection, three different strategies to choose the update rate $f_u = \frac{1}{T_u}$ of the controller are briefly explained.

[1] Note that, during the transistor dead-time, (1) does not hold as $v_{oi}(t)$ is determined by the sign of the inductor current. Following the approach from [28], dead-time is neglected in the following derivations, which is justified based on the analysis provided in Appendix B.

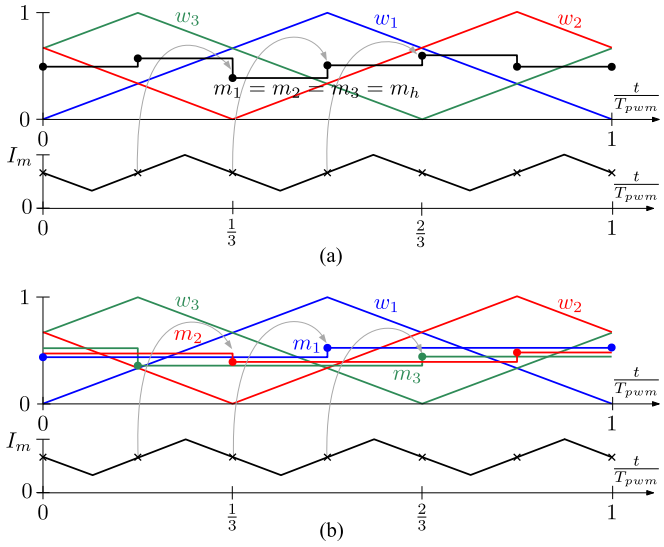

Fig. 3. Illustration of sampling and update instants for BPS-DPWM with $N = 3$ using different strategies. (a) MSMU. (b) MSDU. Both strategies feature one step computational delay.

For all strategies, the sampling rate is determined by the ripple frequency, i.e., $f_s = 2f_{\text{rip}}$.

In the MSMU strategy $f_u = f_s$, i.e., the modulating signal, which is the same for all cells, is updated as often as the current sampling is performed, yielding $m_{ui}[k] = m_s[k]$. This is illustrated in Fig. 3(a), where BPS-DPWM with $N = 3$ is used as an example. As it will be analytically shown in the next section, the MSMU strategy offers a significant reduction in modulation delay. However, since the modulating signal update is performed more than twice per switching period, around certain steady-state operating points (SSOPs), vertical crossings between the modulating signal and the carriers may appear, which results in a nonlinear behavior of the DPWM [7], [19], [20]. The analysis of this phenomenon is beyond the scope of this article, whose focus is on assessing the system properties around SSOPs where the linear behavior is guaranteed.

In the MSDU strategy, the update frequency is determined as $f_u = 2f_{\text{pwm}}$. The digital modulating signal for the ith cell, m_{ui}, is obtained by resampling m_s at instants that coincide with the peaks and valleys of the ith carrier,[2] as illustrated in Fig. 3(b). For certain applications, MSDU may be more suitable than MSMU, as it avoids the modulator nonlinearities caused by the vertical intersections between m_i and w_i [7], [16], [19].

E. Small-Signal Representation

Another possible update strategy is MSSU, where $f_u = f_{\text{pwm}}$ and the modulating signal for each cell is updated at either peaks or valleys of the corresponding carrier, resulting in the symmetric-on- or -off-time modulation [28]. As shown in Appendix A, MSSU introduces a larger modulation delay than MSDU. Thus, when it is of interest to avoid modulator nonlinearities caused by vertical intersections, MSDU is usually preferred, although MSSU may be necessary in computationally demanding applications.

[2]Note that, in case of MSDU control with U- and UPS-DPWM, number of update instants is two times lower than the number of available samples. Thus, half of the samples are discarded. In this article, it is assumed that the samples closest to the update instants are kept.

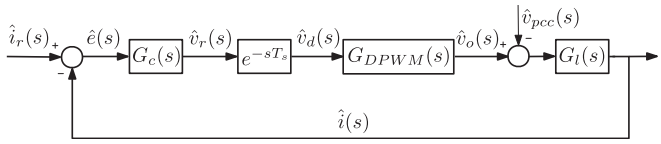

Fig. 4. Small-signal s-domain representation of the system from Fig. 1(a).

In Fig. 4, the small-signal s-domain representation of the system from Fig. 1(a) is shown. The output filter is represented by the transfer function G_l

$$G_l(s) = \frac{\hat{i}(s)}{\hat{v}_o(s) - \hat{v}_{pcc}(s)} = \frac{1}{sL} \tag{2}$$

where s is the complex variable of the Laplace transform, $\hat{i}(s)$, $\hat{v}_{\text{pcc}}(s)$, and $\hat{v}_o(s)$ are Laplace transforms of small-signal perturbations of $i(t)$, $v_{\text{pcc}}(t)$, and $v_o(t)$. The transfer function of the current controller in s-domain is denoted by $G_c(s)$. The computational delay, which is assumed to be equal to one sampling period T_s and is denoted by z^{-1} in Fig. 1(a), is represented in Fig. 4 as e^{-sT_s}.

The main contribution of this article is the derivation of the DPWM small-signal model, represented by $G_{\text{DPWM}}(s)$ in Fig. 4, for the modulation strategies described earlier. The following variables will be useful for the derivation of $G_{\text{DPWM}}(s)$: $x_{\text{eq}}(t)$, defined in (1), and $m_{\text{eq}}(t)$

$$m_{\text{eq}}(t) = \frac{v_d(t)}{E} = N(2m(t) - 1) \tag{3}$$

where v_d is the delayed controller output and m is the continuous-time equivalent of m_s, which when sampled at f_s yields m_s. Laplace transforms of small-signal perturbations of $x_{\text{eq}}(t)$ and $m_{\text{eq}}(t)$ are given by

$$\hat{x}_{\text{eq}}(s) = \frac{\hat{v}_o(s)}{E} = \sum_{i=1}^{N} \hat{x}_{ai}(s) + \hat{x}_{bi}(s) \tag{4}$$

$$\hat{m}_{\text{eq}}(s) = \frac{\hat{v}_d(s)}{E} = 2N\hat{m}(s) \tag{5}$$

where $\hat{x}_{ai}(s)$, $\hat{x}_{bi}(s)$, $\hat{v}_d(s)$, and $\hat{m}(s)$ are Laplace transforms of small-signal perturbations of $x_{ai}(t)$, $x_{bi}(t)$, $v_d(t)$, and $m(t)$, respectively. By defining $G_{\text{DPWM}}(s)$ as

$$G_{\text{DPWM}}(s) = \frac{\hat{v}_o(s)}{\hat{v}_d(s)} = \frac{\hat{x}_{\text{eq}}(s)}{\hat{m}_{\text{eq}}(s)} = \frac{\sum_{i=1}^{N} \hat{x}_{ai}(s) + \hat{x}_{bi}(s)}{2N\hat{m}(s)} \tag{6}$$

the current controller can be seen to result in a reference voltage which, after being processed by $G_{\text{DPWM}}(s)$, appears at the output of the CHB. This equation will be used in the following derivations to determine the small-signal representation of DPWMs.

III. DPWM Small-Signal Modeling

The goal of this section is to derive accurate small-signal models of U-, BPS-, and UPS-DPWM, for the MSMU and

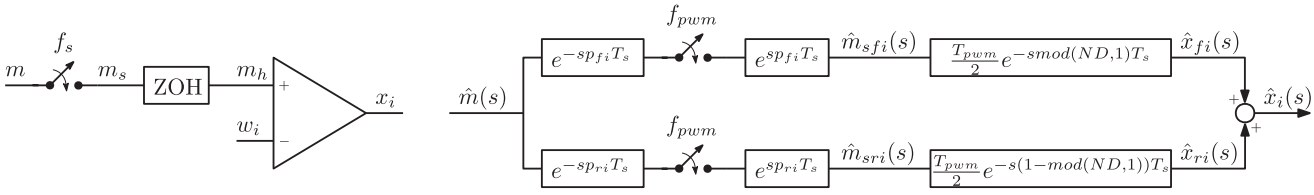

Fig. 5. Modulation of the ith cell for MSMU-BPS-DPWM. (a) General representation of DPWM$_i$. (b) Block diagram of DPWM$_i$ in s-domain.

MSDU strategies. The procedure from [26] and [28] is used as a basis. The operating-point-dependent DPWM models are derived using pulse-to-continuous transfer function in s-domain, which is adequate for both s- and z-domain modeling of the overall system [27], [28], [32].[3]

A. Multisampled Multiupdate Strategy

First, MSMU-BPS-DPWM is considered. Since in bipolar modulation $x_{ai} = x_{bi}$, (6) reduces to

$$G_{\text{DPWM}}^{\text{MSMU-BPS}}(s) = \frac{\sum_{i=1}^{N} \hat{x}_{ai}(s)}{N\hat{m}(s)}. \tag{7}$$

To simplify notation, $\hat{x}_{ai}$ is replaced by $\hat{x}_i$ and further used to denote the DPWM$_i$'s output. In the following analysis, the waveforms of MSMU-BPS-DPWM with $N = 3$, shown in Fig. 6, are used. Nevertheless, the analytical expressions are provided for a general case of N cells.

The continuous input of the modulator $m(t)$ is separated into a steady-state part M and a small perturbation: $m(t) = M + \hat{m}(t)$. By sampling $m(t)$ at T_s, the sampled modulating signal $m_s(t)$ is obtained. The DPWM$_i$ performs ZOH of $m_s(t)$ and the comparison with the triangular carrier $w_i(t)$. This results in the switching signal $x_i(t)$, as seen in Fig. 5(a).

Assuming an ideal sampler, its small-signal output can be represented as a series of Dirac impulses [26], [28], denoted by $\hat{m}_s(t)$. In order to distinguish between impulses that impact the rising from those that impact the falling edges of the modulator's output, this series is divided into two subseries $\hat{m}_{sf}(t)$ and $\hat{m}_{sr}(t)$. Each of these two subseries is further divided into N subseries, corresponding to each individual cell

$$\hat{m}_s(t) = \hat{m}_{sf}(t) + \hat{m}_{sr}(t) = \sum_{i=1}^{N} \hat{m}_{sfi}(t) + \hat{m}_{sri}(t) \tag{8}$$

where

$$\hat{m}_{sfi}(t) = \sum_{n=-\infty}^{n=+\infty} \hat{m}(t)\delta(t - nT_{\text{pwm}} - p_{fi}T_s) \tag{9}$$

$$\hat{m}_{sri}(t) = \sum_{n=-\infty}^{n=+\infty} \hat{m}(t)\delta(t - nT_{\text{pwm}} - p_{ri}T_s) \tag{10}$$

δ is the Dirac delta function and $p_{fi}, p_{ri} \in [0, N-1]$ are indices that determine which sample within one T_{pwm} affects

[3]For z-domain modeling $G_{\text{DPWM}}(s)G_l(s)$ is transformed to z-domain using modified $\mathcal{Z}$ transform or impulse-invariant method [28], [32].

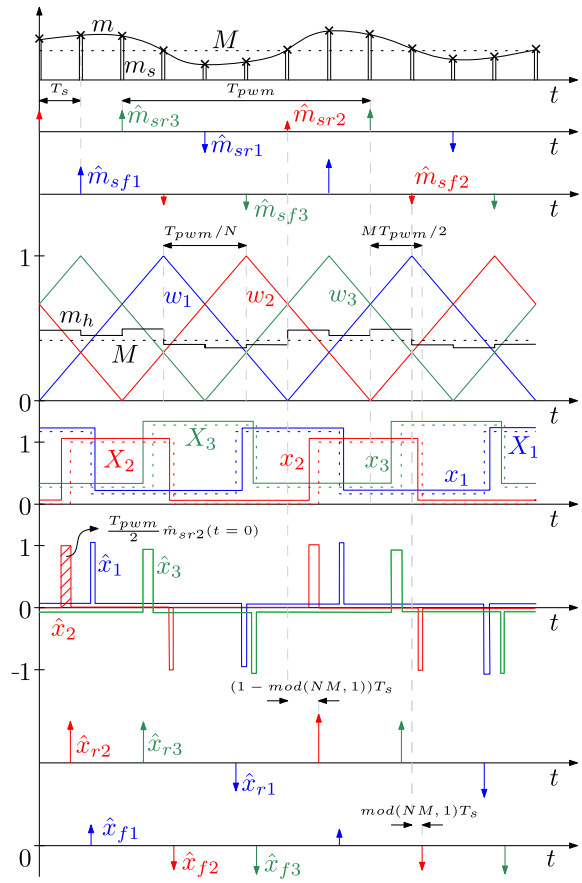

Fig. 6. Waveforms of interest for MSMU-BPS-DPWM with $N = 3$, which are used for the derivation of the modulator's small-signal model. Switching signals are vertically offset for visualization, to avoid their overlap.

which cells' falling and rising edges of the output. These indices are defined by $p_{fi} = \text{div}(NM, 1) + (N-1)(i-1)$ and $p_{ri} = (N-1) - \text{div}(NM, 1) + (N-1)(i-1)$, where div is the integer division operator.

As for $m(t)$, $x_i(t)$ can be separated into two parts: $x_i(t) = X_i(t) + \hat{x}_i(t)$, where $X_i(t)$ and $\hat{x}_i(t)$ represent DPWM$_i$'s response to M and $\hat{m}(t)$, respectively. As illustrated in Fig. 6, $\hat{x}_i(t)$ is a series of pulses. Provided that $\hat{m}(t)$ is sufficiently small, $\hat{x}_i(t)$ can be approximated by a series of Dirac impulses positioned at the edges of $X_i(t)$, such that each impulse has the same integral over time as the pulse that it approximates [26], [28]. This series of impulses can be separated into two subseries

$$\hat{x}_i(t) = \hat{x}_{fi}(t) + \hat{x}_{ri}(t) \tag{11}$$

where $\hat{x}_{fi}(t)$ and $\hat{x}_{ri}(t)$ represent DPWM$_i$'s response to $\hat{m}_{sfi}(t)$ and $\hat{m}_{sri}(t)$, respectively.

The impulses $\hat{x}_{fi}(t)$ are positioned at the falling edges of $X_i(t)$ and delayed with respect to $\hat{m}_{sfi}(t)$ by τ_{Fi}. Similarly, the impulses $\hat{x}_{ri}(t)$ are positioned at the rising edges of $X_i(t)$ and are delayed with respect to $\hat{m}_{sri}(t)$ by τ_{Ri}. For example, if $\hat{m}_{fi}(t) = \delta(t)$, then $\hat{x}_{fi}(t) = \frac{T_{\text{pwm}}}{2}\delta(t - \tau_{Fi})$. Similarly, if $\hat{m}_{ri}(t) = \delta(t)$, then $\hat{x}_{ri}(t) = \frac{T_{\text{pwm}}}{2}\delta(t - \tau_{Ri})$. The delays τ_{Fi} and τ_{Ri}, found from Fig. 6, are shown to be the same for each cell and equal to $\tau_{Fi} = \tau_F = \text{mod}(NM, 1)T_s$ and $\tau_{Ri} = \tau_R = (1 - \text{mod}(NM, 1))T_s$, where mod is the modulo operator. Thus, and taking into account that $\mathcal{L}\{\delta(t - t_0)\} = e^{-st_0}$, the Laplace transforms of $\hat{x}_{fi}(t)$ and $\hat{x}_{ri}(t)$ can be expressed as

$$\hat{x}_{fi}(s) = \frac{T_{\text{pwm}}}{2} e^{-s\text{mod}(NM,1)T_s} \hat{m}_{sfi}(s) \tag{12}$$

$$\hat{x}_{ri}(s) = \frac{T_{\text{pwm}}}{2} e^{-s(1-\text{mod}(NM,1))T_s} \hat{m}_{sri}(s) \tag{13}$$

where $\hat{m}_{sfi}(s)$ and $\hat{m}_{sri}(s)$ are the Laplace transforms of $\hat{m}_{sfi}(t)$ and $\hat{m}_{sri}(t)$, respectively. Summation of (12) and (13) yields DPWM$_i$'s output in s-domain

$$\hat{x}_i(s) = \frac{T_{\text{pwm}}}{2}\left(e^{-s\text{mod}(NM,1)T_s}\hat{m}_{sfi}(s) + e^{-s(1-\text{mod}(NM,1))T_s}\hat{m}_{sri}(s)\right). \tag{14}$$

This is illustrated in Fig. 5(b) where the block diagram of DPWM$_i$ is shown. Since, according to (9) and (10), $\hat{m}_{sfi}(t)$ and $\hat{m}_{sri}(t)$ are obtained from the same continuous signal $\hat{m}(t)$, by sampling it at T_{pwm}, $\hat{m}_{sfi}(s)$ and $\hat{m}_{sri}(s)$ can be expressed as [33]

$$\hat{m}_{sfi}(s) = \frac{1}{T_{\text{pwm}}} \sum_{h=-\infty}^{h=+\infty} e^{jh\omega_{\text{pwm}}p_{fi}T_s} \hat{m}(s - jh\omega_{\text{pwm}}) \tag{15}$$

$$\hat{m}_{sri}(s) = \frac{1}{T_{\text{pwm}}} \sum_{h=-\infty}^{h=+\infty} e^{-jh\omega_{\text{pwm}}p_{ri}T_s} \hat{m}(s - jh\omega_{\text{pwm}}) \tag{16}$$

where j is the imaginary unit. Substitution of (15) and (16) into (14), while focusing on the input–output relation at the same frequency, i.e., assuming $h = 0$, yields

$$\hat{x}_i(s) = \frac{1}{2}\left(e^{-s(1-\text{mod}(NM,1))T_s} + e^{-s\text{mod}(NM,1)T_s}\right)\hat{m}(s). \tag{17}$$

By substituting (17) into (7), a small-signal model of MSMU-BPS-DPWM is obtained

$$G_{\text{DPWM}}^{\text{MSMU-BPS}}(s) = \frac{1}{2}\left(e^{-s(1-\text{mod}(NM,1))T_s} + e^{-s\text{mod}(NM,1)T_s}\right). \tag{18}$$

Using the same approach as for MSMU-BPS-DPWM, the small-signal model of MSMU-UPS-DPWM can be derived as

$$G_{\text{DPWM}}^{\text{MSMU-UPS}}(s) = \frac{1}{2}\left(e^{-s(1-\text{mod}(N|2M-1|,1))T_s} + e^{-s\text{mod}(N|2M-1|,1)T_s}\right). \tag{19}$$

TABLE I
OVERVIEW OF THE PROPOSED AND TYPICALLY CONSIDERED SMALL-SIGNAL DPWM MODELS

Proposed small-signal DPWM models: $G_{\text{DPWM}}(j\omega)$				
Strategy	Type	№	Gain	Delay
DSDU	B	1	$\cos\left(\omega T_s\left(M - \frac{1}{2}\right)\right)$	$e^{\frac{-j\omega T_s}{2}}$
MSMU	U	2	$\cos\left(\omega T_s\left(\lvert 2M-1\rvert - \frac{1}{2}\right)\right)$	
	BPS	3	$\cos\left(\omega T_s\left(\text{mod}(NM,1) - \frac{1}{2}\right)\right)$	
	UPS	4	$\cos\left(\omega T_s\left(\text{mod}(N\lvert 2M-1\rvert,1) - \frac{1}{2}\right)\right)$	
MSDU	U BPS UPS	5	$\cos\left(\omega\frac{T_{\text{pwm}}}{2}\left(M - \frac{1}{2}\right)\right)$	$e^{\frac{-j\omega T_{\text{pwm}}}{4}}$
Typically considered models: $G_{\text{DPWM}}(j\omega)$				
Name		№	Gain	Delay
Zero-order hold		6	$\frac{2}{\omega T_u}\sin\frac{\omega T_u}{2}$	$e^{\frac{-j\omega T_u}{2}}$
Delay		7	1	

For $N = 1$, (19) yields small-signal model of MSMU-U-DPWM

$$G_{\text{DPWM}}^{\text{MSMU}-U}(s) = \frac{1}{2}\left(e^{-s(1-|2M-1|)T_s} + e^{-s|2M-1|T_s}\right). \tag{20}$$

The same expression can be obtained from (18) for $N = 2$, by substituting $\text{mod}(2\,M, 1) = |2M - 1|$. This is clear considering that U-DPWM with $N = 1$ can be realized in the same way as BPS-DPWM with $N = 2$.

B. Multisampled Double-Update Strategy

Using the Dirac impulse-based approach from [26] and [28] and following the same methodology as for MSMU, small-signal models of DPWMs employing MSDU startegy can be derived. It can be shown that, contrary to MSMU, where each type of modulation, i.e., U-, BPS-, and UPS-DPWM, features a different small-signal model, with MSDU, the model is the same regardless of the modulation type used. Moreover, the model does not depend on the number of cells nor on the sampling period, but only on the switching period and the SSOP. Due to space limitations, detailed derivation is not included—only the final expression of the MSDU-DPWM small-signal model is provided

$$G_{\text{DPWM}}^{\text{MSDU}}(s) = \frac{1}{2}\left(e^{-s(1-M)\frac{T_{\text{pwm}}}{2}} + e^{-sM\frac{T_{\text{pwm}}}{2}}\right). \tag{21}$$

C. Overview of the Presented DPWM Models

By providing the frequency response of G_{DPWM}, an overview of all DPWM small-signal models derived in the previous two subsections is presented in Table I, in order to emphasize different gains and delays. As a benchmark, the conventional double-sample double-update bipolar DPWM (DSDU-B-DPWM) is also included [26]. First, it can be seen that for the DSDU and MSMU strategies, the delay is determined in the same way, using the sampling period T_s. On the other hand, for MSDU, the delay is determined by the switching period T_{pwm}.

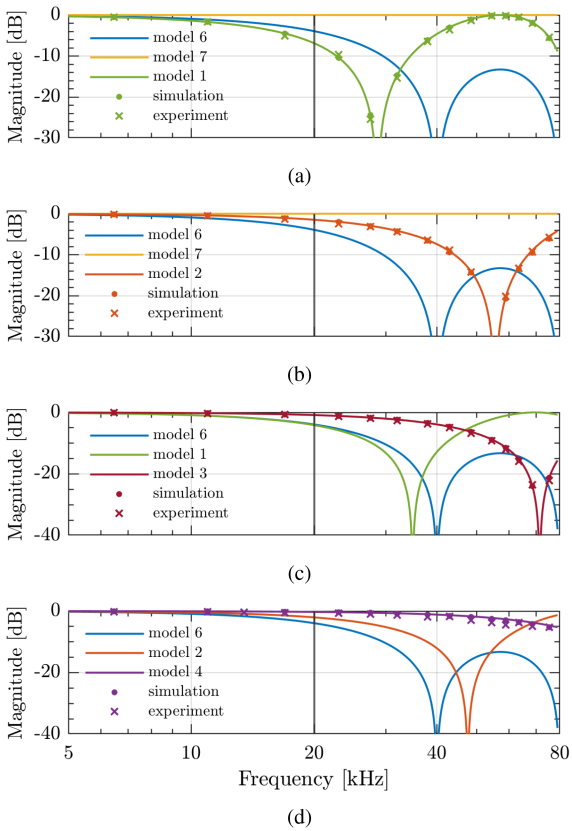

Fig. 7. Magnitude of the DPWM's frequency response obtained from different small-signal models, and simulated and experimental FRMs. (a) DSDU-B-DPWM at $M = 0.85$. (b) MSMU-U-DPWM at $M = 0.66$. (c) MSMU-BPS-DPWM at $M = 0.79$. (d) MSMU-UPS-DPWM at $M = 0.57$. The gray vertical line marks the NF.

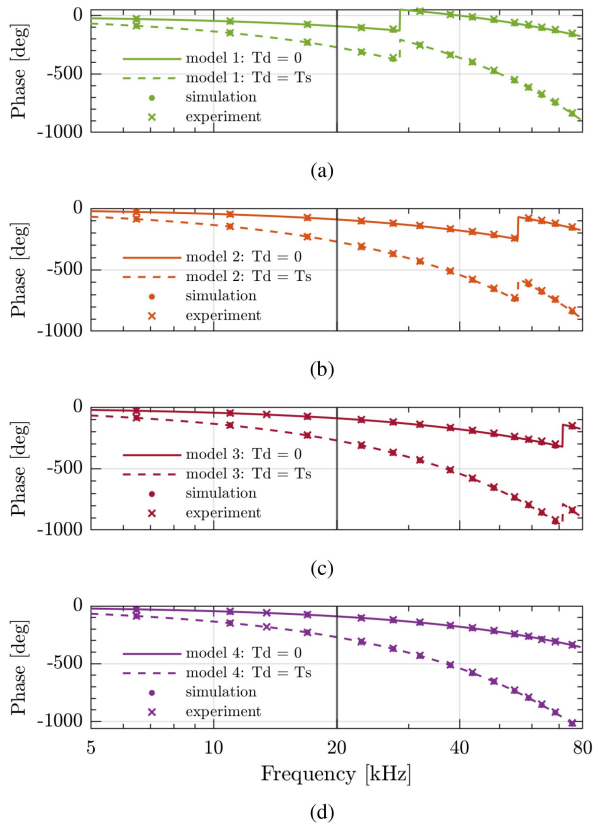

Fig. 8. Phase of the DPWM's frequency response, with and without one step computational delay, obtained from the proposed model, and simulated and experimental FRMs. (a) DSDU-B-DPWM at $M = 0.85$. (b) MSMU-U-DPWM at $M = 0.66$. (c) MSMU-BPS-DPWM at $M = 0.79$. (d) MSMU-UPS-DPWM at $M = 0.57$. The gray vertical line marks the NF.

Next, since for MSMU strategies $T_s = \frac{T_{\text{pwm}}}{2\,N}$ with bipolar and $T_s = \frac{T_{\text{pwm}}}{4\,N}$ with unipolar modulation, it can be observed that MSMU-DPWMs feature either N or $2\,N$ times lower delay compared to MSDU-DPWMs. This is an important remark, since it points to higher control-loop bandwidth capabilities of systems with MSMU-DPWMs.

For comparison, the ZOH and pure delay models are also included in Table I, as they are often used in the literature to represent DPWM [3], [16], [19], [23], [24]. As it will be demonstrated by means of simulated and experimental FRMs, in order to obtain an accurate small-signal representation of MSMU- and MSDU-PS-DPWMs, the proposed models are necessary.

IV. Verification and Benchmarking

A goal of this section is to verify the derived small-signal DPWM models. For the purposes of the following validations, all modulation strategies from Table I are realized in simulations as well as in a standardly available control platform. BPS- and UPS-DPWM are implemented with $N = 3$. The switching frequency for each DPWM type is chosen to correspond to a sampling frequency of 40 kHz. Thus, f_{pwm} is set to {20, 10, 6.67, 3.33} kHz for B-, U-, BPS-, and UPS-DPWM, respectively.

For each modulation strategy, FRMs are performed for two different implementations: with and without one step computational delay, denoted by $T_d = T_s$ and $T_d = 0$, respectively. For MSMU strategies, validations are given for SSOPs around which nonlinear effects due to vertical crossings are not present [20].

MATLAB Simulink is used to perform the simulated FRMs. Perturbation generation, as well as postprocessing of $v_d(t)$ and $v_o(t)$ to obtain the FRMs of DPWMs is performed using the frequency response estimator block. The sinestream experiment mode is used with the perturbation frequencies in the range [6, 80] kHz. Settling and acquisition time are set to 20 and 40 ms, respectively. The perturbation magnitudes are set so that they produce a 3% peak–peak variation of m. To force the operation around the desired SSOPs, an appropriate dc bias is imposed.

For experimental FRMs, the DPWMs from Table I are implemented on a DSP TI f28379 d. The measurements are performed in the following manner. A signal generator is configured to provide a small sinusoidal perturbation superimposed on the dc bias. The perturbation magnitudes and frequencies are chosen in the same way as in the simulations. The output of the signal generator, representing $m(t)$, is sampled by the DSP. The DPWM outputs, i.e., the switching waveforms $x_{ia,b}(t)$, and the ADC input $m(t)$ are measured using the Rigol MSO5354 oscilloscope, with a data length of 40 ms. The acquired data are imported into MATLAB, where $x_{ia,b}(t)$ and $m(t)$ are algebraically transformed so that $x_{\text{eq}}(t)$ and $m_{\text{eq}}(t)$ are obtained, as in (1) and (3). Fast Fourier transform (FFT) of $m_{\text{eq}}(t)$ and $x_{\text{eq}}(t)$ is performed to obtain the spectral components at the

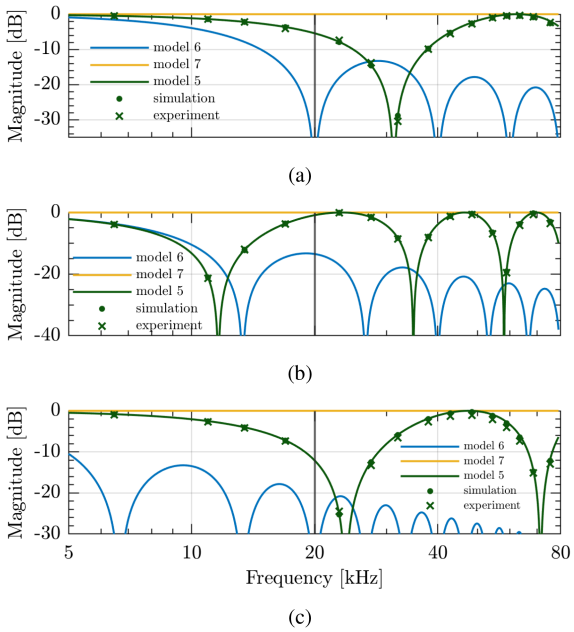

Fig. 9. Magnitude of the DPWM's frequency response obtained from different small-signal models, and simulated and experimental FRMs. (a) U-MSDU-DPWM at $M = 0.66$. (b) BPS-MSDU-DPWM at $M = 0.79$. (c) UPS-MSDU-DPWM at $M = 0.57$. The gray vertical line marks the NF.

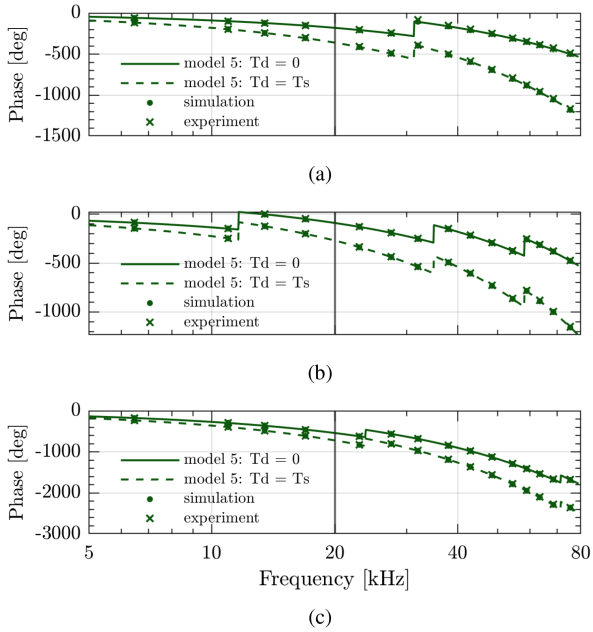

Fig. 10. Phase of the DPWM's frequency response, with $T_d = T_s$ and $T_d = 0$, obtained from the proposed model, and simulated and experimental FRMs. (a) U-MSDU-DPWM at $M = 0.66$. (b) BPS-MSDU-DPWM at $M = 0.79$. (c) UPS-MSDU-DPWM at $M = 0.57$. The gray vertical line marks the NF.

perturbation frequency f_p. The ratio between these components determines the frequency response of the DPWM at f_p.

The experimental and simulated FRMs of the DPWMs are compared with the analytical models, both those derived in this article and those typically used in the literature.

First, results for MSMU strategies are presented. DSDU-B-DPWM is also included. In Fig. 7, the magnitudes of the simulated and experimental FRMs are compared with the different small-signal models. It is clearly visible that only the proposed models accurately predict the DPWMs' small-signal dynamics. Phases of the DPWMs' frequency responses, with and without one step computational delay, are compared with the proposed models in Fig. 8. Note that comparison between different models is shown only for magnitude, and not for phase, since all compared models predict the same phase delay. According to the presented results, the proposed models match the simulated and experimental FRMs, up to four times the NF.

The results for MSDU strategies are presented next. In Fig. 9, the magnitudes of the simulated and experimental FRMs are compared with the different small-signal models. As seen, only the proposed MSDU model accurately predicts the modulators' dynamics. Note that even though all MSDU-DPWMs feature the same small-signal model, the results shown in Fig. 9(a)–(c) differ from each other for the following two reasons. First, U-, BPS-, and UPS-DPWMs are all implemented with different f_{pwm}, since the design criterion was to keep the sampling frequency the same. Next, different SSOPs are used to obtain the results in Fig. 9(a)–(c). Phases of the frequency responses for MSDU-DPWMs, with and without one step computational delay, are compared with the proposed model in Fig. 10. An excellent match is achieved between the proposed model, and simulated and experimental FRMs, up to four times the NF.

The presented results showcase that the proposed small-signal models accurately predict the modulators' dynamics in a very wide frequency range. Moreover, the proposed DPWM models are able to predict the dependence of the system properties on the SSOP, which the ZOH and pure delay models are not. For analyses at lower frequencies, up to approximately one sixth of the update frequency, the ZOH, pure delay, and proposed DPWM models can be used indistinguishably, since they result in identical phase response and magnitude response within 1 dB from the unity gain. However, for analysis at higher frequencies, around and above $\frac{f_u}{6}$, the use of the proposed DPWM models is essential to accurately predict the modulator's dynamic response. The importance of accurate high-frequency modeling is evident, for example, in the stability analysis of grid-tied converters [23], [27], which is illustrated in the following section.

V. Application Example

Passivity-based controller design has been shown to be an effective tool that ensures stable operation of the system containing numerous power electronic converters [23], [24]. Using the impedance-based stability approach as a basis, it implies that, in order to prevent the harmonic instability issues, the converter's input admittance should be designed dissipative, i.e., such that its phase is within the range $[-\frac{\pi}{2}, \frac{\pi}{2}]$, in as wide frequency range as possible [24]. Recent studies have shown that destabilization of poorly damped grid resonances might also occur at frequencies near and above the NF [23], [34].

TABLE II
VSC AND CONTROL LOOP PARAMETERS

VSC	Label	Value	Unit
Nominal power	P_n	3	kW
Nominal dc-link voltage	E	400	V
Nominal PCC voltage	V_g^{rms}	230	V
Filter inductance	L	2.5	mH
Fundamental frequency	f_1	50	Hz
Switching frequency	f_{pwm}	10	kHz
Dead-time	$\frac{t_{\text{dt}}}{T_{\text{pwm}}}$	1	%
Control loop	**label**	**value**	**unit**
Sampling frequency	f_s	40	kHz
Crossover frequency	f_c	2	kHz

It is shown in [27], that the accurate DPWM model is of vital importance to predict the dependence of the admittance measurements (AMs) on the SSOP. Following the methodology from [27], this section addresses high-frequency admittance modeling of center-pulse sampled grid-following MC-VSCs, to showcase the importance of the DPWM models presented in the previous section.

A. Multiple-Frequency Admittance Model

Using similar mathematical procedures as in [27], it can be shown that cancelation of additional loops induced by the PWM sidebands also holds for the center-pulse sampled MC-VSCs. Thus, an accurate small-signal admittance model of the MC-VSC from Fig. 1 can be obtained by incorporating an appropriate DPWM model from Table I in the following multiple-frequency admittance model [27]

$$Y_m(s) = \frac{G_l(s)}{1 + \frac{H(s)}{1+H_{sb}(s)-H(s)}} \tag{22}$$

where

$$H(s) = \frac{\hat{i}(s)}{\hat{e}(s)} = G_c(s)e^{-sT_s}G_{\text{DPWM}}(s)G_l(s) \tag{23}$$

and

$$H_{sb}(s) = \sum_{h=-\infty}^{\infty} H(s - jh2\pi f_s). \tag{24}$$

The resulting admittance models are verified using a great number of consistent simulated AMs performed at different SSOPs. Due to space limitations, the results are presented only for a single-cell full-bridge VSC employing MSMU-U-DPWM. Experimental AMs are performed for the same case.

B. Simulated Admittance Measurements and Benchmarking

Simulated AMs are performed using MATLAB Simulink environment, in the same way as in [27]. The VSC used for the following validations is modulated using the MSMU-U-DPWM and its hardware parameters are given in Table II. As an example, a proportional-resonant current controller is used. Its s-domain

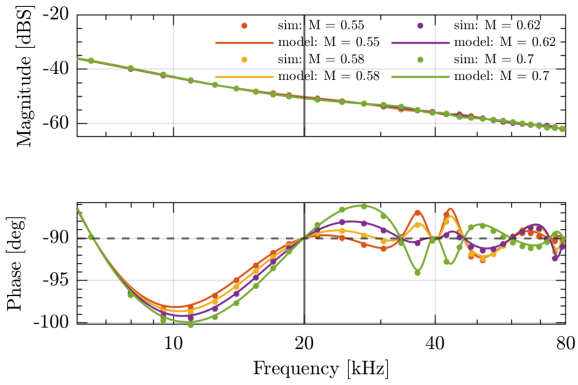

Fig. 11. Comparison among the proposed model and simulated AMs of the VSC modulated using MSMU-U-DPWM at different SSOPs. The gray vertical line marks the NF.

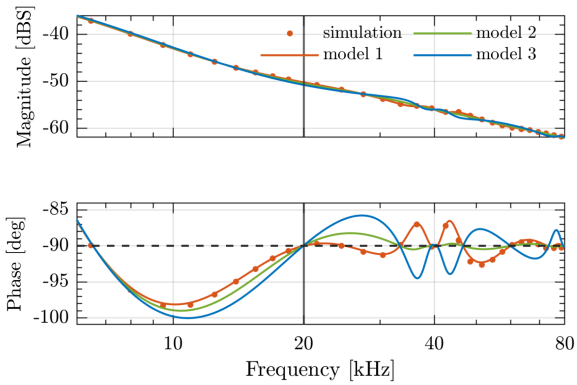

Fig. 12. Comparison among different models and simulated AMs of the VSC modulated using MSMU-U-DPWM at $M = 0.55$. Model 1, 2, and 3 denote admittance model (22) using different DPWM models, denoted by Model 2, 6, and 7 in Table I, respectively. The gray vertical line marks the NF.

transfer function is

$$G_c(s) = \frac{\hat{v}_r(s)}{\hat{e}(s)} = k_p + k_r\frac{s}{s^2 + \omega_1^2} \tag{25}$$

where w_1 is the angular fundamental frequency, k_p and k_r are proportional and resonant gain, respectively, set as in [27] to achieve the crossover frequency $f_c = 0.05f_s$. In Fig. 11, the simulated AMs are compared with the analytical predictions, for different SSOPs. Operation around the different SSOPs is achieved by imposing an adequate bias voltage at the output of the converter, $V_o = (2M - 1)E$. For analytical predictions, the admittance model from (22) is used with the G_{DPWM} from (20). The infinite sum in (22) is replaced by a finite sum of 1000 elements. According to the presented results, the proposed model accurately predicts the AMs up to four times the NF.

In order to illustrate the importance of using the appropriate DPWM model, in Fig. 12, the simulated AMs at $M = 0.55$ are compared against the multiple-frequency admittance model (22) obtained with different DPWM models. The presented results clearly show that neither the ZOH nor the pure delay model can be used to accurately predict AMs for MSMU-U-DPWM. For a precise prediction of the system's behavior, the proposed MSMU-U-DPWM model is essential.

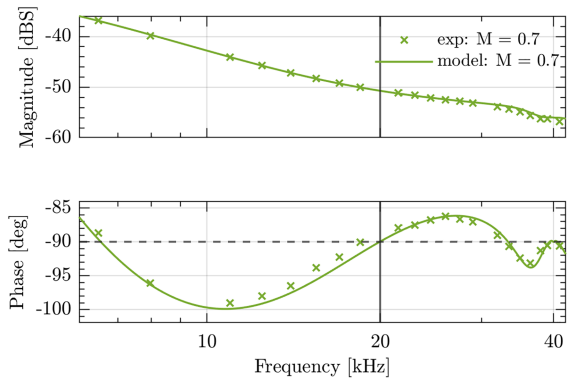

Fig. 13. Comparison between the proposed model and experimental AMs of the VSC modulated using MSMU-U-DPWM at $M = 0.7$. The gray vertical line marks the NF.

C. Experimental Admittance Measurements

As a final verification, an industrial full-bridge VSC modulated using MSMU-U-DPWM and the VSC described in Table II is used for the experimental AMs. The input voltage is provided by the Keysight RP7962 A dc power supply.

The control system is implemented on an NI sbRIO-9606, which is based on a Xilinix Zynq 7020 all programmable system on chip. The inductor current is sensed by a custom interfacing board based on a shunt resistor. The board uses conditioning circuits, a 12-bit AD9226 ADC module by Analog devices, and digital isolators. The DPWM clock runs at 160 MHz.

Admittance is found by injecting a voltage perturbation at the PCC and measuring the current response, as in [27]. The sinusoidal perturbation voltage is generated using the MP118 power operational amplifier from APEX. The perturbation is injected at 21 different frequencies, one at a time, starting from 6 kHz and up to 41 kHz. The perturbation voltage is calculated to obtain at least 100 mA of the perturbation component of i, to achieve a good measurement resolution. The inductor current i and the PCC voltage v_{pcc} are measured using a Tektronix 5 series oscilloscope with a data length of 40 ms. The FFT of i and v_{pcc} is performed in MATLAB to obtain the spectral components of i and v_{pcc} at the perturbation frequency. These components are then used to calculate the admittance at the perturbation frequency. More details on the measurement procedure can be found in [27].

In Fig. 13, the experimental AMs obtained at $M = 0.7$ are compared to the proposed admittance model. As seen, the analytical model predicts the experimental AMs well up to twice the NF. This attests to the accuracy and robustness of the proposed model.

VI. Conclusion

This article addresses accurate small-signal modeling of phase-shifted DPWMs used in MC-VSCs. The operating-point-dependent pulse-to-continuous s-domain transfer functions of U-, BPS-, and UPS-DPWM for MSMU, MSDU, and MSSU strategies are derived analytically and verified in simulations and experimentally, up to four times the NF. Comparison with models typically considered in the literature is provided to highlight the accuracy obtained. It is shown that for low-frequency analyses, the ZOH, pure delay, and proposed DPWM models can be used indistinguishably, since they all predict the same phase response and nearly the same magnitude response, close to unity. However, as the frequencies of interest approach one-sixth of the update frequency, the use of the presented DPWM models becomes essential for system modeling. As an application example, which illustrates the importance of accurate DPWM models, the admittance of a single-cell, full-bridge, VSC modulated using MSMU-U-DPWM is modeled, simulated, and experimentally measured.

Appendix A

Following the same methodology as for MSMU and MSDU, small-signal models of MSSU-BPS-DPWM and MSSU-UPS-DPWM are derived, for the arbitrarily chosen symmetric-off-time modulation [28]

$$G_{\text{DPWM}}^{\text{MSSU-BPS}}(s) = \frac{1}{2}\left(e^{-sM\frac{T_{\text{pwm}}}{2}} + e^{-s(2-M)\frac{T_{\text{pwm}}}{2}}\right) \tag{26}$$

$$G_{\text{DPWM}}^{\text{MSSU-UPS}}(s) = \frac{1}{4}\left(e^{-sM\frac{T_{\text{pwm}}}{2}} + e^{-s(1-M)\frac{T_{\text{pwm}}}{2}} + e^{-s(1+M)\frac{T_{\text{pwm}}}{2}} + e^{-s(2-M)\frac{T_{\text{pwm}}}{2}}\right). \tag{27}$$

Similarly to the MSDU, the MSSU models do not depend on the number of cells. Thus, (26) and (27) are also valid for the case of a single cell, which is in agreement with the results from [26]. As seen from (26) and (27), compared to MSDU, the MSSU strategy introduces two times larger modulation delay. The derived MSSU-DPWM models are verified by comparing them with the simulated FRMs, up to four times the NF. The results are not shown because of space limitations.

Appendix B

In order to avoid shoot-through faults within one leg of the converter, the dead-time is introduced. With the goal of providing an insight into the impact of the dead-time on DPWM's small-signal dynamics, an approximate representation of dead-time effect is considered [21]. During dead-time, the switched-node voltage is assumed to be constant and defined by the sign of the output current I. Although this representation is often used in the literature, it is important to note that it neglects nonlinear phenomena that may appear [35]. Since, due to dead-time, the cell's output voltage v_{oi} is no longer defined only by x_{ai}, x_{bi}, and E, the output voltage v_o must be used instead of x_{eq} in (6)

$$G_{\text{DPWM}}^{\text{DT}}(s) = \frac{\hat{v}_o(s)}{\hat{v}_d(s)} = \frac{\hat{v}_o(s)}{2NE\hat{m}(s)}. \tag{28}$$

Using the same methodology as in Section III, general expression for the extended DPWM model, which includes dead-time, is obtained

$$G_{\text{DPWM}}^{\text{DT}}(s) = \frac{1}{2}\left(e^{-s\left(\tau_R + t_{\text{DT}}\frac{\text{sgn}(I)+1}{2}\right)} + e^{-s\left(\tau_F - t_{\text{DT}}\frac{\text{sgn}(I)-1}{2}\right)}\right) \tag{29}$$

where sgn is the sign function, t_{DT} is the imposed dead-time value, and τ_R and τ_F are determined based on the chosen modulation and control strategy, just like in Section III. By

substituting the appropriate values of τ_R and τ_F in (29), the extended DPWM models can be obtained for all considered MSMU- and MSDU-DPWMs. Substitution of $t_{\rm DT} = 0$ in (29) yields the same expressions as those reported in Table I.

The proposed extended DPWM models are verified for several different dead-time values and both signs of the output current by comparing them to the simulated FRMs, up to four times the NF. The results are not shown because of space limitations. It was shown that for dead-time values below $t_{\rm DT} \approx 0.01 T_{\rm pwm}$, the impact on the modulator's small-signal dynamics is negligible. Nevertheless, it should be noted that the model from (29) does not take into account the nonlinear impact of the dead-time, which affects the damping of the system [35].

REFERENCES

[1] M. Malinowski, K. Gopakumar, J. Rodriguez, and M. A. Pérez, "A survey on cascaded multilevel inverters," *IEEE Trans. Ind. Electron.*, vol. 57, no. 7, pp. 2197–2206, Jul. 2010.

[2] B. Li, R. Yang, D. Xu, G. Wang, W. Wang, and D. Xu, "Analysis of the phase-shifted carrier modulation for modular multilevel converters," *IEEE Trans. Power Electron.*, vol. 30, no. 1, pp. 297–310, Jan. 2015.

[3] J. Ma, X. Wang, F. Blaabjerg, W. Song, S. Wang, and T. Liu, "Multisampling method for single-phase grid-connected cascaded H-bridge inverters," *IEEE Trans. Ind. Electron.*, vol. 67, no. 10, pp. 8322–8334, Oct. 2020.

[4] R. H. Wilkinson, T. A. Meynard, and H. d. T. Mouton, "Natural balance of multicell converters: The general case," *IEEE Trans. Power Electron.*, vol. 21, no. 6, pp. 1658–1666, Nov. 2006.

[5] O. Garcia, P. Zumel, A. de Castro, and A. Cobos, "Automotive DC-DC bidirectional converter made with many interleaved buck stages," *IEEE Trans. Power Electron.*, vol. 21, no. 3, pp. 578–586, May 2006.

[6] B. Miwa, D. Otten, and M. Schlecht, "High efficiency power factor correction using interleaving techniques," in *Proc. 7th Annu. Appl. Power Electron. Conf. Expo.*, 1992, pp. 557–568.

[7] X. Zhang and J. W. Spencer, "Study of multisampled multilevel inverters to improve control performance," *IEEE Trans. Power Electron.*, vol. 27, no. 11, pp. 4409–4416, Nov. 2012.

[8] G. Bonanno and L. Corradini, "Digital predictive current-mode control of three-level flying capacitor buck converters," *IEEE Trans. Power Electron.*, vol. 36, no. 4, pp. 4697–4710, Apr. 2021.

[9] Y. Qiu, M. Xu, K. Yao, J. Sun, and F. Lee, "Multifrequency small-signal model for buck and multiphase buck converters," *IEEE Trans. Power Electron.*, vol. 21, no. 5, pp. 1185–1192, Sep. 2006.

[10] Y. Li, Y. Wang, and B. Q. Li, "Generalized theory of phase-shifted carrier PWM for cascaded H-bridge converters and modular multilevel converters," *IEEE Trans. Emerg. Sel. Topics Power Electron.*, vol. 4, no. 2, pp. 589–605, Jun. 2016.

[11] B. McGrath and D. Holmes, "Multicarrier PWM strategies for multilevel inverters," *IEEE Trans. Ind. Electron.*, vol. 49, no. 4, pp. 858–867, Aug. 2002.

[12] Y. Liang and C. Nwankpa, "A new type of STATCOM based on cascading voltage-source inverters with phase-shifted unipolar SPWM," *IEEE Trans. Ind. Appl.*, vol. 35, no. 5, pp. 1118–1123, Sep./Oct. 1999.

[13] G. Joos, X. Huang, and B. T. Ooi, "Direct-coupled multilevel cascaded series VAR compensators," in *Proc. 32nd Annu. Meeting Ind. Appl. Soc.*, 1997, vol. 2, pp. 1608–1615.

[14] D. G. Holmes and T. A. Lipo, "Modulation of one inverter phase leg," in *Pulse Width Modulation for Power Converters: Principles and Practice*. New York, NY, USA: Wiley-IEEE Press, 2003, pp. 95–153.

[15] J. Yang et al., "Carrier-based digital PWM and multirate technique of a cascaded H-bridge converter for power electronic traction transformers," *IEEE Trans. Emerg. Sel. Topics Power Electron.*, vol. 7, no. 2, pp. 1207–1223, Jun. 2019.

[16] J. I. Y. Ota, Y. Shibano, N. Niimura, and H. Akagi, "A phase-shifted-PWM D-STATCOM using a modular multilevel cascade converter (SSBC)–Part I: Modeling, analysis, and design of current control," *IEEE Trans. Ind. Appl.*, vol. 51, no. 1, pp. 279–288, Jan./Feb. 2015.

[17] G. Walker and G. Ledwich, "Bandwidth considerations for multilevel converters," *IEEE Trans. Power Electron.*, vol. 14, no. 1, pp. 74–81, Jan. 1999.

[18] J. Ma, X. Wang, F. Blaabjerg, W. Song, S. Wang, and T. Liu, "Real-time calculation method for single-phase cascaded h-bridge inverters based on phase-shifted carrier pulsewidth modulation," *IEEE Trans. Power Electron.*, vol. 35, no. 1, pp. 977–987, Jan. 2020.

[19] H. Fujita, "A single-phase active filter using an H-bridge PWM converter with a sampling frequency quadruple of the switching frequency," *IEEE Trans. Power Electron.*, vol. 24, no. 4, pp. 934–941, Apr. 2009.

[20] I. Z. Petric, P. Mattavelli, and S. Buso, "Investigation of nonlinearities introduced by multi-sampled pulsewidth modulators," *IEEE Trans. Power Electron.*, vol. 37, no. 3, pp. 2538–2550, Mar. 2022.

[21] S. Buso and P. Mattavelli, *Digital Control in Power Electronics*, 2nd ed. San Rafael, CA, USA: Morgan & Claypool, 2015.

[22] G. Walker, "Digitally-implemented naturally sampled PWM suitable for multilevel converter control," *IEEE Trans. Power Electron.*, vol. 18, no. 6, pp. 1322–1329, Nov. 2003.

[23] L. Harnefors, R. Finger, X. Wang, H. Bai, and F. Blaabjerg, "VSC input-admittance modeling and analysis above the Nyquist frequency for passivity-based stability assessment," *IEEE Trans. Ind. Electron.*, vol. 64, no. 8, pp. 6362–6370, Aug. 2017.

[24] L. Harnefors, X. Wang, A. G. Yepes, and F. Blaabjerg, "Passivity-based stability assessment of grid-connected VSCs—An overview," *IEEE Trans. Emerg. Sel. Topics Power Electron.*, vol. 4, no. 1, pp. 116–125, Mar. 2016.

[25] I. Z. Petric, P. Mattavelli, and S. Buso, "Multi-sampled grid-connected VSCs: A path toward inherent admittance passivity," *IEEE Trans. Power Electron.*, vol. 37, no. 7, pp. 7675–7687, Jul. 2022.

[26] D. Van de Sype, K. De Gusseme, A. Van den Bossche, and J. Melkebeek, "Small-signal laplace-domain analysis of uniformly-sampled pulse-width modulators," in *Proc. IEEE 35th Annu. Power Electron. Spec. Conf.*, 2004, vol. 6, pp. 4292–4298.

[27] R. Cvetanovic, I. Z. Petric, P. Mattavelli, and S. Buso, "Accurate high-frequency modeling of the input admittance of PWM grid-connected VSCs," *IEEE Trans. Power Electron.*, vol. 37, no. 9, pp. 10534–10545, Sep. 2022.

[28] D. VandeSype, K. DeGusseme, F. DeBelie, A. VandenBossche, and J. Melkebeek, "Small-signal z-domain analysis of digitally controlled converters," *IEEE Trans. Power Electron.*, vol. 21, no. 2, pp. 470–478, Mar. 2006.

[29] L. Corradini and P. Mattavelli, "Modeling of multisampled pulse width modulators for digitally controlled DC–DC converters," *IEEE Trans. Power Electron.*, vol. 23, no. 4, pp. 1839–1847, Jul. 2008.

[30] M. H. Hedayati and V. John, "Filter configuration and PWM method for single-phase inverters with reduced conducted EMI noise," *IEEE Trans. Ind. Appl.*, vol. 51, no. 4, pp. 3236–3243, Jul.-Aug. 2015.

[31] D. Holmes and B. McGrath, "Opportunities for harmonic cancellation with carrier-based PWM for a two-level and multilevel cascaded inverters," *IEEE Trans. Ind. Appl.*, vol. 37, no. 2, pp. 574–582, Mar./Apr. 2001.

[32] L. Corradini, D. Maksimovic, P. Mattavelli, and Z. Regan, *Digital Control of High-Frequency Switched-Mode Power Converters*. New York, NY, USA: Wiley-IEEE Press, 2015.

[33] K. J. Åström and B. Wittenmark, *Computer-Controlled Systems: Theory and Design*. Chelmsford, MA, USA: Courier Corporation, 2013, pp. 269–271.

[34] I. Z. Petric, P. Mattavelli, and S. Buso, "Passivation of grid-following VSCs: A comparison between active damping and multi-sampled PWM," *IEEE Trans. Power Electron.*, vol. 37, no. 11, pp. 13205–13216, Nov. 2022.

[35] M. Berg, T. Messo, T. Roinila, and P. Mattavelli, "Deadtime impact on the small-signal output impedance of single-phase power electronic converters," in *Proc. 20th Workshop Control Model. Power Electron.*, 2019, pp. 1–8.

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