Enablers for Overcurrent Capability of Silicon-Carbide-Based Power Converters: An Overview

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***Abstract*—With the increase in penetration of power electronic converters in the power systems, a demand for overcurrent/ overloading capability has risen for the fault clearance duration. This article gives an overview of the limiting factors and the recent technologies for the overcurrent performance of SiC power modules in power electronics converters. It presents the limitations produced at the power module level by packaging materials, which include semiconductor chips, substrates, metallization, bonding techniques, die attach, and encapsulation materials. Specifically, technologies for overcurrent related temperatures in excess of 200 °C are discussed. This article also discusses potential technologies, which have been proven or may be potential candidates for improving the safe operating area. The discussed technologies are use of phase-change materials below the semiconductor chip, Peltier elements, new layouts of the power modules, control and modulation techniques for converters. Special attention has been given to an overview of various potential phase-change materials, which can be considered for high-temperature operations.**

***Index Terms*—Bonding techniques, high temperature, new layouts, overcurrent (OC), packaging, parasites, phase-change materials (PCMs), power modules, wide band gap semiconductors.**

I. Introduction

RENEWABLE energy sources (RES) play a critical role in reducing the emissions of carbon dioxide [1]. It is, therefore, likely that the number of RES will increase in most power grids, and that RES will dominate the power generation in some grids (at least occasionally). At present, power generation units based on both wind and solar cells have power-electronics interfaces toward the power grid. Such interfaces are typically two-level or multilevel voltage source inverters (VSIs) based on insulated-gate bipolar transistor (IGBT) technology. The characteristics of RES are quite different compared to conventional synchronous generators from several points of view. The most important difference is that synchronous generators can endure several minutes of overcurrent (OC), whereas IGBTs can withstand OC for approximately one millisecond. For longer durations of OC, the increased current will generate so much heat that the maximum temperature is exceeded. This is due to the insufficient thermal capacity of the chip/s, and heat conduction to adjacent material is not sufficiently effective in this timeframe. A simple solution to this is to increase the chip area by increasing the chip size or the number of chips. In case of short-circuit faults in the grid, therefore, the control system of the VSI would try to keep the output current below a specified maximum current. If this is not successful, the VSI will trip in order to prevent the semiconductor chips of the IGBTs and other components of the VSI from overheating (hence, saving them from potential failures). Consequently, protection relays, which rely on the fault current exceeding a certain tripping value, may not detect the fault. Another problem related to the reduction of fault currents from VSIs is that the point of connection voltage drops to a much lower value than that with sufficient reactive current provided. This may lead to tripping of both sensitive loads, such as thyristor-controlled dc motor drives, and other RES, which may have problems to identify to what voltage they should synchronize with. This situation may last for approximately 200 ms (for unsymmetrical faults [2]), until the circuit breakers have cleared the fault. From the grid security point-of-view, the fault handling becomes more challenging with the higher proportion of RES in comparison to the legacy power grids with conventional synchronous generators.

When planning for the future, it tends to be more common for transmission and distribution system owners to foresee an ever more difficult scenario regarding the aforementioned fault

Manuscript received 28 January 2022; revised 22 July 2022 and 7 October 2022; accepted 11 November 2022. Date of publication 21 November 2022; date of current version 26 December 2022. The work was supported by the Hitachi Energy Research and Swedish Energy Agency. Recommended for publication by Associate Editor M. Harfman Todorovic. *(Corresponding author: Shubhangi Bhadoria.)*

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Color versions of one or more figures in this article are available at https://doi.org/10.1109/TPEL.2022.3223730.

Digital Object Identifier 10.1109/TPEL.2022.3223730

TABLE I
DURATIONS FOR OL OR OC

Duration	10 ms	200 ms	1.5 s	5 s	∼7–8 s	7 s	10 s	10 min	2 h	7 h	Continuous OL
Overloading	20%	-	30%	16%, 64%	30%	-	15%, 25%	20%	10%, 10%, 31%	10%	10–20%
References	[12]	[13]	[14]	[15], [16]	[11]	[17], [18]	[19],[20]	[21]	[22], [20], [16]	[23]	[24]

handling, as the proportion of RES will increase continuously in the next decades. The lack of OC capability of state-of-the-art VSIs also makes it difficult to provide ancillary services for the power grid during large disturbances, such as giving frequency support and synthetic inertia.

In recent years, silicon-carbide (SiC)-based devices have been introduced [3], [4]. At present, metal oxide field-effect transistors (MOSFETS), junction field-effect transistors (JFETs), and Schottky diodes are available. These devices offer new possibilities regarding design optimization by using the total chip area as a design variable. Contrary to the silicon IGBT, the choice of chip area of available SiC devices is strongly correlated to the efficiency of the VSI because the ON-state resistance is inversely proportional to the chip area. In addition, the area providing heat transport to the chips scales linearly with the chip area. The idea of massive parallel connection to increase the total chip area can potentially yield efficiencies well above 99% [5], and values exceeding 99.5% have been reported [6]. Contrary to what one might expect, the aggregated commutation inductance of the circuit is reduced when using massive parallel connection despite the fact that the physical area increases. Efficiency values exceeding 99.5% should be attractive if life-cycle costs are evaluated before purchase. The large total chip area also gives excellent cooling, such that the cost of the cooling system is substantially reduced. Some SiC MOSFET power modules are equipped with SiC Schottky antiparallel diodes. This practice is not advisable regarding OC capability, since the SiC MOSFET has a fully functional body diode, which is used during the blanking time and adding Schottky diode will consequently not provide any significant benefit. Typically, however, the MOSFET channel will be gated ON when the current is negative. It has also been shown in [7] that adding an antiparallel diode does not increase the surge capability of the body diode. Therefore, from an OC perspective, it is better to use all available chip area for SiC MOSFETS. If an efficiency-based design optimization as described earlier is performed, the chip temperature at rated operation will be well below the maximum allowable chip temperature. This automatically yields a temperature margin, which potentially could be used for OC operation. Depending on various design choices, margins of the order of 50–100 K are possible with a maximum chip temperature of 175 °C. With adapted designs of the semiconductor packaging, significantly higher maximum temperatures are possible. This could, potentially, yield temperature margins up to 200 K. Several other methods for enabling OC capability can also be considered. Adding a suitable heat-absorbing material (for instance copper) on the top surface of the semiconductor chip is one alternative. Phase-change materials (PCMs) can also be used to clamp the temperature for a specific duration [8]. It may also be possible to introduce Peltier elements into the package [9]. OC capability may also be enabled through control [10] of the VSI, or by temporarily reducing the switching frequency. For a proper design, it is necessary to review metallizations, die attach materials, bond wire technologies, passivations, ceramic substrates, and encapsulation materials.

The overload (OL) capability on various time scales has been introduced in the literature (as presented in Table I) and it is influenced mainly by thermal limits of the critical components. The significance of OL capacity is to provide frequency reserve sharing, emergency power, and power oscillations damping [11].

The duration of OC is related to the fault duration. The OC duration depends on whether it is due to a primary frequency reserve (PFR) response or a fault clearance event. However, the exact duration and OC vary for different countries and systems. The maximum activation is 2 s along with duration for PFR from 30 s to 1 h [25]. On the other hand, the fault clearance duration varies from 0.5 to 10 cycles (10–667 ms) depending the severity and location of faults [26], [27], [28], [29], [30].

The purpose of this article is to provide a structured review of all possibilities to achieve OC capability of a grid-connected VSI. Various levels of OC and durations are considered, such that multiple enabling technologies can be evaluated against each other for different cases. This article focuses on the power module package level and briefly discusses the control and modulation of the converter. The information provided is intended to be a valuable starting point for researchers and design engineers aiming for OC capability of power modules and power converters.

The rest of this article is organized as follows. In Section II, advantages of wideband-gap devices are given. In Section III, various components of power modules and their challenges are discussed for OCs. Section IV provides a discussion on the applicability of the described enabling technologies for OC capability. Finally, Section VI concludes this article.

II. SEMICONDUCTOR CHIPS

The main problem with OC for power semiconductor devices is the excessive heat generation and the associated high temperatures. In power semiconductor devices, there is typically a low-doped n-layer with a doping concentration dependent on the maximum blocking voltage. Due to the low doping in silicon based power semiconductor devices, the thermally generated intrinsic carrier concentration may increase to levels close to the doping level at high temperatures. When this occurs, the n-doping is masked by the thermally generated carriers such that the rectifying function of the pn junction disappears. This translates to a nonfunctional power device with an excessive leakage current. This phenomenon can almost be disregarded in SiC [31], because the intrinsic carrier concentration is several

orders of magnitude lower than in silicon and also because higher doping levels can be used in SiC.

In bipolar silicon power devices, there are also other mechanisms that may prevent operation at high currents and temperatures. These include dynamic avalanche, current filamentation, latch-up, and thermal runaway. Among those, thermal runaway is the only phenomenon that can occur in an SiC MOSFET. The driving reason for this is the temperature dependent ON-state resistance.

When comparing the characteristics of a silicon IGBT with an SiC MOSFET from an OC perspective, there are five remaining differences, which have not been covered above. The first is that SiC has a three times higher thermal conductivity than Si [32], which means that heat generated during the OC event is transported away much more effectively, and that uneven temperature distributions will be less prominent in SiC than in Si. The second difference is that the oxide layer of an SiC MOSFET is less stable than the oxide layer of an Si IGBT for several reasons [33]. Unfortunately, high temperatures have shown to be very harmful for oxide layers in SiC MOSFETS [34], [35] and, therefore, this is one of the limiting factors for OC capability at present. The third difference is that SiC has a much higher Young's modulus than Si [36], [37], which implies that an SiC die is much stiffer than its Si counterpart, and that this difference in stiffness results in larger thermomechanical stresses, especially in the die attach below the corners of the chip during OC events [38]. This problem is accentuated as the chip size increases and, hence, it relates to the fourth difference, which is that SiC chips at present are typically smaller than Si chips due to material and process-related yield issues [39]. Accordingly, some of the stress issues can be alleviated by the smaller chips in SiC. The fifth and final difference is that the temperature coefficient of the ON-state resistance of SiC MOSFETS may be lower than that of corresponding Si IGBTs [32]. The main reason for this is that the channel below the oxide layer of an SiC MOSFET is not ideal, resulting in a comparably high channel resistance masking the temperature coefficient of the bulk SiC of the drift layer. Consequently, low-voltage SiC MOSFETS may have very low thermal coefficients for the ON-state resistances [40], a fact that is beneficial during OC events because it reduces the risk for thermal runaway. A high-voltage SiC MOSFET may, however, not exhibit this phenomenon because almost the entire voltage drop is associated with the drift layer. On the other hand, also an Si IGBT for high voltages has a higher thermal coefficient of the ON-state voltage because of the thick drift layer and the associated low doping level.

All these reasons discussed earlier give differences in thermal response of SiC MOSFETS and Si IGBTs during transients. However, the temperature change of SiC MOSFET would be higher because of the smaller size of the chip [41], [42]. The deciding factor is that the temperature margin during OC is much higher for SiC MOSFETS (about 400 K) and heat removal is quicker and more effective in SiC devices.

Excessive OCs can be very harmful for SiC MOSFETS. During short-circuits temperatures exceeding 300 °C close to the top-side of the chip can occur already after 500 ns [43]. If the current is not turned OFF sufficiently rapidly, the oxide layer, source metallization, or top-side passivation may suffer permanent damage, either as a single-event burnout or as a gradual decay of performance following repetitive stress. Also OCs through the body diode may be harmful, but the current levels have to be so high that voltage drops exceeding 10 V are obtained [7]. At present, the weakest spots of an SiC MOSFET from an OC perspective are the gate oxide, the top side metallization, and bond-wires. From short-circuit tests, it has been observed that the device fails either as a result of gate-oxide breakdown [44] (with possible subsequent thermal ruanway) or top-metallization and bond wire fusion. During transient heating, therefore, cooling of the top side of the chip is likely to be significantly more effective than conventional bottom-side cooling. However, the interdigitated structure of the top side with gate and source metallizations makes cooling of the top side intricate.

Nevertheless, it is the opinion of the authors that the development of the manufacturing processes of SiC MOSFETS is so rapid currently that the maximum operating temperatures will increase from today's 175 °C to 250 °C within ten years [45], [46], [47].

Critical energy over the chip area is defined as the amount of heat energy (generated by high-temperature operation or OC operation) required in order to cause permanent failure of power modules. This concept is also utilized to check the short-circuit capability [43], [48]. The normal operation of the semiconductor keeps the parameters of the semiconductor die and the components of the power module below the critical values (corresponding to the critical energy) so that it has the specified lifetime. OC operation causes the module to reach above the critical energy resulting in the decrease in the standard lifetime. Hence, modifications at the module level and at the converter level are needed in order to keep the operation of the module and semiconductor die below the critical energy point, as shown in Fig. 1.

III. Challenges for OC: Packaging Materials

The structure of a basic power module can be described, as shown in Fig. 2. It consists of a semiconductor die connected to the external circuit by bondwires, a metallization to connect the chip to the ceramics and a baseplate for transferring the heat to the heat sink. Fig. 2 shows the locations of the emerging technologies in green for OC improvements. The exact temperature distribution across the whole volume of the die depends on the type of device [49] and looks similar for transients and steady state, although with different temperature values [50]. However, the hotspots would be located close to the top surface for SiC MOSFETS and SiC JFETs [49]. Consequently, application of technologies from Fig. 2 on the top side of the chip would be more effective in removing the heat from hotspots. Nevertheless, applying these technologies on the bottom side of the chip would also be good if the top side cannot be implemented because of the power module design. It would also result in reducing the junction temperature and the temperature swing during OCs, leading to increased reliability. For the rest of the power module structure (from chip to heatsink), the temperature would be lower than the chip in steady state as one goes further

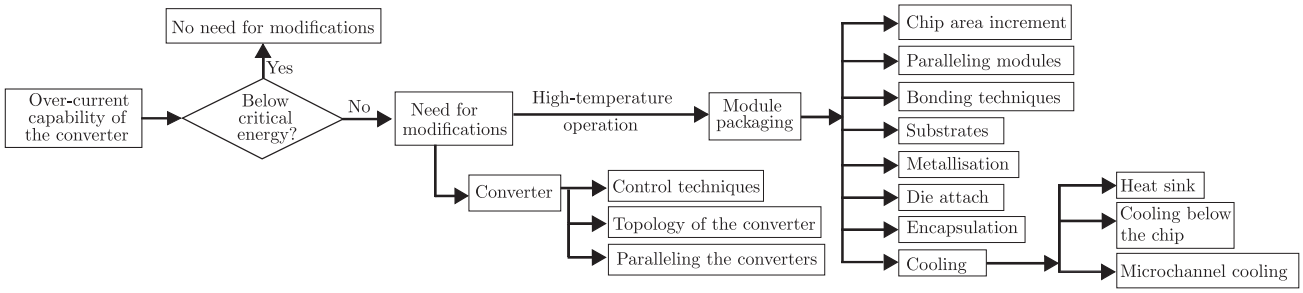

Fig. 1. OC and high-temperature flow diagram according to critical energy concept.

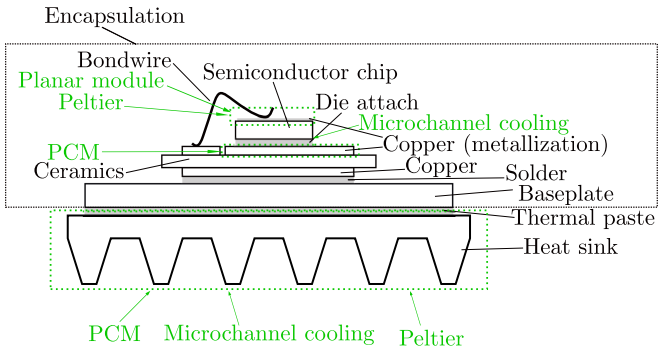

Fig. 2. Emerging technologies and their locations within power modules for OC improvement.

away from chip [51], [52]. The components closer to the chip would be subjected to much higher temperature during OCs while the components further away from the chip would not be affected until a few milliseconds and would be at almost the same temperature as the pre fault value [53], [54].

The main failure mechanisms of power modules subjected to OCs are metallization reconstruction, solder fatigue, corrosion of interconnections [55], heel and toe cracking of the bond wires, bond-wire lift-off, die crack, and fracture [56]. The occurrence of failures has the highest probability at the interface between two materials due to mismatch in the coefficient of thermal expansion (CTE) [55]. Bond wire fatigue, i.e., the degradation in the performance of bond-wires is sensitive to power cycles with duration of seconds whereas solder fatigue and bond-wire failure are sensitive to power cycles with duration of minutes [57]. SiC chips are smaller than Si chips for the same electrical ratings. This results in smaller thermal expansion for identical conditions and better heat distribution on the substrate. SiC has much higher thermal conductivity than Si, the distribution of heat near hot-spots is quicker and better in SiC devices. SiC chips have slightly higher CTE (SiC: 4 ppm/°C) [58], and hence, it is easier to match the CTE with the packaging materials, resulting in lower thermal resistance for steady state [58]. Last but not the least, Young's modulus of SiC (455 GPa) [36] is much higher than Si (188 GPa) [37]. Hence, SiC devices are more susceptible to break or crack upon thermal cycles and reliability should be addressed in future research. Since SiC devices can operate up to 250 °C with a margin for temperature swing of 150 °C or more, different packaging components of

TABLE II
SUBSTRATES PERFORMANCE FOR TEMPERATURE >200 °C

Substrate technology	Temperature variation/junction temperature (°C)	Cycles after	Cycles before
Cu sealed stepped edge/Al_2O_3/DBC [62]	–55–250 in 45 min	850–1200	20
Cu/ZTA/DBC [63]	–40–250	100	26
Cu/Al_2O_3/DBC [59]	35–350	< 250	-
Cu/Si_3N_4/AMB [59]	35–350	250<x<500	< 250
Cu/Si_3N_4/AMB [64]	–55–250 in 60 min	>600	< 100
Al/AlN/DBA [60]	–55–250 in 50 min	>1500	-
Cu/Si_3N_4/AMB [58]	65–200	<2500	35000

TABLE III
DIE ATTACH MATERIALS FOR TEMPERATURE >200 °C

Die attach type	Maximum operating temperature (°C)
Organic die attach [59]	200 (Ag filled die attach)
Solders [59], [86]	400
Diffusion soldering [59]	961 (depending on Ag–Sn content)
Silver nano sintering [59]	961 (care needs to be taken care for silver migration [87])

power modules and their failures due to OCs and the associated high-temperature operations are discussed in this section, such as substrates, bonding techniques, chip metallization, die attach, and encapsulation.

A. Substrates and Their Metallizations

Substrates below the semiconductor chip are either direct bonded copper (DBC), active metal braze (AMB), or direct bonded aluminium (DBA). Substrates are used to provide electric insulation. They also decrease the thermal resistance and, hence, increase the current capacity. Since increase in current in the semiconductor die is directly reflected into increase in temperature in the components of the semiconductor module, analyzing the changes of power modules due to high-temperature operation is equivalent to considering the high-currents/OCs. The number of high-temperature cycles before failure depends on the material of substrate, CTE, the temperature swing, metallization and ceramic thickness, and the bonding technology of the substrate (i.e., DBC, DBA, or AMB) [59], [60], [61].

Table II illustrates the performance of different substrates technology for high temperature and large temperature swings

($> 150\,^{\circ}$C). One of the main reason for failures of substrates is the mismatch of CTEs among different materials. The DBC technology fails under extreme temperatures due to the CTE mismatch between the copper and ceramic (Al_2O_3: 7 ppm/°C, AlN: 4 ppm/°C, Cu: 16 ppm/°C) [63], however, the performance is improved with AMB [59], [64]. An exceptional increase in the reliability is obtained when CTE of the combination (metal and ceramic: 5 ppm/°C) is matched very well with SiC chip (4 ppm/°C) as presented in [58]. It led to an increased number of cycles by 14 times [58].

B. Bonding Techniques

Wire bond and press-pack technologies are the two mounting technologies. The high cost of press-pack technology and the need for a mechanical clamping arrangement makes wire bonds more popular, although press-pack has better reliability, higher power density, and better cooling capability [65]. Wire bond interconnection techniques include ball bonding, wedge bonding, ribbon bonding, and PCB embedded technology [66]. Al wire bonds are the most commonly used in high-power modules [67], [68]. In conventional power modules, bond wires are used to connect semiconductor dies to the external circuit via a substrate. Approximately 25%–30% of the total failures in a module are the result of failing/faulty wire bonds in the conventional temperature range (-30 to $150\,^{\circ}$C) [69]. These failures include lift-off (from toe and heel) and heel cracking. Lift-off is due to the CTE mismtach of Al (23.8 ppm/°C) and Si (2.5 ppm/°C), whereas heel crack is due to the thermo-mechanical stresses, caused by heating of semiconductor chip and Joule self-heating [67], [70], [71].

The current capability of the module due to bond wires depends on at least four factors, i.e.:

1) number of bond wires [66];
2) geometry [69];
3) type of current flowing (AC or DC);
4) material.

One of the most important is the number of bond wires. Insufficient number of bond wires causes oveheating due to large currents flowing in them, leading to burn out of the wires reaching the melting point of metal (mostly Al) and, hence, the failures [66].

However, removing bond wires along with the modification in the metallization can significantly improve the thermal performance of the power module. Ribbon technology leads to an improvement in the power module by increasing its current capacity as demonstrated by Fraunhaufer in Germany [72] and Hitachi ABB Power Grids in Switzerland [73]. Tesla Model 3 also uses SiC modules produced by STMicroelectronics specially designed for improved thermal performance using copper clips connected to the terminal, specially manufactured die attach, and copper baseplate assembled on the pin-fin heatsink [74], [75]. A similar concept with the heavy copper wires along with copper metallization on the top of standard die has demonstrated a superior thermal performance as shown in RoadPaK with SiC devices by Hitachi [76]. Other industries have also implemented similar strips of copper (STMicroelectronics) or silver (Vitesco Technologies), copper blocks just above the semiconductor die (Denso), double sided sintered semiconductor die to the heat sinks (Hitachi) [77]. The connections by strips and blocks not only lead to the removal of bond wires but can also provide some heat capacity during OCs.

C. Chip Metallization

In conventional modules, the chip metallization (typically 3 μm [78]) provides a platform for connecting bond wires and a good electrical connection for the entire chip area [79]. The metallization also provides room for OC and short-circuit energy capability by providing a considerable heat capacity. In [80], for a 1200 V IGBT, changing a thin Al metallization to a thick Cu metallization alone at the top side of the die leads to an increase of 20%–25% of the short-circuit energy. Another modified metallization is introduced in [78]. An additional layer of thicker ($\gg 10$ μm) metallization layer of Cu, referred to as Danfoss bond buffer, sintered on top of an IGBT leads to an increment of short-circuit capability by 21% in time and energy by 24%. It could withstand 4.5 times OC for 14.9 μs.

Metallization may pose a limit on the operation of high/short-circuit currents because of metal fusion beyond the melting point of metallization (660–1000 °C) [81]. The metal fusion is caused by the heat, for semiconductor devices with high current capability, such as JFETs and BJTs as observed in [82] at 660 °C since they do not have limiting gate oxide like MOSFET.

Thermal cycles with large temperature swings can cause degradation in the performance of metallization [83], [84]. An investigation for MOSFETS was performed with a constant OC of twice the nominal value for 5.7 ms in [85]. Because of an increase in metallization resistance by 10 times in 250 k cycles, the junction temperature increased from 172 to 256 °C, along with a degradation near the source region.

D. Die Attach

Die attach are also called backside interconnects as they connect chip to substrate and substrate to base plate. Die attach materials can play an important role in the current capability and, hence, in high-temperature operation. Conventionally, lead (Pb) based alloys have been used for high-temperature applications. However, because of the environmental hazards by Pb-based materials, alternative materials have been investigated as shown in Table III. They include organic (or epoxy) die attach, traditional solders (tin, copper, silver), diffusion soldering, and silver nano- and micropastes.

Silver sintering has shown the highest thermal conductivity among all die attach techniques [88]. Apart from the performance of the die attach at high temperature, the type of die attach affects the current capability and the short-circuit energy. Silver sintered dies led to an increase in short current energy by 11% as compared to SnAg3.5 solder of 100 μm, as shown in [78]. While in [80], silver sintering or diffusion soldering leads to increase in critical short-circuit energy by 20%–25%. When metallization is accompanied by silver sintering at the back instead of soldering, it leads to an of increment 85%

TABLE IV
ENCAPSULATION MATERIALS FOR TEMPERATURE >200 °C (T_g IS GLASS TRANSITION TEMPERATURE)

Encapsulation material	Maximum temperature/operating range – Values (°C)
Epoxy Resin [93]	Operating temperature–200
Poly (dimethyl diphenyl) siloxane [94]	Maximum operating temperature–265
Silica-filled poly (dimethyl) siloxane [94]	Maximum operating temperature–275
Phenolics resin [95]	Operating range – –250 to 260
Silicones [96]	Continuous maximum operating temperature–260
Poxy-phenolic alloy [96]	Continuous and short term operation–177 and 371
Parylene F [97], [98]	Operating temperature–200
Polyamide [97]	Operating temperature (T_g >260 °C)– >200
Parylene HT [98]	Maximum operating temperature–600
Benzocyclobutene [99]	T_g >350 °C
Cyanate Ester [92]	Application temperature–260 to 280

of short-circuit critical energy [80]. Silver sintering has been applied in SKiNTER Technology of Semikron power modules, which can support its operation as high as its melting point without aging drastically [89], [90].

E. Encapsulation Materials

As long as the overheating is not causing melting of bond wires, the encapsulation material comes next to limit the temperature of the module as a consequence of severe OCs [66]. The module is encapsulated with various materials in order to protect the SiC die from environmental factors, for example, the presence of oxygen, moisture, and various pollutants. The main materials for encapsulation are silicone gel and epoxy resin. In conventional modules with Si dies, encapsulation materials, such as silicone gel with operating temperature up to 175 °C are used. Encapsulation materials for high-temperature include polyparaxylene, acrylic, polyurethane, and epoxy [91]. Table IV shows the various potential encapsulation materials for high-temperature applications of SiC devices. Care should be taken while choosing the encapsulation materials as they could show decline in shear strength [92], degradation upon cycling [93], and generation of voids [59].

IV. ENABLING TECHNOLOGIES FOR OC CAPABILITY

This section discusses multiple ways to handle OC for different time-scales using metals, PCMs, microchannel cooling, Peltier elements, modified power modules, and adapted converter control.

A. Adding Materials on the Top of the Chip

Heat absorbing materials can be placed both below and on the top of the semiconductor chip. Below is easier to achieve because the bottom of the chip has one big drain metallization, but the added material will increase the thermal resistance for the cooling path during nominal operations. Adding material on the top of the chip is complicated because of the interdigitated top-side metallization. However, if this piece of material is electrically conductive, it can also be used as a conductor for the source current, i.e., acting like an additional metallization.

TABLE V
THERMO-PHYSICAL PROPERTIES OF IMPORTANT PCMS AND MATERIALS FOR HIGH-TEMPERATURE OPERATIONS OF >200 °C IN SOLID (S) AND LIQUID (L) PHASE IF APPLICABLE [101]

Compound (Mass ratio)	MP* (°C)	ME* (kJ/kg)	Specific heat (J/(kg·K))	Thermal conductivity (W/(m·K))	Density (kg/m^3)
$LiNO_3$–NaCl (87–13)	208	369	1540 (s), 1560 (l)	1.350 (s), 0.630 (l)	2350
KNO_3–KOH (80–20)	214	83	1030 (s), 1350 (l)	0.880 (s), 0.540 (l)	1905
KNO_3–$NaNaO_3$ (55–45)	222	110	1010 (s), 1490 (l)	0.730 (s), 0.510 (l)	2028
LiBr–$LiNO_3$ (27–73)	228	279	1340 (s), 1380 (l)	1.140 (s), 0.570 (l)	2603
LiOH–$NaNO_3$–NaOH (6–67–27)	230	184	1300 (s), 2000 (l)	0.780 (s), 0.670 (l)	2154
$NaNO_2$–$NaNO_3$ (55–45)	233	163	1310 (s), 2130 (l)	0.590 (s), 0.640 (l)	2210
$CaCl_2$–$LiNO_3$ (13-87)	238	317	1500 (s), 1530 (l)	1.370 (s), 0.690 (l)	2362
LiCl–$LiNO_3$ (9–91)	244	342	1580 (s), 1610 (l)	1.370 (s), 0.640 (l)	2351
$NaNO_3$–NaOH (86–14)	250	160	1190 (s), 1860 (l)	0.660 (s), 0.600 (l)	2241
Copper (Cu)	1084.6	-	381 (s)	387.6 (s)	8978
Silver (Ag)	961.9	-	237 (s)	429 (s)	10490
Gold (Au)	1064.4	-	129 (s)	401.0 (s)	19300
Aliminium (Al)	660.2	-	910 (s)	237.0 (s)	2800
Nickel (Ni)	1450.0	-	440 (s)	90.3 (s)	8910
Diamond [102]	900*	-	540 (s) [103]	2500 (s)	3500

*Burn out of diamond at 900 °C and melting point is 3550 °C
*MP: Melting point, ME: Melting enthalpy

There are two classes of materials, which can be used to absorb the transient heat generation [100]. First, sensible heat materials are materials that do not change their physical state upon heat absorption. Only an increase in temperature is observed because the operating temperature is significantly below the melting point. They generally include metals, diamond, and graphite. Second, PCMs are types of materials that change their physical state by absorbing heat (equal to latent heat or melting enthalpy) resulting in almost constant temperature during the phase-change phenomenon. It results in an overall smaller temperature change as compared to sensible heat storage, which does not change phase on heat addition/absorption [100]. Important thermo-physical properties of relevant metals and PCMs for the operating temperature 250 °C are presented in Table V.

1) Basic Response of a Sensible Heat Storage During OC: The example shown in Fig. 3 assuming a homogeneous adiabatic heating of a heat absorbing material attached ideally on top of a semiconductor chip gives a first indication of what is achievable in terms of slowing down the rate of rise of the surface temperature of the chip during an OC event. The example is, however, massively oversimplified, especially as the thickness of the attached top-side material increases. The other sides of the heat absorbing material (those ones not in contact with heating

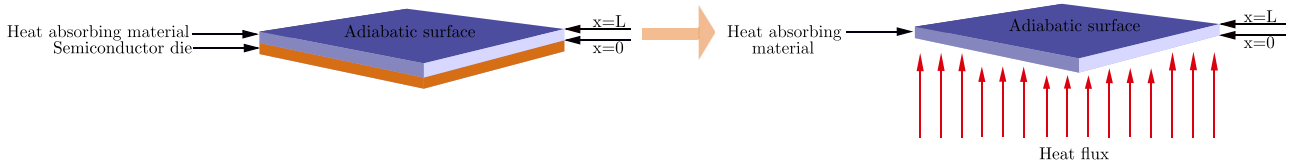

Fig. 3. Arrangement of material just above the semiconductor die during OC operation and its equivalent.

material) are assumed adiabatic surfaces since the duration of heat pulses is short (in ms). This assumption is a worst case scenario, which overestimates the temperature compared to the real case. The longer the duration of the heat pulse, the larger the overestimation would be because of the neglected heat transfer across the assumed adiabatic surfaces. Assuming a homogeneous heating of the attached top-side material actually implies the assumption of infinite thermal conductivity. By introducing a finite thermal conductivity, a significantly more realistic model is created. The complexity of the problem is, however, also dramatically increased because of the transient heat-flow equation. Equation (1), which describes the temperature (T) in the volume defined by the co-ordinates x, y, and z as a function of time t [104], is given by

$$\frac{\partial^2 T}{\partial x^2}+\frac{\partial^2 T}{\partial y^2}+\frac{\partial^2 T}{\partial z^2}=\frac{1}{\alpha}\frac{\partial T}{\partial t} \tag{1}$$

where α is the thermal diffusivity. This partial differential equation, which excludes heat generation in the body itself, is a special case of the diffusion equation. Fortunately, it is possible to find analytical solutions to this equation for specific geometries, initial conditions, and boundary conditions. The simplest case applicable to the problem with an attached top-side material is a one-dimensional rod, which is thermally isolated on all sides except on the surface, which is attached to the top-side of the chip. For such a simple geometry, the equation simplifies to

$$\frac{\partial^2 T}{\partial x^2}=\frac{1}{\alpha}\frac{\partial T}{\partial t}. \tag{2}$$

On the surface attached to the chip, an initial temperature is specified along with an imposed heat flux $\dot{Q}$ into the rod. For the rest of the geometry only an initial temperature

$$T(x,t=0)=T(x=0,t=0) \tag{3}$$

is specified. Now, the problem is fully defined with initial temperature (T_i), height of the material (L), heat flux in W/m^2 (q''), thermal conductivity (k), density (ρ), specific heat capacity (c), thermal diffusitivity ($\alpha = k/\rho c$), and the solution [105] is given by

$$\theta(X,Fo)=Fo+\frac{X^2}{2}-X+\frac{1}{3}-\frac{2}{\pi^2}\sum_{n=1}^{\infty}\frac{\cos(n\pi X)}{n^2}e^{-(n\pi)^2 Fo} \tag{4}$$

where

$$\theta=\frac{T-T_i}{q''L/k}, X=\frac{x}{L}, Fo=\frac{\alpha t}{L^2}. \tag{5}$$

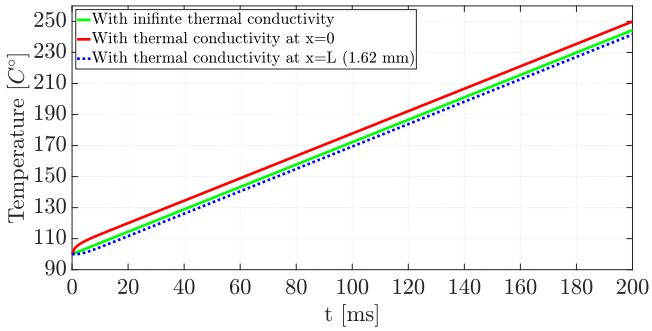

Fig. 4. Cu response: $P = 400$ W/cm^2, h = 1.62 mm (1.45 g).

The abovementioned solution is applicable when there is no internal heat generation and thermo-physical properties, such as specific heat capacity, CTE, thermal conductivity, are assumed constant.

As already mentioned in Section I, it is reasonable to assume that the SiC power devices will be able to operate without failure at temperatures up to 250 °C in a close future. Using (1)–(5), the calculations have been performed for two time scales, i.e., 200 ms and 1.0 s timescale for two times the nominal rating (200 A) and ON-state resistance of 10 m Ω with 100 ° C as initial junction temperature and 250 °C as the limiting temperature for OC in SiC devices. Hence, 400 W (P) of heat flux has been considered for the standard die of 1 cm^2 as assumed future standard.

The thermal response of the additional metallization (Cu here) is shown in Fig. 4 with infinite (resulting in instantaneous distribution of heat across the whole volume) and finite values of thermal conductivities. The height of the metallization (Cu) corresponds to the minimum amount of Cu needed to keep the temperature below 250 °C. As it can be observed in Fig. 4, the temperature in the immediate vicinity to the chip surface (at $x = 0$) is approximately 6 °C higher than the case with infinite thermal conductivity and 10 °C higher than the side of Cu (at $x = L$). The same observation for thermal response of Cu just below the chip has been made using finite-element modeling (FEM) in COMSOL. Similar calculations have been done for the temperature of the eutectic salt $NaNO_3$–NaOH using (1) below its melting point of 250 °C, assuming infinite thermal conductivity and same physical properties even after its melting point. However, the difference in the temperature (1629 °C) between the immediate vicinity to the chip surface and the one with infinite thermal conductivity becomes significant as observed in Fig. 5. The difference is very large for the eutectic salt as compared to the case of Cu because of lower value of thermal conductivity for the eutectic salt. Similar analysis for

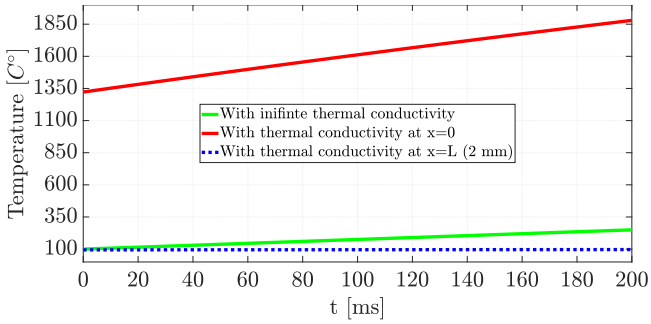

Fig. 5. Eutectic salt ($NaNO_3$–NaOH) response: $P = 400$ W/cm^2, $h = 2$ mm (22.41 g).

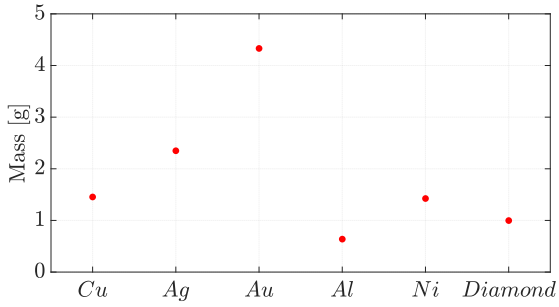

Fig. 6. Comparison of the mass of the materials needed to limit the temperature to 250 °C for 200 ms.

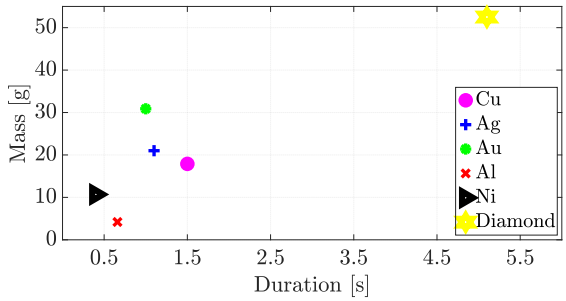

Fig. 7. Mass of the materials needed to limit the temperature to 250 °C for sensible duration for the sensible height.

the PCMs mentioned in Table V can be done using FEM for phase transition and liquid state, however, (4) cannot be used for computing the thermal response as eutectic salts (or any other PCMs) will change their physical state from solid to liquid state after the temperature reaches the melting point. Diamond has been used as an excellent heat spreader [106]. It can be useful for short pulses of few milliseconds because of extremely high thermal conductivity, high melting, and burnout temperatures. Since diamond is an electrical insulator, it will not need special isolation from the electrical circuit and can be placed just below the semiconductor chip. However, if it is placed above the chip, it may be problematic because it would aggravate the current transport from the source metallization. Another interesting material for thermal management is graphene film [107]. It has different thermal conductivity values for in-plane and through-plane directions. In-plane refers to the plane parallel to the graphene film and through-plane refers to the plane perpendicular to the graphene film. It has thermal conductivity upto 5000 W/(m·K) and as low as 0.08 W/(m·K) for in-plane and through-plane, respectively, depending on the production method and physical properties, such as grain size, and impurities. Because of the very high value of in-plane thermal conductivity, it takes the heat and spreads it quickly from the hot-spots in the plane. It results in almost instant removal of heat from hot-spots. Since graphene is an electrical conductor in both (in-plane and through-plane) [108], depending on if it has been placed above or below the chip, electrical isolating material will be needed.

2) Mass of Materials and the Sensible Height: Using (5), Fig. 6 shows the amount of materials needed for keeping the surface close to the semiconductor die (equivalent to junction temperature) below 250 °C for 200 ms. If the amount of material is increased as compared to given in Fig. 6, the temperature can be lower than 250 °C. However, some proportion of the material will not be used as the surface close to the semiconductor chip will be heated up (the temperature depends on the amount of the material) but the other surface will remain at much lower temperature or even at the initial temperature.

The *sensible height* is defined as the minimum height of (PCM) materials needed to keep the temperature within a specific temperature for a given area, chosen as 250 °C in our calculations. If the height is increased beyond the sensible height, there will be no improvement in terms of junction temperature reduction and the duration in seconds. Fig. 7 shows the sensible mass on y-axis (corresponding to the sensible height) and the maximum durations (on x-axis) for two times OC possible with different materials, calculated by (5). The values of sensible mass and height along with the maximum possible duration and the mass needed for 200 ms have been presented in Table VI. The sensible height, mass, and duration should play an important role since the problems of parasitic components in electrical circuit could be prominent with the increase in the materials used at high-frequency operation of converters.

TABLE VI
SUMMARY OF THE CALCULATIONS FOR 200 MS AND SECONDS (SENSIBLE HEAT AND SENSIBLE MASS) OF TWO TIMES OC

Compound	For 200 ms		For seconds (s) range		
	Mass (g)	Height (mm)	Mass (g)	Height (mm)	Duration (s)
Copper (Cu)	1.45	1.6	17.9	20.0	1.50
Silver (Ag)	2.34	2.2	21.0	20.0	1.10
Gold (Au)	4.33	2.2	30.9	16.0	1.00
Aliminium (Al)	0.64	2.3	4.2	15.0	0.66
Nickel (Ni)	1.42	1.6	10.7	12.0	0.40
Diamond	0.99	2.8	52.5	150.0	5.10

3) Application of PCMs for OC Applications: The phase-change process can be classified as solid-solid, solid-liquid, solid-gas, and liquid-gas. Solid- and liquid-gas have been used for extremely limited applications because of the significant change in volume when converted to the gaseous state. Additionally, these materials have a very low thermal conductivity, which

is in the range of 0.2–0.7 W/(m · K), as compared to metals which is in the range of 90–429 W/(m · K) [101]. When evaluating the thermal properties of a PCM, there are primarily four quantities to consider, namely melting temperature, latent heat per unit volume, values of specific heat, and thermal conductivity in the liquid as well as solid state [101]. Melting point should be in the desired operating range and the rest should as high as possible. Desired physical properties include a small variation in volume during the phase change and a high density, which results in small size of storage. Required chemical properties are chemical stability over the operating temperature range, reversibility of freezing/melting cycle, nontoxicity, nonflammability, and nonexplosivity. Cost effectiveness and availability in abundance are also the economic factors to be taken into account. PCMs have been classified as organic, inorganic, and eutectics [101]. Organic PCMs include paraffins and nonparaffin organic compounds. Organic PCMs have low thermal conductivity, high specific heat, low-melting point (in the range of 50–60 °C [109], [110]), and high-volume expansion after melting [109], [110]. Inorganic compounds include salt hydrates, metallic alloys, and metals. Salt hydrates have lower thermal conductivity, higher specific heat, and lower melting points as compared to metals. Eutectic compounds include the combination of two or more compounds with similar melting-points. Eutectic compounds have melting points in the range from 25 to 250 °C, high melting enthalphy, very high specific heat, but lower thermal conductivity as compared to metals. Since the thermal conductivity of eutectic salts is more than hundred times lower as compared to metals, eutectic salts require more time to transfer the same amount of heat as compared to metals. Hence, a reasonable duration of OC when using eutectic salts would be of the order of 1–10 s. Considering all properties of the abovementioned types and metals, metals seem to be the most suitable choices for handling of OCs of SiC power devices for miliseconds range and they will operate entirely in the solid state as they have a much higher melting point as compared to the operating temperature.

The choice of PCM depends on the operating temperature. In [111], various commercial PCMs are described and categorized as follows: organic, solid-solid PCM, hydrated salts, and metallic PCM. Among all, chlorides and eutectic salts are available in the range of melting points of 110–650 °C [112]. In [113], a set of hydroxide and nitrate PCMs are stated to have the same range of melting points while organic PCMs for the range from 150–200 °C are described in [114]. $LiNO_3$–NaCl $(87 - 13)$ has a melting temperature of 208 °C and has the highest phase-change enthalpy (369 kJ/kg), which may prove to be thermally advantageous for junction temperature around 200 °C. As the thermal conductivity of these materials is much lower as compared to pure metals, an adapted mechanical structure will be required to increase the thermal conductivity. These set up include having a metallic mesh around/through the PCM and metallic containers having PCMs in them.

Metallic PCMs (and alloys) have melting points in the same range as that of junction temperature of SiC/Si devices [115]. Hence, they have proven to be advantageous for transient applications during faults.

The application of PCM is investigated to keep the junction temperature below 130 °C for 150% and 300% OCs [8], [116]. This temperature would have been reached for 20% OC in a commercial module without PCM in the same time [116], [117], as compared to OC increased for 3 and 5 p.u. The application of various PCMs for keeping the junction temperature within limits are given in Table VII. From the table, it is clear that metallic PCMs can be significantly useful up to 5 p.u. for three seconds.

The investigated arrangement of PCM with metals for increasing the thermal conductivity of the overall arrangement are shown in Fig. 8. As shown in Table VII, the OC capability for the Si/SiC modules can be increased by using an appropriate quantity of PCM below the chip and hence, the safe operating area (SOA) can be increased beyond the ratings for short durations and large power or thermal transients.

As clear from the abovementioned discussion, the choice of PCM affects significantly the junction temperature, response time, and the quantity required [115]. Phase-change time or the response time is shorter with a smaller amount of PCM while a larger amount increases the thermal capacity. Hence, the optimum quantity of PCM must be chosen for the required operation depending on the duration and % OC. Because of their high thermal conductivity, metal PCMs, and their alloys have shown superior performance in terms of maintaining the temperature on their melting points. The junction temperature for metallic PCMs can be lower by 60–80 °C for very short pulses of even 20 ms than dielectric or organic PCMs for heat fluxes of 888.9–3555.5 W/cm^2. They also have application in fast transient response at time scale of $<$0.1 s, 1 s, 25 s, and 50 s for power levels of 100 [120], 11 [121], 600, and 300 W/cm^2 [122], respectively.

From Figs. 4–7 and Table VII, it is clear that the response time or the heat removal speed from the junction depends on the thermal conductivity of the material used below or above the chip. Metallic PCMs generally have higher thermal conductivity as compared to organic PCMs or Eutectic salts. In order to speed up the thermal performance of PCMs, a container having excellent thermal conductivity should be used, possibly in combination with an inner grid structure to support the heat distribution internally.

Apart from thermal performance, other factors might be important in order to have reliable performance. Sometimes, voiding in PCMs might lead to degraded performance after a number of cycles. This has been reported for metallic PCMs [123], paraffin [124], and eutectic PCMs [125].

In order to achieve OCs without increasing thermal resistance during nominal operation, the bond wires could be replaced by planar connections for source connections and PCM along with its thermally conducting container could be placed above it as shown in Fig. 8(d). It is expected to absorb heat during OCs when the temperature reaches the melting point of PCM. For practical reliable applications, the container of the PCM and other materials should be attached to the die with high-temperature die attach techniques, such as silver sintering. One should also consider modifying the metallization of the chip for reliable interconnection.

TABLE VII
APPLICATION OF PCM JUST BELOW THE CHIP TO KEEP JUNCTION TEMPERATURE BELOW REQUIRED VALUE FOR OC

Type of module and rating	OC, Duration (s)	PCM, Melting point (°C)	Amount of PCM (in gm) per switch	Location of PCM	Improvement in junction temperature	Reference
Semikron SKM50GB12T4 half bridge IGBT, 1200 V, 50 A	1.5 p.u., 30	LM108, 108	3.6	Cu frame with 4 holes below the die	Kept below 130 °C with pre-fault value of 100 °C	[116], [8]
Semikron SKM50GB12T4 half bridge IGBT, 1200 V, 50 A	3 p.u., 3	LM108, 108	3.6	Cu frame with 4 holes below the die	Kept below 130 °C with pre-fault value of 100 °C	[116], [8]
Infineon FF1000R17IE4 half-bridge IGBT (simulated), 1700 V, 1000 A	1.5 p.u., 30	LM108, 108	17.88	Cu frame with 6 holes below the die	Reduction by 20 °C	[116]
Infineon FF1000R17IE4 half-bridge IGBT (simulated), 1700 V, 1000 A	3 p.u., 3	LM108, 108	17.88	Cu frame with 6 holes below the die	Reduction by 20 °C	[116]
Multichip press-pack IGBT/FRD 3300 V, 100 A	1.5 p.u. to 3 p.u., 3	Bismuth base alloy, 60–135	4.1	Molybdenum platelet with 3 holes above the die	Reduction 5.6 °C for 3 pu as compared 1.5 pu	[117]
Multichip press-pack IGBT/FRD 3300 V, 100 A	1.5 p.u. to 5 p.u., 3	Bismuth base alloy, 60–135	4.1	Molybdenum platelet with 3 holes above the die	Reduction by 10.5 °C for 5 pu as compared 1.5 pu	[117]
Infineon F4-50R12KS4 1200 V, 70 A (Simulated)	3 p.u. 10	LM135 and LM150, 135, and 150	50% PCM by volume in metal frame	Metal Frame (19× 19 mm^2) below the chip	Reduced from 300 °C to 178 °C	[118], [119]

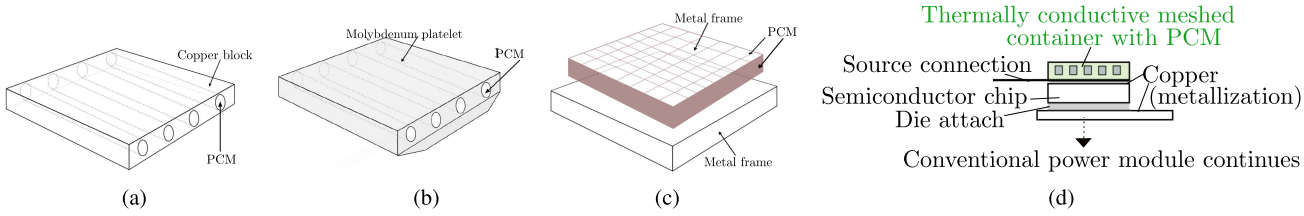

Fig. 8. Combination of PCM and metals in order to have the advantages of PCM and metals at the same time. (a) [8], [116]. (b) [117]. (c) [118], [119]. (d) Proposed solution.

B. Microchannel Cooling

Microchannel cooling refers to the creation of small/thin channels in heatsinks close to the junction or semiconductor buffer. Microchannels can be applied at various levels from the semiconductor die to the system-level. The exact configuration needed depends on the heat flux values and the response time. A fast response with a high heat flux can be achieved by cooling close to the source of heating. A system-level microchannel (or indirect cooling of semiconductor) cooling is one where microchannels are fabricated on pieces of Silicon, to form cold plates that can then be attached to each power device, as presented in [126], [127], and [128]. It has been proved to be effective for heat fluxes up to 100 W/cm^2. The heat sink with microchannels is located on another side of the PCB. The package level microchannels are made on an Si substrate in which the Si substrate functions as a microfluidic heat sink. Package-level cooling is capable of cooling for heat fluxes up to 500 W/cm^2 [129] while microchannels closer to the semiconductor die are effective for heat fluxes up to 2000 W/cm^2 [130], [131]. In [131], Cu and diamond have been used just below the semiconductor for instant removal of heat, resulting in reduction of thermal resistance. The value of temperature reduction depends on the thickness and relative thickness of the substrate with respect to the radius of the substrate of the wafer. The value of thermal resistance decreases with the thickness of the microchannels in the substrate of power module. In [130], the cooling has been done just below the semiconductor in an Si substrate. These three microchannel cooling concepts for different heat fluxes are shown in Fig. 9 [132]. These channels have led to an increment in the power density of a prototype converter. However, these channels will be operational even during normal operation and result in increased power density of the converters. Another advantage of this concept is that the temperature swing reduces, which promotes lifetime.

These concepts of mircochannel cooling might have the possibility to limit the junction temperature during OCs if implemented with a controller. The controller can be used to change the coolant flow depending on the heating of the semiconductor of the chip. There are two possibilities to use controller. First, the speed (hence, the volume) of coolant flowing can be increased when OC occurs and decreased when OC operation is finished. Second, the coolant flow can be switched ON and OFF in order to activate and deactivate the microchannel cooling, respectively. Typically, the current controller of the converter orders the current increase in advance before the heat in the chip rises, so the reference value for the current control can be used as input for activating and changing the microchannel cooling. For the efficient utilization of microchannels, an advanced inverter control system detecting the fault in the power system would be needed. In a typical case, the fault would be detected by the alternating voltage controller, such that the current reference is increased in

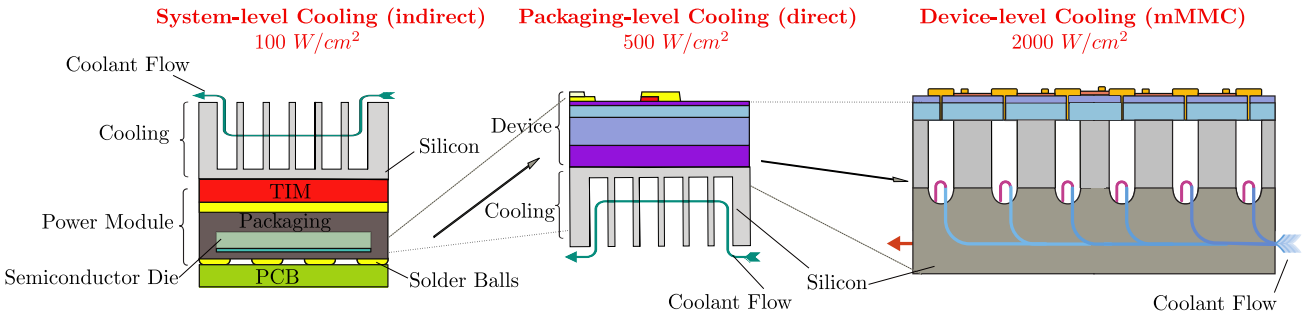

Fig. 9. Microchannel cooling at various levels [132].

order to achieve reactive current support. Alternatively, the fault might be detected by a nearby relay. In this case, the complexity of the system would be increased as a dedicated communication channel must be established along with an additional system for detecting the failures in microchannels themselves.

In order to achieve a reliable operation of microchannels in the long term, one should optimize their design by taking into account of pressure drop in microchannels and their heating due to hotspots of the die [133].

Device level microchannel cooling (effective for 2000 W/cm^2) is an interesting concept and is in the early phase of its research. Currently, it is complicated and expensive to implement it. However, if it becomes commercial, production will be developed in order to reduce the cost.

C. Peltier Elements

Thermoelectric cooling (TEC) is a result of the so-called Peltier effect, which results in a heat flux when current flows across a junction of two dissimilar conductors or semiconductors. The same system of conductors (or semiconductors) can be used as a thermoelectric generator. By applying a heat gradient to the system, a voltage is generated. This effect is called the Seebeck effect [134]. A suitable material combination for TEC has a high Seebeck coefficient, a high electrical conductivity, and a high thermal conductivity [135]. An example of such a material is bismuth telluride. Compared to several other ways of cooling, TEC involves no moving parts, which is advantageous from a reliability perspective, and so, TEC has been employed for waste-heat removal [136], LED cooling [137], and solar energy storage [138].

In power electronics, TEC has been used to reduce the chip temperature during steady-state operation [139]. It was shown that a 40 K reduction in chip temperature and 60% reduction in heat sink volume could be achieved for the case with 31.5 W of semiconductor losses. A single element was shown to provide a 120 W heat flux in [140]. For higher heat fluxes, a single element may not be sufficient. Then, layering is an alternative [141]. However, placing a Peltier element in the cooling path (for instance, below the chip) may not be a suitable solution for transient OCs, because the thermal resistance is increased. Instead, lateral heat flux must be enabled for the TEC. TEC has also been investigated in combination with PCMs [142]. In this work, the junction temperature could be kept at 130 °C for one minute of 150% OC.

In [143], the following six problems of using TECs for OC handling are identified:

1) need for the additional power source;
2) expensive materials for their construction;
3) low thermal conductivity of conventional TEC puts a limitation of the cooling capacity during heat transients;
4) optimization of geometrical and current parameters is needed;
5) limited literature is available for transient application;
6) pulsed heat fluxs of few hundreds W/cm^2 can cause large thermal stress at the interface of the TECs, and hence, it results in degraded cooling performance.

The need for a power source is a complication, but the gate driver will, typically, have a power supply, so power is available although an increase of this is required. The high cost of bismuth telluride is problematic, but new, even more effective, material combinations are developed, and some of them may come with a significant cost reduction [144]. The low thermal conductivity is a problem if the Peltier element is placed in the normal cooling, but as already explained, this can be solved by providing a lateral heat flow. Regarding the optimization of the design, this step is necessary in the development of any power module, so even though the complexity is increased by the TEC, it should not be a show-stopper. However, regarding thermomechanical stress due to transient heat fluxes, there is still a need for research to establish that this operation mode can be sustained reliably of long periods of time.

D. New Layout of Power Modules

Since wire bonds and encapsulation impose limitations for OC operation, many research works have attempted to eliminate wire bonds with interconnect technologies and planar modules.

In the following, improvements are discussed and shown in Fig. 10 for high-temperature operation of power modules without wire-bonds, press-pack technology, and multifunctional components (MFCs).

1) Planar modules and other modifications in power modules by removing wire bonds: Planar modules facilitate double-sided cooling and, hence, lead to reduction in thermal resistance. This directly has an impact on the

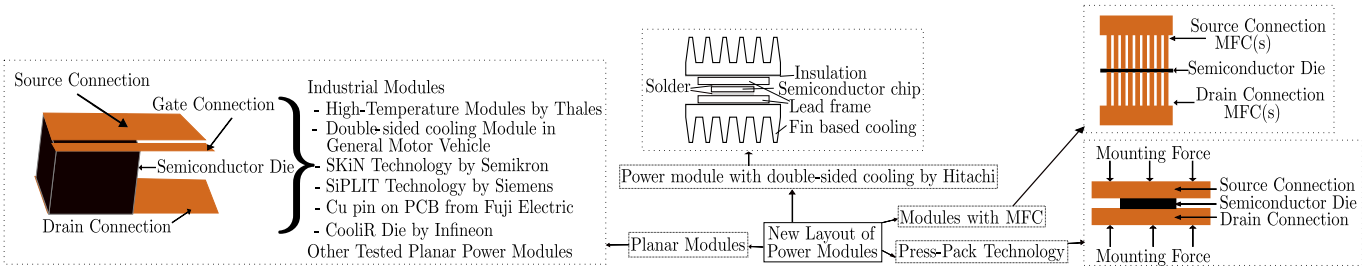

Fig. 10. New layouts of power modules.

current capability of the modules. They should be applied with materials suitable for high temperature, such as paralene HT and, silver sintering with silver microparticles paste [145]. Thermo-mechanical simulations show that double-sided cooling leads to decrease in junction temperature by 15%–42% with sintered die attach for double-sided cooling simulations as compared to single sided cooling [146].

a) A high-temperature planar module for Thales has been developed [147], [148], [149]. The module consists of SiC MOSFETS and Schottky free-wheeling diodes for 1200 V, 100 A with an integrated driver circuit. AlSiC baseplate, AlN substrates, and silver sintering are used for CTE match with SiC devices. Hence, it has a superior performance since all the components used are extremely good for high temperature, and robust for thermal cycling.

b) Double-sided cooling module in General Motor vehicle 360 V 325 A (peak) [150]: In Chevrolet VOLT-2 by General Motors, double-sided cooling with two AlN DBCs substrates, whose CTE matches with Si and metal injected moulded heat sink, have been used to handle large currents. Elimination of wire-bonds with topside solderable interconnect technology leads to increment in current capability. Another double-sided module has been developed by Hitachi, Japan, in which the semiconductor is directly connected by lead frames to fin based heating system and resulted in 50% reduction in thermal resistance [77].

c) SKiN technology from Semikron [93], [151]: Wire bonds are replaced by flexible circuit. The semiconductor die is connected to a flexible circuit and heat sink by Ag sintering. It leads to an increase in high surge-current capability and short-circuit capability of IGBT because of rise in heat capacity by flexible circuit. The junction temperature was lowered by 35% as compared to conventional modules with the same ratings.

d) Siemens Planar Interconnect Technology [93], [152], [153]: Planar structure with Cu interconnect of 50–200 μm thickness replaces wire-bonds. It leads to an increased power cycling and surge current capability as compared to wire-bonds modules. It results in a more uniform junction temperature with a 13% lowered peak temperature. It also leads to a thermal resistance decrement by 15%.

e) Cu pin on PCB from Fuji Electric [93]: Bond-wires are replaced by Cu pins sintered directly onto the PCB and the die is sintered on Si_3N_4, sandwiched between Cu blocks. This planar arrangement shows one-third of thermal resistance as compared to a conventional structure with Al_2O_3 because of the heat spreading effect provided by the by Cu blocks.

f) CooliR Die FF400R07A01E3_S6 by Infineon [154], [155], [156]: It has a double-sided DBC and double-sided cooling [157] along with solderable front metal for connections instead of wire-bonds. It also leads to the decrease in the junction temperature by 15%–42% for a 680 V and 300 A IGBT module.

g) Planar power packaging technology with two alumina-based DBC substrates enable double sided cooling [158]. Two substrates are joined by silver nano sintering and Cu tab terminal which lead to reduction in transient thermal impedance by more than 30%. This structure allowed the operation at a junction temperature of 200 °C for 90 min without failure. Another planar module with double cooling module is given in [159]. It consists of microcooling channels on both the sides in Cu layer of AMB. It has led to decrement in the thermal resistance by 30%.

h) A packaging form is introduced for operation at 300 °C [160], [161]. The SiC chip has been sandwiched between the two lead frames made of molybdenum with high-temperature encapsulation material (hydrosetting ceramic). Die attach materials, such as solder (Au solder)/braze materials are used to attach die to the leads such as AuIn, PbInAg, and PbSn. A 4 μm Au layer was also introduced at the top and bottom sides. The module is expected to have high-current capability since it eliminates the weakest part of the module.

2) Press-pack technology: Press-pack technology has a better performance at high-temperatures operations since it does not have wirebonds and DBC. A novel press-pack module is presented in [162] in which the pressure is applied on two perpendicular directions on heat sink and the semiconductor die. The tested module resulted in 61% junction-to-case thermal resistance as compared to CREE

CAS300M12BM2 commercial module of the same ratings. It is because of good thermal contacts of heat sinks without thick thermal interface material. The thermal performance of the module can further be improved by using electroplating coating instead of Ag foils between the surfaces. Hence, a reduction in thermal resistance can lead to an increase in the current capability of the module without failures. However, it is important to choose a suitable metal for platelet/base plate/cover plate so that the CTE of the plate matches with that of Si (CTE: 2.5 ppm/K)/SiC (CTE: 4.28 ppm/K) die, which will ultimately reduce the probability of failure for high temperature and OC operations. Molybednum (CTE: 5.35 ppm/K) is a better candidate in this regard as compared to Al (CTE: 24 ppm/K) and Ag (CTE: 19 ppm/K) [162], [163], [164]. The combined advantage of both, stacking and press-pack technology along with microchannels in heatsink, has been utilized in [165].

3) Stacking the devices with MFCs: Stacking of devices results in reduction in parasitic elements but stacked devices have less efficient heat dissipation [166]. The concept of MFCs with stacking of devices inside a power module for eliminating the weakest points of failures is introduced in [167] and [168]. Failures at wire-bonds, between die attach and substrate, and DBC are eliminated by providing Cu MFCs in order to improve thermal, electrical, and mechanical performances. A solid dielectric layer was replaced by dielectric liquid which act as a cooling liquid as well as dielectric. This arrangement led to reduction in overall thermal resistance of the module and the von Mises stresses by more than 50%. The same structure for diodes was tested and presented in [169]. Hence, this structure is expected to have superior and reliable performance at high temperatures. The performance is further improved in terms of failure for power module with four sides of cooling [170]. A SiC chip is sandwiched between two AlN fins and the electrical connection is established by Cu pillars which also act as thermal and mechanical connections. AlN (ceramic) fins perform as thermal connections as well as act for voltage isolation. Cu on four sides of the stacked module can act as heat sink as well as housing.

E. Modulation and Control Techniques for Converters

Control techniques in the power converters also play an important role in extending the short-term OL/OC capability at the system level. Injecting higher order harmonics to increase the arm current of the inverter without increasing the current in the switches may lead to the extension of SOA or operating area [10], [14], [171], [172]. There are three other methods, which can influence the SOA of the converter by modifying zero-sequence voltage component (ZS voltage), symmetrical circulating currents, and combining these two with dc capacitor voltage of modular mutlilevel converter cell [10], [171]. Injection of lower order harmonics (second, third, fourth) in the circulating currents leads to an extension of the maximum apparent power from 500 MVA to 900 MVA (an increment by 80%). The same observations are made by combining with other two methods (ZS voltage and symmetrical circulating currents) during transients without violating the constraints of the grid. Combing all the three methods, i.e., optimized ZS voltage, circulating current, and dc capacitor voltage leads to change in maximum apparent power from 500 to 1200 MVA (an increment by 140%) [10], [171]. Another method of increasing SOA is increase reactive power by injecting second-order circulating currents from 296 MVar to 434 MVar [172].

There is another method of handling the OC based on junction temperature. The limitation is caused at the module level by the thermal rating of the power electronic devices, hence, temperature dependent control techniques can be implemented in order to keep the converter within thermal limits [14], [15], [173]. As the heating of the junction depends on the amount of OL and its duration, a dynamic control to keep the junction temperature within the safe limit (100 °C) is introduced in [14]. The controller lowers the power of the converter to 1.1 p.u. power as soon as the overloading reaches the thermal limit of the semiconductor since the converter can withstand 1.10 p.u. for 25 s, which provides sufficient time for fault clearance. Another approach for limiting the junction temperature by using a linear current controller for OLs is presented in [173]. The controller is activated as soon as the temperature reaches the set critical temperature, i.e., 80 °C in this case. The controller is activated and the current limit is reduced to 1.13 p.u. from 1.15 p.u. as soon as the junction temperature reaches to 80 °C for OLs. The similar response for temperature control is obtained in case of 100 ms fault. The combined application of injection of circulating currents and temperature based converter control is implemented in [15]. It combines the OL capability occurrence and the thermal limitations of the IGBT devices. However, the maximum duration and the maximum amount of OL depends on the temperature safety margin, i.e., the temperature above the steady-state value. The recovery durations for an OL of 127.5% is 5 s and 20 s for safety margins of 5 °C and 15 °C, respectively.

Although the available literature about modulation and control techniques showed the results for seconds range or steady state and did not mention about transients, there should be no limitation by the control and modulation techniques since converter control inherently would respond within in few milliseconds. It may not be possible to handle OCs within nano-seconds.

F. Paralleling the Modules

Another way to increase the current capability of the converter is to connect switching devices in parallel. Parallel connections leads to reduction in both ON-state resistance (hence in ON-state voltage) and thermal resistance [174]. However, the absolute values of losses depend on the device, operating voltage, and operating temperature. Paralleling of the switches creates differences in switching characteristics and current imbalances as shown in [175] for SiC JFETs because of difference in pinch-off voltage and static characteristics. This unbalance of currents might lead to thermal runaway of the devices with lower pinch-off voltage for JFETs. Other reasons for unbalance in high power include parameter variation of each switch and package parasitics in

TABLE VIII
SUMMARY OF CONCLUSIONS AND LIMITATIONS OF TECHNOLOGIES FOR OC AND HIGH-TEMPERATURE OPERATIONS

Technologies	Conclusions, limitations and future directions
PCMs	1) Metallic PCMs, graphene, and diamond are better for short pulses of few miliseconds as compared to eutectic salts as former allow faster transfer of heat. 2) Eutectic salts and alloys could be useful for OC of few seconds with proper set up to increase their thermal conductivity. 3) A proper metal frame or container is needed for keeping PCM in place in liquid state and increasing thermal conductivity. 4) As a result, the SOA can be increased in terms of increasing the OC capability while keeping the junction temperature below the critical limit with a very small amount of PCM placed adjacent to the semiconductor chip.
Microchannel cooling	1) Microchannel cooling, depending on its location, leads to lowering of junction temperature for different orders of heat flux. 2) The fastest response is expected when the cooling is just below the semiconductor die. 3) Since microchannels remain operational during nominal operation, they in general lead to increment in the power density of the converters. Hence, special control for the coolant flow depending upon the OC could be a possibility to have it operational only during transients.
Peltier elements	Placing the Peltier elements just below the semiconductor die has not been explored much for OC. However, it may not achieve the best performance because of inherent need of voltage source for its operation and increase in thermal resistance if the Peltier element is placed between the die and next layer below.
New layout of power modules	1) Eliminating wire-bonds have proven to be successful for OC, surge-current capability and high-temperature operation. 2) Planar technologies have proven to provide better cooling because of double-sided cooling. 3) Press-pack technology has better thermal performance for high-temperature operations. 4) MFCs could be beneficial for high-temperature operation.
Modulation and control, paralleling the modules	The variation in the performance due to the current unbalance is prominent for the time-scale of nanoseconds, for example, during transients or switching of devices. The behaviour at steady state is not drastically different.

each JFETs [176]. One should even consider matching more parameters (such as delay times, dv/dt and di/dt) apart from traditional parameters (voltage and current ratings) in order to ensure effective current sharing [177].

Paralleling SiC devices or modules can create unbalance of parasitic elements, which affect devices dynamics and transient performance [178], [179], however, the circuit layout can help in mitigating these effects [176]. Massive paralleling of switches requires special arrangement of the switches. One such arrangement for SiC JFETs is presented in [6] and [180]. The 40 kVA inverter arrangement presented consists of 10 SiC JFET TO-247 discrete packages in parallel at one switch position in order to reach an efficiency of more than 99.5%. The space between the boards was filled with dc capacitors used in order to reduce the parasitic inductances and capacitances.

The configuration for a 312 kVA inverter with five MOSFET modules at one switch position (i.e., 10 modules in each half-bridge leg) is presented in [5]. The modules were placed symmetrically in order to reduce and balance the stray inductance while the capacitors were distributed throughout the circuit in order to place energy source close to the power modules. Other parasitic inductance reduction steps included distributed gate drivers attached to power module gate pins and using optical fibres for electrical signal transmission. It resulted in fast switching operation as well as high-efficiency operation (>99%). Another aspect is the mismatch of currents in the parallel devices. The mismatch in currents is reduced at high temperatures [181], hence, the lesser difference in the thermal behavior is expected.

Cost increases for systems with parallel devices if efficiency is considered to be a design parameter. The exact increase in the cost depends on the amount of OC and duration needed. The ON-state resistance of the overall system decreases and leads to a reduction in conduction losses. The switching losses will also decrease for MOSFETS in parallel operation [182], [183] but this statement may not be true for high frequencies since the turn on losses increase due to increase in parasitic capacitance [184]. The decrease in the losses in turn increases the margin for OC along with savings of energy and reduced need for cooling (and hence, cost), resulting in reduced life cycle cost. Hence, one would gain some amount of OC capability just by designing it for high efficiency.

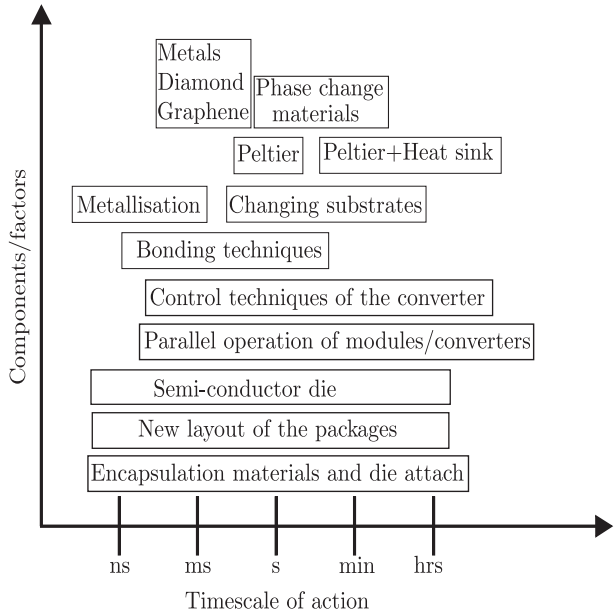

Fig. 11. Timescale of components and factors affecting OC.

V. DISCUSSION AND FUTURE DIRECTIONS

A summary of the previous section is provided in Table VIII. It can be also concluded that the different technologies enable OC in different time ranges for SiC power devices. Fig. 11 shows the timescale at which the components and the factors discussed in this article affect operation for OCs.

The performance at high temperatures caused by OCs could be improved by removing wirebonds as they are the weakest point of the power modules. Special attention should be given while selecting the components of the power modules in order to match

CTE. Planar modules connected by silver sintering to the substrates and with materials for high temperatures can increase the OC capability significantly. Since hotspots in the chip are located close to the top surface, application of PCMs, and other materials (metals, diamond, graphene, and graphite) would be more effective on the top side. Even though application of, for instance, PCMs is less complicated on the bottom-side of the chip, this will inevitably reduce the cooling performance at normal operation. The selection of technology depends on the timescale of the OC. OCs of longer duration than a few hundreds of milliseconds might be possible by integrating PCM with the metallic container as PCMs take a few seconds to distribute the heat. Replacing the bond wires with interconnection technologies, such as copper clips, ribbons, blocks, silver clips, silver sintering, and diffusion soldering would lead to much higher thermal capabilities for OCs. It would also be interesting for future research to combine multiple functionalities of the components, such as embedded power modules with high-temperature techniques as discussed in [185]. Since temperature swing affects the reliability of the power modules, care should be taken in the selection of components that they can operate reliably for a temperature swing of 150 °C and up to 250 °C for SiC power modules. Nevertheless, the technology should aim at decreasing the temperature swing. Apart from the discussed modifications of power modules for the thermal requirements, special attention should be paid to the issues associated with the gate drivers and high-frequency operations for SiC devices [186]. The reason for this is that operation at high switching frequency requires minimization of the physical size of the gate loop in order to minimize gate loop inductance. Consequently, the gate driver will be very close to the power device and, therefore, it may have to be designed by high-temperature operation.

VI. Conclusion

This article has discussed the operation and performance of SiC semiconductor dies and power modules for OCs. Limitations and the potential solutions for the packaging components including substrates, metallization, bonding techniques, die attach, and encapsulation materials have been discussed. It has been concluded that the limitation for OC operation is the junction temperature. Hence, techniques for reducing the junction temperature are also discussed. Metallic PCMs, metals (such as copper), diamond, and graphene attached to the top-side of the chip are expected to reduce the junction temperature for heat pulses of a few hundred milliseconds. Other PCMs have proven to be effective in reducing the junction temperature without adding a drastic amount of material for heat pulses of a few seconds. Because of lower thermal conductivity, PCMs should be combined with a metallic arrangement in order to increase the effective thermal conductivity of the arrangement and utilize the melting-enthalpy of PCMs. Peltier materials might also have application for OCs. However, the need of an auxiliary power source adds complexity in the setup, and hence, it is less attractive in the power electronics field. Since bondwires are the weakest point in power modules, designs without bond wires are preferable when aiming for OC capability. Influence of control techniques of the converters and paralleling the power modules for OC operation are briefly introduced too as they are on the converter level.

Acknowledgment

The authors would like to thank people who have supported in revising this article, especially S. Singh.

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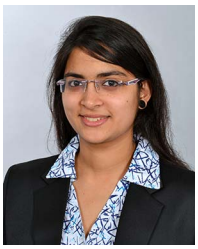

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