Accurate Condition Monitoring of Semiconductor Devices in Cascaded H-Bridge Modular Multilevel Converters

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***Abstract*—This article presents an online condition monitoring (CM) scheme for semiconductors used in modular multilevel converters (MMCs) that comprise cascaded H-bridge submodules. The CM algorithm is based on detecting changes in the ON-state resistance of the semiconductors over time. The proposed method is shown to successfully perform a curve tracing of semiconductors in MMCs while the semiconductor junction remains at a temperature that is readily measurable and undergoes minute changes during the measurement process. The ON-state resistance value is estimated from the measured ON-state voltage drop of the semiconductors and the measured arm current. Measuring the ON-state resistance at known temperatures allows for separating temperature-dependent variations of the ON-state resistance from age-dependent variations of this parameter. Suitable methods for reducing the effect of noise on the curve-traced data are proposed, and a recursive least square estimator is used to extract the optimum ON-state resistance from the traced $v_{CE} - i_C$ curve. Simulation results show that the proposed scheme can accurately determine the ON-state resistance of semiconductors at a known temperature and under various levels of measurement noise. Moreover, experimental results on a low-power prototype show that the proposed scheme is applicable in practice, and provides similar online curves to what a commercial curve tracer can produce offline. The experimental verification has been conducted under constant load conditions; however, the proposed methods can be used under any variable load condition as well.**

***Index Terms*—Cascaded H-bridge, condition monitoring (CM), flexible ac transmission systems (FACTS), health estimation, modular multilevel converter (MMC), online monitoring, reliability, semiconductors.**

I. Introduction

FLEXIBLE ac transmission systems (FACTS) have long been used to provide stability to the power grid, increase the overall power quality of the power network, regulate the grid voltage, and, in some cases, regulate the grid frequency [1], [2], [3], [4], [5]. Among the many FACTS converters, the static synchronous compensator (STATCOM) has gained much attention due to its ability to provide all the aforementioned functionalities. For controlling the frequency response, an enhanced STATCOM is needed. This family of STATCOMs is equipped with a form of energy storage system that allows for temporary active power exchange between the STATCOM and the power grid [4], [5], [6]. Modern high-voltage and high-power STATCOMs are based on a modular multilevel converter (MMC) topology, where a string of series connected submodules (SMs) are used to improve the harmonic performance of the generated output voltage, reduce the overall converter losses, and reduce the electromagnetic interference by lowering the generated $\mathrm{d}v/\mathrm{d}t$ in the system.

In STATCOM applications, the use of the full-bridge SM is prevalent as this type of SM—unlike the half-bridge counterpart—can operate in all four operating quadrants. That is, the full-bridge SM can generate both positive and negative voltage outputs. Each full-bridge SM consists of four semiconductor devices and an SM capacitor unit. Under normal operation of the converter, the SM capacitor and the semiconductors are subject to high voltages and high currents. Hence, these components undergo temperature fluctuations, which result in thermomechanical degradation over time [7]. If these degraded components are left unattended, they can cause catastrophic failures in the SM. If the number of failed SMs exceeds the number of redundant SMs in each arm, it will result in unwanted operational stoppage of the converter. Hence, it is necessary to monitor the condition of such components online, when the STATCOM is energized and in operation. Hence, it is necessary to monitor the condition of such components online, while the STATCOM is energized and in operation. Condition monitoring (CM) of semiconductors in CHB-MMCs identifies early signs of degradation. So it does not offer a solution for protection in the case of device failure. If a sudden failure eventually occurs, protective measures must already be in place to bypass the SM.

Online CM for SM capacitors in MMCs is well addressed in the literature [8], [9]. Moreover, online monitoring of semiconductor devices in MMCs has been presented in [10], where the ON-state collector–emitter voltage $v_{CE,\mathrm{ON}}$ is used as a health

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indicator. However, the effect of junction temperature on the estimated value of this voltage has not yet been addressed. Since $v_{CE,\mathrm{ON}}$ is a function of temperature, it is not sufficient to use it as a CM parameter without good knowledge of the junction temperature. Smet et al. [11] have explained this complexity. Estimating the device temperature using temperature-sensitive electrical parameters (TSEP) has also been addressed [12], [13], [14], [15]. However, in such methods, it is typically expected that the variations in the TSEPs are dependent on temperature, not aging. It is shown in [16] that the majority of the health indicators are also TSEPs. Consequently, continuous recharacterization is needed in order to include the effect of aging. Other methods of temperature estimation have also been presented in the literature. For example, negative temperature coefficient sensors [17] or the electroluminescence effect [18] have been used for temperature estimation. Despite complications with accurate measurements in these methods, all such methods are load dependent. That is, the effect of load variations must be considered online, and temperature variations as a result of load variations must not be attributed to aging. It is, therefore, important to have a load independent method when assessing the component health. Many suitable parameters have been identified for CM of semiconductors [19], [20]. It is reported that changes in the ON-state resistance is the result of both gate oxide- and package-related degradations, whereas the threshold voltage mainly reveals gate oxide-related issues. In other methods of CM, the Miller plateau duration [21] and the gate emitter voltage overshoot [22] of the semiconductors have been used as CM parameters. Although proven to be effective, all of the said parameters are dependent on the temperature of the semiconductor as well, which in turn is dependent on the load conditions of the converter. For a fixed temperature, an increase in the ON-state voltage larger than 20% of its initial value is reported as an end-of-life (EOL) criterion [19], [23]. Moreover, in AQG324, a 5% increase in the ON-state voltage of insulated-gate bipolar transistors (IGBTs) is selected as the EOL criteria [24]. Although the reported EOL values are attributed to changes in the ON-state voltage, it is the ON-state resistance that reflects aging, and is the important CM parameter. This is because the changes in the ON-state voltage as a result of package degradation are mainly attributed to the changes in the ON-state resistance. This is shown in [25] for IGBTs and in [26] for the body diode of silicon carbide (SiC) MOSFETs. The ON-state voltage of IGBTs comprises a relatively constant forward voltage plus a resistive voltage drop at higher currents. Hence, the 5% variation of v_{CE} reported in AQG324 consists of both these voltage terms. For commercial IGBT modules, a 5% variation in the ON-state voltage as a result of aging corresponds to a range of 10–20% variation in the ON-state resistance, depending on the type of IGBT module.

Although tracking the component temperature itself has also been identified as a suitable CM parameter [19], accurate junction temperature measurements of semiconductor devices is complicated. Also, a fair comparison of the device temperature over time would require temperature measurements at fixed operation of the converter, or comprehensive premapping of device temperature at different loads. Both alternatives create extra complexity to the monitoring scheme. Furthermore, in many applications, such as in high-power STATCOMs, the converter is typically subject to intermittent loads; hence, conducting measurements under fixed load conditions may not be feasible in normal operation. Consequently, estimating a CM parameter under known and controlled temperatures has significant value in increasing the accuracy of the estimations and simplifying the health state assessment of the component.

Gate-emitter threshold voltage $v_{GE,\mathrm{th}}$, $v_{CE,\mathrm{ON}}$, ON/OFF switching delay times, Miller plateau duration, and gate voltage overshoots have all been identified as potential parameters for CM of IGBTs and SiC MOSFETs [19], [20]. In this study, the focus has been on using the ON-state resistance of semiconductors as the main CM parameter; however, the methods used in this article are also suitable for measuring other CM parameters at a constant and readily measurable temperature. Although the ON-state resistance is also dependent on circuit-driven parameters—such as the dependency of the ON-state voltage on the gate-emitter or gate–source voltages—it is relatively straightforward to keep such circuit parameters constant during the data acquisition period for CM.

In the literature, many of the studies on CM of semiconductor devices have been conducted on conventional two-level and three-level converters. In such converter systems, it is difficult to associate TSEP variations to temperature changes or to aging over long periods of time. This is mainly because in normal operation of such converters, all the semiconductors are engaged. Hence, it is difficult to keep the temperature of semiconductors constant during normal operation of these converters. In contrast, in MMCs, there are many redundant modulation schemes that result in the same output voltage of the converter. This provides a natural advantage in the CHB-MMCs—compared with other converter topologies—for providing accurate CM of semiconductors. In this article, these redundancies are utilized to measure the ON-state resistance of semiconductors at a controlled junction temperature. In fact, the core innovative step of this paper is that the proposed solution can provide online monitoring of the semiconductors without significantly increasing their temperature during the monitoring process. Under this condition, after thermal equilibrium is reached, the heat sink or case temperature can be attributed to the device temperature as well. When the measurements are conducted under a fixed or known temperature, the variation of the ON-state resistance over time can be attributed to the aging alone. The concept of using online curve tracing for semiconductor monitoring was initially presented in [27]. This concept is further developed in this article with the addition of hardware design for ON-state voltage recording, experimental verification of the concept, and effective estimation techniques considering the presence of measurement noise. Although the ON-state resistance can increase as a result of bond-wire lift off, solder delamination, or aging of the gate-oxide layer, the focus of this article is on accurate measurement of the ON-state resistance for identifying possible device degradation without assessing the failure mechanism itself. This is because from a predictive maintenance perspective, the type of failure mechanism is not of immediate importance, whereas an accurate indication of degradation is needed. Hence, all such failure mechanisms would cumulatively—not separately—be observed

in the ON-state resistance. The main contribution of this article is presenting a method of semiconductor CM in CHB-MMCs that

1) provides accurate monitoring of the ON-state resistance by conducting the measurement at a fixed temperature,
2) is independent of load conditions,
3) does not require precharacterization,
4) does not require accurate knowledge of the thermal model of the semiconductor and heat sink,
5) does not significantly increase the junction temperature of the semiconductor during the monitoring process,
6) and does not interfere with the normal operation of the MMC converter during the monitoring process.

Existing methods of semiconductor CM in the literature do not possess the aforementioned advantages. Therefore, in other methods of CM, more steps are needed to correctly assess the estimated parameters. Hence, the proposed CM method significantly simplifies the monitoring and data processing compared with state-of-the-art techniques.

This rest of this article is organized as follows: Section II shows the converter system for which the solution is intended. Section III presents the method for ON-state voltage measurement of semiconductor devices. The effect of temperature variations on the ON-state resistance, and the online curve tracing at a controlled temperature are described in Section IV. In Section V, simulation results for the extraction of ON-state resistance from the ON-state voltage are presented. Experimental results are provided in Section VI, and the conclusions are given in Section VII.

II. System Layout

CHB-MMC-based STATCOMs are mostly developed in the form of delta-STATCOM [28], wye-STATCOM [29], and double-wye-STATCOM topologies [4]. All of these topologies consist of one or more arms of series-connected full-bridge SMs. The concepts presented in this article have been conducted on a single-phase converter comprising only one arm. However, these concepts can be separately applied to each arm of the aforementioned converter topologies.

Grid-connected STATCOMs are designed to control the voltage at the point of common coupling (PCC) through reactive power exchange with the network. A general layout of a single-phase grid-connected STATCOM is shown in Fig. 1. The voltage and current of the STATCOM are governed by Kirchhoff's voltage law shown in (1), where a reference voltage at PCC defines the required amount of current injection into the network. This, in turn, defines the desired voltage generated by the converter. Hence, the STATCOM controls the voltage at the PCC through an internal current control system [30]. In Fig. 1, v_g and v_c represent the grid voltage and the voltage generated by the string of SMs, respectively. Moreover, L_g represents the equivalent inductance of the grid, whereas L_arm is the inductance of each arm.

$$v_\mathrm{PCC} = v_\mathrm{c} - L_\mathrm{arm}\frac{\mathrm{d}i_\mathrm{arm}}{\mathrm{d}t} = v_\mathrm{g} + L_\mathrm{g}\frac{\mathrm{d}i_\mathrm{arm}}{\mathrm{d}t}\,. \quad (1)$$

The control system used in this article is shown in Fig. 2, which consists of a proportional-resonant controller for the inner current control loop, a voltage balancing control for the SM capacitors, a total energy control of the converter, and a reference generator for the transferred reactive power. The converter operates in current control mode; hence, a phase-locked loop (PLL) is used to track the angular frequency of the grid ω. The active and reactive powers are governed by the direct and quadratic axes in the dq reference frame, respectively. The sum energy control and the voltage balancing control are equipped with a proportional-integral controller. Moreover, the measured capacitor voltages used in these controllers are passed through a low-pass filter and a band-stop filter in order to eliminate the effect of capacitor voltage ripples on their control dynamics. In this study, a phase-shifted carrier-based pulsewidth modulation

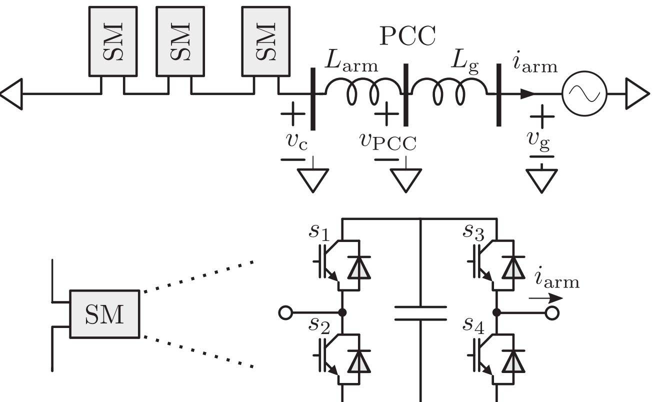

Fig. 1. Single-phase MMC-based STATCOM with full-bridge SMs.

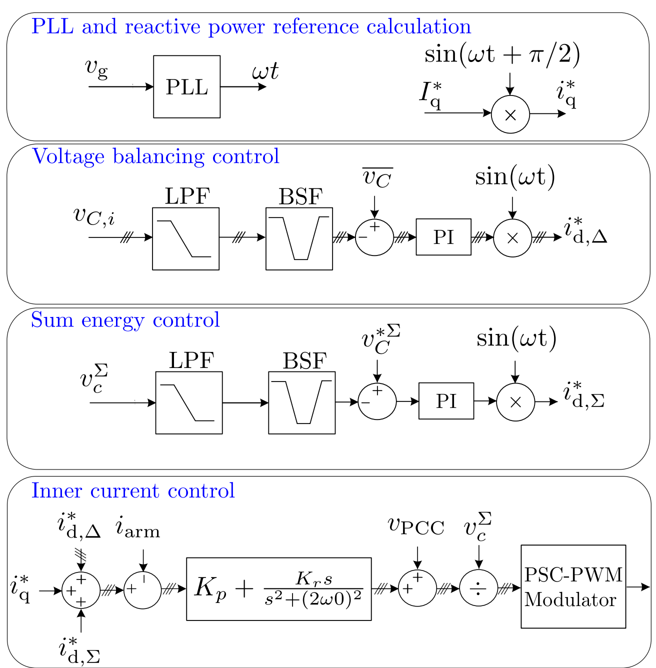

Fig. 2. Proportional–resonant current control system used for a single-phase STATCOM. The lines containing "///" represent N signals, where N is the number of SMs in an arm. The parameter $v_{C,i}$ represents the capacitor voltage of the ith SM, while v_c^Σ and $\overline{v_C}$ represent the sum and average value of all SM capacitor voltages, respectively.

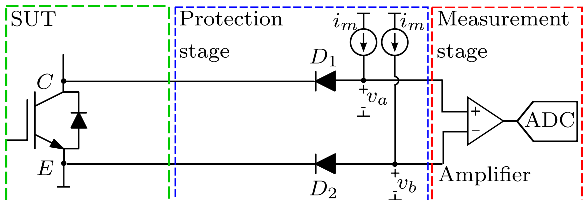

Fig. 3. ON-state voltage measurement circuit using two diodes for protection against high voltages of the SUT. The measurement stage is equipped with a differential probe and an ADC.

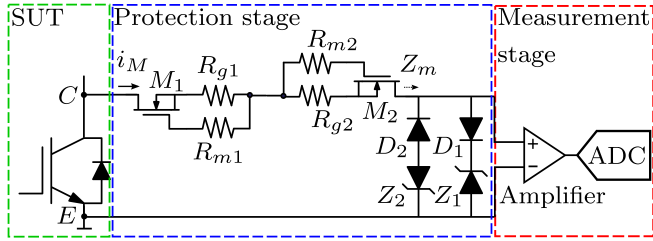

Fig. 4. ON-state voltage measurement circuit using depletion-mode MOSFETs for protection against high voltages of the SUT. The measurement stage is equipped with a differential amplifier and an ADC. This design is based on the solution provided in [33].

scheme (PSC-PWM) is used for creating the switching commands. Nevertheless, the CM technique presented in this article can be used with any other modulation and control scheme. The novelty here is in conducting CM of the semiconductors devices $s_i, i \in \{1, 2, 3, 4\}$, at a controlled junction temperature and without interfering with the generation of i_{arm} and v_{c} in (1).

III. ON-State Voltage Measurement

A prominent challenge in online measurement of the semiconductor ON-state voltage in high-voltage converters is that the measurement circuit must be able to withstand the voltage stress of the semiconductor when it is in OFF-state. Different techniques have been proposed for separating this high voltage from the ON-state voltage measurement circuit [31], [32], [33], [34], [35]. The double-diode circuit shown in Fig. 3 is a suitable circuit that provides this functionality. A different embodiment of this design is also proposed in [32]. One issue with these solutions is the potential parameter mismatch between the blocking diodes. Specifically, a small difference exists between their ON-state junction voltages, V_{PN}. Consequently, the voltage difference between v_a and v_b shown in Fig. 3, $v_{CE} = v_a - v_b = v_C + V_{\text{PN},D_1} - v_E - V_{\text{PN},D_2}$, may exhibit an offset error. Moreover, if not positioned correctly in the circuit, the blocking diodes in Fig. 3 can be subject to different temperatures. Since the junction voltage drop in these diodes is strongly affected by temperature variations, an additional differential error might be introduced in the measured value of v_{CE}. Nonetheless, as shown in Section V, unwanted offset voltages can simply be eliminated by data postprocessing. Utilizing integrated circuits (ICs) with parameter-matched double diodes can minimize the effect of different junction voltages and different diode temperature problems. However, complying with the clearance and creepage requirements in high-voltage circuits complicates the use of such ICs. Another suitable isolation circuit is shown in Fig. 4 [33], [34], [35]. This circuit provides voltage isolation using a self-triggered depletion-mode MOSFET. When the voltage over the semiconductor device under study is positive and below the breakdown voltage of the Zener diode Z_1, the connection including R_{g1}, R_{g2}, M_1, and M_2 provide a conductive path with the sum resistance of $R_{g1} + R_{g2} + R_{\text{ON},M1} + R_{\text{ON},M2}$. Under this condition, the ON-state voltage of the semiconductor under test (SUT) can be readily measured as

$$v_{\text{meas}} = v_{CE} \frac{Z_m}{Z_m + R_{g1} + R_{g2} + R_{\text{ON},M1} + R_{\text{ON},M2}}, \quad (2)$$

where Z_m is the input impedance of the measurement stage, including the Zener-diode arrangements Z_1, D_1 and Z_2, D_2 of Fig. 4. The measurement stage consists of a differential amplifier and an analog-to-digital converter (ADC). In this study, an accurate differential probe AP033 from Teledyne LeCroy has been used.

In contrast to ON-state conditions, when the voltage over the semiconductor device increases beyond the breakdown voltage of the Zener diode Z_1, a small current passes through the MOSFETs. As a result of this current flow, a negative voltage builds on the gate–source of the MOSFET M_1, which results in its automatic turn-OFF. Clearly, a larger value of R_{g1} results in the negative $V_{GS,\text{th}}$ achieved at a lower current level i_M drawn from the measurement circuit. However, the larger the value of R_{g1}, the more significant the voltage split would be between the measurement stage and R_{g1}. Hence, a tradeoff must be made when selecting the value of R_{g1}. As seen in (2), aside from R_{g1} and R_{g2}, the ON-state resistances of the MOSFETs M_1 and M_2 also affect the voltage split between the isolation circuit and the measurement circuit. Unlike power MOSFETs, M_1 and M_2 are designed for low-current operation, and can exhibit large ON-state resistances. Although it is expected that Z_m is much larger than the total resistance of the isolation circuit, it should still be considered when designing the circuit, especially when choosing the values of R_{g1} and R_{g2}, and the type of Zener diodes Z_1 and Z_2. Nevertheless, these impedances can be measured and their effect on the measurements can be compensated. The section of the isolation circuit comprising R_{g2} and M_2 has a similar function as R_{g1} and M_1, except that they protect the measurement circuit against large negative voltages. Even though large negative voltages are not expected to be seen in normal conditions, having this circuit helps to protect against negative voltage transients in the circuit. Compared with the double-diode solution in Fig. 3, the isolation circuit of Fig. 4 is less sensitive to temperature-dependent parameter variations of M_1 and M_2 due to their small ON-state channel resistance relative to Z_m, while a compensation for the additional resistive voltage split of (2) may be needed. On the other hand, the double-diode solution of Fig. 3 is more easily scalable for high-voltage solutions. In this study, the isolation circuit based on depletion-mode MOSFETs is opted mainly for its temperature stability and zero measurement offset. The components used in the isolation circuit are summarized in

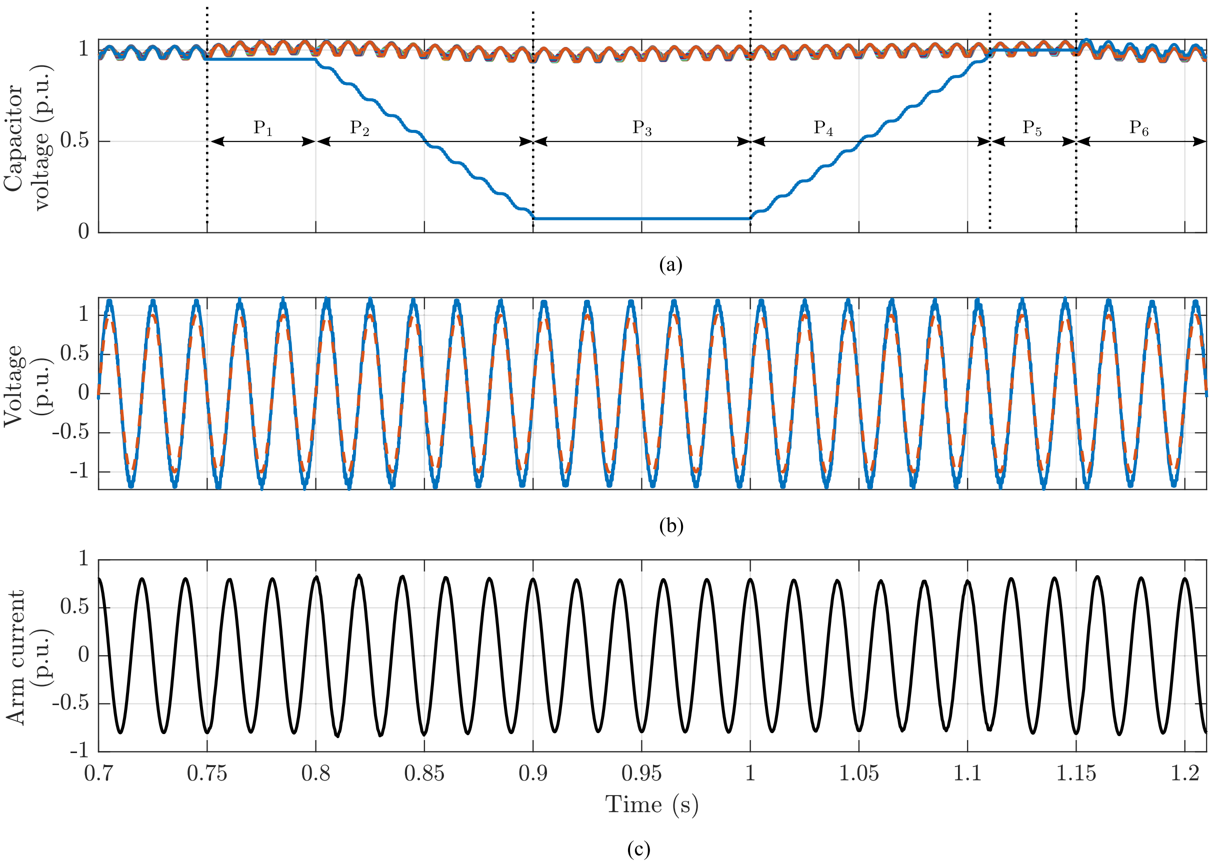

Fig. 5. Selective SM bypass (P_1), discharge (P_2), sampling (P_3), recharge (P_4), bypass (P_5), and reinsert (P_6) during normal operation of the converter. (a) Capacitor voltages with selected module discharged to 10% nominal value. (b) PCC voltage (dashed line) and converter voltage (solid line). (c) Arm current of the converter at 0.8 per unit, capacitive.

TABLE I
SELECTED COMPONENTS FOR THE ON-STATE VOLTAGE MEASUREMENT CIRCUIT OF FIG. 4

Symbol	Model	Value
M_1, M_2	BSS126	–
R_{g1}, R_{g2}	–	3.3 kΩ
R_{m1}, R_{m2}	–	1.0 kΩ
D_1, D_2	BAS70-04	–
Z_1, Z_2	3SMAJ5922B	–

Table I. For the design with parameters of Table I, the analog bandwidth (BW) is approximately 1 MHz. This BW is sufficient for the CM method of this article. The measured signal quality can be further improved by placing a capacitor in parallel to the input of the measurement stage; however, this would further reduce the measurement BW and was not considered in this study.

IV. SEMICONDUCTOR MONITORING SCHEME AT KNOWN TEMPERATURE

Temperature variations of semiconductor devices are mainly caused by conduction and switching losses in the circuit. Therefore, for different load conditions, different losses and junction temperatures are expected. As a result, during normal operation of the converter, load-dependent variations of semiconductor ON-state resistances are expected. These variations complicate accurate online CM of semiconductors. In order to minimize this temperature coupling, a special operation mode is proposed that allows for independent operation of the SM that holds the SUT. The general steps of the proposed solution are listed in the following:

1) Bypass the SM that holds the current SUT through (s_1, s_3) or (s_2, s_4) switch groups (Section IV-A and time period P_1 depicted in Fig. 5).
2) Change the carrier phase of the PSC-PWM in the remaining SMs to maintain a low total harmonic distortion (Section IV-A and time period P_1 depicted in Fig. 5).
3) Reduce the direct voltage of the selected SM to a desired value (Section IV-B and time period P_2 in Fig. 5).
4) Bypass the selected SM through (s_1, s_3) or (s_2, s_4) switch groups and wait for the SUT to reach thermal equilibrium with its heat sink (Section IV-C and time period P_3 in Fig. 5).
5) Periodically toggle between (s_1, s_3) and (s_2, s_4) switch groups for v_{CE} sampling (Section IV-C and time period P_3 in Fig. 5).

6) Measure the ON-state voltage during each short ON-state duration of the SUT (Section IV-C and time period P_3 in Fig. 5).
7) Increase the direct voltage of the SM to its nominal value (time period P_4 in Fig. 5).
8) Temporarily bypass the SM after it reaches its nominal voltage (time period P_5 in Fig. 5).
9) Reinsert the selected SM and change the carrier phase of all SMs to their initial state (time period P_6 in Fig. 5).

These steps are further explained in the following sections.

A. SM Bypassing

Due to the SM redundancies and typical operating conditions, the arm of each STATCOM is normally operating at a lower voltage than what it is rated for. Hence, there is more than one switching pattern that complies with any modulation requirement. Out of the many possible switching solutions, one simple solution is to temporarily bypass an SM and use the remainder of the SMs to create the desired output voltage. In a full-bridge SM, there are two bypassing alternatives. Specifically, it is possible to bypass an SM by either switching ON s_1 and s_3 or by switching ON s_2 and s_4. This is a redundant state within each SM. For the purpose of semiconductor CM, the current within the bypassed module must be conducted by the semiconductors that are not subject to curve tracing. For example, assuming that s_4 is to be monitored, the corresponding SM should first be bypassed through the switch group (s_1, s_3). This results in no current passing through the switch group (s_2, s_4). Hence, the junction temperature of s_4 gradually decreases until it reaches the temperature of its heat sink. If the ON-state resistance of s_4 is measured under this thermal equilibrium, the measurement is achieved at a known temperature of the heat sink of the semiconductor. Unlike the junction temperature of the semiconductor, measuring the temperature of its corresponding heat sink is straightforward, and can be achieved using a simple thermocouple or other similar sensors.

When bypassing an SM, it is important not to interfere with the normal operation of the converter. Also, the harmonic content of the produced voltages and currents should not vary significantly. In order to assure an acceptable voltage and current quality after the SM bypassing, a modified modulation scheme is proposed. The PSC-PWM scheme in CHB converters provides low harmonic content in the output voltage by eliminating certain switching and sideband harmonic contents. This is achieved by phase shifting each carrier waveform by $180°/N$, where N is the number of SMs in each arm. After bypassing an SM, in order to maintain a similar harmonic performance, the carrier signals of the remaining active SMs are changed such that each SM's carrier is phase shifted by $180°/(N-1)$ instead. The entire bypassing process of an SM is shown in Fig. 5, where no notable harmonic distortion is observed in the arm current while the SM is bypassed. The system parameters used for the simulation results of Fig. 5 are summarized in Table II. The simulation results shown in Fig. 5 are only a demonstration of the bypassing, discharging, recharging, and inserting the SM of interest. In reality, the time period P_3 during which the sampling of the SUT occurs is much longer than what is shown in Fig. 5. The duration of P_3 is dependent on many parameters, such as the power rating of the SUT, how fast the SUT cools down, and how much data are needed to be extracted. There is, however, no time limit on how fast this should be conducted.

TABLE II
SYSTEM PARAMETERS USED FOR THE SM BYPASSING METHOD SHOWN IN FIG. 5

System parameter	Symbol	Value	Unit
Nominal power	S	33	MVA
Nominal line-to-line voltage	V_{LL}	25	kV-rms
SM capacitance	C	15	mF
Number of SMs	N	20	–
Arm inductance	L_{arm}	12	mH

B. Reduction of Direct Voltage of the Selected SM

In an online setup, there are both conduction and switching losses associated with the switching instances needed for the ON-state voltage sampling. If not minimized, these losses can cause large temperature changes in the devices and reduce the accuracy of the measurements. The conduction losses can be minimized by choosing a short sampling pulse. In order to minimize the switching losses, it is advisable to reduce the SM voltage before starting the curve tracing procedure. The energy of the SM under test can, therefore, be buffered with the grid, i.e., the SM can be discharged by temporarily transferring its energy to the network, and recharged once the data acquisition is finalized. In this process, the energy of the SM is not lost, but rather temporarily buffered with the network.

After bypassing the selected SM, the remainder of the circuit is still operating in current control mode of operation, whereas the bypassed SM is free to be controlled in any mode of operation. In order to discharge the bypassed SM, it is temporarily controlled in voltage control mode, that is, the bypassed SM is forced to create a modulated sinusoidal voltage that is 180° out of phase with respect to the arm current. This results in the gradual discharge of the SM capacitor. The proposed voltage control is performed in an open loop, where the reference alternating voltage provided to the bypassed SM has a constant magnitude. It is important not to completely discharge the bypassed SM; otherwise, both switch groups (s_1, s_3) and (s_2, s_4) could conduct current regardless of the switching status of the semiconductors. Hence, it would not be possible to actively separate these two paths in a completely discharged SM.

C. Sampling the ON-State Voltage

In an industrial curve tracer, the ON-state voltage of the semiconductor is measured while multiple short current pulses are injected into the device. The pulse duration is typically kept short (in the order of 10–100 μs) such that the junction temperature of the device does not change significantly during the sampling period. Considering a 1 MHz BW of the measurement circuit used in this article, a pulse shorter than 10 μs is not advised. The amplitude of the current pulses are gradually increased in order to create a sweeping function of the measured ON-state

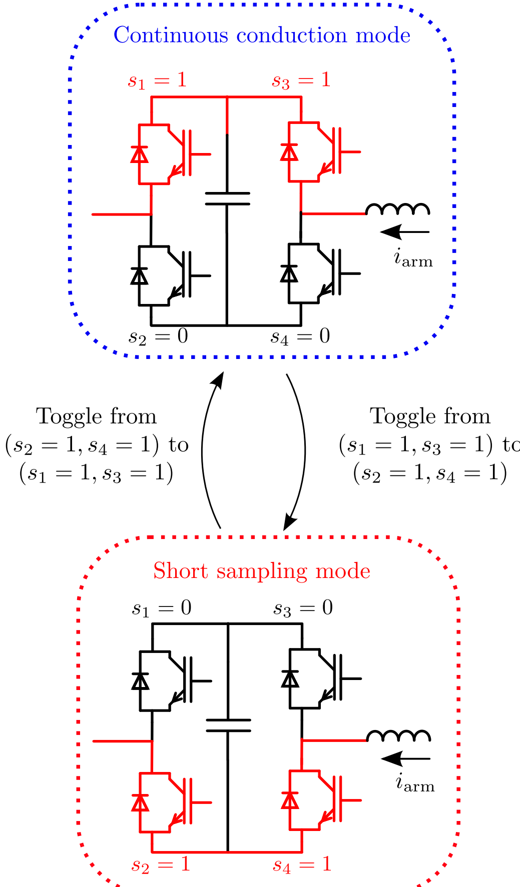

Fig. 6. Procedure for sampling $v_{CE,\mathrm{ON}}$ in a bypassed SM.

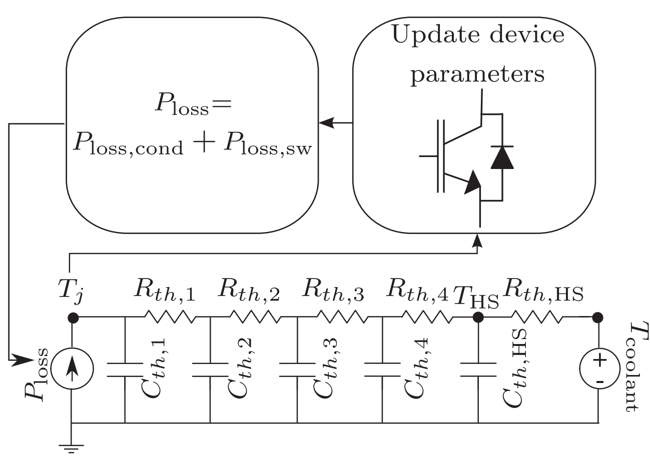

Fig. 7. Thermal model of IHW40N60RF with parameters summarized in Table III.

TABLE III
SELECTED PARAMETERS OF THE IHW40N60RF IGBT

Symbol	Value	Unit
$R_{th,1}$	0.1097	K/W
$R_{th,2}$	0.1303	K/W
$R_{th,3}$	0.1745	K/W
$R_{th,4}$	0.0755	K/W
$R_{th,\mathrm{HS}}$	6	K/W
$C_{th,1}$	0.0016	J/K
$C_{th,2}$	0.0071	J/K
$C_{th,3}$	0.0553	J/K
$C_{th,4}$	0.9784	J/K
$C_{th,\mathrm{HS}}$	56	J/K
K_{T1}	0.002	1/K
K_{T2}	-2.175×10^{-4}	1/K
K_{T3}	0.0054	1/K
K_v	0.6415	–

voltage versus the injected current. Here, this process is replicated online in an arm of a CHB-MMC. Since the converter is operating in current–source mode of operation, the large currents needed for the current pulse injection are readily available in the arm. In order to replicate the temporary current pulse injection, the bypassing redundancy is utilized. For example, in order to sample the ON-state voltage of s_4 in an SM bypassed through (s_1, s_3), for the desired duration of the current pulse, devices (s_1, s_3) are switched OFF and (s_2, s_4) are switched ON. As a result of this transition, the SM under study is still bypassed but the arm current temporarily passes through s_2 and s_4 instead. The ON-state voltage of s_4 is measured in the duration of this current pulse, and one sample data for the $v_{CE} - i_C$ curve is achieved. Repeating this procedure at different instances of the load current cycle, and thus different current levels, results in an online curve tracing of the semiconductors. Fig. 6 depicts the process for sampling the ON-state voltage of s_4.

A proposed open-loop method to achieve sampling at different current levels is to conduct the measurements with a fixed sampling frequency that is not an integer multiple of the fundamental frequency. This choice of sampling frequency creates a natural curve-tracing behavior as it assures that the SUT is sampled at different points of the load current cycle. In this study, a sampling frequency of 290 Hz is used. The choice of this sampling rate is mainly due to the limitation of the recording time of the data logger used in the experimental section. However, if the data logging allows it, any slower sampling rate could also be used.

D. Loss and Thermal Considerations

Temperature variations in a semiconductor device are dependent on the power losses generated in the device, as well as its thermal impedance. The thermal impedance of a semiconductor—from the junction to the back plate—is typically provided in its datasheet. In this study, the IGBT discrete package IHW40N60RF has been used. The thermal model of this device is depicted in Fig. 7, where the equivalent Cauer model parameters are extracted from the Foster model representation provided in the datasheet. Each semiconductor device is connected to an Ohmite RA-T2X-64E heat sink. The thermal parameters of the semiconductor and the heat sink are summarized in Table III.

The conduction losses of a semiconductor device are defined as

$$P_{\rm loss,cond}(t, T_j) = v_{CE,\rm ON}(t, T_j).i_C(t), \tag{3}$$

and the switching energies are given as

$$E_{\rm sw}(t, T_j)$$

$$= E_{\rm sw}(T_{j,\rm ref}, v_{CE,\rm ref}, i_C).(1 + k_{T_1}.(T_j(t) - T_{j,\rm ref})).\left(\frac{v_{CE}}{v_{CE,\rm ref}}\right)^{k_v}, \quad (4)$$

where k_{T_1} and k_v are extracted from the datasheet [36]. The parameters $T_{j,\rm ref}$ and $v_{CE,\rm ref}$ are reference values for the junction temperature and the collector-emitter voltage, at which the switching energies are provided in the datasheet. The switching energies can be scaled according to (4) for temperatures and voltages other than the reference values. The switching power losses are calculated using (4), and the switching time $t_{\rm sw}$ as follows:

$$P_{\rm loss,sw} = \frac{E_{\rm sw}}{t_{\rm sw}}. \quad (5)$$

In its simplest form, the ON-state voltage of an IGBT is represented by a linear curve given as

$$v_{CE,\rm ON}(t, T_j) = v_{CE,i_{C0}}(1 + k_{T_2}.(T_j(t) - T_{j,\rm ref})) + r_{CE}(1 + k_{T_3}.(T_j(t) - T_{j,\rm ref}))).i_C(t), \quad (6)$$

where k_{T_2} and k_{T_3} represent the temperature coefficient of the intercept and slope of the $v_{CE} - i_C$ curve, respectively. $v_{CE,i_{C0}}$ represents the voltage intersection of the linearized $v_{CE} - i_C$ curve at zero current, and r_{CE}, the slope of the $v_{CE} - i_C$ curve, represents the ON-state resistance. The temperature coefficients k_{T1}, k_{T2}, and k_{T3} of IHW40N60RF are extracted from the relevant datasheet and summarized in Table III. These coefficients are used to calculate the switching and conduction losses of the SUT. This in turn reveals the expected variations in r_{CE} during the data acquisition period.

The $v_{CE} - i_C$ curves of another TO-247 IGBT, namely the IHW40N135R5 device, were measured with a curve tracer and under controlled temperature conditions. That is, the device was placed in a nonconductive solution with a temperature-controlled heating system. The results are summarized in Fig. 8. The aim of this measurement is to show the general temperature coefficient of the r_{CE}, $v_{CE,i_{C0}}$ and $v_{CE,0}$ parameters of IGBTs. In Fig. 8, linear fitting for each curve results in the identification of r_{CE} and $v_{CE,i_{C0}}$. $v_{CE,i_{C0}}$ must not be mistaken with $v_{CE,0}$. The parameter $v_{CE,0}$ is the forward voltage of the IGBT at low—but not zero—current, whereas $v_{CE,i_{C0}}$ is the intersection of the linear fit of the $v_{CE} - i_C$ curve with the v_{CE} axis. In this article, low current refers to values smaller than 1 A where $r_{CE}.i_C$ is negligible, and high current refers to above 10% of the IGBT's nominal current rating, beyond which $r_{CE}.i_C$ becomes significant in comparison to $v_{CE,i_{C0}}$. Both $v_{CE,0}$ and r_{CE} vary linearly as a result of junction temperature, where $v_{CE,0}$ and r_{CE} exhibit a negative and positive temperature coefficient, respectively [36]. Temperature variations of r_{CE} and $v_{CE,0}$ for the IHW40N135R5 IGBT are shown in Fig. 9(a) and (b), respectively. Compared with $v_{CE,0}$, $v_{CE,i_{c0}}$ exhibits smaller relative variations as a result of temperature changes, and is not necessarily linear as seen in Fig. 9(c). Nevertheless, since r_{CE} is the extracted parameter for CM, changes in $v_{CE,i_{c0}}$ or

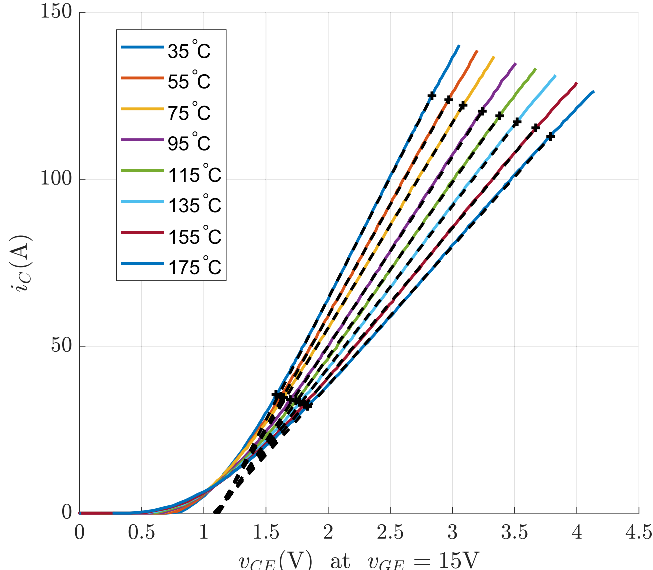

Fig. 8. Measured $v_{CE} - i_C$ curve of the IHW40N135R5 IGBT at ($v_{GE} = 15\ V$ and different temperatures. Solid lines show the actual curves extracted from a curve tracer. Dashed lines show the linear fit used to extract r_{CE}. "+" depicts the two data points on the $v_{CE} - i_C$ curve that are used for linear fitting. The selected points are 40% and 90% of the largest sampled current point in each curve. The intersection of each dashed line with the v_{CE} axis represents $v_{CE,i_{c0}}$, whereas the slope of each dashed line represents $1/r_{CE}$.

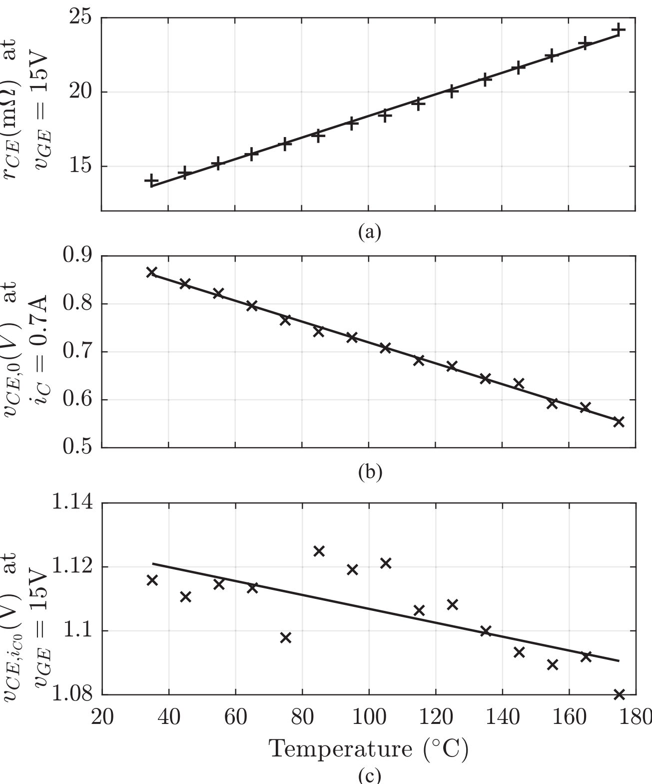

Fig. 9. Extracted parameters of IHW40N135R5 at different temperatures using the linear fits from Fig. 8. (a) Extracted r_{CE} values at different temperatures. (b) Forward voltage at i_C=0.7 A ($v_{CE,0}$) at different temperatures. (c) Zero-current voltage intersect ($v_{CE,i_{C0}}$) at different temperatures. In all figures, the sampled values are represented by "+" and the linear fit of the data is shown with a solid line.

TABLE IV
SYSTEM PARAMETERS USED IN SIMULATIONS THAT MATCHES THE HARDWARE PROTOTYPE

System parameter	Symbol	Value	Unit
Nominal line-to-ground voltage	$V_{\mathrm{LG,nom}}$	50	V-rms
Nominal current	I_{nom}	20	A-rms

$v_{CE,0}$ as a result of temperature variations do not interfere with the CM accuracy.

As seen in (4), switching losses are strongly dependent on the SM voltage and arm current. Therefore, if the SM voltage is significantly reduced before the sampling of $v_{CE,\mathrm{ON}}$, the switching losses become negligible in comparison to when the SM is operating at rated voltage. This is the main reason for discharging the selected SM before sampling the SUT, as described in Fig. 5. The CM technique presented here is suitable for full-bridge SMs that comprise of single position semiconductor device modules, such as HiPak or StakPak modules. Moreover, it is best to have separate heat sinks for each module in order to avoid any thermal coupling between the conducting and nonconducting semiconductors.

V. SIMULATION STUDIES

In this section, the proposed method of online curve tracing of semiconductors under known temperatures is verified through simulations. The simulation model described in this section is designed to match the hardware prototype.

A. *Simulation Model Representing the Hardware Prototype*

After bypassing the SM of interest, the arm can be divided into two subsystems: 1) the bypassed SM, and 2) the remainder of the circuit (including the group of SMs operated under current control mode, the arm inductor, and the grid). Since the aim of the current controller is to control the arm current to a reference sinusoidal value, the entire system of Fig. 1 can be represented as the bypassed SM series connected with a controlled current source. The ON-state voltage and resistance of the conducting semiconductors in the bypassed SM have negligible effect on the operation of the remaining components in the system. Hence, these two subsystems can operate independently as long as the SM under test remains in the bypassed state. The simulated model uses the parameters given in Tables III and IV in order to replicate the hardware prototype. In the simulations, the semiconductor's ON-state voltage is modeled linearly, as described in (6). Both losses are dynamically calculated during the simulation. The total loss in each semiconductor is the sum of the switching and conduction losses. This value is injected into the thermal model of the semiconductor and its cooling system described in Fig. 7 and Table III. The junction temperature T_j is then used to estimate the new values of r_{CE} and $v_{CE,i_{C0}}$ for the next simulation time step. Simulation results of the junction temperature are shown in Fig. 10, and the corresponding ON-state resistance is shown in Figs. 11 and 13. In this simulation study, a sampling pulse duration of 50 μs, a sampling rate of

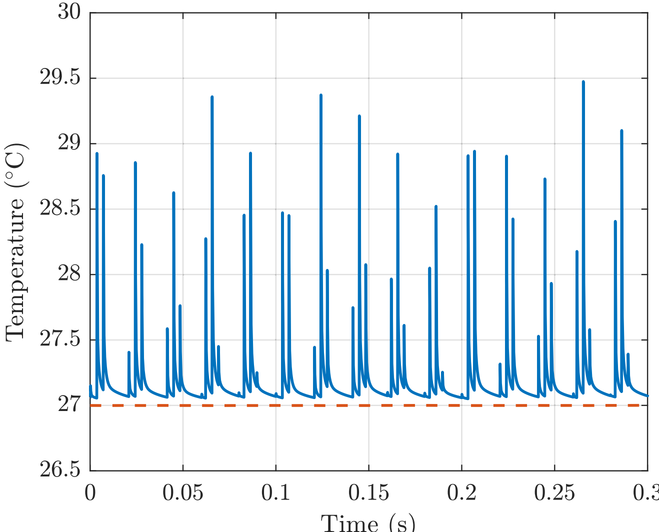

Fig. 10. Temperature variations of the semiconductor junction (solid) and heat sink (dashed), when the parameters of Tables III and IV are used. The converter is operating at 20 A-rms. The sampling pulse duration and sampling rate are 50 μs and 290 Hz, respectively.

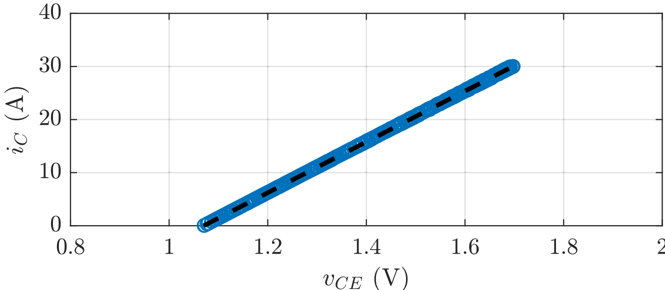

Fig. 11. Simulation results of the sampled $v_{CE,\mathrm{ON}}$ and i_C values (○), and the corresponding linear fit (dashed) assuming no measurement noise is present. The parameters of Tables III and IV are used in the simulation, and the estimated r_{CE} value is 20.9 mΩ.

290 Hz, and a sinusoidal arm current of 20 A-rms is used. Under these conditions, it is observed that as a result of sampling, the maximum variation of the ON-state resistance is 1.5%, which corresponds to an average temperature variation of 2.5 °C. The value of resistance is extracted through a linear fitting of the simulated $v_{CE} - i_C$ curve, as shown in Figs. 11 and 12. A 2.5 °C variation as a result of the sampling current pulse does not create a significant change in the ON-state resistance value. Such small temperature variations are also expected while conducting offline curve tracing using commercial curve tracers since they use a very similar concept for curve tracing. Furthermore, the example shown in this article is for a small semiconductor package with relatively small thermal capacity in the semiconductor die and packaging. For larger semiconductor devices used in high-power applications, an even smaller junction temperature variation is expected for the same current pulses. This is because larger power modules typically possess a larger thermal capacity, which can be observed from their relevant datasheets [27]. Nevertheless, as shown in Fig. 10, the temperature variation in

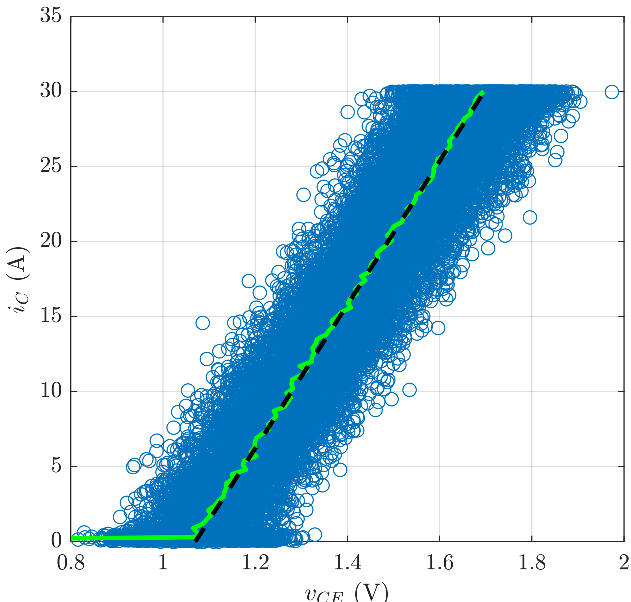

Fig. 12. Simulation results of the sampled $v_{CE,\mathrm{ON}}$ and i_C values (○), the corresponding linear fit (dashed), and the moving median (solid) over current windows of $\Delta I_m = 0.3$ A. The current and voltage measurements are subject to Gaussian noises with $3\sigma = 2\%$ and $3\sigma = 20\%$, respectively. The parameters of Tables III and IV are used in the simulation, and the estimated r_{CE} value is 20.9 mΩ.

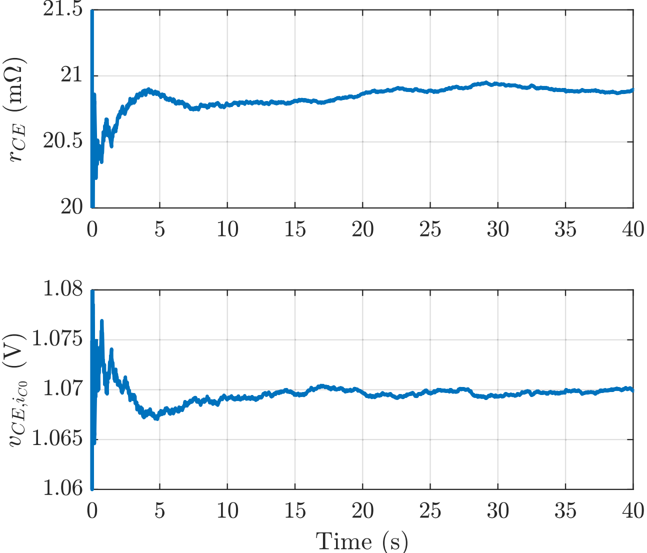

Fig. 13. Estimated values of r_{CE} and $v_{CE,i_{C0}}$ with the simulation data of Fig. 12, and using the RLS estimator.

the heat sink is 1.9 °C. This temperature can be readily measured and used to correct the estimated ON-state resistance. As a result, the actual error in the estimated ON-state resistance is 0.33%, which corresponds to a temperature error of $2.5 - 1.9 = 0.6$°C. The sampling rate of 290 Hz chosen for the simulation studies corresponds to the value used in the hardware prototype. A slower sampling rate leads to smaller temperature variations of the junction. Furthermore, the simulation and hardware prototype have a small heat sink with natural convection cooling. In high-power SMs, much larger heat sinks are utilized, which results in a larger thermal capacity of the heat sink, and in turn, much smaller temperature fluctuations of the heat sink.

In this article, the periodic sampling is simply opted for its simplicity in implementation. In practice, any method of sampling can be adopted as long as the sampling is conducted at different current values, which result in a *V–I* curve. For example, the sampling can be done at predefined levels of arm current. This could be periodic or aperiodic. Consequently, the proposed CM procedure is not dependent on the type of load or the mission profile of the converter. For any mission profile, the sampling can be performed at a known temperature and predefined arm current levels.

B. Measurement Noise and Extraction of the ON*-State Resistance*

Both voltage and current measurements are subject to measurement errors. This consists of both offset errors and measurement noise [8]. Offset errors can be readily compensated. Such errors are, therefore, already corrected in the experimental setup. What is referred to as measurement noise in this article is the overall measurement error having a stochastic nature. Here, both current and voltage measurements are chosen to have a Gaussian distribution, which is seen from measurement data as well. In simulations, a current measurement noise with a standard deviation of $\sigma = 0.2$ A ($3\sigma = 2\%$ of a 30 A nominal value) and a voltage measurement noise with a standard deviation of $\sigma = 7$ mV ($3\sigma = 20\%$ of a 1 V nominal value) are considered. These noise levels are higher than what is actually recorded in practice. For the experimental results of Section VI, a maximum noise of 1% and 10% are recorded in the current and voltage measurements accordingly. It is important to minimize the effect of measurement noise on the estimated parameter values. Simulation results considering the aforementioned measurement noise is shown in Fig. 12, which reveals that postprocessing of the measured data is necessary for accurate estimation of the ON-state resistance.

One method of noise reduction in the traced $v_{CE} - i_C$ curve is to select certain windows of current with a mid-point of I_m and a width of ΔI_m from the current axis. Then, the median of the ON-state voltages corresponding to that window of current can be used as the representative ON-state voltage of the current I_m. This is shown in Fig. 12, where ΔI_m is chosen to be 0.3 A. The benefit of this method is that even nonlinear regions of the $v_{CE} - i_C$ curve—such as the one of an IGBT at low currents—can be traced effectively. On the other hand, the disadvantage of this method is the large data storage requirement and computational intensity.

The main parameter of interest in the $v_{CE} - i_C$ curve is the slope of the linear region, which represents the ON-state resistance. In order to estimate this value in an online setup, a recursive least square (RLS) estimator is proposed. This estimator extracts both the slope (r_{CE}) and the intersection ($v_{CE,i_{C0}}$) of (6). Even though the estimated value of $v_{CE,i_{C0}}$

Algorithm 1: RLS Estimation Algorithm for the Estimation of r_{CE}.

0. Define $X = [i_C \; 1]^T$ and $A = [\hat{r}_{CE} \; \hat{v}_{CE.i_{C0}}]^T$, and initiate matrices A and P:
$A[1] = [0 \; 0]^T$, and $P[1] = \begin{bmatrix} 10 & 0 \\ 0 & 10 \end{bmatrix}$.
1. Sample $v_{CE}[n]$ and $i_C[n]$.
2. Calculate the estimation error:
$e[n] = v_{CE}[n] - \hat{v}_{CE}[n] = v_{CE}[n] - X[n]^T A[n-1]$.
3. Update the Kalman gain $K[n]$:
$K[n] = \frac{P[n-1]X[n]}{(\lambda + X^T[n]P[n-1]X[n])}$.
4. Update the covariance matrix $P[n]$:
$P[n] = \frac{1}{\lambda (P[n-1] - K[n]X^T[n]P[n-1])}$.
7. Update the estimated values of $A[n]$:
$A[n] = A[n-1] + K[n]e[n]$
8. $n = n + 1$, and repeat.

is not needed, it must be included in the linear model so that a correct representation of the system is provided to the estimator. The linear representation of (6) can be reformulated as

$$\hat{v}_{CE} = X^T A, \tag{7}$$

where $X = [i_C \; 1]^T$, $A = [\hat{r}_{CE} \; \hat{v}_{CE.i_{C0}}]^T$, and the parameters $\hat{v}_{CE}$, $\hat{r}_{CE}$, and $\hat{v}_{CE.i_{C0}}$ represent the estimated values of v_{CE}, r_{CE}, and $v_{CE.i_{C0}}$, respectively. After each sampling instance, the error between the measured and estimated value of v_{CE} is calculated as

$$e = v_{CE} - \hat{v}_{CE} = v_{CE} - X^T A. \tag{8}$$

Thereafter, the Kalman gain K, covariance matrix P, and estimated parameter matrix A are updated as described in Algorithm 1. The parameter λ used in the RLS estimator represents the forgetting factor. In this article, λ is chosen to be $1 - 1 \times 10^{-5} = 0.99999$ since the RLS estimator is reset each time an SUT is curve-traced, and during a curve-tracing sequence, large variations of r_{CE} are not expected.

The RLS estimator is included in the simulation model where the measurement noise at the levels shown in Fig. 12 is present. The estimated values of r_{CE} and $v_{CE,i_{C0}}$ through the RLS estimator are shown in Fig. 13. The estimated value of r_{CE} through this method is 20.9 mΩ, which is the same as the postprocessed linear fit of Fig. 12. A strong advantage of the RLS estimator is that it can separate the r_{CE} value not only from $v_{CE,i_{C0}}$, but also from any voltage offset that might appear in the voltage measurements. These offsets can only deteriorate the accuracy of the estimated $v_{CE,i_{C0}}$, which is already deemed unsuitable for CM, and therefore discarded. Aside from measurement noise, certain line transients might occur during the estimation process. Such transient events are usually short-lived and may at most interrupt one sampled data point among the thousands of samples inputted to the RLS estimator during an estimation process. If a transient results in a data point that is far out of bounds of typical voltage and current values, it can simply be omitted. However, even if such data points are not eliminated,

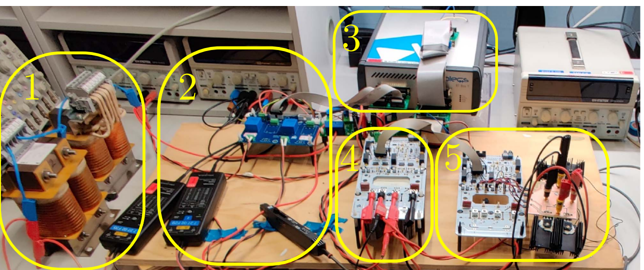

Fig. 14. Experimental setup of the CHB-MMC with two SMs. The setup comprises (1) an arm inductor, (2) measurement boards and probes, (3) control hardware, (4) current controlling SM, and (5) SM containing the SUT.

TABLE V
LABORATORY EQUIPMENT USED IN THE EXPERIMENTS

Equipment	Manufacturer	Model
Voltage sensor	Teledyne LeCroy	AP033
Current sensor	Teledyne LeCroy	CP030
Curve tracer	Keysight	B1505
Control hardware	Plexim	RT Box 1
Thermal camera	FLIR	E40
Data logger (ADC)	Teledyne LeCroy	HDO4000A

they would have little effect on the output of the RLS estimator since they are not frequently occurring. The minimum duration of data acquisition to achieve a stable estimation is dependent on many parameters, such as the sampling rate, noise levels, and the forgetting factor of the RLS estimator. Hence, there is no fixed time duration that could suit all converter systems. Clearly, a longer period of data acquisition leads to a larger array of data samples, which results in a better estimation of the ON-state resistance.

VI. Experimental Results

The CHB-MMC STATCOM shown in Fig. 1 is realized in a laboratory environment using two SMs. One SM is used to govern the arm current and the other SM holds the SUT. The experimental setup is shown in Fig. 14, and Table V summarizes the equipment used in this experimental setup. The operating conditions and important parameters of the SUT are summarized in Tables III and IV.

Fig. 15 shows the H-bridge SM under different test conditions, where Fig. 15(b) and (c) is acquired by a thermal camera. In the experiments of Fig. 15(b) and (c), the thermal images were taken 60 s into the sampling. In both experiments, the converter was initially operated until thermal equilibrium was reached. In Fig. 15(b), the proposed bypass and sampling method is applied, where the SM under study is initially bypassed, and when thermal equilibrium is reached for the nonconducting devices, the sampling procedure is carried out at a frequency of 290 Hz. Unlike offline curve tracing, the online measurements can only be conducted up to the rated current of the semiconductor device. This is because in an online setup, the remainder of the semiconductors that are not under test are conducting the full load current. In contrast, in an offline setup, short current pulses higher than the nominal current value are

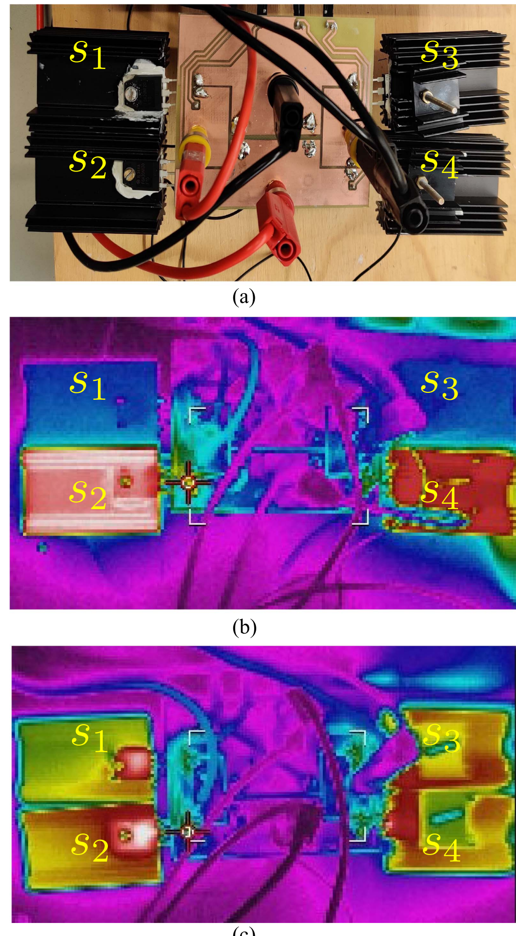

Fig. 15. H-bridge SM containing the SUT. (a) Physical layout. (b) Temperature distribution when the SUT is sampled using the proposed curve-tracing method. The heat sink of s_1 and s_3 are at 28 °C. (c) Temperature distribution when the SUT is sampled in normal operation and without the proposed curve-tracing method. The heat sink temperatures of s_1 and s_3 are 130 °C.

allowed as they would not significantly increase the device temperature. From Fig. 15(b), it is apparent that the switch group (s_1, s_3) remains very close to the ambient temperature during the sampling procedure. The recorded heat sink temperature on s_1 and s_3 is 28 °C. This is slightly higher than what the simulation studies yielded. Nevertheless, this variation is small and can only cause minor errors. The extracted $v_{CE} - i_C$ data as well as the offline $v_{CE} - i_C$ curve produced from a commercial curve tracer at a room temperature of 25 °C are plotted in Fig. 16. Moreover, the moving median of the recorded data with a window of $\Delta I_m = 0.3$ A is shown in this figure. The temperature measurements of Fig. 15 were conducted with a thermal camera. Although these sensors are not suitable for measuring fast thermal transients, they provide accurate measurements in steady state when calibrated. The thermal recordings in this study were conducted after thermal equilibrium was reached. This was verified by having no change in the device surface/heat sink temperature after multiple minutes of sampling. When reading the temperature of the device surface, the camera was placed very close to the device. This replicated the procedure used to characterize the camera, and assured an accurate reading.

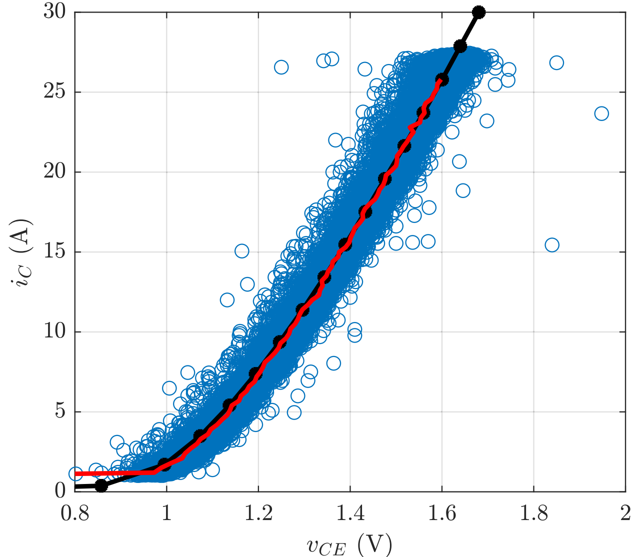

Fig. 16. Experimental results of the sampled $v_{CE,\mathrm{ON}}$ and i_C values of one IHW40N60RF device when the SUT is sampled using the proposed CM method (○). The moving median over current windows of $\Delta I_m = 0.3$ A (solid). Offline measurement of the $v_{CE} - i_C$ curve using a commercial curve tracer at 25 °C (–●).

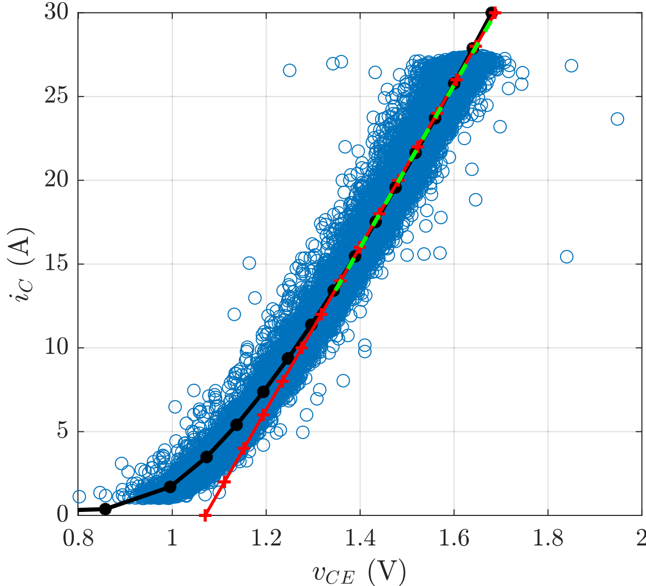

Fig. 17. Experimental results of the sampled $v_{CE,\mathrm{ON}}$ and i_C values of IHW40N60RF when the SUT is sampled using the proposed curve-tracing method (○). Offline measurement of the $v_{CE} - i_C$ curve using a commercial curve tracer at 25 °C (–●). Estimated linear fit of online measurements using the RLS estimator at a current range of 10–27 A (– +). Linear fit of the offline $v_{CE} - i_C$ curve for a current range of 10–27 A (–).

The linear fit of the online and offline $v_{CE} - i_C$ curves is calculated and is shown in Fig. 17. The curve fitting and the RLS estimation are conducted over the current range of 10–27 A for both offline and online measurements. The minimum current of 10 A is chosen to stay in the linear region of the $v_{CE} - i_C$ curve. This is especially important for IGBTs since they have a nonlinear curve at lower currents. The estimated r_{CE} value for

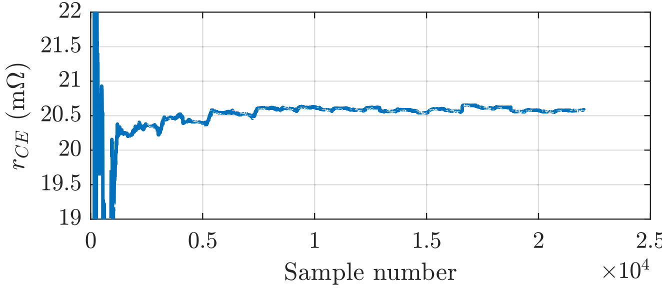

Fig. 18. Estimated r_{CE} of IHW40N60RF from the data in Fig. 17 using the RLS estimator at a current range of 10–27 A.

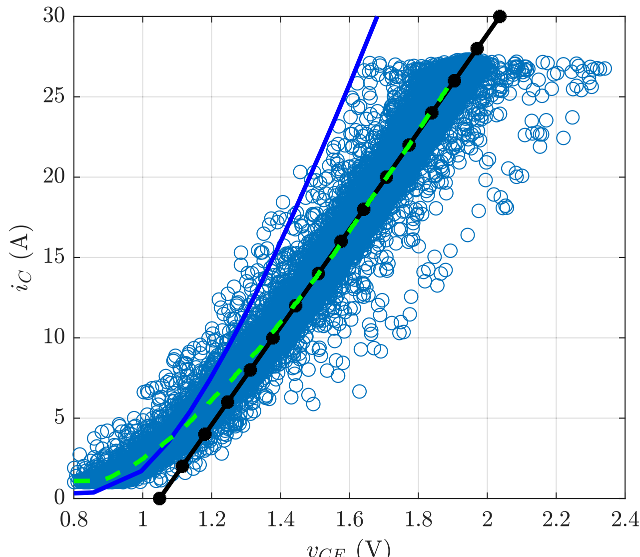

Fig. 19. Experimental results of the sampled $v_{CE,\mathrm{ON}}$ and i_C values of IHW40N60RF when the SUT is sampled in normal operation and without the proposed curve-tracing method (○). Offline measurement of the $v_{CE} - i_C$ curve using a commercial curve tracer at 25 °C (solid). Estimated linear fit of online measurements using the RLS estimator at a current range of 10–27 A (–●). Moving median over current windows of $\Delta I_m = 0.3$ A (–).

both online and offline curves is 20.6 mΩ. However, considering the temperature correction for the online measurements, an r_{CE} of 20.9 mΩ is expected. This results in an error of approximately 1.5% compared with the offline results. Fig. 18 shows the online estimation results of r_{CE} using the proposed RLS estimator. It is evident that a stable estimated value is achieved. In Fig. 18, the number of samples is shown instead of time, but due to the fixed sampling frequency of 290 Hz, these two parameters are interchangeable.

In a second experiment, the converter is operated in a normal operation mode. That is, both SMs are modulated with a PSC-PWM. Fig. 15(c) shows the temperature distribution under this mode of operation. The surface temperature of all four semiconductors is similar and approximately 130 °C. This equal loss distribution is also analytically demonstrated in [37]. However, depending on where the temperature is monitored on the heat sink, a wide range of temperatures might be recorded. Specifically, as we move away from the center of the semiconductor device, the temperature of the heat sink drops. Hence, in normal operation of the converter, the junction temperature of

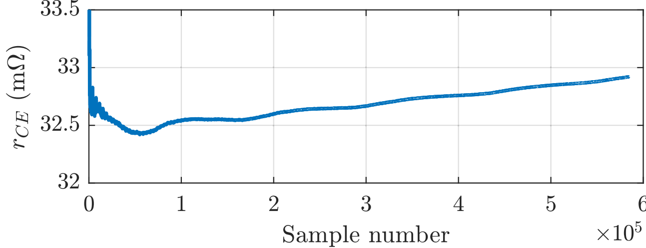

Fig. 20. Estimated r_{CE} of IHW40N60RF from the data in Fig. 19 using the RLS estimator in a current range of 10–27 A.

the SUT cannot be represented by temperature measurements at any point of the heat sink. The online curve tracing is conducted under this operation and shown in Fig. 20. The ON-state resistance is estimated to be 33 mΩ in this condition, which is approximately 60% different from what was measured by the curve tracer at 25 °C. Hence, it would be complicated to reach a conclusion about the junction temperature or the device health when the sampling is made at an uncontrolled temperature. This complexity increases when the CHB-MMC operates at a variable load. Therefore, if the sampling is conducted at uncontrolled temperatures, the added complication of identifying an accurate adaptive thermal model for each semiconductor—together with its cooling system—is needed to compensate for the temperature variations online. On the other hand, in the proposed method, as long as the semiconductors are given sufficient time to reach thermal equilibrium with their heat sink, it is sufficient to monitor the temperature of the heat sink and associate that to the junction temperature. As a result, no offline precharacterization of the semiconductors are needed. The first measurement of ON-state resistance is used as the reference value, and any large drift of the ON-state resistance seen during the consecutive measurements can be attributed to aging. Consequently, the most prominent advantages of the proposed method are as follows:

1) Eliminating the need for an accurate thermal model of the semiconductors.
2) Accurate sampling of the SUT under any operating condition.
3) Not interfering with the generated voltages and currents of the converter during the sampling process.
4) Not requiring any offline precharacterization of the devices.

VII. Conclusion

In this article, a novel method for online CM of semiconductor devices in CHB-MMCs is proposed. The method extracts the ON-state resistance of the semiconductors under known and controlled temperatures. Moreover, the measurements are carried out without significantly increasing the device temperature. The ON-state resistance is estimated using an RLS estimator, which facilitates the identification of a drift in ON-state resistance in noisy environments. The effectiveness of the RLS algorithm in identifying the ON-state resistance under practical noise levels was first studied through simulations. It is shown that under noise levels of 20% for measured v_{CE} and 2% for measured i_C, the ON-state resistance can be estimated with less than 1.5% error.

This error is much smaller than the 20% change that represents the EOL, and therefore, is acceptable for CM of semiconductor devices. The efficacy of the proposed method has also been verified through experimental results using a low-power prototype. An estimated error of 1.5% was observed in the experimental results compared with the offline curve-traced data. The experiments presented in this article have been conducted under a constant load; however, the proposed solution is also applicable to variable loads. Although the focus of this article has been on extracting the ON-state resistance of semiconductor devices for CM, the proposed method can be used for extracting other known health indicators, such as threshold voltage and Miller plateau voltage, under known temperatures as well. Moreover, the proposed method can be used for any MMC that consists of full-bridge SMs.

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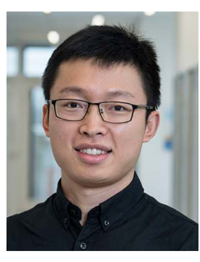

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