A Clamping-Circuit-Based Voltage Measurement System for High-Frequency Flying Capacitor Multilevel Inverters

Georgios Kampitsis, *Member, IEEE*, Efstratios I. Batzelis, *Senior Member, IEEE*, Paul D. Mitcheson, *Senior Member, IEEE*, and Bikash C. Pal, *Fellow, IEEE*

***Abstract*—In an era where high-frequency flying capacitor (FC) multilevel inverters (MLIs) are increasingly gaining attention in energy conversion systems that push the boundaries of power density, the need for a compact, fast, and accurate FC voltage monitoring system is also increasing. In this article, we designed and developed a new FC measurement system, based on precise sampling of the inverter switching node voltage, through a bidirectional clamping circuit. The deviation of FC voltages from their nominal values is extracted by solving a set of linear equations. With a single sensor per phase and no isolation requirements, as opposed to dozens of sensors in traditional FC monitoring, our approach results in significantly lower cost, complexity, and circuit size. Detailed device-level simulations in LTspice and system-scale simulations in MATLAB validate the accuracy and speed of the proposed measurement system and the balancing strategy in steady-state, abrupt load change, and imbalance conditions. Experiments carried out in a three-phase gallium nitride five-level inverter prototype reveal a gain in precision and bandwidth that is more than 30 times that of conventional methods, at a fraction of their cost and footprint. The recorded performance renders the developed sensor an ideal solution for fast MLIs based on wide-bandgap technology.**

***Index Terms*—Active balancing, clamping circuit, flying capacitor, gallium nitride, multilevel inverters, voltage measurement, wide band gap semiconductors.**

I. Introduction

The emergence of wide-bandgap technology in the last decade has revolutionized the field of power electronics and opened the road for more efficient and miniaturized energy conversion systems. Particularly, the advantageous characteristics of gallium nitride (GaN) devices, such as high switching speed capability and low ON-state resistance, in combination with their relatively low breakdown voltage rating, make them the ideal candidate for future multilevel inverters (MLIs) for distributed energy resources (DERs). Such systems favor the use of smaller magnetic components and the elimination of bulky and unreliable electrolytic capacitors, reaching record-level power densities. More importantly, the lateral structure of GaN high-electron-mobility transistors allows the monolithic integration of several power devices and potentially the entire MLI on a single chip [1]–[4].

Among different MLI topologies [5], the flying capacitor (FC) GaN inverter has the highest potential for miniaturization [6]–[11], due to the absence of clamping diodes and the redundancy of switching states. But like any MLI, the reliable operation of the FC inverter requires a balancing mechanism to ensure that the capacitor voltages remain constant.

The simplest way to achieve this is through natural balancing, an open-loop control technique that drives the transistors such that the average current flowing through the capacitors remains zero. A review of the modulation strategies that offer natural balancing is performed in [12]. Among them, phase-shifted pulsewidth modulation (PSPWM) is the most widely used technique in the literature due to its implementation simplicity, but it exhibits very slow balancing response times in low modulation indices. To overcome this limitation, a modified PSPWM technique with optimal utilization of the switching state redundancies is proposed in [13]–[15]. A combination of natural balancing and improved output harmonic content is achieved with the modified phase disposition (MPD) PWM, which uses multiple trapezoidal-shaped carriers or reshaped reference signals [16]–[19]. To further assist the natural balancing process, an *RLC* circuit, known as a balancing booster, can be placed at the inverter output [16], [17], [20], but it introduces additional power losses and increases the system size.

Although natural balancing can be proven effective in steady-state conditions, in practical implementations, there are many factors that can lead to voltage imbalance among the FCs, such as asymmetric load disturbances [21], [22], input source nonidealities [23], circuit parasitics, mainly the power device voltage drop, and timing mismatches introduced by the dead-band and the drivers' propagation delay [23], [24]. The voltage imbalance

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becomes a major concern in high power density MLIs due to the use of small-value thin-film or ceramic capacitors to replace the large electrolytic capacitors [25]. Consequently, it is necessary to adopt a reliable closed-loop active balancing control.

However, regardless of the control structure, precise knowledge of the voltage of each FC in real time is always required. This is traditionally done via individual and galvanically isolated voltage sensors coupled with each FC [22], [25]–[32]. However, such sensors are expensive and bulky components that increase the system cost, size, and complexity, especially in MLIs with a large number of levels. For example, a 7-level, 3-phase inverter requires 15 isolated voltage sensors. Particularly for high-voltage applications, these sensors are becoming increasingly complex, expensive, and less accurate due to the high-insulation requirements and the wide measurement range [33].

One of the most prevalent alternatives found in the literature is based on real-time state estimation algorithms that use only the phase current measurement as input. There are several implementations of this method, and the most promising of which are based on the discrete Kalman filter [34], [35], the backstepping approach [36], the discrete-time model [37], the sliding-mode observation [38], the peak inductor current detection [21], and the finite-control-set model predictive control [24]. The major drawback of such techniques is their low response speed because of their computational burden. At the same time, the requirement for a high sampling rate for the measured current, higher than the switching frequency, makes this approach practically unsuitable for high-frequency MLI applications.

A viable alternative is to compute the FC voltages by sampling the inverter output voltage at the switching node through a single voltage sensor during different switching states [33]. Once an adequate sampling has been obtained, the FC voltages can be calculated by solving a system of algebraic equations [37]. This ac-side monitoring technique was used in [39] to estimate the voltage states of a dc/dc FC multilevel converter and investigate the system observability and controllability. This technique requires a fixed duty cycle and cannot be directly applied to an inverter. In [40] and [41], the dc voltages of a cascaded H-bridge (CHB)-MLI-based static synchronous compensator were extracted by a single voltage sensor per phase. Specifically, in [40], the sampling was performed close to the zero-crossing of the inverter output voltage waveform, where only one cell of the CHB is active, directly associating the measured value with the capacitor's voltage. Although simple, this approach is not applicable to FC MLIs, where each FC is charged to a different voltage level. A modified technique is proposed in [41] and [42], where the samples are not restricted around zero-crossing but are also taken when the output reaches its maximum and minimum voltages. A generalized voltage estimation method is proposed in [43] and [44], applicable to several MLI topologies. The voltage extraction is performed after every switching transition with a sampling frequency twice the switching frequency, resulting in high resolution of the estimated capacitor voltages.

However, all ac-side monitoring techniques found in the literature suffer from a limited sensor bandwidth with respect to the dc voltage level, which prevents their application to the modern GaN-based high-switching-frequency (above 10 kHz) inverters. The problem lies in the need for a large time delay (typically a few tenths of microsecond) between the beginning of the voltage transient and the measurement instance, the value of which is determined by the resistors of the commonly used voltage divider and the internal capacitor of the analog-to-digital conversion (ADC) module [39], [41], [44]. The higher the dc voltage level, the larger the value of voltage divider resistors, resulting in narrower sensor bandwidth.

Therefore, it is evident that accurate voltage detection remains an open issue in high-frequency MLIs, especially GaN-based MLIs that typically operate at a few hundreds of kilohertz. Our voltage detection approach is an ac-side monitoring technique that relies on the precise measurement of the inverter phase voltage around zero-crossing, via a novel bidirectional clamping circuit. By clamping and sampling the inverter voltage solely during the zero switching states (ZSS), we capture only the FC voltage variation, meaning that we need a smaller measurement range and, thus, we achieve faster sample-and-hold (S&H) acquisition. This, in turn, helps increase the sensor resolution by 30 times, compared to traditional monitoring systems, and accordingly broadens the measurement bandwidth ($>$200 kHz) while keeping the complexity and cost to a minimum using a single voltage sensor per phase. To the best of the authors' knowledge, this is the first attempt to implement a voltage detection system for FC MLI, which combines high measurement bandwidth and high resolution with low cost, simplicity, and small footprint. Several applications with strict size and weight restrictions could benefit from our compact and reliable voltage monitoring system, including electric aircraft drive systems [45], distribution systems for data centers [46], electric vehicle chargers [8], and grid-connected DERs [47].

The rest of this article is structured as follows: The principles of operation of the new measurement system are given in Section II, with focus on the optimum PWM strategy. The theoretical analysis of the bidirectional clamping circuit is presented in Section III, followed by the simulation and experimental results in Sections IV and V, respectively. A comparative assessment of the performance of the proposed system against other FC sensing solutions is presented in Section VI, and the final remarks and conclusions are reported in Section VII.

II. Switching Node Measurement System

The proposed solution employs a single measurement unit at the switching node of each MLI phase to sample the output voltage with respect to the midpoint of the dc-link, v_{x0} (where x denotes the phase, $x = a, b, c$), only during the ZSS, i.e., the inverter states that correspond to zero output voltage. This selective sampling along with the small voltage deviation of the FCs from their ideal value (a few volts in the worst case) allows us to clamp the v_{x0} voltage close to zero and, thus, substantially increase the measurement resolution. This is in contrast to the methods presented in [40]–[44], which measure v_{x0} at the entire range of output voltage and suffer from delays, low bandwidth, and moderate resolution.

A. Switching States for Zero Output Voltage

A five-level inverter has six ZSS, all of which are illustrated in Fig. 1. Three of these modes involve the conduction of

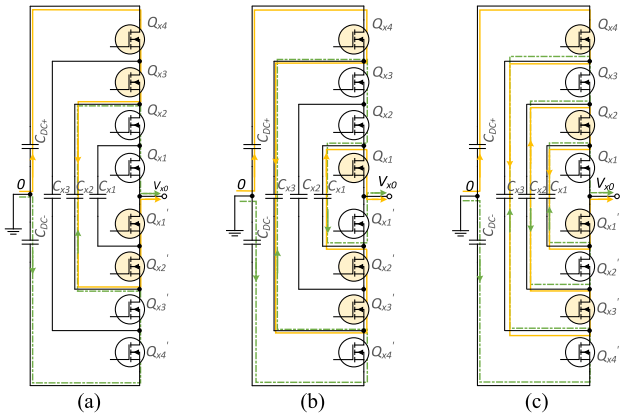

Fig. 1. Three operation modes of a five-level FC inverter leg that corresponds to zero output voltage. The unique switching states involve the conduction of $C_{\mathrm{DC}+}$ and are highlighted with a yellow line, and the complementary states involve the conduction of $C_{\mathrm{DC}-}$ and are marked with green dashed-dotted lines.

TABLE I
ZSS AND FC CURRENT DIRECTION IN A FIVE-LEVEL FC INVERTER

State	*Fig.1*	Q_{x1}	Q_{x2}	Q_{x3}	Q_{x4}	C_{x1}	C_{x2}	C_{x3}	v_{x0}
S_1	(a)	0	0	1	1		+		Δv_{Cx2}
S_2	(b)	1	0	0	1	-		+	$\Delta v_{Cx3} - \Delta v_{Cx1}$
S_3	(c)	0	1	0	1	+	-	+	$\Delta v_{Cx3} - \Delta v_{Cx2} + \Delta v_{Cx1}$
S_1'	(a)	1	1	0	0		-		$-\Delta v_{Cx2}$
S_2'	(b)	0	1	1	0	+		-	$-\Delta v_{Cx3} + \Delta v_{Cx1}$
S_3'	(c)	1	0	1	0	-	+	-	$-\Delta v_{Cx3} + \Delta v_{Cx2} - \Delta v_{Cx1}$

the top-side dc-link capacitor $C_{\mathrm{DC}+}$ and are represented with the yellow line, whereas the complementary states involve the condition of the bottom-side capacitor $C_{\mathrm{DC}-}$ and are represented with the green dashed-dotted line.

The ZSS, along with the transistors and the FC that are conducting the load current, are listed in Table I. Note that the conduction or blockage of a power device Q_j, $j = 1, \ldots, 4$, is denoted by a binary number 1 or 0, and the positive and negative signs represent charging and discharging of the FC, respectively. For ease of reference to the circuits shown in Fig. 1, the table also includes the respective subfigure numbers. The last column describes the inverter output voltage as a function of the FCs' voltage deviation from their nominal value, i.e., $\Delta v_{Cj} = v_{\mathrm{DC}} \cdot j/(N-1) - v_{Cj}$, where $j = 1, \ldots, N-2$, and N is the number of levels.

The presence of three independent equations proves that sampling only during the ZSS is adequate for extracting all FC voltages (solving three equations with three unknowns). However, the traditional PWM techniques normally generate up to two ZSS. Therefore, the challenge lies in finding the optimal PWM technique that combines natural balancing with low total harmonic distortion and provides all the ZSS.

B. PWM Strategy

As mentioned earlier, the conventional PWM techniques fail to generate the right number of redundant states to solve the system of linear equations. The well-known phase disposition (PD), phase opposition disposition (POD), and alternative POD (APOD) result in poor balancing due to the single switching state around zero-crossing, i.e., S_1 (0011). This is attributed to the inherent structure of these PWM techniques that require a level shift of the carriers only in the *Y*-axis, thus keeping the two sets of carriers separated at either side of the reference around zero-crossing. An alternative to the conventional PD is proposed in [18], where a trapezoidal carrier replaces the triangular waveforms. The resulting pulse sequence of the MPD matches the sequence of the commonly used phase shift (PS) PWM technique, which is $S_1(0011) - S_2(1001) - S_1'(1100) - S_2'(0110)$. It is the shift of the carriers in time that facilitates the production of different switching states. Therefore, these techniques increase the independent switching states to two, but they are still insufficient for the proposed measurement system.

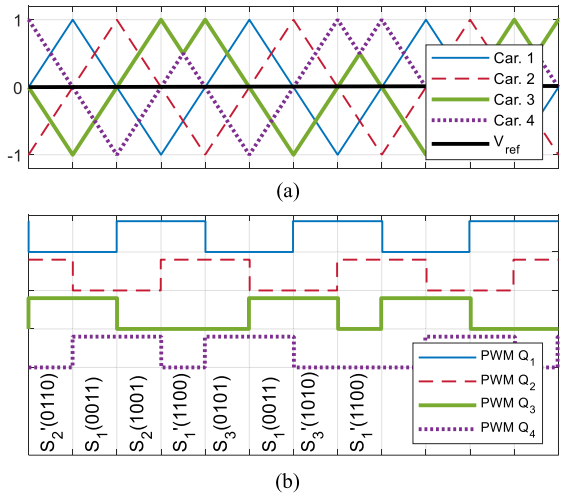

Fig. 2. ZSS sequence around $v_{\mathrm{ref}} = 0$ for the CSPS PWM [13]. (a) Carrier and reference signals around zero-crossing and (b) respective generated pulses.

In contrast to the previously mentioned techniques, the carrier swapping PS (CSPS) PWM, which was first introduced in [13], not only generates an appropriate combination of ZSS but also improves the passive natural balancing. The principle of operation of this method is based on the exchange of two carriers at their meeting point, as presented graphically in Fig. 2. In this example, carriers 3 and 4, marked with thick lines, swap directions when they both reach the 0.5 mark in every period. A complete switching sequence is now comprised of eight pulses, as shown in Fig. 2(b), which is $S_2'(0110) - S_1(0011) - S_2(1001) - S_1'(1100) - S_3(0101) - S_1(0011) - S_3'(1010) - S_1'(1100)$.

Having ensured that all the required ZSS can be produced, the system of linear equations of Table I can now be solved, as shown analytically in following equation:

$$\begin{bmatrix} \Delta v_{Cx1} \\ \Delta v_{Cx2} \\ \Delta v_{Cx3} \end{bmatrix} = \frac{1}{2} \cdot \begin{bmatrix} 1 & -1 & 1 \\ 2 & 0 & 0 \\ 1 & 1 & 1 \end{bmatrix} \cdot \begin{bmatrix} v_{x0}\,(S_1) \\ v_{x0}\,(S_2) \\ v_{x0}\,(S_3) \end{bmatrix}. \quad (1)$$

C. Minimizing the Measurement Error

The two capacitors forming the dc-link, $C_{\mathrm{DC}+}$ and $C_{\mathrm{DC}-}$, may be charged to slightly different voltage levels: $v_{\mathrm{DC}+} = v_{\mathrm{DC}}/2 + \Delta v_{\mathrm{DC}}$ and $v_{\mathrm{DC}-} = v_{\mathrm{DC}}/2 - \Delta v_{\mathrm{DC}}$. Such oscillations

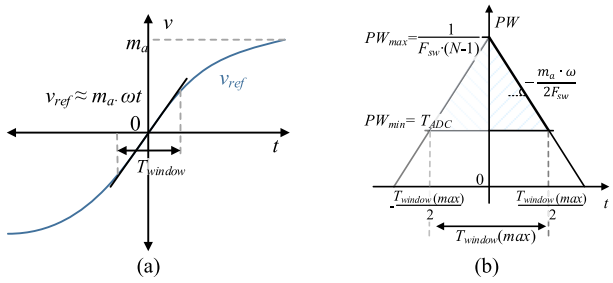

Fig. 3. (a) Representation of the measurement window length around zero-crossing of the reference signal and (b) corresponding PW variation with time, when $m_a = 1$.

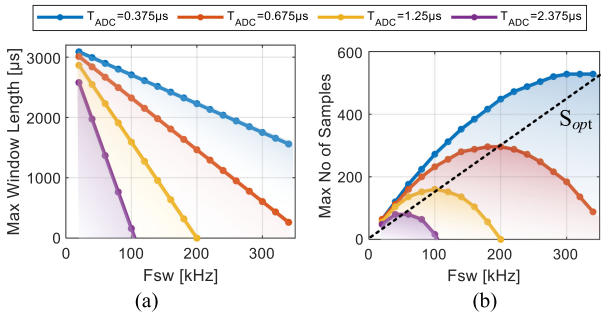

Fig. 4. Variation of (a) maximum window length $T_{\mathrm{window}}(\mathrm{max})$ and (b) maximum number of samples with the switching frequency for a five-level inverter with $m_a = 1$ and various S&H times T_{ADC}.

usually occur in single-phase inverters with small dc-link capacitors or three-phase grid-connected inverter applications under grid voltage disturbances. This deviation will also be reflected in the inverter output voltage and our measurements, given that the current flows through $C_{\mathrm{DC}+}$ during the unique switching states and through $C_{\mathrm{DC}-}$ during their complementary ones. For example, the output inverter voltage during the ZSS S_2 and $S_2{}'$ are accurately presented in (2). To eliminate the effect of the dc-link capacitor mismatch, we need to calculate the difference of the two measurements that correspond to two complementary ZSS, as described in (3). To increase the measurement accuracy even further, we can sample multiple sequences of pulses and calculate the average for each state, as shown in (4), where M is the number of repetitive sequences (measurement window). The only exception to this equation is for the S_1 state that is sampled twice within one complete sequence

$$\begin{cases} v_{x0}\ (S_2) = \Delta v_{Cx3} - \Delta v_{Cx1} + \Delta v_{\mathrm{DC}} \\ v_{x0}\ (S_2{}') = -\Delta v_{Cx3} + \Delta v_{Cx1} + \Delta v_{\mathrm{DC}} \end{cases} \tag{2}$$

$$v_{x0}\ (j) = \frac{v_{x0}\,(S_j) - v_{x0}\,(S_j{}')}{2},\ j = 1, \ldots, 3 \tag{3}$$

$$\bar{v}_{x0}\ (j) = \frac{1}{M} \sum_{1}^{M} \frac{v_{x0}\,(S_j) - v_{x0}\,(S_j')}{2},\ j = 1, \ldots, 3. \tag{4}$$

However, care should be taken on the length of the measurement window (i.e., the number of the sampled sequences) because the pulsewidth (PW) of the ZSS gets narrower as we move away from the zero-crossing point of the reference voltage. More specifically, the maximum length of the measurement window depends on the number of levels of the inverter, the switching frequency, F_{sw}, the amplitude modulation index, m_a, and the S&H time of the ADC module, T_{ADC}.

To quantify this relation, we consider a linear approximation of the reference sin-wave close to zero-crossing, $v_{\mathrm{ref}} = m_a \cdot \sin(\omega t) \cong m_a \cdot \omega t$, as illustrated in Fig. 3(a). The corresponding PW of the ZSS gets its maximum value at $t = 0$, $\mathrm{PW}_{\mathrm{max}} = 1/[(N-1) \cdot F_{\mathrm{sw}}]$ and drops with a rate of $m_a \cdot \omega/(2F_{\mathrm{sw}})$, according to Figs. 3(b) and (5). The maximum PW also defines the sampling period, $F_{\mathrm{smpl}} = (N-1) \cdot F_{\mathrm{sw}}$.

Given that the minimum PW should be equal to T_{ADC}, the maximum number of repetitive sequences is given by (6), where L_{sq} is the number of pulses in one full switching cycle ($L_{\mathrm{sq}} = 8$ in CSPS PWM). Note that the measurement window extends on either side of the zero-crossing point, and thus the final M_{max} is double the value of (6). Let us take as an example a five-level inverter operating at $F_{\mathrm{sw}} = 200$ kHz, 50 Hz reference frequency, $T_{\mathrm{ADC}} = 0.675\ \mu$s and assume the extreme case of a unity amplitude modulation index. The maximum number of repetitive sequences is 36, i.e., 18 sequences on either side of the zero-crossing point

$$\mathrm{PW} = -\frac{m_a \cdot \omega t}{2F_{\mathrm{sw}}} + \frac{1}{(N-1) \cdot F_{\mathrm{sw}}} \tag{5}$$

$$\frac{M_{\mathrm{max}}}{2} = \frac{2 \cdot \left(\frac{1}{N-1} - F_{\mathrm{sw}} \cdot T_{\mathrm{ADC}}\right)}{m_a \cdot \omega} \cdot \frac{F_{\mathrm{sw}}}{L_{\mathrm{sq}}} \tag{6}$$

By substituting (4) into (1), we obtain the core equations (7), which give the FC voltage deviation from their nominal values and will later be implemented in the microcontroller

$$\begin{bmatrix} \Delta v_{Cx1} \\ \Delta v_{Cx2} \\ \Delta v_{Cx3} \end{bmatrix} = \frac{1}{4M} \cdot \begin{bmatrix} 1 & -1 & 1 \\ 2 & 0 & 0 \\ 1 & 1 & 1 \end{bmatrix} \cdot \begin{bmatrix} \frac{1}{2} \cdot \sum_1^{2M} \left(v_{x0}\,(S_1) - v_{x0}\,(S_1')\right) \\ \sum_1^{M} \left(v_{x0}\,(S_2) - v_{x0}\,(S_2')\right) \\ \sum_1^{M} \left(v_{x0}\,(S_3) - v_{x0}\,(S_3')\right) \end{bmatrix}. \tag{7}$$

D. Sensitivity Analysis

In this section, a sensitivity analysis is performed to evaluate the effect of specific parameters on the operation of the measurement system.

1) Variable F_{sw} *and* T_{ADC}*:* Here, we investigate the effectiveness of the proposed measurement system in a wide range of switching frequencies and acquisition speeds. Particularly, for lower F_{sw}, the measurement window can be extended further away from the zero-crossing due to the wider pulses, considering we keep the same value for T_{ADC}. The relation between the maximum measurement window length, $T_{\mathrm{window}}(\mathrm{max})$, and the switching frequency is given in (8), which was derived by solving (5) for t and substituting the PW with T_{ADC}. This relation is graphically represented in Fig. 4(a) for realistic values of the S&H durations. At very low frequencies, all traces converge to the same value given by (9), making the selection of T_{ADC} less

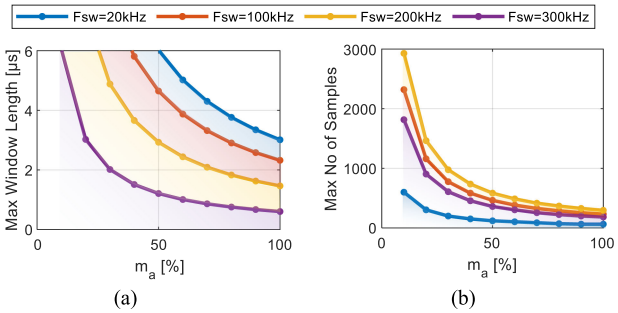

Fig. 5. Variation of (a) maximum window length $T_{\text{window}}(\text{max})$ and (b) maximum number of samples with the amplitude modulation index, for a five-level inverter and various switching frequencies F_{sw}.

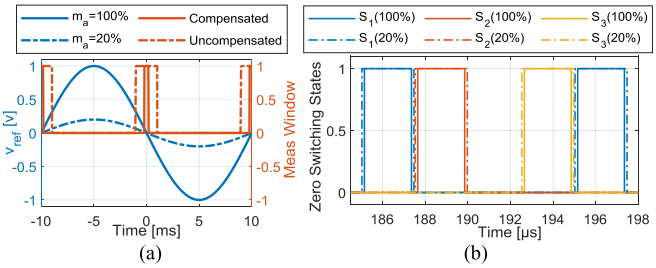

Fig. 6. (a) Reference signals and measurement window for two cases of m_a. (b) Duration of the states S_1, S_2, and S_3 at the edge of the measurement window for two cases of m_a, when T_{window} is 2% of the fundamental frequency.

significant

$$T_{\text{window}}\ (\text{max}) = -\frac{4 \cdot T_{\text{ADC}}}{m_a \cdot \omega} \cdot F_{\text{sw}} + \frac{4}{m_a \cdot \omega \cdot (N-1)} \quad (8)$$

$$T_{\text{window}}\ (\text{max})\,|_{F_{\text{sw}} \to 0} = \frac{4}{m_a \cdot \omega \cdot (N-1)}. \quad (9)$$

More importantly, however, the maximum number of repetitive sequences, $M_{\max}$, has a quadratic relation to the switching frequency, as shown in Fig. 4(b). To find the optimum point where the sample intake is maximized, we take the derivative of (6) equal to zero, as expressed in (10). Substituting the latter into (6) yields the global maximum of the repetitive sequences in (11), which describes a linear relation to the optimum operating frequency and is represented in the number of samples ($S_{\text{opt}} = L_{\text{sq}} \cdot M_{\text{opt}}$) by the black dashed line in Fig. 4(b)

$$\frac{dM_{\max}}{dF_{\text{sw}}} = 0 \leftrightarrow \quad F_{\text{opt}} = \frac{1}{2 \cdot T_{\text{ADC}} \cdot (N-1)} \quad (10)$$

$$M_{\text{opt}} = \frac{2}{m_a \cdot \omega \cdot L_{\text{sq}} \cdot (N-1)} \cdot F_{\text{opt}}. \quad (11)$$

This analysis shows that the proposed measurement system can operate in the entire range defined by the area below a particular trace in Fig. 4, from low to very high switching frequencies. However, at low frequencies, we have the additional option of taking multiple samples within the same state to suppress the noise and increase the measurement accuracy.

2) Variable m_a*:* In the previous examples, we have considered the extreme case of a unity amplitude modulation index, m_a, which is not always the case. In practice, as m_a gets smaller, more ZSS appear further away from the zero-crossing point. This, in turn, increases the maximum measurement window and the respective number of samples, according to (6) and (8). In fact, both are inversely proportional to m_a, as depicted in Fig. 5 for a range of switching frequencies. In most practical applications, where m_a is not a fixed value but is the output of a closed-loop controller, it is recommended to select the measurement window $< T_{\text{window}}(\text{max})$ that corresponds to $m_a = 100\%$.

The continuously varying m_a value poses a challenge for detecting the instance that the system enters the measurement window. More specifically, if the measurement window is detected by comparing $|v_{\text{ref}}|$ with a fixed positive value, its length will constantly change, leading to an arbitrary number of samples intake. This can be resolved by considering a varying upper bound that accounts for the m_a swing, so that the window length remains constant. Its value can derive by tacking the linear approximation of the sine reference close to zero for $t = T_{\text{window}}$, as in (12). Fig. 6(a) illustrates the measurement windows (in red trace) for two modulation indices, $m_a = 20\%$ and 100%. The wider dashed line represents the window length when $m_a = 20\%$ and the modulation index variation is not taken into consideration (uncompensated). On the other hand, the window length stays the same for all modulation indices (solid red line) when (12) is applied

$$|v_{\text{ref}}| \le m_a \cdot \omega \cdot T_{\text{window}},\ T_{\text{window}} \in [0, T_{\text{window}}\ (\text{max})]\,. \quad (12)$$

More importantly, the ZSS always appear in the same predefined positions, regardless of the amplitude modulation index. This is supported by Fig. 6(b), which shows the ZSS S_1, S_2, and S_3 at the edge of the measurement window. Only a small reduction of the pulse duration is observed for larger indices, indicating that synchronizing the sampling action for $m_a = 1$ is adequate for the entire range of m_a values.

3) Application Limits: The reduction of the maximum window length with the switching frequency and the amplitude modulation index (see Figs. 4 and 5) signifies that there are operational limitations of the proposed measurement system, which may become confining in FC MLIs with a large number of levels. To calculate the boundaries of the switching frequency for which the proposed system continues to be applicable, we consider the case where only a single complete sequence of pulses is sampled ($M = 1$). This corresponds to $T_{\text{window}}(\text{max}) = 2/F_{\text{sw}}$, given that one complete sequence is unfolded within two switching periods, as shown in Fig. 2. At the same time, we can consider the worst-case scenario of unity amplitude modulation index, $m_a = 1$, which corresponds to the narrowest measurement window. Solving (8) for F_{sw} we get the quadratic relationship (13), which leads to the minimum and maximum applicable frequencies of (14). Note that the positive sign in (14) corresponds to $F_{\text{sw}}(\text{max})$ and the negative sign corresponds to $F_{\text{sw}}(\text{min})$. The latter also defines the maximum number of levels, expressed in (15), so that the argument of the square root

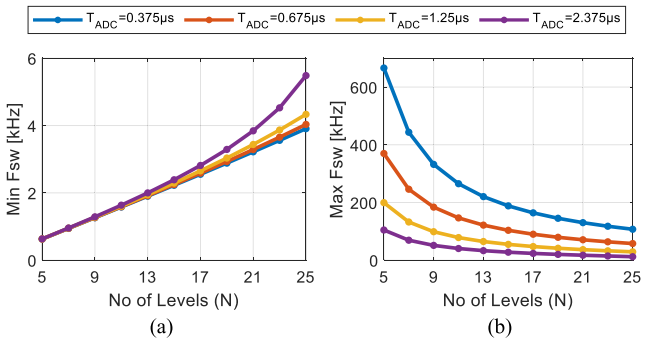

Fig. 7. (a) Minimum and (b) maximum switching frequencies for which the proposed clamping circuit continues to be applicable for various numbers of levels and S&H times.

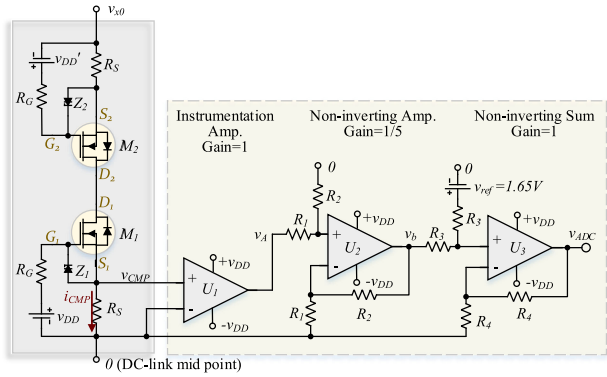

Fig. 8. Schematic diagram of the proposed bidirectional clamping circuit with two n-type MOSFETs in common drain configuration.

is positive

$$\left(\frac{2\cdot T_{\text{ADC}}}{\omega}\right)F_{\text{sw}}^2-\left(\frac{2}{\omega\cdot(N-1)}\right)F_{\text{sw}}+1\;=\;0 \tag{13}$$

$$F_{\text{sw}\,\text{min}}^{\text{max}}=\frac{1\pm\sqrt{1-2\cdot T_{\text{ADC}}\cdot\omega\cdot(N-1)^2}}{2\cdot T_{\text{ADC}}\cdot(N-1)} \tag{14}$$

$$N\le 1+\sqrt{\frac{1}{2\cdot T_{\text{ADC}}\cdot\omega}} \tag{15}$$

Fig. 7 illustrates the minimum and maximum boundaries of the switching frequency for a variable number of levels and T_{ADC} values. Considering, for example, $F_{\text{sw}}=100$ kHz and $T_{\text{ADC}}=0.675$ μs, the proposed clamping circuit is applicable in inverters of up to 15 levels by reducing the number of repetitive sequences to be sampled. However, in practical applications, this reduction might come at the cost of lower measurement accuracy in the presence of switching noise.

III. Bidirectional Clamping Circuit

Placing a clamping mechanism at the inverter switching node allows us to capture just the FC voltage variation with a narrow measurement range and fast sampling. At the same time, the rest of the acquisition circuit (amplifiers, ADC module, and microcontroller) remains safe from the high voltage swing of v_{x0}.

There are several different clamping circuits for high-voltage, high switching frequency waveforms, commonly used in short-circuit protection schemes (e.g., desaturation approach) or in the evaluation of the dynamic ON-resistance of the GaN devices, known as current collapse phenomenon, [48]–[54]. The basic idea is that when the input voltage surpasses a predefined level, it gets clamped, allowing accurate measurements within a narrow window around zero voltage. Thus, the resolution of the data acquisition is increased by $v_{\text{PP}}/v_{\text{CLP}}$, where v_{PP} is the peak-to-peak input voltage and v_{CLP} is the clamping voltage (e.g., 30 times for $v_{\text{pp}}=600$ V and $v_{\text{CLP}}=20$ V). However, these circuits provide only unipolar clamping capability, meaning that they cannot clamp or they should not be operated with negative voltages altogether, which prevents their adoption in inverter applications.

The simplest bidirectional clamping method consists of two identical clamping diodes in a half-bridge configuration, biased to $\pm\,v_{\text{DD}}$, and a high-power resistor R_{CLP} that connects the inverter output to the midpoint of the diode configuration. When $|v_{x0}|>v_{\text{DD}}$, the diodes conduct, saturating their midpoint voltage to $\pm|v_{\text{DD}}-v_{D\text{-on}}|$, where $v_{D\text{-on}}$ is the diode voltage drop. As the clamping resistor's value increases, the current flowing through the diodes decreases, decoupling the measurement from the diodes' *I–V* characteristics, and the power dissipation on the resistor also decreases, meaning that a smaller package device can be used. However, the value of R_{CLP}, along with the parasitic capacitance of the diodes and the input capacitance of the next stage (e.g., amplifier), dictates the time response of the measurement unit. Therefore, this approach is viable in low switching frequencies (below 10 kHz) and high-voltage applications.

In this article, we propose a new circuit for precise bidirectional clamping, with low power dissipation, a small footprint, and low implementation cost.

A. Principle of Operation

The core of the new clamping topology consists of two n-type MOSFETs of similar characteristics in common drain configuration and two source resistors, R_S, as shown in Fig. 8. For each device, a fixed voltage source is connected across the gate terminal and the source resistor, so that the gate-to-source voltage, v_{GS}, depends on the value of v_{x0} and the resulting voltage drop across R_S. The principles of operation of the circuit are described in three separate modes.

1) *Mode 1. M_1 and M_2 are conducting:* For small positive values of v_{x0}, both MOSFETs are ON and the current i_{CMP} flows with a direction from S_1 to the midpoint of the dc-link, and thus the clamping output voltage is given by (16). v_{CMP} can also be expressed as a function of the switching node voltage, as in (17), where R_{DSon} is the transistors' ON-resistance. Under these conditions, the gate-to-source voltage levels are given by (18) and (19), considering that both polarization sources have the same amplitude $v_{\text{DD}}{}'=v_{\text{DD}}$

$$v_{\text{CMP}}=i_{\text{CMP}}\;\cdot R_S \tag{16}$$

$$v_{\mathrm{CMP}} = \frac{v_{x0}}{2} \cdot \frac{1}{1+\frac{R_{\mathrm{DSon}}}{R_S}} \tag{17}$$

$$v_{\mathrm{GS1}} = v_{\mathrm{DD}} - v_{\mathrm{CMP}} \tag{18}$$

$$v_{\mathrm{GS2}} = v_{\mathrm{DD}}{}' + i_{\mathrm{CMP}} \cdot R_s = v_{\mathrm{DD}} + v_{\mathrm{CMP.}} \tag{19}$$

2) *Mode 2. M_1 is blocking, and M_2 is conducting:* As the switching node voltage increases, the controlling voltage of the low-side MOSFET drops according to (18) and enters the blocking mode when v_{GS1} reaches the threshold voltage, v_{th}, as expressed in (20). At this point, a voltage equilibrium is established, where the current i_{CMP} remains constant, the clamping circuit outputs a fixed value of $v_{\mathrm{DD}} - v_{\mathrm{th}}$, and the transistor M_1 operates in the critical blocking mode with its $v_{\mathrm{GS1}} = v_{\mathrm{th}}$. At the same time, the high-side MOSFET remains in the conduction mode with its controlling voltage saturated at its maximum value, given by (21). This mode holds for all the inverter output voltage values above the upper bound described by (22)

$$v_{\mathrm{GS1}} = v_{\mathrm{th}} \leftrightarrow v_{\mathrm{CMP}} = v_{\mathrm{DD}} - v_{\mathrm{th}} \tag{20}$$

$$v_{\mathrm{GS2max}} = 2 \cdot v_{\mathrm{DD}} - v_{\mathrm{th}} \tag{21}$$

$$v_{x0} \geq 2 \cdot (v_{\mathrm{DD}} - v_{\mathrm{th}}) \cdot \left(1 + \frac{R_{\mathrm{DSon}}}{R_S}\right). \tag{22}$$

3) *Mode 3. M_1 is conducting, and M_2 is blocking:* Similarly, when $v_{x0} < 0$, M_2 enters the blocking mode when (23) is satisfied. During this state, the low-side MOSFET gets its maximum controlling voltage, given in (24) and the clamping circuit output is a fixed value of $-v_{\mathrm{DD}} + v_{\mathrm{th}}$. This operating mode corresponds to the switching node voltage range given in (25), i.e., below the lower bound

$$v_{\mathrm{GS2}} = v_{\mathrm{th}} \leftrightarrow v_{\mathrm{CMP}} = -(v_{\mathrm{DD}} - v_{\mathrm{th}}) \tag{23}$$

$$v_{\mathrm{GS1max}} = v_{\mathrm{GS2max}} = 2 \cdot v_{\mathrm{DD}} - v_{\mathrm{th}} \tag{24}$$

$$v_{x0} \leq -2 \cdot (v_{\mathrm{DD}} - v_{\mathrm{th}}) \cdot \left(1 + \frac{R_{\mathrm{DSon}}}{R_S}\right). \tag{25}$$

It is important to note that the integrated antiparallel diodes of the MOSFETs are connected in a common-cathode configuration, and thus there is no unregulated conduction under any circumstances.

The instrumentation amplifier U_1 shown in Fig. 8 is used as a buffer between the clamping point and the ADC module of the microcontroller, with the advantage that it rejects the common mode noise because of the well-matched integrated resistors. An amplifier with very low noise and a wide operating range should be selected for this stage, such as the AD8421ARMZ. The dual operational amplifier U_2–U_3 that follows is used for scaling and shifting the measured signal to the appropriate values for the ADC. The signal is first scaled down to fit within the acceptable ADC range (normally 3.3 V) and then shifted by 3.3/2 V = 1.65 V. The operational amplifier should exhibit a high slew rate and low peak-to-peak noise, such as the OPA2189.

The advantage of the proposed clamping circuit is that it can measure both positive and negative voltages with a resolution gain of $v_{\mathrm{DC}}/v_{\mathrm{DD}}$ in contrast to traditional voltage measurements. This addresses the noise sensitivity that most ac-side monitoring systems suffer from.

B. Design Recommendations and Reliable Operation

In this section, we lay out some key design specifications to ensure the safe operation of the proposed circuit, based on the previous mathematical analysis.

An important requirement is to ensure that the v_{GS} voltage never exceeds the limits set by the manufacturer. This, in turn, determines the maximum allowable voltage source used for the polarization of the transistors. According to (24), v_{DD} should be lower than $0.5{\cdot}(v_{\mathrm{GSmax}}{+}v_{\mathrm{th}})$.

Equation (17) reveals the dependence of the clamped voltage on the transistors' ON-resistance, quantified by the factor $\lambda = R_{\mathrm{DSon}}/R_S$. To minimize this effect, transistors with low ON-state resistance should be selected, compared to the value of R_S. However, it should be noted that large R_S values may introduce a time delay caused by the transistor parasitic output capacitance, and thus a tradeoff between measurement deformation and acquisition speed needs to be found.

A general concern with clamping circuits that use active devices is the large voltage spike in transients with large dv_{x0}/dt. A sharp transition causes high current flowing through the transistors' parasitic capacitance and the source resistors. The simplest way to suppress these voltage peaks is to select transistors with small output and gate capacitance. Alternatively, a Zener diode can be placed between the gate and source terminals of each power device to clamp their voltage to values below $(2{\cdot}\mathrm{v_{DD}}{-}v_{\mathrm{th}})$, as illustrated in Fig. 8.

An example of the aforementioned recommendations is presented here, based on the STD8N60DM2 transistor and $R_S = 200\ \Omega$. According to the datasheet, –25 V $\leq v_{\mathrm{GS}} \leq$ +25 V and $v_{\mathrm{th}} = 4$ V, and thus the maximum allowable value for the polarization voltages is $v_{\mathrm{DDmax}} = 14.5$ V. With a typical $R_{\mathrm{DSon}} = 0.55\ \Omega$ and 13.5 nC gate charge, the distortion factor λ is just 0.275% and the voltage spikes do not exceed 30 V.

IV. Simulation Results

To evaluate the performance of the proposed FC measurement system, a series of simulations were performed, starting with device-level simulation of the clamping circuit followed by system-scale simulations of the entire grid-connected MLI.

A. Device-Level Simulation

This section focuses on the detailed simulation of the clamping circuit in LTspice, using the analytical MOSFET and amplifier models, provided by the manufacturers. To reduce the simulation complexity and time, we can replace the entire power circuit (dc-link, inverter leg, and load) with an independent source that represents the inverter switching node and has a predefined time–voltage sequence. This sequence can be generated by a high-level simulation platform, such as MATLAB/Simulink.

The simulation parameters along with the component values are tabulated in Table II. The v_{x0} voltage source corresponds to a five-level FC inverter, operating at 100 kHz switching frequency,

TABLE II
LTSPICE SIMULATION PARAMETERS, COMPONENTS, AND VALUES

Parameter	Name/Value	Parameter	Value
Levels	5	F_{sw}	100 kHz
nMOSFETs	STP8NM60	v_{DC}	700V
Zener Diodes	KDZ22B	RS	200 Ω
Instrumentation Amplifier	AD8421	R_G	1 Ω
		v_{DD}	15 V

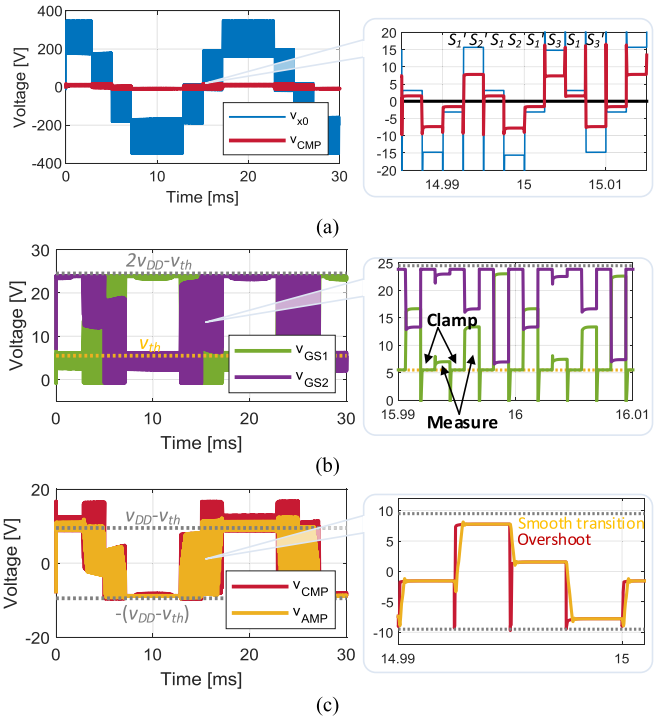

Fig. 9. LTspice simulation results of the proposed clamping circuit. (a) Switching node voltage and clamping circuit output. (b) Gate–source voltages of M_1 and M_2. (c) Instrumentation amplifier output against v_{CMP}.

50 Hz fundamental frequency, and $v_{\mathrm{DC}} = 700$ V. A relatively large voltage deviation from the nominal values has deliberately been introduced to all FC to evaluate the accuracy and speed of the clamping circuit in extreme conditions.

The inverter switching node voltage and the clamping circuit output are presented in Fig. 9(a). In addition, the sequence of eight states of the applied CSPS PWM is indicated in the zoomed view. It can be observed that the proposed scheme safely contains the voltage to the desired range ±19 V, in accordance with (22) and (25). Additionally, v_{CMP} follows closely the v_{x0} waveform around zero-crossing with half its amplitude, which agrees with (17) if we neglect the effect of the distortion factor ($\lambda = 0.45\%$ in this scenario). A small voltage overshoot is evident during each transient, which is effectively limited by the Zenner diode across the gate–source terminals of the clamping transistors.

Fig. 9(b) illustrates the gate–source voltages of the two transistors, along with the v_{th} line and the maximum allowable voltage level, given by (24). The zoom box focuses on a small timeframe around $t = 16$ ms; when v_{x0} switches between 0 V and $v_{\mathrm{DC}}/4$, M_1 clamps the positive switching node voltage. As expected, $v_{\mathrm{GS1}} = v_{\mathrm{th}}$ and $v_{\mathrm{GS2}} = 2{\cdot}v_{\mathrm{DD}} - v_{\mathrm{th}}$ during the non-ZSS.

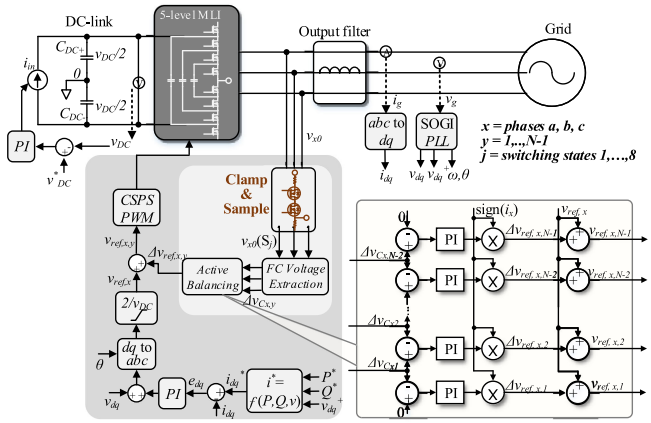

Fig. 10. Complete control scheme of the grid-connected MLI with active FC balancing using the measurements of the proposed clamping circuit.

TABLE III
MATLAB/SIMULINK SIMULATION PARAMETERS

Parameter	Value	Parameter	Value
Levels	5	$k_{P\text{-}PLL}$	0.2
P_{nom}	5 kW	$k_{I\text{-}PLL}$	3
v_{DC}	700 V	k_{SOGI}	3
F_{sw}	100 kHz	$k_{P\text{-}current}$	20
C_{DC+}, C_{DC-}	50 µF	$k_{I\text{-}current}$	2000
C_{FC}	10 µF	$k_{P\text{-}bal}$	$2{\cdot}10^{-5}$
L_F	270 µH	$k_{I\text{-}bal}$	0.02

The output of the instrumentation amplifier, v_{AMP}, is plotted against the v_{CMP} waveform in Fig. 9(c). The zoomed view reveals that v_{AMP} matches v_{CMP} in amplitude but exhibits smoother transients as a result of the limited slew rate (35 V/μs) of the AD8421.

B. System-Scale Simulations

The complete control scheme of a grid-tied MLI with the active balancing of the FC, based on the proposed measurement system, was developed in MATLAB/Simulink and is presented in Fig. 10. A simple grid-following current control was employed, as presented in [55], and a double second-order generalized integrator phase-locked loop (PLL) helps extract the positive sequence of the grid voltage and calculate the instantaneous phase. The switching frequency was set at 100 kHz, allowing for small dc-link and FC values of 50 μF and 10 μF, respectively. All the simulation parameters are listed in Table III.

The implemented active balancing scheme is based on the work of Gias *et al.* [56], according to which the voltage of each FC can be regulated from the duty cycle of the two adjacent switches. In particular, the average current through each FC is given by (26) as a function of the output current and the duty cycles produced by the current controller. According to this equation, if the output current is positive and the FC C_{xy} is overcharged, the controller should reduce the current $\overline{i_{Cx,y}}$ by slightly increasing $d_{x,y}$ and decreasing $d_{x,y+1}$. Similarly, if the capacitor is undercharged, the controller should increase $\overline{i_{Cx,y}}$ by increasing $d_{x,y+1}$ and decreasing $d_{x,y}$. The opposite holds

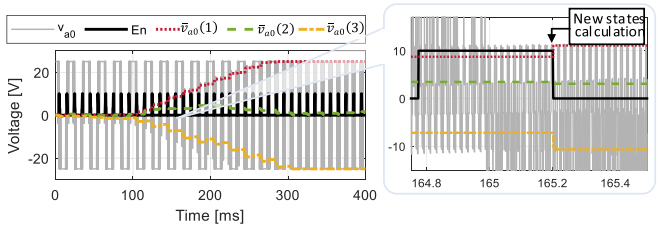

Fig. 11. Sampling of the clamped inverter output voltage during the three independent ZSS, around zero-crossing.

for a negative load current

$$\overline{i_{Cx,y}} = (d_{x,y+1} - d_{x,y}) \cdot \overline{i_o}, \quad x = \text{a, b, c and } y = 1, \ldots, N-2. \tag{26}$$

However, contrary to the work presented in [56], we generate this small variation around $d_{x,y}$ by adjusting the PWM reference voltage of each power device, $v_{\text{ref }x,y}$, separately, instead of feeding an offset directly to the resulting duty cycle. This approach achieves equivalent results but in a more efficient manner for practical implementation in a microcontroller. The active balancing control is mathematically represented by (27) and is illustrated in the control diagram shown in Fig. 10. A $\Delta v_{\text{ref }x,y}$ offset is introduced to the original reference voltage for each phase, $v_{\text{ref }x}$, tuned by a proportional-integral (PI) controller, the gains of which are listed in Table III. The controller's output is multiplied by the sign of the output current to ensure proper operation during both the positive and negative phase currents. The error signals correspond to the voltage variation of the FC, as described by (28)

$$v_{\text{ref }x,y} = v_{\text{ref }x} + \underbrace{\text{sign}\,(i_o)\left(\text{k}_{P-\text{bal}} + \frac{k_{I-\text{bal}}}{s}\right)(e_{x,y-1} - e_{x,y})}_{\Delta v_{\text{ref }x,y}} \tag{27}$$

$$e_{x,y} = \Delta v_{Cx,y} \text{ and } e_{x,0} = e_{x,N-1} = 0. \tag{28}$$

To simulate a voltage imbalance in the FCs, we simply introduce an asymmetry in phase leg a, in the form of a higher leakage current in one transistor, specifically the $Q_{a,2}{}'$. The asymmetry is enforced in a step manner at $t_0 = 100$ ms. During this scenario, the balancing control is disabled to facilitate better understanding of the clamping circuit and the measurement system in an extreme case.

Fig. 11 shows the clamped inverter voltage v_{a0}, along with the measurements over the three independent ZSS, according to (4). The window around zero-crossing during which the samples are captured and the averaging is performed is marked with a thick black line (En). As can be seen from the zoom box on the right, the new values of $\bar{v}_{a0}(j)$ are extracted at the end of the measurement window. Due to the introduced imbalance, the measurements reach the clamping value (25 V) at $t_1 = 285$ ms. After this point, the acquired data no longer capture the actual voltage deviation of the FC.

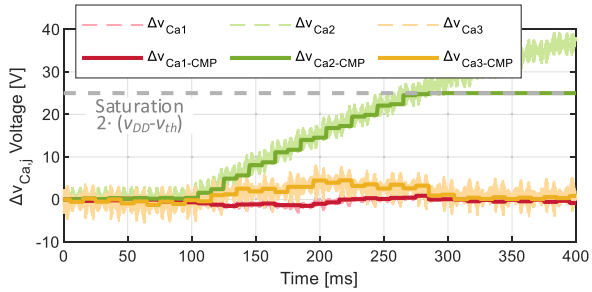

Fig. 12. Extracted volage deviation of the FC from the clamping circuit measurements, during imbalanced conditions.

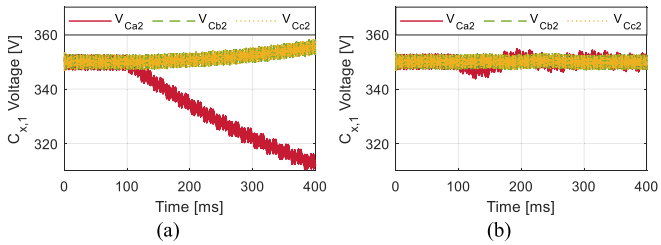

Fig. 13. Variation of the FC $C_{x,2}$ voltages with time, during asymmetric conditions, (a) without and (b) with an active balancing control.

The extracted values from the clamping circuit, $\Delta v_{\text{Ca},j}$, are presented in Fig. 12 with thick solid lines. For comparison purposes, this graph also includes the reference Δv_C waveforms calculated from direct measurements across the FC and the dc-link, as if we had a separate sensor over each capacitor. It can be observed that the proposed approach follows the reference data accurately, with an update rate of double the fundamental grid frequency (steps of 10 ms). In this unbalanced scenario, the calculated $\Delta v_{\text{Ca},j}$ reaches its maximum value at t_1.

Next, we repeat the simulation with the balance mechanism enabled. The voltage variation $C_{x,2}$ during the imbalance with and without the enforcement of the active balancing control is illustrated in Fig. 13. It is important to highlight that the asymmetry is cascaded in all phases, regardless of the origin of the initial imbalance, as can be observed from Fig. 13(a). The imbalance is largely mitigated when the active balancing scheme is activated, as revealed in Fig. 13(b). The added benefit of the active balancing controller is that the $\bar{v}_{x0}(j)$ measurements do not reach the clamping voltage, ensuring accurate acquired data even under disturbances.

Fig. 14 illustrates the active balancing controller output for phase a, during the introduction of the asymmetry. These offsets are added to the reference signal $v_{\text{ref},x}$, and driven to the top-side transistors.

C. Performance Under Dynamic Conditions

In this section, we investigate the effectiveness of the voltage monitoring system and the controllability of the FC during sudden load change, power factor (PF) variations, and grid imbalances.

More specifically, the grid-connected MLI was initially simulated with a step change of the active power fed to the grid, from 50% to 100% of the nominal value, as shown in Fig. 15(a).

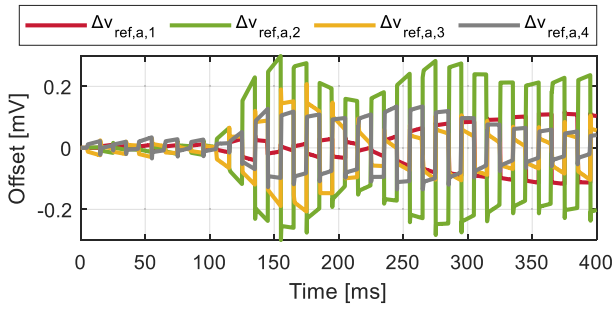

Fig. 14. Active balancing control output. Added offset on the reference voltage, $\Delta v_{\mathrm{ref}\ x,y}$, for each transistor in phase a.

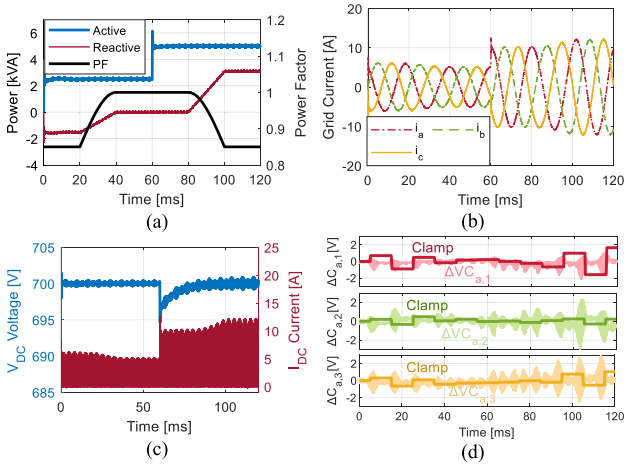

Fig. 15. Response of the proposed measurement system under abrupt load change and PF variations. (a) Active and reactive powers along with the PF variation. (b) Grid injected current. (c) DC-link voltage and current. (d) Proposed measurement output against the actual FC voltage variation $\Delta V_{a,y}$.

At the same time, the reactive power increases with rampwise increments from -1.55 kVar to 0 and then to $+3.1$ kVar, which corresponds to a PF variation from 0.85-lagging to 1 and then back to 0.85-leading. Note that the active power step change happens when PF $= 1$ to decouple the effect of these two variations. The grid current waveforms are depicted in Fig. 15(b). The dc-link capacitors experience a sudden voltage drop, shown in Fig. 15(c), the extent of which is regulated by the PI dc-link controller. Under these conditions, the measurements extracted by the clamping circuit for phase a are plotted against the actual voltage deviation of the FC from their nominal values in Fig. 15(d). It is evident that even under abrupt load changes, the clamping circuit precisely captures the FC voltages. However, small oscillations exist for low PF values, which is a reflation of the FC charge variation under a nonzero capacitor current within the sampling window. Still, these oscillations are found to be acceptable for the 0.85 PF, which is a typical lower bound for many grid-connected inverters.

Furthermore, the response of the system is examined under an abrupt grid imbalance, triggered by a single-phase grid voltage drop to 20% of its nominal value for 100 ms according to Fig. 16(a) (e.g., a nearby single-line fault). This fault condition results in excess current flowing in phase a [see Fig. 16(b)] and subsequently in oscillations of the active and reactive powers of double the fundamental frequency, as shown in Fig. 16(c). These

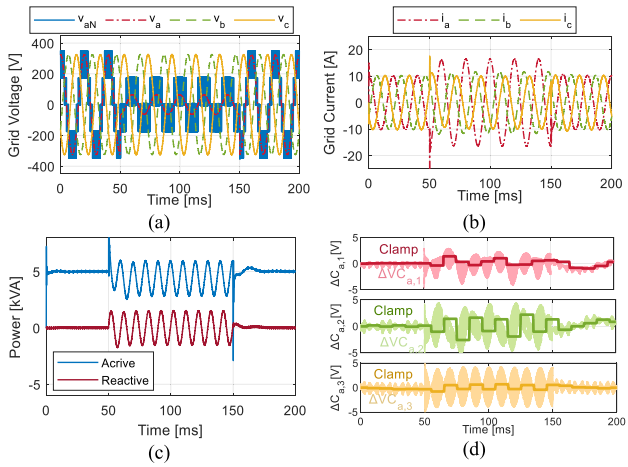

Fig. 16. Dynamic response of the proposed measurement system under load imbalances. (a) Inverter and grid voltage. (b) Grid current. (c) Active and reactive powers. (d) Proposed measurement output against the actual FC voltage variation $\Delta V_{a,y}$.

oscillations are also reflected to the FC voltages in the form high-frequency (F_{sw}) ripple enclosed within the low-frequency envelope of 100 Hz, as shown in Fig. 16(d). Despite the large FC charge variation under these extreme conditions, the proposed sensor performs well and follows the target voltages closely.

V. Experimental Validation

The objective here is to experimentally validate the operating principles of the proposed clamping circuit and assess the accuracy of the synchronous sampling and the resulting FC voltage measurements. For this purpose, we designed and developed the FC MLI described in the following section.

A. Hardware Design

All experiments we performed using the five-level, all-GaN FC inverter prototype, shown in Fig. 17(a). The main printed circuit board (PCB) holds the dc-link, the dc and ac input and output measurement sensors, the microcontroller, and the output relays. Each of the dc-link capacitors, $C_{\mathrm{DC}+}$ and $C_{\mathrm{DC}-}$, is comprised of 12 parallel connected polypropylene film capacitors, with a total capacitance of $12 \cdot 4.7\mu\mathrm{F} = 56.4\ \mu\mathrm{F}$, which is very close to the simulation model. The power and measurement modules, as well as the output filter, are mounted on separate boards for maximum flexibility in the design.

Each phase unit consists of two circuit boards: 1) the power board, in white solder-mask, shown in Fig. 17(b), that contains the GaN power devices, the gate drivers, and the voltage and power isolators. The FCs are mounted on the backside of this board, as depicted in Fig. 17(c). As can be seen, each FC consists of several multilayer ceramic capacitors (MLCCs) connected in parallel to match the 10 μF value of the simulation model at the rated conditions. However, the number of paralleled MLCCs is determined by the voltage stress on each FC, given that MLCCs exhibit a sharp capacitance decline with the applied dc bias. Particularly for the capacitors used in our prototype (C5750X6S2W225K250KA), the dc bias curve is provided in the manufacturer's characterization sheet [57], from which we

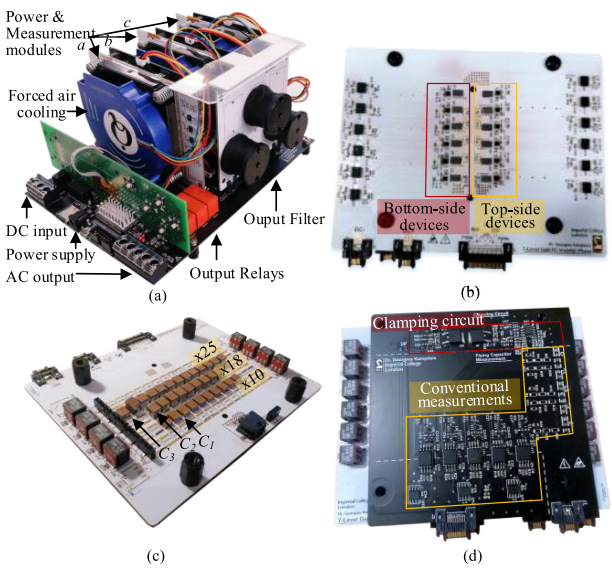

Fig. 17. (a) All-GaN three-phase MLI prototype used for the experimental validation. (b) Top and (c) bottom view of a single-phase power board. (d) FC measurement board containing the clamping circuit and conventional measurements.

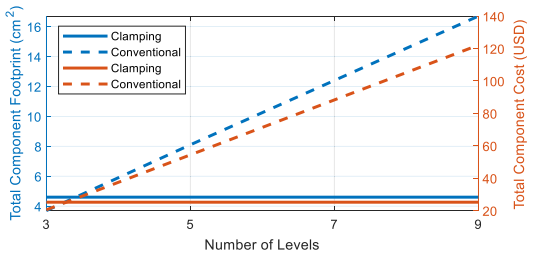

Fig. 18. Cumulative component footprint and total component cost for the conventional and the proposed measurement systems when varying the number of levels.

TABLE IV
LIST OF COMPONENTS OF THE SEVEN-LEVEL INVERTER PROTOTYPE

Main and Filter Board		**Power Board**			
Component	*Part No*	*Component*	*Part No*		
DC-link Capacitors	ECW-FD2W475KC 12p2s configuration	Flying Capacitors	C5750X6S2W225K250KA		
			$C_{x,1}$ 10p1s	$C_{x,2}$ 18p1s	$C_{x,3}$ 25p1s
microcontroller	F28384D	GaN Devices	EPC2034		
Current sensor	MLX91221	Gate Driver	UCC27611DRVT		
Voltage isolator	ACPL-C87A	Digital isolator	Si8610BC-B-IS		
ADC module	ADS7953	Power isolator	MTU1S1205MC		
Output relays	RZ03-1A4-D012	Heatsink	ATS-UC-DFLOW-100		
Filter Inductors	1140-271K-RC	F_{sw}	100 kHz		
Measurement Board					
Clamping Circuit		**Conventional Measurement**			
Component	*Part No*	*Component*	*Part No*		
MOSFETs	STD8N60DM2	voltage isolator	ACPL-C87A		
Instrumentation Amp	AD8421ARMZ	Operation Amp	TLC277		
Operation Amp	OPA2189				
Zener Diodes	KDZVTFTR20B				
R_S	200 Ω				
v_{DD}	12V				

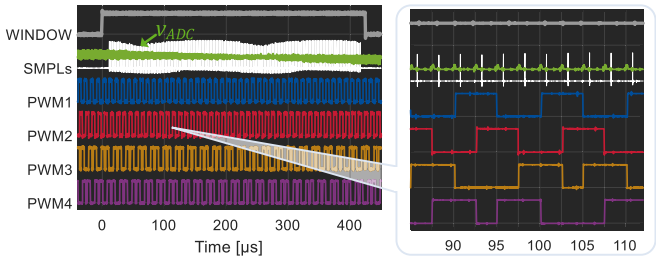

Fig. 19. ZSS sequence for the CSPWM strategy in a five-level inverter. The measurement window is represented by the gray trace, the samples by the white solid line, and the v_{ADC} signal by the green waveform. The zoomed view highlights that the samples are taken shortly after the beginning of the pulses, avoiding the transient overshoots.

calculate that 10, 18, and 25 MLCCs are needed for $C_{x,1}$, $C_{x,2}$, and $C_{x,3}$, respectively.

Although the prototype can support up to seven levels, two cells have been bypassed to investigate a five-level inverter, for consistency with the rest of this article. 2) The measurement board in black solder-mask is shown in Fig. 17(d), which contains the proposed clamping circuit, marked with a red line. For comparison purposes, this board also holds a conventional measurement system with separate voltage sensors for every FC, marked with yellow line. For maximum heat extraction, a forced-air cooling heatsink is placed in contact with the top side of all power devices and regulated by the microcontroller through a temperature feedback signal. A complete list of the components used in this experimental setup is given in Table IV.

From Fig. 17(d), it is evident that the footprint of the clamping circuit is smaller than that of the traditional measurements circuit, and, more importantly, it does not scale with the number of levels. This is also supported by Fig. 18, which shows the cumulative component footprint (in blue traces), for a fair comparison of both circuits, for a different number of levels. In practice, however, the resistive divider method in the conventional measurement approach requires an even wider PCB area to account for the isolation zones (clearance and creepage) between the different voltage levels. The same figure also includes an indicative cost of the two approaches (red traces), considering the prices of individual components, as of January 2022. From this graph, it can be concluded that the proposed approach is preferable when $N \geq 5$. For example, when $N = 7$, the clamping circuit occupies 2.7 times less space and costs 3.5 times less than the traditional measurement system.

B. Experimental Results

Here, we aim to capture the characteristic waveforms of the clamping circuit in balanced and unbalanced conditions, under different dc-link voltage levels.

First, the switching frequency was set at $F_{\mathrm{sw}} = 100$ kHz, which leads to a ZSS PW of 2.5 μs. The CSPS PWM technique was applied with carriers 3 and 4 switching positions at their intersecting point, as shown in Fig. 19. It should be noted that the implementation of this PWM strategy barely adds any computational cost to the microcontroller, since the direction swapping is done in a single command. The same figure also captures the measurement window around zero-crossing (in gray line) and the sample instances (in white). With the measurement window extending to 1% of the fundamental period on either

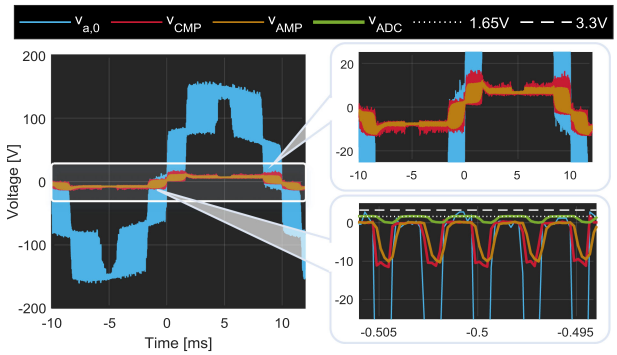

Fig. 20. Waveforms at the different stages of the clamping circuit when $v_{\mathrm{DC}} = 300$ V. The inverter output is shown in blue line, the clamped voltage in red, and v_{AMP} corresponds to the brown curve. The zoomed view on the bottom right includes the waveform fed to the ADC module, the reference, and maximum lines at 1.65 V and 3.3 V, respectively.

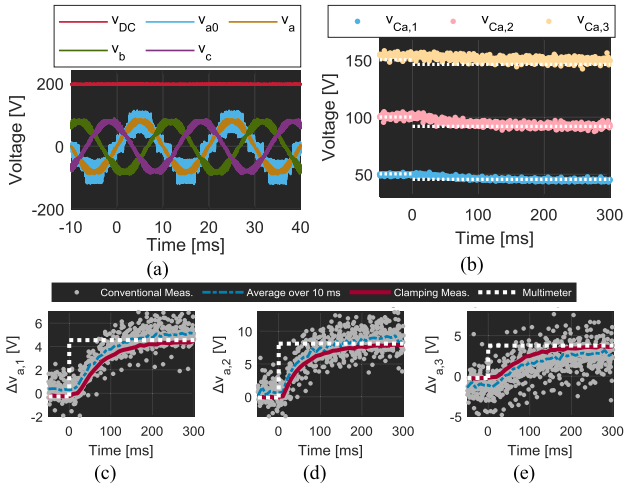

Fig. 21. (a) Input and output voltage waveforms for the five-level inverter when $v_{\mathrm{DC}} = 200$ V. (b) FC voltages measured with the conventional voltage divider and digital multimeter values under stepwise asymmetry introduced on $C_{a,2}$ at $t_0 = 0$. Comparison of the voltage variation of the FC (c) $\Delta v_{\mathrm{Ca},1}$, (d) $\Delta v_{\mathrm{Ca},2}$, and (e) $\Delta v_{\mathrm{Ca},3}$, between the traditional voltage devider sensor and the proposed clamping method.

side of the zero-crossing point, we get 160 samples in total, one every 2.5 μs, which corresponds to 20 complete ZSS sequences.

It is important to note that the acquisition action happens synchronously in every zero-crossing, starting always from the same ZSS, which is S_2 in our system. This is achieved by having the microcontroller initiate the sampling action the first time this state is reached, given that the measurement window signal has been pulled high, indicating the beginning of a new zero-crossing event. Additionally, every sample is taken shortly after the start of the pulse, as can be seen from the zoomed view in Fig. 19, to avoid the transient overshoots and to ensure that the ADC S&H process, $t_{\mathrm{ADC}} = 0.675$ μs, fits well within the 2.5 μs pulse. This fixed delay from the beginning of the pulse is tuned through the microcontroller.

Fig. 20 shows the output waveform of the clamping circuit against the switching node voltage of phase a and the output of the instrumentation amplifier when the system was operated at $v_{\mathrm{DC}} = 300$V. The top-right zoomed view highlights the clamping action that takes place when the switching node voltage exceeds the boundaries expressed in (22) and (25), and the bottom-right view reveals the smoother transition of the amplifier, as a result of its limited slew rate. It also includes the scaled and shifted signal fed to the ADC module with a reference voltage of 1.65 V and a maximum value of 3.3 V.

To evaluate the performance of the proposed measurement system in static and dynamic conditions, we disabled the active balancing control, and we introduced a step-like asymmetry in the form of a resistor, R_{asym}, connected in parallel with $C_{a,2}$ at $t_0 = 0$. This artificial asymmetry is an effective method to induce a voltage drop on all the FC of the same phase leg. Both three-phase and single-phase inverter topologies were tested over a wide range of dc-link voltages.

For the first experiment, we investigated a three-phase inverter feeding a symmetrical resistive load, $R_{\mathrm{load}} = 210$ Ω, under $v_{\mathrm{DC}} = 200$ V and $R_{\mathrm{asym}}. = 11.75$ kΩ. Fig. 21(a) shows the inverter input and output voltage waveforms under these conditions, whereas the FC voltage levels, measured by the traditional resistive divider, are illustrated in Fig. 21(b). All capacitor voltages drop from their steady-state level, with $C_{a,2}$ exhibiting the highest drop. The white dotted lines in this graph correspond to the true-rms voltages before and after the imbalance, measured via a digital multimeter and considered the benchmark in the following comparison.

The true advantage of the proposed system is highlighted in Fig. 21(c)–(e), which presents the voltage difference $\Delta v_{\mathrm{Ca},y}$ extracted with three different measurement techniques.

1) The gray markers represent the data taken from the traditional measurement system. The dashed line corresponds to the average value of these data, taken every 10 ms for a direct comparison with the clamping circuit.
2) The red solid lines indicate the waveforms recorded from the proposed clamping method.
3) The white dashed lines represent the true-rms reference levels, measured by a digital multimeter.

The measurements from the clamping circuit match perfectly with the steady-state voltage deviation, both before and after the imbalance. On the contrary, the conventional method exhibits higher steady-state error and a wider standard deviation around its average value. More specifically, the clamping method exhibits 32 times smaller steady-state error compared to the resistive divider technique (22.7 mV compared to 727 mV) and an equally smaller standard deviation (57.3 mV as opposed to 818 mV). Note that these are average values over all three FCs.

Note that the settling time in Fig. 21(c)–(e) depends on the FC and R_{asym} values and is not representative of the measurement system response. Additionally, these error values are not expected to deviate significantly for a higher number of levels, since all measurements are taken from the same node, whereas the maximum voltage range is determined by the clamping circuit. We also do not expect any noticeable changes with the loading levels, as already shown in the simulations.

For the second experiment, we increased the dc bus voltage to 400 V and configured a single-phase inverter feeding a resistive load $R_{\mathrm{load}} = 600$ Ω. The asymmetric resistor was set to $R_{\mathrm{asym}} = 47$ kΩ. Contrary to the symmetrical three-phase inverter, a

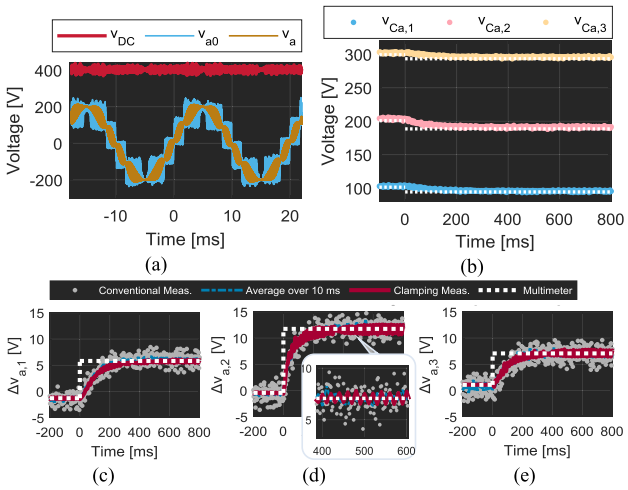

Fig. 22. (a) Input and output voltage waveforms for the five-level inverter when $v_{\mathrm{DC}} = 400$ V. (b) FC voltages measured with the conventional voltage divider and digital multimeter values under stepwise asymmetry introduced on $C_{a,2}$ at $t_0 = 0$. Comparison of the voltage variation of the FC (c) $\Delta v_{\mathrm{Ca},1}$, (d) $\Delta v_{\mathrm{Ca},2}$, and (e) $\Delta v_{\mathrm{Ca},3}$, between the traditional voltage devider sensor and the proposed clamping method.

single-phase topology introduces larger dc-link and FC voltage oscillations of double the fundamental frequency. Neither the oscilloscope waveforms [in Fig. 22(a)] nor the traditional voltage divider measurements [see Fig. 22(b)–(e)] can capture these oscillations, since their peak-to-peak range is smaller than the standard deviation of the recorded data. However, the clamping measurement system can precisely capture the voltage variation of every FC, as shown in Fig. 22(c)–(e), revealing the advantages of this method.

VI. Comparative Analysis

In this section, the performance of the developed clamping-based measurement system is compared against other FC voltage sensing methods found in the recent literature. More specifically, the techniques under investigation are grouped into two categories: 1) the *direct FC sensing* and 2) the *ac-side monitoring* systems, as shown in Table V. It is noted that only hardware-based solutions have been considered for this comparison; model-based approaches can be perceived as add-ons that can enhance any hardware solution. The criteria of the comparison are the measurement error, the frequency capability, the total component footprint, and cost, calculated for a three-phase five-level FC inverter application.

Unfortunately, most earlier works did not report the bandwidth of their ac measurement system. Therefore, we have included the switching frequency at which the inverter was operated, which gives us a rough estimation of the frequency range of their application. Let us also underline that the cost, footprint, and steady-state error for the voltage divider method are based on the experimental results of this work, since such data are not reported in [7] and [10].

The tabular data indicate that the proposed clamped-based solution exhibits the highest resolution at a low cost, similar to the approach presented in [39]. At the same time, it allows

TABLE V
Comparison of Different FC Voltage Sensing Methods

	Sensor Type and Reference	Error	Freq (kHz)	No of Sensors	Footprint (cm^2)	Price (USD)	Limitations
Direct FC sensing	LEM LV25-P [25] [26]	±0.8%	DC	15	76.8	837 - 1980	Cost & Footprint
	Voltage divider [7], [10]	±2.8%	DC	15	24.3	163.2	Accuracy, Cost & Footprint
AC side monitoring	[39]	±0.2%	[1]nr	3	[2]**3.7**	[2]**70.9**	Speed, Noise Sensitivity
	[40], [43]	<2.6%	0.6-2	3	nr	nr	Accuracy, Speed, Noise Sensitivity
	[44]	nr	0.5	3	nr	nr	Accuracy, Speed, Noise Sensitivity
	This work	**±0.01%**	**100**	**3**	13.8	75.6	Samples per Fund. Period

[1] nr = not reported.
[2] Estimation based on the schematics and experimental setup pictures.

for high switching frequency applications, i.e., more than 50 times the capabilities of other ac-side monitoring systems. It is therefore evident that the proposed measurement system is a competitive solution, combining the advantages of both worlds.

VII. Conclusion

In this article, we introduced a new ac-side monitoring system, based on a bidirectional voltage clamping circuit, for the precise extraction of the FC voltage levels in MLI. The proposed approach uses only a single sensor per phase, as opposed to dozens of sensors in the traditional FC monitoring methods, resulting in significantly lower cost, complexity, and circuit size, factors that do not scale with the number of levels. No isolation is required since all three-phase measurements have the same reference, which simplifies the topology even further. The new monitoring system exhibits high resolution (more than 30 times that of the resistive divider method), which helps overcome the noise sensitivity issue that is common in most ac-side voltage sensors. The clamping mechanism provides a larger measurement bandwidth (>200 kHz), allowing its application in high-frequency GaN-based inverters. The proposed measurement system was combined with a reliable active balancing control, to address disturbances and asymmetric loading. The theoretical analysis was supported by device-level and system-scale simulations and thorough experimental testing in a three-phase, five-level all-GaN inverter. Although the developed sensing system was designed and tailored for an FC inverter, the ac-side monitoring concept and the prototype clamping circuit can be adopted in other multilevel converter topologies.

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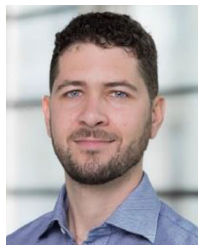

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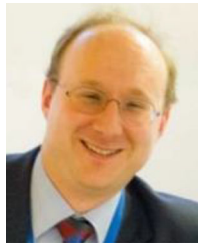

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