Accurate High-Frequency Modeling of the Input Admittance of PWM Grid-Connected VSCs

Ruzica Cvetanovic, *Student Member, IEEE*, Ivan Z. Petric, *Student Member, IEEE*, Paolo Mattavelli, *Fellow, IEEE*, and Simone Buso, *Member, IEEE*

***Abstract*—This article addresses high-frequency admittance modeling of current-controlled voltage source converters (VSCs). Recent studies have shown that harmonic instability may also occur at frequencies above the Nyquist frequency. To form an accurate multiple-frequency model in this frequency range, sidebands that originate from modulation and sampling must be examined. In this article, an accurate small-signal model is developed taking into account an adequate digital pulsewidth modulator (DPWM) representation, which allows to predict dependence of the frequency response on the steady-state dc (SS-dc) operating point. It is shown that when center-pulse sampling is implemented, pulsewidth modulation sidebands do not create additional loops leaving only sampling sidebands to be considered. Using the same approach as for SS-dc operation, a model that accurately represents admittance measurements during sinusoidal ac (S-ac) operation is developed. Its basis is a novel DPWM model suitable for S-ac regime, which allows to predict dependence of the VSC's input admittance on the grid voltage magnitude. Experimental and simulated admittance measurements, performed on a single-phase two-level VSC during various SS-dc and S-ac regimes, match with the proposed models up to twice the sampling frequency.**

***Index Terms*—Admittance measurements (AMs), multiple-frequency model, passivity, sideband harmonics, voltage source converters (VSCs).**

I. Introduction

CONSIDERABLE growth in the number of grid-connected voltage source converters (VSCs) in contemporary power systems has brought in harmonic instability issues [1]–[3]. Depending on the root cause of the harmonic instability, affected frequency range might be below and above fundamental frequency [1]. At higher frequencies, which are the focus of this article, destabilization of poorly damped grid resonances is a consequence of current control loop dynamics in the presence of delays, such as those caused by sampling, computation, and modulation [1], [4], [5]. Contributing to the phenomenon are also the sampling and pulsewidth modulation (PWM) sidebands [1], [4], [6]–[8].

Originating from the impedance-based stability approach [9], [10], passivity-oriented controller design for VSCs has recently drawn significant attention [8], [11]–[13]. Even though an upper frequency limit for passivity compliance is not clearly defined even by traction standards [14], it is usually considered to be the Nyquist frequency (NF) [11]. However, recent studies have shown that harmonic instability may also be caused by resonances above the NF [4], [6]–[8].

These observations have motivated extensive research in the field of high-frequency admittance modeling. Several approaches have been proposed, with the differences between them being the small-signal modeling of the digital pulsewidth modulator (DPWM), its generation of sidebands, and the modeling of aliasing due to the sampling process [4], [6], [7], [15]–[17]. In [4], a multiple-frequency model is developed which takes all sampling sidebands into account, but none of those originating from PWM. Certain discrepancies are observed between simulated admittance frequency response (FR) and the proposed model, due to incomplete DPWM representation. In [4], as well as in most of the works on this topic, DPWM is modeled as a zero-order hold (ZOH). However, it is well known that this is not a precise small-signal model [5]. In [18] and [19], a small-signal model of DPWM is derived using the describing function approach. The resulting model is dependent on the steady-state operating point (SSOP), unlike the ZOH. Contrary to [4], where only sampling sidebands are considered, the model presented in [15] and [20] considers only the lowest order PWM sideband. In [20], it is reported that, around the NF, this sideband causes the admittance to depend on the grid voltage magnitude, which model from [4] fails to predict. However, neither [15] nor [20] provide a clear comparison between the proposed model and admittance measurements (AMs). Using [4] as a basis, the authors in [6] and [7] sought to include sideband influence from both sampling and PWM. Again, the derived models rely on ZOH approximation, which limits their accuracy. As an alternative to the previously described continuous time-domain modeling, intersample modeling is proposed in [16], again considering the DPWM dynamics equal to ZOH.

To fill in the gaps of previous research, this article aims to provide a systematic approach for high-frequency admittance

Manuscript received 6 January 2022; revised 16 March 2022; accepted 19 April 2022. Date of publication 3 May 2022; date of current version 23 May 2022. This work was supported by the project MultiportGrid "Cross-Sectoral Energy Control through Interconnected Microgrids by Multiport Converter" funded within the call "ERA- Net Smart Energy Systems RegSys Joint Call 2018." Recommended for publication by Associate Editor F. D. Freijedo. *(Corresponding author: Ruzica Cvetanovic.)*

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Color versions of one or more figures in this article are available at https://doi.org/10.1109/TPEL.2022.3171611.

Digital Object Identifier 10.1109/TPEL.2022.3171611

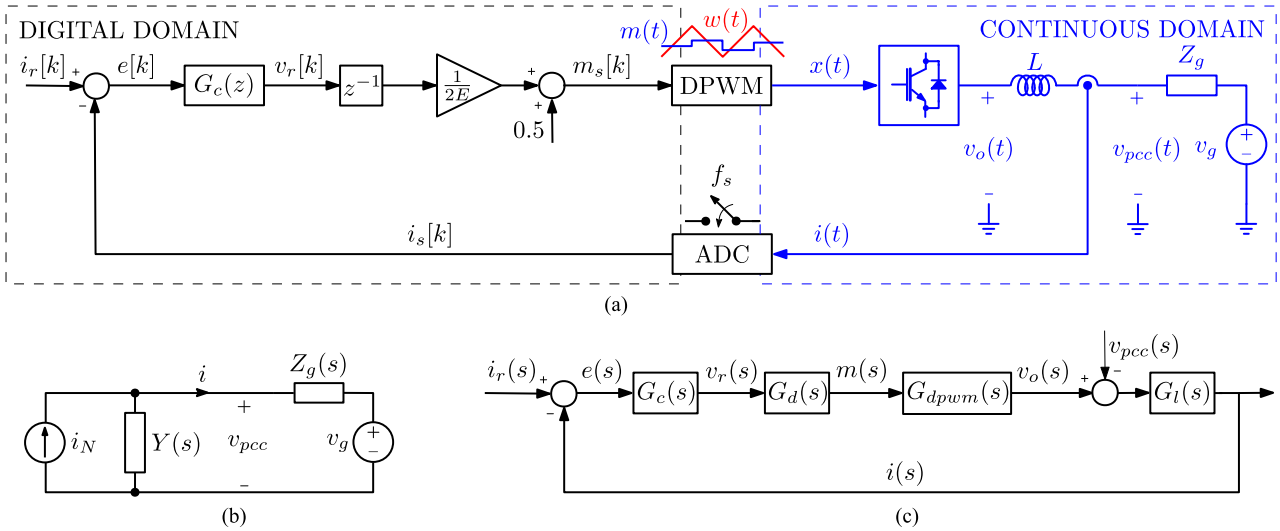

Fig. 1. Digitally controlled, pulsewidth modulated, single-phase, two-level grid-following VSC. (a) System block diagram. (b) Norton equivalent circuit used for impedance-based stability analysis. (c) Single-frequency small-signal representation of the current control loop.

modeling of digitally controlled VSCs. Main novelties and contributions of the manuscript are summarized as follows.

1) An impact of operating point (OP) on AMs is revealed. It is shown that AM obtained during sinusoidal ac (S-ac) regime lies in between AMs obtained for steady-state dc (SS-dc) regimes, within the same OP range.
2) It is mathematically derived and validated that additional loops induced by PWM sidebands are not created when sampling is aligned with the center of the voltage pulse (i.e., center-pulse sampling).
3) Relying on the previous two points, a new small-signal model for accurately predicting VSC's high-frequency properties is presented. Previously reported models and the proposed SS-dc model are compared against simulated AMs all the way up to twice the SF, to show the better accuracy of the proposed approach.
4) A novel, accurate, high-frequency model for predicting AMs during S-ac operation is presented. The model is capable of predicting dependence of the FR on the grid voltage magnitude. Benchmarking against state-of-the-art models is provided to highlight the obtained advantages.

Experimental AMs, performed on single-phase, two-level, VSC with an inductive filter during different SS-dc and S-ac regimes, match with the proposed models up to twice the NF.

This article is organized as follows. Influence of OP on AMs is revealed in Section II. An accurate small-signal model for current-controlled VSC is derived in Section III and compared to the existing models. The model that predicts AM during S-ac operation is presented in Section IV and benchmarked against state-of-the-art models. Experimental AMs, performed during different SS-dc and S-ac regimes of the VSC, are provided in Section V. Finally, conclusions and summary of the manuscript are given in Section VI.

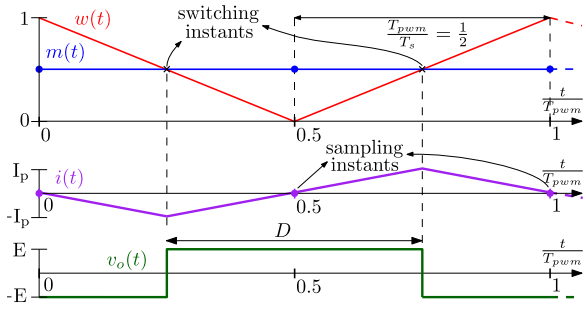

Fig. 2. Synchronization between current sampling instant and switching carrier w to obtain average value of the current i. Sampling is performed at peaks and valleys of w, ideally corresponding to the center of the applied voltage pulse.

II. Influence of Operating Point on Admittance Measurements

A. System Description

Throughout this article, a digitally controlled, pulsewidth modulated, single-phase, two-level, grid-following VSC with an inductive filter is considered. Nevertheless, the presented approach is directly applicable to the analysis of three-phase four-wire grid-connected VSCs in stationary reference frame, as well as to any output filter.

A block diagram of the system considered is shown in Fig. 1(a). The system is current-controlled, with the control period T_s being half the switching period T_{pwm}, i.e., double-update rate is used [5]. Nonetheless, as discussed in Appendix B, the analysis presented throughout the manuscript is applicable to single-update systems as well. Transition from continuous to digital domain is performed by an analog-to-digital converter (ADC). The current sampling instant is synchronized with the carrier w so that center-pulse (synchronous) sampling [5] is obtained, as illustrated in Fig. 2. This removes the switching ripple

from the current i and results in its average value. The sampled current i_s is subtracted from the reference i_r, resulting in the error signal e that is used as an input to the current controller G_c. Due to finite algorithm execution time, the controller output update is delayed by one sampling period [5]. Voltage reference generated by the current controller is scaled to the range [0,1] to obtain the digital modulating signal m_s. The DPWM serves as an interface between digital and continuous domains. Its inherent ZOH function transforms m_s to m and compares it with the carrier w. The DPWM output, i.e., switching waveform x, is used to control the power transistors within the VSC. The output voltage of the VSC, v_o, is applied to the output filter G_l

$$G_l(s) = \frac{i(s)}{v_o(s)} = \frac{1}{sL} \tag{1}$$

where L is the filter inductance and s is the complex variable of the Laplace transform.

B. Admittance Passivity Criterion

The impedance-based approach has proven to be adequate for small-signal stability assessment of systems containing numerous power electronic devices [10]. For current-controlled systems, this method assumes representing the converter by its Norton equivalent circuit, which consists of a current source i_N paralleled with an admittance Y, as shown in Fig. 1(b) [9]. The elements of the Norton equivalent circuit can be found from a small-signal representation of the system, such as in Fig. 1(c), where G_d and G_{dpwm} model the computational delay and the digital modulation, respectively. The current source and admittance are defined by

$$i_N(s) = W_{cl}(s) i_r(s) \tag{2}$$

where $W_{cl}(s) = \frac{i(s)}{i_r(s)}\big|_{v_{\text{pcc}}=0}$, and

$$Y(s) = -\frac{i(s)}{v_{\text{pcc}}(s)}\bigg|_{i_r(s)=0}. \tag{3}$$

Relying on the impedance stability approach [9], admittance passivity criterion implies that, if the grid impedance Z_g is passive, a sufficient condition for system stability is that converter's admittance Y is also passive [12]. Note that a linear single-input single-output system is considered to be passive if the real part of its FR is nonnegative for all frequencies, i.e., if its phase is within the range $[-\frac{\pi}{2}, \frac{\pi}{2}]$ [11]. Since, due to delays, passivity of the converter's admittance cannot be achieved for all frequencies, the requirement for passivity is relaxed in practice [4], [21], [22]. Namely, the goal is to shape converter's input admittance such that its real part is nonnegative in a range as wide as possible, to achieve robustness against grid-resonances that may appear [4], [6], [21], [22].

C. Admittance Measurements for Passivity Compliance

Admittance passivity criterion has inspired related grid-connection requirements to be imposed in recent traction standards [14]. In this article, AM procedure is chosen to be compliant with EN 5038802 standard, which is imposed in railway systems of several European countries [4], [6]–[8], [11], [12], [14], [17].

TABLE I
VSC AND CONTROL LOOP PARAMETERS

VSC	label	value	unit
Nominal power	P_n	3	kW
Nominal DC link voltage	E	400	V
Nominal PCC voltage	V_g^{rms}	230	V
Filter inductance	L	2.5	mH
Fundamental frequency	f_1	50	Hz
Switching frequency	f_{pwm}	20	kHz
Dead-time	$\frac{t_{dt}}{T_{pwm}}$	1	%
Control loop	**label**	**value**	**unit**
Sampling frequency	f_s	40	kHz
Crossover frequency	f_c	4	kHz

The EN 50388-2 requires the VSC admittance to be measured while being connected to an ac source, i.e., while generating fundamental frequency voltages at its output. Waveforms of interest are to be acquired for a time interval equal to 8 or more multiples of the fundamental periods. This approach may bring to misleading conclusions, due to nonlinear nature of certain elements in the current control loop. The main nonlinearity comes from DPWM itself because its small-signal input–output relation depends on the duty cycle, i.e., on SSOP [18]. The result of this is that in SS-dc regime, FR of the system depends on the SSOP for which AM is performed. As a consequence, when the system is operating in an ac regime, where the fundamental frequency is considerably smaller than the switching frequency, influence of all OPs spanned during each fundamental period is present. In the following subsection, the impact of the OP on AMs is showcased providing simulation results. The necessity of a clear definition of the OP for which the VSC admittance should be measured is emphasized.

D. Comparison Between AMs During SS-DC and S-AC Regime

For the following validations, simulations were performed in MATLAB Simulink environment, with a full-bridge VSC, operated using the bipolar modulation and described in Table I. AMs during different SS-dc regimes, i.e., for different duty cycles D, as well as during different S-ac regimes are performed. Each S-ac regime is defined by the peak–peak value of the duty cycle's fundamental frequency variation u_{pp}. AMs are performed by applying sinusoidal voltage perturbation at the point of common coupling (PCC) and measuring the current response. For AMs during SS-dc operation, a dc source is connected in series with the perturbation source. Magnitude V_g of the dc source is set depending on the desired OP, i.e., as $V_g = (2D-1)E$. For AMs during S-ac operation, a sinusoidal ac source with $f_1 = 50$ Hz is connected in series with the perturbation source. Magnitude V_g of the ac source is set depending on the desired u_{pp}, as $V_g = u_{\text{pp}}E$.

Perturbation generation as well as postprocessing of i and v_{pcc} to obtain the admittance FR is performed using FR estimation block in Simulink. Sinestream experiment mode is used with the perturbation frequencies from the range [6, 80] kHz, whereas perturbation around multiples of switching frequency is avoided. Note that perturbation frequencies are chosen to be multiples of 25 Hz but not of 50 Hz, to minimize the impact of nonlinear effects related to fundamental frequency operation [6]. A fixed voltage perturbation magnitude of 50 V is used to obtain the magnitude of the perturbation current flowing through the VSC in the range of 100 mA [4], [6]. Fixed settling and estimation periods equal to 20 and 40 ms, respectively, are used. The estimation time was set lower than eight times the fundamental period, due to data length and simulation time. Note that this does not compromise the measurement precision, as the window length is equal to an integer multiple of each perturbation frequency. A sufficient dc bias current reference is also imposed to avoid zero crossings that are reported to cause nonlinear effects related to dead-times [23]. Note that dc component of the inductor current has no influence on AMs in the frequency range of interest.

As an application example, proportional resonant (PR) controller is used in this article [24]. Its s domain transfer function is

$$G_c(s) = \frac{v_r(s)}{e(s)} = k_p + k_r \frac{s}{s^2 + \omega_1^2} \tag{4}$$

where k_p and k_r are proportional and resonant gains, respectively, and ω_1 is the fundamental angular frequency. The proportional gain is set as $k_p = \omega_c L$, where ω_c is the desired angular crossover frequency of the current loop [5]. The resonant gain k_r is designed so that its influence on crossover frequency is negligible [5], e.g., $k_r = \frac{1}{10} k_p$. The desired crossover frequency f_c is set depending on the required stability margin. In typical double-update applications, due to delays, the crossover frequency is usually limited to 10% of the SF [11].

In order to illustrate that during S-ac operation, all OPs, throughout which the system goes, have an impact on AM, results for an S-ac and many SS-dc regimes, covering the same range of D, are shown in Fig. 3. Note that, in this as well as in all other figures presented in this article, dots represent simulated AM points. AM during S-ac operation is obtained for $u_{\text{pp}} = 0.8$, which corresponds to the nominal PCC voltage from Table I. AMs for SS-dc regimes are performed for duty cycles calculated as the arithmetic sequence starting from $0.5 - u_{\text{pp}}/2 = 0.1$ and ending at $0.5 + u_{\text{pp}}/2 = 0.9$. Note that only results for the duty cycles between 0.5 and 0.9 are shown in Fig. 3, due to symmetry of the small-signal DPWM model around $D = 0.5$, as seen from (6). According to the presented results, AM during S-ac operation is somewhere in between AMs for SS-dc regimes, covering the same duty cycle variation range. This finding is of paramount importance since it underlines the necessity for a clear definition of the measurement conditions used for passivity compliance. Therefore, it might serve as a starting point for modifying existing or creating new standards related to passivity of the grid-connected VSCs.

To analytically predict AM during S-ac operation, an accurate small-signal model for SS-dc regimes is considered to be a prerequisite. Development of such a model is addressed in the following section.

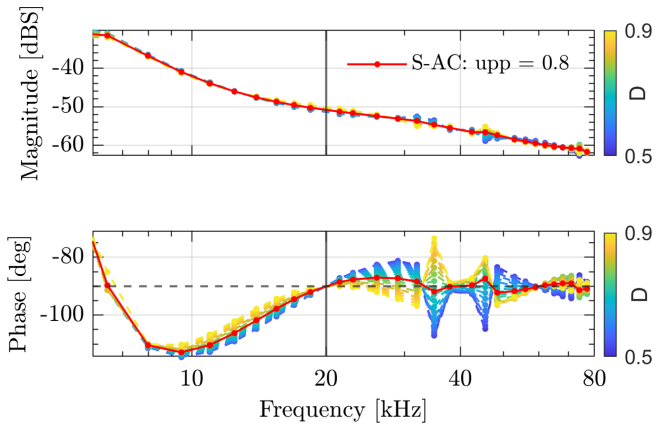

Fig. 3. Comparison between AM during S-ac regime with $u_{\text{pp}} = 0.8$ (red plot) and multiple AMs during SS-dc regimes for the same duty cycle variation range (gradient from blue to yellow). The gray vertical line marks the NF.

III. Small-Signal Modeling of VSCs

In this section, an accurate small-signal model of the system from Fig. 1(a) is derived. Modeling is performed in s domain [5], as effects above the NF are the main focus of the article.

A. DPWM Model

Compared to the analog implementation, uniformly sampled PWM introduces delay [5]. The phase lag due to modulation is shown to be equal to that of a pure time delay of $T_s/2$ [5]. Therefore, DPWM is often modeled as a pure delay [12]. For the purposes of predicting the system behavior at frequencies considerably below the NF, this model is sufficient [12]. However, to analyze the behavior near and above the NF, a more accurate small-signal model is required, which accounts for magnitude attenuation at higher frequencies [4]. Motivated by the fact that sample and hold function is an inherent part of the DPWM process, the ZOH model is often considered to be an adequate DPWM model for higher frequencies [4], [6]. Nevertheless, as shown in [18], neither pure delay nor ZOH are accurate small-signal models of DPWM. In this article, the small-signal model of the asymmetrical uniformly sampled PWM, obtained using the describing function approach [5], [18], is used

$$G_{\text{dpwm}}(s) = \frac{d(s)}{m(s)} = \frac{1}{2}\left(e^{-sDT_s} + e^{-s(1-D)T_s}\right) \tag{5}$$

where d is the continuous-time duty cycle of $x(t)$, used in averaged modeling [5]. Expression (5) can be represented in the frequency domain as

$$G_{\text{dpwm}}(j\omega) = \cos\left(\omega T_s\left(D - \frac{1}{2}\right)\right) e^{-j\omega\frac{T_s}{2}} \tag{6}$$

where ω is the angular frequency and j is the imaginary unit. Contrary to ZOH and delay models, the small-signal DPWM

model in (5) shows dependency on the SSOP, i.e., on the steady-state value of the duty cycle D.

B. Single-Frequency Admittance Model

At first, a single-frequency small-signal model of the system from Fig. 1(a) is derived, which neglects the influence of sideband harmonics. A small-signal continuous time-domain representation of the current control loop is given in Fig. 1(c). One step computation delay is modeled by

$$G_d(s) = e^{-sT_s}. \tag{7}$$

Using the small-signal DPWM model from (5) and load representation given in (1), the loop gain of the system from Fig. 1(c) is defined by

$$T(s) = \frac{i(s)}{e(s)} = G_c(s)G_d(s)G_{\text{dpwm}}(s)G_l(s). \tag{8}$$

Based on (3), single-frequency model of the input admittance of the VSC is then given by

$$Y(s) = \frac{G_l(s)}{1 + T(s)}. \tag{9}$$

C. Sidebands in Digitally Controlled PWM Systems

Two types of sidebands exist in a digitally controlled pulsewidth modulated system [1], [7], [25]. Sidebands of the first type, which are throughout our manuscript referred to as PWM sidebands, originate from the modulation process. They appear due to the fact that in addition to the desired frequency component f_p, DPWM creates components symmetrically around switching frequency multiples, i.e., at frequencies $mf_{\text{pwm}} \pm nf_p$, where m and n are integers [26]. These PWM sidebands are usually analyzed using double Fourier analysis [15], [27], [28]. In addition to PWM sidebands, a second type of sidebands, which originates from sampling process, exists. Throughout our manuscript, these are referred to as sampling sidebands. They are created due to the fact that the sampling process generates an infinite number of aliases [4], [29]. Sampling sidebands are created around each multiple of the sampling frequency, i.e., at $kf_s \pm f_p$, where f_p is the frequency of the original signal [4].

Coupling between perturbation component, PWM, and sampling sidebands creates additional loops in the control system, which have a nonnegligible impact on the system performance around and above the NF [4], [7], [15], [25], [27]. Thus, the influence of these sidebands has to be taken into account in order to accurately model system behavior at high frequencies. Modeling is especially complex in case of the double-update rate since, due to the switching and sampling frequencies being different, PWM and sampling sidebands are not created around the same frequency. For illustration, consider only the first, lower, sidebands generated by PWM and sampling. In case of the single-update, since $f_s = f_{\text{pwm}}$, these sidebands appear at the same frequency $f_s - f_p$. Therefore, only one additional loop exists. In case of the double-update, the sampling and PWM sidebands appear at different frequencies: $f_s - f_p$ and $f_{\text{pwm}} - f_p = 2f_s - f_p$. Therefore, two additional loops exist. Not only are these loops coupled with the perturbation loop, but they are also mutually coupled. Complexity increases as more sidebands are considered. Note that, to the best of the authors' knowledge, modeling which accounts for all of the aforementioned effects has not been presented so far.

Nevertheless, as elaborated by the detailed analytical derivation and validation provided in Appendix A, when the center-pulse sampling is employed, PWM sidebands that create additional loops are canceled out and, therefore, not introduced in feedback. This significantly simplifies the accurate high-frequency modeling since only sampling sidebands need to be considered. Benefits of PWM sideband cancelation, achieved in any center-pulse sampled system, are especially visible in the double-update implementation. Nonetheless, the cancelation effect contributes to a considerable simplification of the modeling procedure in the single-update case, as well. This article will focus on the double-update case, while derivations for single-update are placed in Appendix B.

D. Multiple-Frequency Admittance Model

In this article, to derive a multiple-frequency small-signal model of the system from Fig. 1, the approach from [4] is used to include the influence of sampling sidebands only. According to the derivation provided in Appendix A, if the sampling instants are properly synchronized with the carrier, these sidebands are the only ones that create additional loops in the closed loop operation of the digitally controlled VSC. Thus, as it will be validated through simulations and experiments, the multiple-frequency model derived below accurately predicts the small-signal properties of the system from Fig. 1(a) even above the NF. Considering the aliases generated by the sampling process, sampled current i_s is given by [4], [29]

$$i_s(t) = i(t)\sum_{k=1}^{\infty}(1 + 2\cos(jk\omega_s t))^1 \tag{10}$$

where $\omega_s = 2\pi f_s$. Applying Laplace transform to (10) gives

$$I_s(s) = \sum_{k=-\infty}^{\infty} I(s - jk\omega_s). \tag{11}$$

Using (11) as a basis and following the procedure from [4], the multiple-frequency input admittance of the converter is derived as

$$Y_m(s) = \frac{G_l(s)}{1 + \frac{T(s)}{1+T_s(s)-T(s)}} \tag{12}$$

where $T_s(s)$ is

$$T_s(s) = \sum_{k=-\infty}^{\infty} T(s - jk\omega_s). \tag{13}$$

[1]If signal $i(t)$ contains spectral component above the NF, magnitude of the corresponding component in i_s depends on the relation between sampling instant and initial phase of the considered component. This is not analyzed in [4] and not included in this model of the sampling process. The impact of this sampling instant dependency is shown to be negligible, by repeating simulations and experiments with various initial phases of the perturbation component.

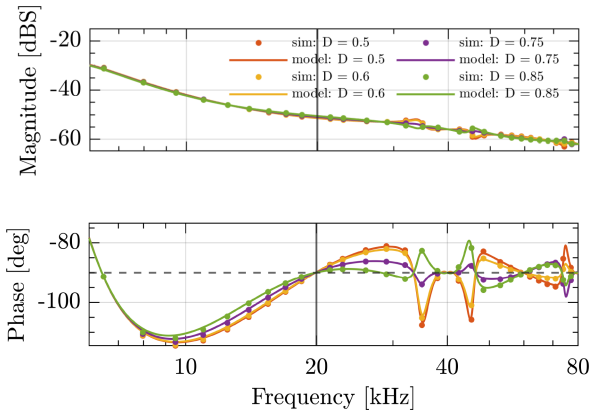

Fig. 4. Comparison between simulated AMs during different SS-dc regimes and the proposed small-signal model given by (12). The gray vertical line marks the NF.

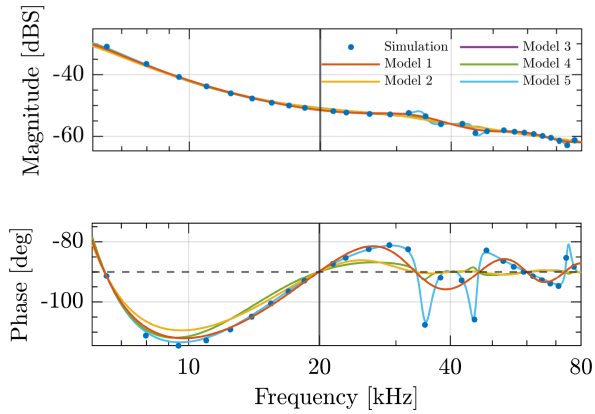

Fig. 5. Comparison between different models and simulated AMs at $D = 0.5$. Results for Model 1 completely overlap with those of Model 3.

TABLE II
DIFFERENT SMALL-SIGNAL MODELS USED FOR BENCHMARKING

Model	DPWM: $G_{dpwm}(j\omega)$ gain	DPWM: $G_{dpwm}(j\omega)$ phase	Sampling: $I_s(j\omega)$
1	1	$e^{-j\omega\frac{T_s}{2}}$	$I(j\omega)$
2	$\frac{2}{\omega T_s}\sin\left(\frac{\omega T_s}{2}\right)$		
3	$\cos\left(\omega T_s\left(D-\frac{1}{2}\right)\right)$		
4	$\frac{2}{\omega T_s}\sin\left(\frac{\omega T_s}{2}\right)$		$\sum_{k=-\infty}^{\infty} I\left(j\left(\omega - k\omega_s\right)\right)$
5	$\cos\left(\omega T_s\left(D-\frac{1}{2}\right)\right)$		

E. Model Performance and Comparison With Existing Models

To illustrate the performance of the proposed multiple-frequency small-signal model, in Fig. 4, AMs simulated during different SS-dc regimes are compared with the FR obtained analytically using (12). The infinite sum from (12) is replaced by a finite sum of 1000 elements since the contribution of higher order elements is shown to be negligible. Simulations were performed in the same way and with the same parameters described in Section II. According to the presented results, the proposed methodology accurately models VSC's input admittance even in the very high-frequency range and is able to predict dependence of the small-signal properties on the SSOP.

In order to illustrate the benefits of the proposed model, it is compared to different models reported in the literature. The models differ from each other in the way PWM and sampling process are modeled, as listed in Table II. Models 1–3 are single-frequency models that represent PWM as a delay, ZOH, and (5), respectively. Model 4 is the multiple-frequency model from [4], whereas Model 5 is the small-signal multiple-frequency model, proposed in this article and given by (12). Note that in the following comparison, system parameters remain the same for all tested models, i.e., equal to those in Table I.

Fig. 5 illustrates the comparison between the analytical models from Table II and simulation results obtained at $D = 0.5$.

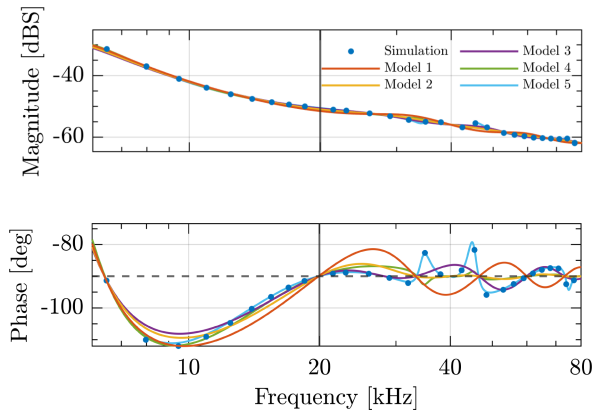

Fig. 6. Comparison between different models and simulated AMs at $D = 0.85$. The gray vertical line marks the NF.

First, it can be seen that different modeling approaches differ more in the admittance phase than in its magnitude. Second, for $D = 0.5$, Models 1 and 3 are identical. Next, for the VSC and control loop parameters considered in this article, Models 2 and 4 show very similar results. Another important observation is that Model 3 matches with simulation results up to a certain frequency, in this case $0.8f_s$. Finally, only Model 5 is able to accurately predict admittance FR in the very high-frequency range (around and above SF). Note that, up to very high frequencies, single-frequency Model 3 negligibly deviates from multiple-frequency Model 5. Fig. 6 illustrates a comparison between the analytical models from Table II and simulation results obtained at $D = 0.85$. Since Models 1, 2, and 4 are unable to predict dependence of the small-signal properties on the OP, they give the same results regardless of the duty cycle. As in the previous case of $D = 0.5$, Model 3 matches with simulation results up to $0.8f_s$, but only Model 5 accurately predicts admittance FR in the full frequency range.

Note that all of the previously presented simulation results were obtained (as specified in Table I), with 1% dead-time, which did not compromise the proposed modeling validation.

TABLE III
DEVIATIONS BETWEEN SIMULATION RESULTS WITH NONIDEAL CENTER-PULSE SAMPLING AND THE PROPOSED SMALL-SIGNAL MODEL (12)

max error [%] @ freq. [kHz]	t_{dt}/T_{pwm}		$L/(RT_{pwm})$	
	0.03	0.1	10	2
magnitude	0.9 @ 6	1.9 @ 11	0.6 @ 6	2.3 @ 33
angle	0.5 @ 22	2.2 @ 51	0.5 @ 41	2.3 @ 29

Dead-time is one of the causes for nonideal center-pulse sampling. In addition, due to nonzero filter resistance, the presence of analog low-pass filters, etc. [30], [31], ideal center-pulse sampling is difficult to achieve in practice. Thus, a question arises if the reasoning for PWM sideband elimination provided in Appendix A is justified in practical applications. To address this issue, multiple simulations for obtaining admittance FR were performed with intentionally increased nonidealities. Two different sets of simulations were performed, each implementing either increased values of dead-time or of filter resistance R. Simulation parameters other than these were the same as previously explained. SS-dc operation with $D = 0.5$ is considered. Deviations between simulation results and the proposed model (12) are expressed relative to the values predicted by the model. Table III shows only the maximum values of deviations and frequencies at which they are obtained. According to the presented results, even with unrealistically high levels of nonidealities, mismatch between the proposed model and simulation results is very low. Thus, PWM sideband influence proves to be negligible even in practical applications where center-pulse sampling is not ideal.

IV. MODEL FOR PREDICTING AM DURING S-AC REGIME

As illustrated in the previous section, the small-signal DPWM model depends on the SSOP. For grid-tied ac operation, OP is changing slowly with respect to the control period. Indeed, during S-ac regime, the OP is exhibiting a sinusoidal change at the fundamental frequency. In practical grid-connected applications, purely S-ac operation may not be present due to significant grid distortion; however, the following approach, derived for S-ac operation, may be extended for any waveform of the grid voltage.

According to the results presented in Section II, FR obtained during S-ac operation is a weighted average of AMs obtained during SS-dc regimes in the same OP range. Therefore, a question arises about which representation of the DPWM model would be accurate for predicting the admittance FR during S-ac operation. As per EN 50388-2 standard, AM should be performed with an estimation data window length which is a multiple of the fundamental period. In order to address this, we present the approach to obtain an adequate DPWM representation compliant with EN 50388-2. The small-signal model from (5) is averaged on the fundamental period

$$G_{\text{dpwm}}^{\text{s-ac}}(j\omega) = \frac{1}{u_{\text{pp}}} \int_{u_1}^{u_2} \cos\left(\omega T_s \left(u - \frac{1}{2}\right)\right) e^{-j\omega \frac{T_s}{2}} du \tag{14}$$

where u is the duty cycle that is assumed to change in a sinusoidal manner with respect to $\theta = 2\pi f_1 t$

$$u = \frac{u_{\text{pp}}}{2} \sin\theta + \frac{1}{2}. \tag{15}$$

Since $\theta \in [-\pi, \pi]$, limits of the integral in (14) are $u_1 = \frac{1}{2} - u_{\text{pp}}$ and $u_2 = \frac{1}{2} + u_{\text{pp}}$. Substitution of (15) in (14) results in

$$G_{\text{dpwm}}^{\text{s-ac}}(j\omega) = \frac{1}{\pi} \int_{-\frac{\pi}{2}}^{\frac{\pi}{2}} \cos\left(\omega T_s \frac{u_{\text{pp}}}{2} \sin\theta\right) e^{-j\omega \frac{T_s}{2}} d\theta \tag{16}$$

which, when solved, yields

$$G_{\text{dpwm}}^{\text{s-ac}}(j\omega) = J_0\left(\omega T_s \frac{u_{\text{pp}}}{2}\right) e^{-j\omega \frac{T_s}{2}} \tag{17}$$

where J_0 is the zero-order Bessel function of the first kind. As it will be verified in simulations and experiments, the derived model is a suitable representation of the DPWM which operates in an ac regime, with the modulating signal exhibiting sinusoidal change at the fundamental frequency, which is considerably lower than the SF. Due to OP dependency, the derived model cannot be considered a small-signal one. Nevertheless, (17) accurately represents response of the DPWM to a small perturbation during S-ac operation, in case variables used for obtaining FR of the modulator are acquired with a data length that is equal to an integer multiple of the fundamental period.

The single- and multiple-frequency models to predict AM during S-ac operation are similar to the ones from (9) and (12), respectively, the only difference being that the DPWM model from (6) is replaced with (17). Therefore, the modified single-frequency model suitable for S-ac operation is given by

$$Y^{\text{s-ac}}(s) = \frac{G_l(s)}{1 + T^{\text{s-ac}}(s)} \tag{18}$$

where $T^{\text{s-ac}}(s) = G_c(s)G_d(s)G_{\text{dpwm}}^{\text{s-ac}}(s)G_l(s)$. The resulting multiple-frequency model is finally obtained as

$$Y_m^{\text{s-ac}}(s) = \frac{G_l(s)}{1 + \frac{T^{\text{s-ac}}(s)}{1 + T_s^{\text{s-ac}}(s) - T^{\text{s-ac}}(s)}} \tag{19}$$

where $T_s^{\text{s-ac}}(s) = \sum_{k=-\infty}^{\infty} T^{\text{s-ac}}(s - jk\omega_s)$.

Since, in order to handle OP dependency, an averaged DPWM model is used in (19), applicability of the proposed S-ac admittance model for system stability assessment has to be further examined. Namely, when the system is operating in S-ac regime, its OP is exhibiting sinusoidal change. The lack of a fixed OP prevents direct application of conventional small-signal linearization techniques that are commonly used in SS-dc operation [1], [32]. To address stability of the VSC during S-ac operation, the tools developed for stability assessment of nonlinear time periodic systems must be used [32]. Yet, as it will be shown, the proposed model accurately predicts AMs, compliant with the EN 50388-2 standard, and, therefore, can be considered a valuable tool when designing control loops to satisfy the prescribed passivity criteria.

A. Model Performance and Comparison With Existing Models

To illustrate performance of the proposed S-ac multiple-frequency model (19), admittance FR obtained from simulations

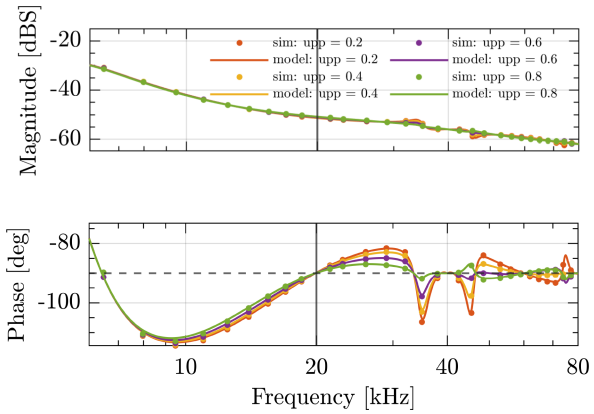

Fig. 7. Comparison between simulated AMs during different S-ac regimes and the proposed model for predicting AM during S-ac operation given by (19). The gray vertical line marks the NF.

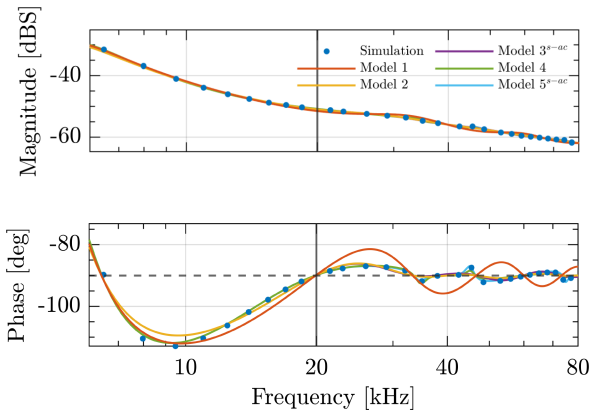

Fig. 8. Comparison between different models and simulated AMs during S-ac operation with $u_{\text{pp}} = 0.8$. The gray vertical line marks the NF.

is compared to the proposed analytical model (19) in Fig. 7. Results are given for different S-ac regimes, defined by peak–peak duty cycle variation u_{pp}. Simulations were performed in the same way and with the same parameters described in Section II. According to the presented results, the proposed methodology accurately models VSC's input admittance even in the very high-frequency range and is able to predict dependence of the system properties on the fundamental frequency peak–peak duty cycle variation.

In order to illustrate the benefits of the proposed model, it is compared to different models reported in the literature. The same models from Table II are used to denote Models 1, 2, and 4, whereas models denoted as Models $3^{\text{s-ac}}$ and $5^{\text{s-ac}}$ are the models defined by (18) and (19). Note that, in [4] and [11], Models 1, 2, and 4 are used for admittance modeling during S-ac operation and, therefore, are considered for benchmarking in this article.

Fig. 8 illustrates the comparison between the analytical models and simulation results obtained at $u_{\text{pp}} = 0.8$. Note that peak–peak duty cycle variation of 0.8 corresponds to the nominal PCC voltage (see Table I). As can be seen, Model 1 fails to predict system performance at high frequencies. All other models give almost the same FR results and predict well the system

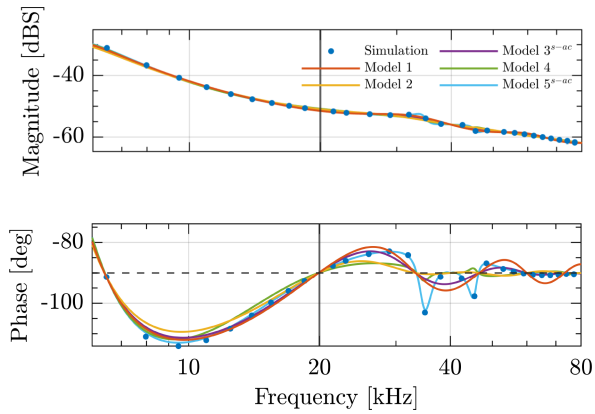

Fig. 9. Comparison between different models and simulated AMs during S-ac operation with $u_{\text{pp}} = 0.4$. The gray vertical line marks the NF.

dynamics. Still, the proposed model gives the best match with simulation results. Note that, since, for $u_{\text{pp}} = 1$, the proposed DPWM model (17) reduces to ZOH model, Models 2 and 4, which use ZOH model to represent DPWM, are expected to give valid AM predictions only for high u_{pp} values. Due to u_{pp} being defined as the ratio between grid voltage magnitude and dc link voltage, lower values of u_{pp} might be present in some applications. In Fig. 9, the analytical models are compared to simulation results obtained with $u_{\text{pp}} = 0.4$. Models 1, 2, and 4 now result in a significant error, whereas Model $3^{\text{s-ac}}$ gives valid predictions until approximately $0.8 f_s$. Again, only Model $5^{\text{s-ac}}$ is able to accurately predict AM during S-ac operation in the entire considered frequency range.

V. Experimental Verification

With the goal of validating the proposed analytical models, experimental AMs during different SS-dc and S-ac regimes are provided in this section. Experimental AMs are performed using the same system configuration, parameters, and core principles of the AMs as for simulations, described in Section II. Note also that experimental AMs are performed with the reduced dc link voltage $E = 250$ V to achieve higher resolution for data acquisition. According to (12) and (19), this has no effect on AM, as it will be validated by the subsequent results.

The setup used for experimental AMs is shown in Fig. 10 and its block diagram is given in Fig. 11. Hardware and control parameters of the system used for experimental AMs are provided in Table I. The setup consists of three main parts denoted by three different colors in Fig. 11. Red part consists of the tested VSC and the perturbation circuit. An industrial full-bridge single-phase VSC operated via bipolar modulation is used. Regenerative power system Keysight RP7962 A is used as VSC's input dc voltage.

The control system, denoted by blue color in Fig. 11, is implemented on an NI sbRIO-9606, which is based on a Xilinx Zynq 7020 all programmable system on chip. The inductor current is sensed by a custom interfacing board, based on a shunt resistor. The board uses conditioning circuits, a 12-b ADC module AD9226 by analog devices, and digital isolators. The DPWM

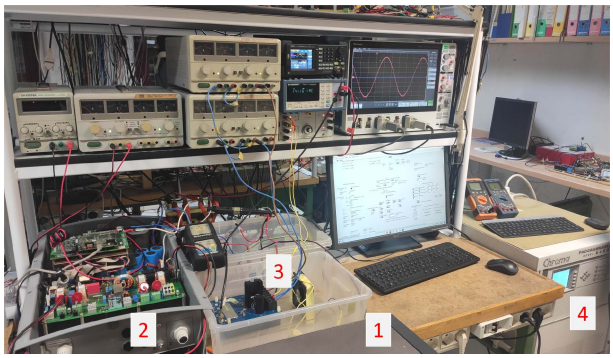

Fig. 10. Experimental setup. (1) Input power supply. (2) VSC and control board. (3) Perturbation circuit. (4) Programmable ac source.

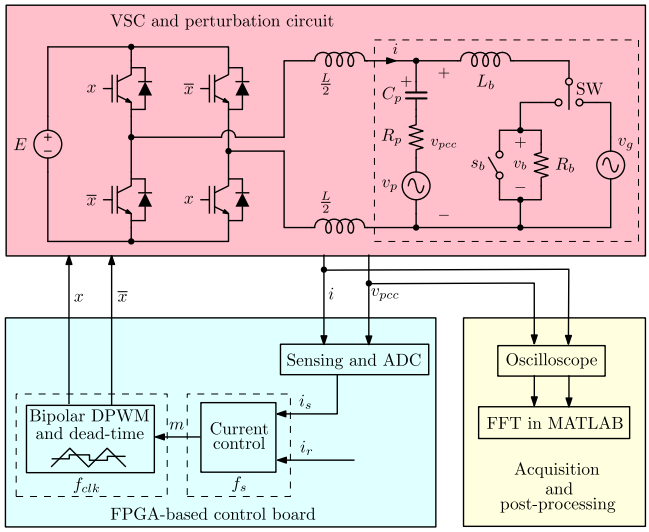

Fig. 11. Block diagram of the experimental setup used for AMs.

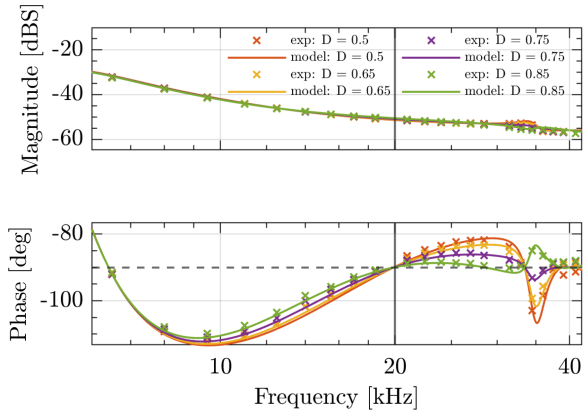

Fig. 12. Comparison between experimental AMs during different SS-dc regimes and the proposed small-signal model given in (12). The gray vertical line marks the NF.

clock runs at 160 MHz. For the purposes of digital implementation of (4), used in the following experiments, PR current controller is discretized using impulse invariant method [24].

Perturbation circuit contains the perturbation branch and bias branch. The perturbation source v_p is implemented using a power operational amplifier MP118, from APEX. The perturbation source is connected in series with a capacitor $C_p = 10$ μF and a resistor $R_p = 1\,\Omega$ that is used to smooth any transients. The capacitor is used to block dc currents as well as to decouple the bias branch from the VSC, so that switching ripple harmonics of i remain the same as if VSC was connected to an ideal grid.

Based on the position of switch SW, two different configurations of the bias branch can be set. When SW is in position 1, circuit configuration used for SS-dc AMs is obtained. When SW is in position 2, circuit configuration used for S-ac AMs is obtained. In both configurations, the bias branch features an inductance $L_b = 2.4$ mH, which suppresses perturbation currents. The bias branch has two functions. First of all, it allows the circulation of any dc current. All AMs are performed for an imposed dc current reference as explained in detail in Section II. Second, bias branch provides the desired PCC voltage, so that AMs can be performed for different SS-dc and S-ac regimes. For the SS-dc AMs, bias branch features a resistor R_b that can be bypassed with a switch s_b. When the switch s_b is opened, the dc component of i provides a voltage drop across R_b. This results in a dc voltage component of v_{pcc}, referred to as the bias voltage v_b. By imposing the adequate bias voltage, it is possible to obtain AMs around specific OPs. These bias values determine the SSOP as $D = 0.5(\frac{v_b}{E} + 1)$, if series voltage drops are neglected. For the S-ac AMs, in series with L_b, bias branch features an adjustable ac source, which is configured to provide a 50-Hz sinusoidal voltage v_g. This results in a sinusoidal ac voltage component of v_{pcc} at the fundamental frequency. By imposing adequate magnitude V_g of the sinusoidal source, it is possible to obtain AMs during different S-ac regimes. Value of V_g determines the S-ac operating regime as $u_{\text{pp}} = \frac{V_g}{E}$. Chroma 6460 programmable ac power supply is used to provide fundamental frequency component.

Perturbation is injected at 22 different frequencies, one at the time, starting from 6 kHz and up to 41 kHz, thereby avoiding multiples of switching frequency. In order to ensure precise measurements in the presence of switching ripple and noise, magnitude of the injected sinusoidal perturbation is calculated for each perturbation frequency to obtain at least 100-mA magnitude of the perturbation current flowing through the VSC. Perturbations above 41 kHz resulted in the required perturbation voltage being above 60 V, which was the upper limit of the amplifier. Therefore, experimental AMs are given up to 41 kHz, which is just above the SF.

Acquisition and postprocessing is denoted by yellow color in Fig. 11. The inductor current i and the PCC voltage v_{pcc} are measured via Tektronix 5 series oscilloscope with the data length of 40 ms. Fast Fourier transform of i and v_{pcc} is performed in MATLAB to obtain spectral components of i and v_{pcc} at perturbation frequency. These components are then used to calculate the admittance at the perturbation frequency.

AMs during different SS-dc regimes are shown in Fig. 12, where they are compared to the proposed small-signal model (12). Note that in this, as well as in the next figure, experimental

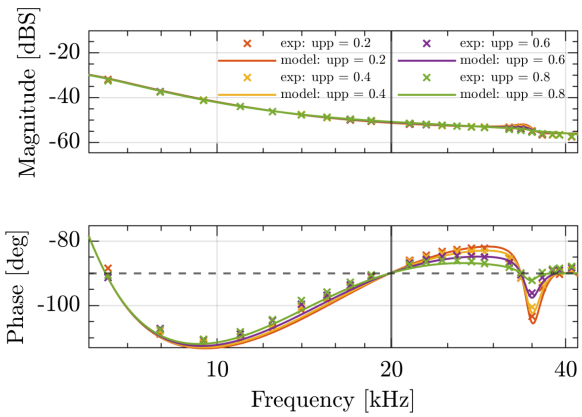

Fig. 13. Comparison between experimental AMs during different S-ac regimes and the proposed model given in (19). The gray vertical line marks the NF.

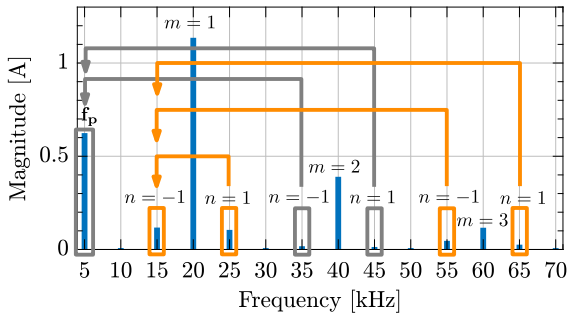

Fig. 14. Spectrum of the inductor current: illustration of the components which, after sampling, are mapped to the first sampled sideband.

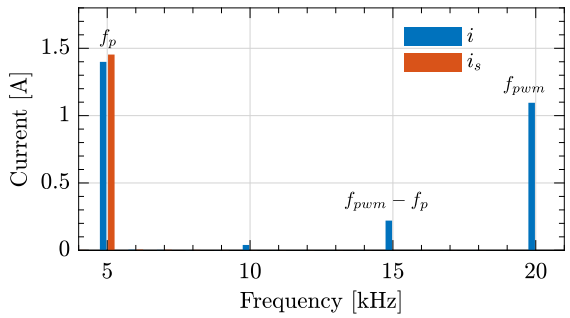

Fig. 15. Comparison between spectra of the current before and after sampling in closed loop operation with 5-kHz perturbation frequency.

AMs are represented by crosses. Less than 2% error between experiments and analytical predictions is achieved up to the SF for all measured SS-dc regimes. This attests to the accuracy and robustness of the proposed high-frequency small-signal modeling approach.

AMs during different S-ac regimes are shown in Fig. 13, where they are compared with the proposed model for S-ac operation (19). Experimental measurements match with the analytical results up to the SF for all measured S-ac regimes, with a less than 2% error.

This verifies that the proposed modeling approach accurately predicts AM during S-ac operation. The proposed model matches with the experimental AMs better than any of the reported models [4], [6], [7], [15]–[17].

VI. Conclusion

In this article, high-frequency modeling of the VSC input admittance is addressed. At first, the impact of the OP on AM is revealed. It is shown that AM obtained while the VSC is operating in S-ac regime is some kind of averaged result of AMs obtained during different SS-dc regimes from the same range. Next, a small-signal model that accurately represents system properties above the NF is presented. Due to the accurate small-signal DPWM representation used, the proposed model is capable of predicting dependence of the FR on SSOP. It is shown that, when center-pulse sampling is employed, PWM sidebands do not create additional loops, which allows only sampling sidebands to be considered. Finally, in order to accurately predict AM during S-ac operation, a novel DPWM model suitable for S-ac operation is derived. Following the same methodology as for SS-dc operation, a model that is capable of predicting dependence of the FR on the grid voltage magnitude is derived. To validate the proposed methodologies, experimental verification is performed on a single-phase two-level VSC. An excellent match between experiments and the proposed analytical models is achieved up to SF during different SS-dc and S-ac regimes. Additionally, in order to illustrate the better accuracy of the proposed techniques, a comparison with the state-of-the-art models is provided.

Appendix A

In order to analytically show that center-pulse sampling eliminates additional loops created by PWM sidebands, the system shown in Fig. 1(a) is considered, without closing the feedback loop. It consists of DPWM, inductor, and sampler. An input to this system $m_s(t)$ is assumed to be

$$m_s(t) = D + M\cos\left(\omega_p t + \phi_p\right) \tag{20}$$

where D is the steady-state duty cycle and M is the magnitude of the sinusoidal perturbation at angular frequency ω_p with initial phase ϕ_p. Expressions for the voltage sidebands u_{sb} generated by asymmetrical uniformly sampled PWM process are [26]

$$u_{sb}^{m,n} = \frac{4E}{\pi}\frac{J_n(q2M\pi)}{q}\sin\left(r\frac{\pi}{2}\right)e^{jn\phi_p} \tag{21}$$

where m and n are the orders of switching and sideband harmonics, respectively, as in [26], $q = m + n\frac{\omega_p}{\omega_{\text{pwm}}}$ is the sideband order, J_n is the Bessel function of the first kind with an order n, and $r = m + n + q(2D-1)$. Expressions for currents i_{sb} resulting from these voltages are derived simply via dividing (21) by inductor impedance at sideband frequency $q\omega_{\text{pwm}}$

$$i_{sb}^{m,n} = \frac{4E}{\pi L}\frac{J_n(q2M\pi)}{\omega_{\text{pwm}}q^2}\sin\left(r\frac{\pi}{2}\right)e^{j\left(n\phi_p-\frac{\pi}{2}\right)}. \tag{22}$$

Finally, to derive an expression for the spectral content of the sampled current $i_{s,sb}$, the model of the sampling process needs to be applied [29]. Due to the double-update rate implementation, the NF coincides with the switching frequency. Therefore, to derive an expression for the sideband components after sampling, only sidebands around odd multiples of the

switching frequency have to be taken into account.[2] To keep the presentation concise, only expression for the first sampled sideband $i^1_{s,sb}$, which is at $\omega_{\text{pwm}} - \omega_p$, is derived. The reasoning shown below holds also for the higher order sidebands: $\omega_{\text{pwm}} - 2\omega_p, \omega_{\text{pwm}} - 3\omega_p, \ldots$. The components of the inductor current which, after sampling, are mapped to $\omega_{\text{pwm}} - \omega_p$ are the first sideband components around odd multiples of the switching frequency, i.e., $|n| = 1$ for $m = 1, 3, 5, \ldots$. This is illustrated in Fig. 14, where the spectrum of the inductor current is shown, resulting from $m_s(t)$ with the following parameters $D = 0.75, M = 0.0625$, and $\omega_p = 2\pi 5$ rad/s.

Following the previously explained procedure, the expression for the first sampled sideband component is derived

$$i^1_{s,sb} = \sum_{m=1,3,5\ldots}^{\infty} \left| i^{m,-1}_{sb} \right| e^{j\phi_{i^{m,-1}_{sb}}} + \left| i^{m,1}_{sb} \right| e^{-j\phi_{i^{m,1}_{sb}}}. \quad (23)$$

As seen, this expression depends on an infinite number of sideband harmonics. Complex mathematical procedures are required to prove that the magnitude of this expression equals zero for any valid set of input parameters D, M, ω_p, ϕ_p. To avoid the added complexity, a numerical search is performed with the parameters being constrained by the following inequalities $0 < D < 1, D + M < 1, D - M > 0, 0 < \omega_p < \omega_{\text{pwm}}, 0 < \phi_p < 2\pi$. For these constraints, the obtained maximum of the first sampled sideband magnitude, relative to the magnitude of the perturbation current, is equal to 0.07%. Therefore, it can be safely assumed that

$$\left| i^1_{s,sb}(D, M, \omega_p, \phi_p) \right| \approx 0. \quad (24)$$

The analysis provided above has shown that center-pulse sampling eliminates PWM sidebands created around odd multiples of the switching frequency. Thus, additional PWM sideband loops are not present in the closed loop operation. As an illustration of this phenomenon, the current spectrum before and after sampling, obtained from the closed loop simulation of the system in Fig. 1, is shown in Fig. 15. The perturbation frequency was set to 5 kHz. As seen from this figure, PWM sideband at 15 kHz is present in the inductor current but not in the sampled signal.

APPENDIX B

For single-update systems ($T_s = T_{\text{pwm}}$), small-signal model of symmetrical uniformly sampled DPWM is given by [18]

$$G_{\text{dpwm\_}su}(j\omega) = \cos\left(\omega \frac{T_s}{2}(D-1)\right) e^{-j\omega\frac{T_s}{2}}. \quad (25)$$

This model should be used in (12) to obtain accurate high-frequency admittance model for SS-dc operation.

In order to obtain an adequate DPWM representation compliant with EN 50388-2 and suitable for predicting AM during S-ac operation in case of the single-update system, the small-signal model from (25) is averaged on the fundamental period, using the same procedure as for the double-update case and given by (14)–(17). This results in

$$G^{\text{s-ac}}_{\text{dpwm\_}su}(j\omega) = \frac{1}{\pi} \int_{-\frac{\pi}{2}}^{\frac{\pi}{2}} \cos\left(\omega T_s \left(\frac{u_{\text{pp}}}{2} \sin\theta - \frac{1}{2}\right)\right) e^{-j\omega\frac{T_s}{2}} d\theta. \quad (26)$$

Compared with (16), analytical solution of (26) does not exist. Nevertheless, means of numerical integration can be used to obtain an accurate high-frequency admittance model suitable for S-ac operation.

Validity of the previously described admittance models is verified by comparing them to the simulated AMs up to twice the SF for different SS-dc and S-ac regimes. The results are not shown due to space limitations. It is noticed that, compared to the double-update system, in case of the single-update system, dependency of the AMs during S-ac operation on the grid voltage magnitude is much less emphasized.

[2]Sidebands around even multiples of the switching frequency are, after sampling, reflected back to the original component ω_p. This does not produce any additional loop; however, it does produce a certain impact on the perturbation component magnitude. These sidebands are always above the NF; hence, resulting sampled current components depend on the relation between their phase and the sampling instant. A great number of consistent simulated and experimental AMs showed that the impact of this effect on closed loop operation is negligible.

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