A MHz-Pulse-Transformer Isolated Gate Driver With Signal-Power Integrated Transmission for Medium-Voltage SiC MOSFETs

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***Abstract*—The conventional isolated gate driver (GD) solution for the medium-voltage (MV) SiC MOSFET separates the signal and power transmissions and requires a bulky GD power supply (GDPS). This article presents a signal-power integrated GD for MV SiC MOSFETs with a compact footprint. The proposed GD transmits both the pulsewidth modulation (PWM) signal and GD power by 20-MHz modulated class-E resonant flyback converters, where the transmitted GD power can maintain constant within the full PWM duty-cycle range (i.e., 0%–100%). In addition, the PWM signal transmission of the proposed GD achieves a low total propagation delay time $<$ 75 ns by utilizing the fast transient of 20-MHz RFCs and the edge-based envelope detector. A printed-circuit-board-based coreless transformer is integrated into the proposed GD to achieve an insulation voltage higher than 10 kV_{RMS} and a low coupling capacitance of 5.85 pF. The common-mode transient immunity of proposed GD is higher than 100 V/ns, which is beneficial to drive MV SiC MOSFETs with high *dv/dt*. The proposed GD does not require additional GDPSs nor fiber-optics, which achieves a smaller size compared to conventional isolated GDs and is promising to be integrated into SiC MOSFET module packages. Experimental results on 3.3 kV and 10 kV SiC MOSFETs are provided to validate the effectiveness of the proposed GD.**

***Index Terms*—Common-mode transient immunity (CMTI), gate driver (GD), medium-voltage (MV) SiC MOSFETs, MHz-pulse-transformer, signal-power integrated transmission.**

I. Introduction

MEDIUM-VOLTAGE (MV) SiC MOSFETs, which span 2.5 to 15 kV range, have attracted the increased attention recently [1]–[3]. Due to the high blocking voltage, fast switching speed, low switching loss, and high-temperature endurability, newly emerged MV SiC MOSFETs have a great potential to improve the efficiency and power density of MV converters and drive down the system complexity [4], [5]. On the other hand, the isolated gate driver (GD) is required to provide the sufficient galvanic isolation and high common-mode transient immunity (CMTI) for MV SiC MOSFET applications [6].

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The conventional isolated GD solution is shown in Fig. 1(a), which consists of a signal-transmission stage and a GD power supply (GDPS) to provide signal and power isolations, respectively. The signal- and power-isolation methods of GDs for SiC devices with different voltage rating are summarized in Fig. 1(b). The signal isolation of GDs can be implemented by the GD integrated circuit (GDIC) [7], digital isolator [8], transformer [9], and fiber-optic (FO) [10]–[15]. For MV SiC MOSFETs, FOs are usually adopted to transmit the signal with a sufficient galvanic isolation and little coupling capacitance C_{cp} on the signal path but with a size and cost penalty [10]–[15]. Like the other signal-isolation method based GDs, secondary circuits of the FO-based GD are tied to the source terminal of SiC MOSFET, the signal-processing circuit is therefore susceptible to the common-mode (CM) current noise induced by the high *dv/dt* and may be malfunctioning [10]. The effect of CM current noise can be mitigated by unbalanced impedance paths, but one additional GDPS and one additional GDIC or digital isolator are required [11], [12].

The power-isolation methods of GDPSs can be categorized into four types: magnetic-core transformer coupling (MCTC) [13]–[18]; wireless power transfer (WPT) [19], [20]; optical power transfer (OPT) [21], [22]; and coreless transformer coupling (CLTC) [23]–[25]. MCTC GDPSs have been widely applied for low-voltage (LV) SiC MOSFETs. To reduce the C_{cp} of MCTC GDPS for 10 kV SiC MOSFETs, printed circuit board (PCB) windings are developed to reduce the overlap of magnetic-core and windings and, thus, enable a $C_{cp} < 3$ pF, but the clearance and creepage distances among the magnetic-core and windings result in a bulky GDPS size [13], [14]. A small magnetic-core transformer (16 mm $\times$ 16 mm $\times$ 14 mm) using separated E-cores is built for a MCTC GDPS with a C_{cp} of 4.1 pF; however, these E-cores require a complex and costly manufacturing process, such as the graphite spray and cores mounting/alignment [15]. Another MCTC GDPS acts like a current-source to supply multiple secondary loads with a single-turn primary winding, where the long cable connection as well as the air gap between magnetic-cores and primary-winding make the GDPS bulky, and extra efforts are needed for the mechanical installation and the fault diagnostic of GD system [16]–[18]. WPT GDPSs for MV SiC MOSFETs utilizes the air gap between transmitter and receiver coils as the isolation barrier [19], [20]. Due to a low dielectric breakdown (2.5–3 kV/mm) of the air, the large air gap is required and, thus, WPT GDPSs usually have a

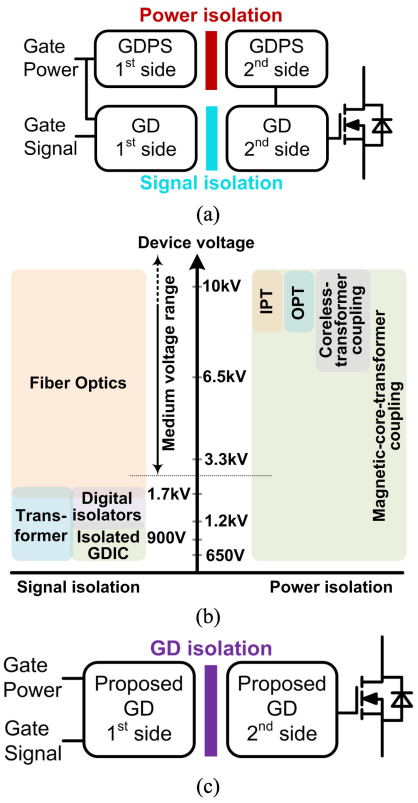


Fig. 1. Isolated GD solutions for SiC MOSFETs. (a) Conventional solution. (b) Signal and power isolation methods of GDs for SiC devices with different voltage rating. (c) Proposed signal-power integrated GD solution.

large form factor. OPT GDPSs deliver the GD power by the laser light via the optical fiber, which ensures an unlimited isolation and eliminates the $C_{\rm cp}$ [21], [22]. However, the transmitted GD power is $<$ 1 W and the transmission efficiency is $<$ 25% [21]. Moreover, the laser transmitter has a very bulky volume [22]. CLTC GDPSs utilizing the solid and liquid dielectrics are explored recently [23]–[25]. They not only remove the insulation issue among the magnetic core and windings but also enable a thinner barrier thickness than the air-based WPT GDPSs. A nonoverlapped PCB windings potted in Epoxy is designed for MV GDPS with a low $C_{\rm cp}$ of 3.89 pF, but the nonoverlapping coils have a relatively large footprint (69 mm $\times$ 69 mm) and decrease the GDPS efficiency ($<$ 50%) [23]. The coreless PCB transformer with FR4 dielectric has an estimated insulating voltage $>$ 40 kV and a $C_{\rm cp}$ $<$ 10 pF [24]. The coreless PCB transformers immersed in the liquid Midel-7131 are verified to withstand the insulating voltage of 33–73 $\rm kV_{RMS}$ [25].

Due to the separate signal and power transmissions and the bulky size of GDPSs, state-of-the-art isolated GDs for MV SiC MOSFETs still exhibit large size and high cost. Moreover, integrating the GD into the MV SiC MOSFET module package will help to improve the reliability and enhance the switching performance, which requires a compact GD design [16], [17]. The pulse-transformer GD has a good potential to achieve the compact design since both signal isolation and power transfer are implemented via the pulse transformer [26]–[29]. However, most pulse transformers operate at the pulsewidth modulation (PWM) frequency and suffer the voltage-second limitation. In addition, these pulse-transformer GDs only can operate in a narrow duty-cycle range and cannot allow the fast change of duty cycle, which limits their applications. Moreover, these pulse-transformer GDs cannot transfer the power at low or zero duty cycle; therefore, the GD secondary circuits, especially the protection circuits, cannot be powered on all the time [26], [27]. High frequency (HF) modulated pulse-transformer GDs are developed to solve these problems [28], [29]. However, the modulation frequency is only 1 MHz due to the high switching loss, which causes a large propagation delay and low duty-cycle resolution [29]. Moreover, magnetic cores are usually adopted by these pulse transformers to achieve high coupling factor, which, however, is challenging to meet the insulation requirements if they are applied for MV SiC MOSFET GDs.

This article proposes a signal-power integrated GD using 20 MHz pulse transformer to transmit the PWM signal and GD power simultaneously for MV SiC MOSFETs, shown in Fig. 1(c). The proposed circuit schematic and modulation principle enables the GD to achieve a constant power transmission regardless of the varied PWM duty cycle. Compared to the existing high-frequency modulated pulse-transformer GDs, the proposed GD has a lower total propagation delay time (i.e., $<$ 75 ns) and a higher PWM duty-cycle resolution (i.e., $\leq$ 0.2%). The 20 MHz class-E resonant flyback converter (RFC) is selected to excite the pulse transformer with the minimum component count. Active clamping circuits are proposed to allow the GD to operate in the full PWM duty-cycle range (i.e., 0%–100%). Aiming at MV SiC MOSFET applications, a PCB-based coreless transformer is adopted to achieve an insulation voltage higher than 10 $\rm kV_{RMS}$, a low C_{cp} of 5.85 pF and a compact GD size. The proposed GD does not need additional GDPSs and FOs, which achieves a smaller size and enables a higher power density for MV SiC-based converters. The CMTI of proposed GD is characterized as $>$ 100 V/ns. The proposed GD is experimentally verified on 3.3 and 10 kV SiC MOSFETs.

The rest of this article is organized as follows. Section II introduces the operation principle and key subcomponents of proposed GD. The low propagation delay time analysis and full PWM duty-cycle range implementation of proposed GD are presented in Section III. Section IV provides the experimental verifications. Finally, Section V concludes this article.

II. Operation Principle and Circuit Description

A. Introduction of Proposed GD and Design Requirement

The block diagram of the proposed signal-power integrated GD is shown in Fig. 2(a). It consists of five subcomponents: an ON/OFF control unit; two identical isolated dc–dc converters (ID2DCs) in input-parallel-output-parallel (IPOP) architecture; a PWM signal regenerator; a dc–dc voltage regulator; and a GD actuator. The ON/OFF control unit is triggered by the PWM input signal to generate complementary ON/OFF control signals that regulate ON/OFF status of two ID2DCs. ID2DC #1 is at ON status when PWM = "1" while ID2DC #2 is at ON status when PWM = "0." Due to the IPOP architecture and complementary operation manner, there is always one ID2DC transmitting the power to supply the GD secondary circuits. Therefore, the output voltage of ID2DCs V_o is maintained constant within the full

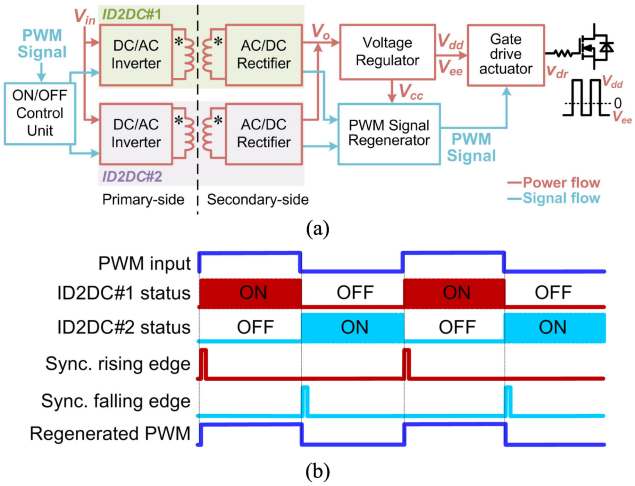


Fig. 2. Proposed signal-power integrated GD. (a) Block diagram. (b) Key waveforms.

PWM duty-cycle range (i.e., 0%–100%). At GD secondary side, the PWM signal regenerator detects the ON/OFF status of two ID2DCs to synchronize the edge signals of the regenerated PWM signal. As shown in Fig. 2(b), OFF-to-ON transitions of two ID2DCs are detected to trigger the rising edge and falling edge, respectively, for the PWM signal regeneration. With the identical edge-triggering mechanism and same circuit parameters, the propagation delay times from low to high and from high to low are the same.

The voltage regulator is fed by V_o of ID2DCs and supplies the positive and negative GD voltages V_{dd} and V_{ee} for the GD actuator, as well as the V_{cc} for PWM signal regenerator and other secondary circuits, such as DESAT and UVLO protection circuits. With the regenerated PWM signal, V_{dd} and V_{ee}, the GD actuator outputs the drive voltage v_{dr} with the desired timing and magnitude. The GD actuator utilizes the MOSFET or BJT based totem-pole bridge to ensure the fast rising/falling time of v_{dr} and the sufficient peak gate current, which could fully leverage the fast switching capability of MV SiC MOSFETs.

The complimentary ON/OFF operation manner of the IPOP ID2DCs not only transfers the GD power continuously, but also transmits the PWM signal. The proposed signal-power integrated GD needs to consider following design aspects.

1) ID2DCs need to operate at the HF or the very HF (VHF) to achieve a low propagation delay time and a high PWM duty-cycle resolution. The PWM duty-cycle resolution, *D.R.*, is determined by the ID2DC's switching frequency f_{id2dc} as

$$D.R. = \frac{f_{\mathrm{pwm}}}{f_{\mathrm{id2dc}}} \times 100\%. \tag{1}$$

Given $f_{\mathrm{pwm}} = 40$ kHz, f_{id2dc} must be ≥ 4 MHz to obtain the *D.R.* of $\leq 1\%$, and ≥ 20 MHz to obtain *D.R.* of $\leq 0.2\%$.

2) Soft switching is required for ID2DCs to obtain the high efficiency at HF/VHF range, which can reduce the thermal stress and thus enable a embedment design into the packages.

TABLE I
COMPONENT COUNTS COMPARISON OF THREE TOPOLOGY CANDIDATES

Topologies	Discrete inductors	Resonant Capacitors	Rectifier diodes	Active switches
Class-E RFC [30]	0	2	1	1
Class-Φ_2 RFC [31]	1	3	1	1
Isolated Class-Φ_2 converter [32]	2	4	1	1

3) ID2DCs should have a simple topology with the minimum component counts for a higher reliability and a smaller size.
4) The galvanic isolation of the proposed GD is provided by the ID2DCs, which must meet the MV insulation requirement and have a low C_{cp} to enhance the CMTI. In addition, a compact size is desired for the insulation solution.
5) The PWM signal regenerator needs to operate normally within the full PWM duty-cycle range (i.e., 0%–100%) and have a minimized propagation delay time.

The detailed description of key sub-components with their features is presented as follows.

B. ID2DC Topology With Minimum Component Counts

Several isolated resonant converter topologies are available for HF and VHF operation with the soft-switching realization. To achieve the high reliability and high power density, the topology with the minimum counts of components, especially active switches and discrete inductors, is desired to implement the ID2DCs of proposed GD. The general architecture of these isolated resonant converter topologies consists of an inverter, a transformer, and a rectifier. In these topologies, the ones with class-E or class-Φ_2 inverter have only one active switch, and this active switch is at the low side and thus easy-to-drive; the ones with class-E rectifier have the minimum count of rectifier diodes. Therefore, the topologies with both class-E or class-Φ_2 inverter and class-E rectifier become candidates, which include class-E RFC [30], class-Φ_2 RFC [31] and isolated class-Φ_2 converter [32]. The component counts of these three topologies are compared in Table I, where the main difference is the count of discrete inductors and resonant capacitors. From Table I, the class-E RFC has zero discrete inductor and the minimum count of resonant capacitors, so it is selected to implement the ID2DCs of proposed GD. To achieve a low propagation delay time and a high PWM *D.R.*, the f_{id2dc} is set as 20 MHz.

The circuit schematic of ID2DCs and ON/OFF control unit is shown in Fig. 3. A 20-MHz VHF signal is generated by the oscillator (OSC). The PWM signal is modulated with 20-MHz VHF signal to produce the gate signals of two class-E RFCs. As the switching frequency of RFCs enters VHF range, a coreless transformer is typically adopted. As shown in Fig. 3, all the inductances L_{l1}, L_M, and L_{l2} are absorbed by the coreless transformer without the extra discrete inductors. The class-E RFC features the high efficiency by the zero-voltage switching (ZVS) for switches $Q_{1\sim2}$ and zero-current switching (ZCS) for diodes $D_{r1\sim2}$. The resonant driving method is applied to reduce the driving loss of $Q_{1\sim2}$. To eliminate another high isolation

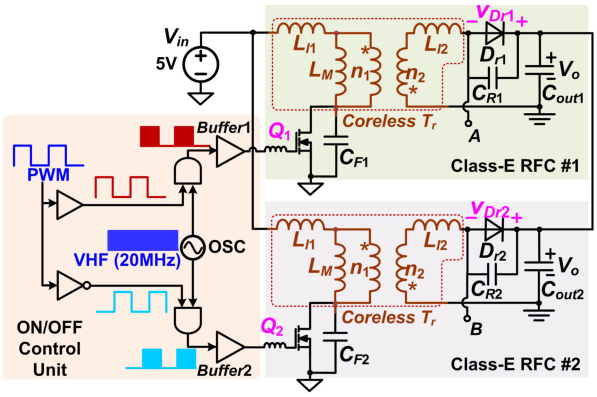


Fig. 3. Circuit schematic of ID2DCs topology and ON/OFF control unit.

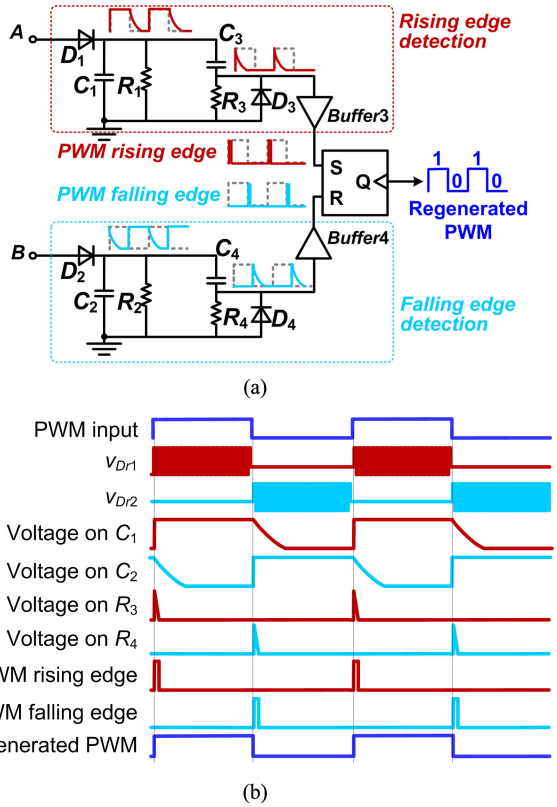


Fig. 4. PWM signal regenerator circuit. (a) Schematic. (b) Key waveforms.

voltage requirement and extra $C_{\rm cp}$ by the isolated feedback loop, class-E RFCs are operated in the open loop.

C. PWM Signal Regenerator With Minimized Propagation Delay Time

The circuit schematic of PWM signal regenerator is shown in Fig. 4(a), where the edge-based signal-processing circuits, including the envelope detector and *RC* differential circuit, are adopted to minimize the propagation delay time.

To detect the ON/OFF status of two class-E RFCs shown in Fig. 3, two envelope detectors, formed by D_1, C_1, R_1 and D_2, C_2, R_2, are connected to the anodes of D_{r1} and D_{r2}, respectively.

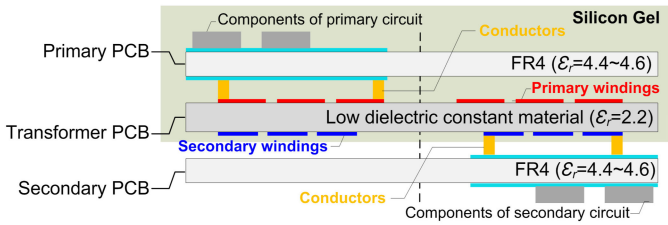


Fig. 5. PCB-based coreless transformer integration into the proposed GD.

The output voltage of the envelope detector, also the envelope voltage (i.e., the voltage on $C_{1\sim2}$), has a step rising edge since $C_{1\sim2}$ is charged abruptly to V_o via $D_{1\sim2}$ at RFCs' OFF-to-ON transitions. So, the rising edge of the envelope voltage can track RFCs' OFF-to-ON transitions with a negligible propagation delay. Two *RC* differential circuits, formed by C_3, R_3, D_3 and C_4, R_4, D_4, respectively, are used to extract the rising edges of envelope voltage with no propagation delay. The extracted edge signals are then buffered as the PWM rising- and falling-edge signals, both of which are sent into a *RS* flip-flop to regenerate PWM signal. The key waveforms of PWM signal regenerator are shown in Fig. 4(b). The propagation delay time of PWM signal regenerator is only contributed by the Buffer$_{3\sim4}$ and *RS* flip-flop, which is less than the comparator-based signal-processing circuits.

D. Transformer Integration With Compact Size

The PCB-based coreless transformer is adopted to achieve a compact size, where PCB itself (a solid dielectric) is utilized as the isolation barrier. The transformer integration into the proposed GD is shown in Fig. 5. The proposed GD is designed within a vertically stacked structure, consisting of the primary PCB, transformer PCB, and secondary PCB. The coreless transformer is printed on the transformer PCB with a spiral winding structure so that the primary and secondary windings are separated at the top and bottom layers of the transformer PCB, respectively. Compared to the helical winding structure, the spiral winding structure avoids the vias and enables the use of two-layer PCB, which simplifies the insulation design and reduces PCB cost. Although only one transformer is visible in Fig. 5 given in the side view, there are two transformers in the proposed GD. With the proposed integration method, only the transformer PCB provides the isolation barrier and contributes the $C_{\rm cp}$. The $C_{\rm cp}$ is mainly determined by the geometry of transformer windings and PCB dielectric constant, that is

$$C \propto \frac{\varepsilon_0 \varepsilon_r S}{d} \tag{2}$$

where $\varepsilon_0\varepsilon_r$ is the dielectric constant of transformer PCB, d is the thickness of transformer PCB, and S is the area of windings.

To ensure a sufficient insulation voltage and a low coupling capacitance, dielectrics with the high breakdown strength and low dielectric constant are preferred. Arlon-DiClad-880, a type of polytetrafluorethylene material, with the dielectric strength $>$ 45 kV/mm and ε_r of $\sim$2.2 is selected. $d = 1.6$ mm is set considering a tradeoff between the coupling factor and the coupling capacitance. The $C_{\rm cp}$ of coreless transformer is extracted by *Ansys*

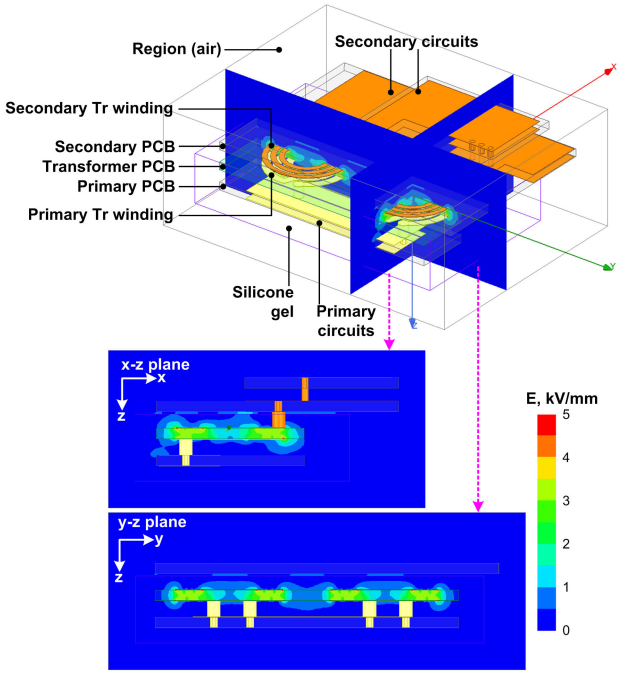


Fig. 6. Simulated E-field distribution of the proposed GD.

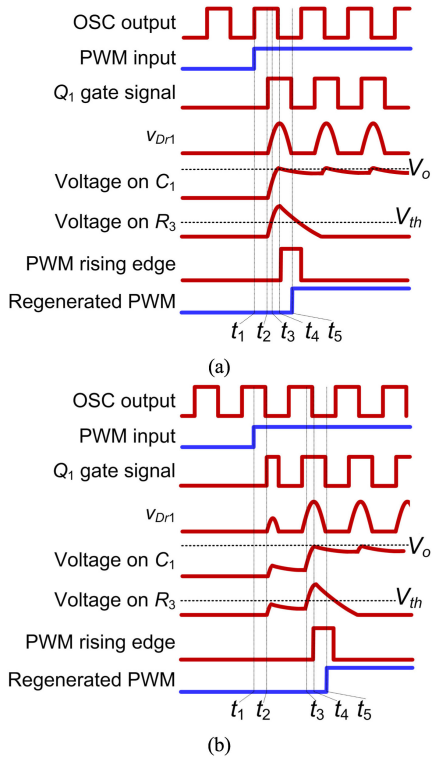


Fig. 7. Total propagation delay time. (a) Minimum propagation delay time. (b) Maximum propagation delay time.

Q3D extractor, which is only 2.3 pF for a single transformer and 5 pF for a pair of transformers. To avoid the surface flashover along the transformer PCB and eliminate the large creepage distance, the silicone gel (SilGel 612) encapsulation is applied to the transformer PCB and primary PCB as shown in Fig. 5. Please note that to enhance the insulation, the secondary PCB can also be encapsulated after GD secondary circuit parameters, such as gate resistances, GD supply voltages (V_{dd}/V_{ee}) and protection circuits are tuned to optimize the device switching performance and protection.

Fig. 6 shows the simulated electric-field distribution of the proposed GD. The electric-field stress mainly occurs in the dielectric of transformer PCB and the surrounding silicone gel. With a potential difference of 5 kV between the primary and secondary sides of GD, the maximum electric-field is observed to be 8.6 kV/mm, which is lower than the dielectric strength of transformer PCB (45 kV/mm) and silicone gel (23 kV/mm).

III. Low Propagation Delay Time Analysis and Full PWM Duty-Cycle Range Implementation

A. Propagation Delay Time Analysis

As illustrated in Fig. 7, the total propagation delay time $T_{pd,\text{total}}$ is the sum of four subintervals ($t_i \sim t_{i+1}$, $i = 1 \sim 4$), that is

$$T_{pd,\text{total}} = \sum_{i=1}^{4}(t_{i+1} - t_i) = T_{pd,\text{gate}} + T_{pd,\text{RFC}} + T_{pd,\text{buf}} + T_{pd,RS} \quad (3)$$

where $T_{pd,\text{gate}} = t_2 - t_1$ is the propagation delay time of GD primary-side logic gates. $T_{pd,\text{RFC}} = t_3 - t_2$ is the delay time caused by class-E RFCs. $T_{pd,\text{buf}} = t_4 - t_3$ and $T_{pd,\text{RS}} = t_5 - t_4$ are the propagation delay times of GD secondary-side *Buffer*$_{3\sim4}$ and *RS* flip-flop, respectively. $T_{pd,\text{gate}}$, $T_{pd,\text{buf}}$, and $T_{pd,RS}$ are all determined by the selected ICs and, thus, remain constant, while $T_{pd,\text{RFC}}$ varies in a specific range due to the asynchronization of OSC's output signal and PWM signal.

The minimum $T_{pd,\text{RFC}}$ occurs when the OSC's output signal and PWM signal are synchronized, which is shown in Fig. 7(a). In this case, the first pulse of Q_1's gate signal after t_1 has a complete pulse width (i.e., one half of OCS's cycle, 1/2 T_{osc}), and the envelope voltage (i.e., the voltage on C_1) reaches V_o within 1/4 T_{osc}. So, the minimum $T_{pd,\text{RFC}}$ approximately equals to

$$T_{pd,\text{RFC,min}} = \frac{V_{th}}{4V_o}T_{\text{osc}} \quad (4)$$

where V_{th} is Buffer$_{3\sim4}$'s threshold voltage for high-level input.

The maximum $T_{pd,\text{RFC}}$ occurs when the OSC's output signal is leading PWM signal by around 1/4 T_{osc}, which is shown in Fig. 7(b). In this case, the first pulse of Q_1's gate signal after t_1 has a pulse-width shorter than 1/4 T_{osc}, and the envelope voltage (i.e., the voltage on C_1) cannot reach V_o until the next OSC cycle. Therefore, the maximum $T_{pd,\text{RFC}}$ approximately equals to

$$T_{pd,\text{RFC,max}} = \frac{1}{4}T_{\text{osc}} + \frac{1}{2}T_{\text{osc}} + \frac{V_{th}}{4V_o}T_{\text{osc}} = \frac{3}{4}T_{\text{osc}} + T_{pd,\text{RFC,min}}. \quad (5)$$

Table II gives the breakdown of total propagation delay time with the selected ICs. When OCS's output signal and PWM

TABLE II
BREAKDOWN OF TOTAL PROPAGATION DELAY TIME

	Delay sources		Delay time
$T_{pd,gate}$	SN74LVC1G02 x2+ SN74LVC2G34		5 ns ×2 + 3.4 ns
$T_{pd,RFC}$	RFC operation, [$T_{pd,RFC,min}$, $T_{pd,RFC,max}$]		[7.3 ns, 44.8 ns]
$T_{pd,buf}$	SN74LVC1G02		5 ns
$T_{pd,RS}$	SN74LVC2G02		5.4 ns ×2
Total propagation delay time		Synchronized mode	36.5 ns
		Asynchronized mode	[36.5 ns, 74 ns]

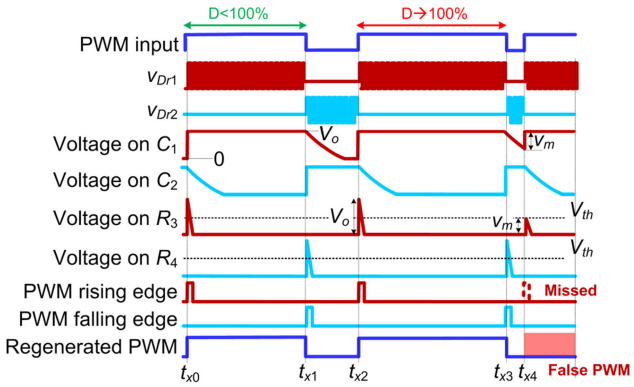


Fig. 8. False PWM signal regeneration with D close to 100%.

signal are synchronized, the total propagation delay time of proposed GD is only 36.5 ns. When OCS's output signal and PWM signal are asynchronized, the total propagation delay time of proposed GD has a range of 36.5–74 ns. This low propagation delay time is comparable with the state-of-the-art commercial isolated GDICs. When OSC's output signal and PWM signal are asynchronized, the difference of $T_{pd,\mathrm{RFC,max}}$ and $T_{pd,\mathrm{RFC,min}}$ may result in a propagation jitter. Like commercial GDICs, this propagation jitter should be considered for setting the dead-time for a phase-leg circuit. This propagation jitter can either be shortened by increasing the operation frequency of ID2DCs, or be eliminated by synchronizing OSC's output signal and PWM signal.

B. Duty-Cycle Range Limitation and Extension

As shown in Fig. 4, $C_{1\sim2}$ is discharged via $R_{1\sim2}$ during RFCs' OFF status and the envelope voltage has a smooth falling edge, which results in a false PWM signal regeneration when the PWM duty cycle D is close to 0% or 100%. For example, the false PWM signal regeneration with D close to 100% is illustrated in Fig. 8.

When D is not close to 100% during $t_{x0} \sim t_{x2}$, the envelope voltage decreases exponentially during $t_{x1} \sim t_{x2}$ and drops to 0 before t_{x2}. With a large time constant $R_{1\sim2}C_{1\sim2}$, the voltage ripple of envelope voltage during class-E RFC's ON status is ignored, so the envelope voltage v_e during the discharging interval ($t_{x1} \sim t_{x2}$) is expressed as

$$v_e = V_o e^{-\frac{t}{R_1 C_1}} = V_o e^{-\frac{t}{\tau_o}} \tag{6}$$

where τ_o is the original time constant and $\tau_o = R_{1\sim2}C_{1\sim2}$.

Since v_e drops to 0 within $5\tau_o < (t_{x2} - t_{x1})$ and remains 0 before t_{x2}, the output voltage of RC differential circuit (i.e., the voltage on R_3) steps from 0 to V_o ($V_o > V_{th}$) at t_{x2}, which will normally trigger the PWM rising-edge signal. However, when D is close to 100% during $t_{x2}\sim t_{x4}$, v_e cannot drop to 0 during $t_{x3} \sim t_{x4}$ ($\Delta t = t_{x4} - t_{x3} = (1\text{–}D)/f_{\mathrm{pwm}}$), and the magnitude of v_e at t_{x4} is

$$v_e(t_{x4}) = V_o e^{-\frac{(t_{x4}-t_{x3})}{\tau_o}} = V_o e^{-\frac{\Delta t}{\tau_o}}. \tag{7}$$

Since $v_e(t_{x4}) > 0$, the output voltage of RC differential circuit (i.e., the voltage on R_3) steps from 0 to V_m ($V_m < V_o$) at t_{x4}, and V_m equals to the difference of V_o and $v_e(t_{x4})$, that is

$$V_m = V_o - v_e(t_{x4}) = V_o\left(1 - e^{-\frac{\Delta t}{\tau_o}}\right) = V_o\left(1 - e^{-\frac{(1-D)}{\tau_o f_{\mathrm{pwm}}}}\right). \tag{8}$$

According to (8), a larger D results in a lower V_m. When $V_m < V_{th}$, the rising-edge signal in Fig. 4(a) cannot be triggered normally and a false PWM signal will be generated. Substitute $V_m = V_{th}$ into (8), leading to the critical value of Δt

$$\Delta t_{\mathrm{crit}} = \tau_o \ln\left(\frac{V_o}{V_o - V_{th}}\right). \tag{9}$$

D should meet (10) to normally trigger the PWM rising-edge signal when D is close to 100%

$$\Delta t_{\mathrm{crit}} < \frac{1-D}{f_{\mathrm{pwm}}}. \tag{10}$$

Similarly, D should meet (11) to normally trigger the PWM falling-edge signal when D is close to 0%

$$\Delta t_{\mathrm{crit}} < \frac{D}{f_{\mathrm{pwm}}}. \tag{11}$$

Substitute (9) into (10) and (11), leading to a limited PWM duty-cycle range D_{limited} as

$$f_{\mathrm{pwm}} R_{1\sim2} C_{1\sim2} \ln\left(\frac{V_o}{V_o - V_{th}}\right) < D_{\mathrm{limited}} < 1 - f_{\mathrm{pwm}} R_{1\sim2} C_{1\sim2} \ln\left(\frac{V_o}{V_o - V_{th}}\right). \tag{12}$$

Given $R_{1\sim2} = 1.2$ kΩ, $C_{1\sim2} = 1.2$ nF and $f_{\mathrm{pwm}} = 40$ kHz, $\Delta t_{\mathrm{crit}} = 1.26$ μs, and $D_{\mathrm{limited}} = [5\%, 95\%]$ are calculated according to (9) and (12). To extend the PWM duty-cycle range, the active clamping circuits, consisting of resistors $R_{5\sim6}$, switches $S_{\mathrm{aux1\sim2}}$ and one-shot triggers, are added into the previous envelop detectors, which are shown in Fig. 9. The gate signal of $S_{\mathrm{aux1\sim2}}$ is provided by the one-shot trigger that is synchronized with the opposite edge signal. The key waveforms of PWM signal regeneration with proposed active clamping circuits are shown in Fig. 10. Since $R_{5\sim6}$ has a much smaller resistance than $R_{1\sim2}$, the envelope voltage can decrease faster than that without the active clamping circuits, the improved envelop detector therefore has a step falling edge.

With the proposed active clamping circuits, the extended PWM duty-cycle range D_{extended} is determined by the pulse width of gate signals for $S_{\mathrm{aux1\sim2}}$, Δt_w, that is

$$f_{\mathrm{pwm}} \Delta t_w < D_{\mathrm{extended}} < 1 - f_{\mathrm{pwm}} \Delta t_w. \tag{13}$$

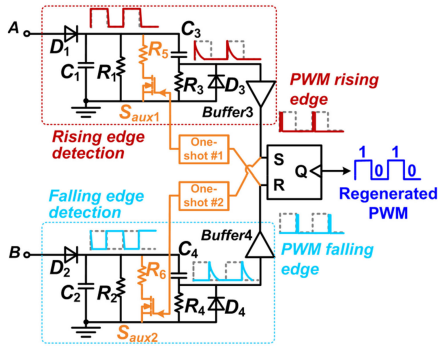


Fig. 9. Proposed active clamping circuit to extend PWM duty-cycle range.

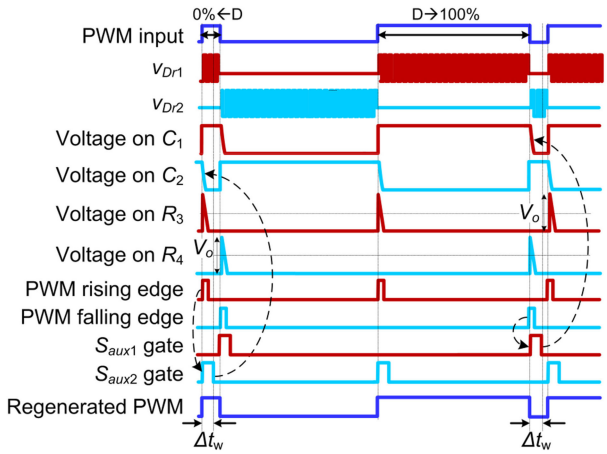


Fig. 10. PWM signal regeneration with active clamping circuits when D is close to 0% and 100%.

The envelope voltage should decrease enough during Δt_w to normally trigger the edge signals, thus the selection of $R_{5\sim6}$ and Δt_w should meet

$$\Delta t_{\text{crit}}{}' = \tau_i \ln\left(\frac{V_o}{V_o - V_{th}}\right) = \frac{R_{1\sim2}R_{5\sim6}}{R_{1\sim2}+R_{5\sim6}} \times C_{1\sim2} \ln\left(\frac{V_o}{V_o - V_{th}}\right) \le \Delta t_w \tag{14}$$

where $\Delta t_{\text{crit}}{}'$ is the critical value of Δt with the active clamping circuits, $\tau_i = R_{1\sim2}R_{5\sim6}/(R_{1\sim2}+R_{5\sim6})\times C_{1\sim2}$ is the improved time constant and the drain-source on resistance of $S_{\text{aux1}\sim2}$ is ignored.

Substitute (14) into (13), D_{extended} can be written as

$$f_{\text{pwm}}\frac{R_{1\sim2}R_{5\sim6}C_{1\sim2}}{R_{1\sim2}+R_{5\sim6}} \ln\left(\frac{V_o}{V_o - V_{th}}\right) < D_{\text{extended}} < 1 - f_{\text{pwm}}\frac{R_{1\sim2}R_{5\sim6}C_{1\sim2}}{R_{1\sim2}+R_{5\sim6}} \ln\left(\frac{V_o}{V_o - V_{th}}\right). \tag{15}$$

Given $R_{1\sim2} = 1.2\ \text{k}\Omega$, $R_{5\sim6} = 5\ \Omega$, $C_{1\sim2} = 1.2$ nF, $f_{\text{pwm}} =$ 40 kHz and $\Delta t_w = 50$ ns, $\Delta t_{\text{crit}}{}'$ is only 10.4 ns and D_{extended} is [0.2%, 99.8%] according to (14) and (15). $\Delta t_w = 50$ ns is compatible with the expected PWM *D.R.* of 0.2%, so the proposed GD can operate in the full PWM duty-cycle range [0%, 100%] with the active clamping circuits.

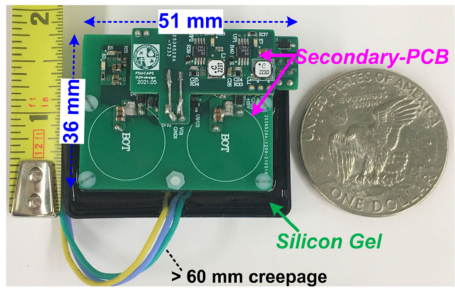
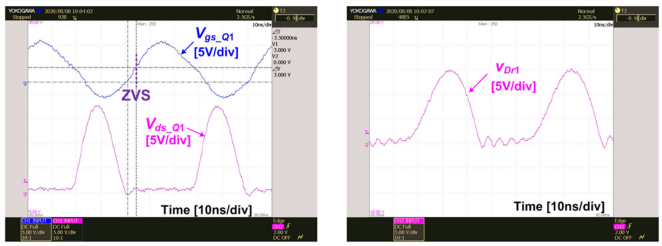


Fig. 11. Photograph of the proposed GD prototype.

TABLE III
PROTOTYPE KEY PARAMETERS

Parameters	Specs	Parameters	Specs
L_m	53.7 nH	C_P	366 pF
L_{l1}	26.4 nH	C_R	293 pF
L_{l2}	61.1 nH	C_{out}	10 μF
$n_1 : n_2$	3:3	Q_1, Q_2	BSD316SN
VHF	20 MHz	D_1, D_2	PMEG3010ER



(a) (b)

Fig. 12. Experimental waveforms of Q_1 and D_{r1} @ $P_o = 1.6$ W. (a) v_{gs_Q1} and v_{ds_Q1} waveforms. (b) v_{Dr1} waveform.

IV. EXPERIMENTAL VERIFICATIONS

The hardware of the proposed GD is built in the laboratory, and the prototype is shown in Fig. 11.

A. ID2DC Operation Verification

The design parameters of class-E RFCs are given in Table III. Class-E RFCs performance is verified experimentally. The waveforms of gate–source voltage v_{gs_Q1}, drain–source voltage v_{ds_Q1} of Q_1 and voltage across D_{r1}, v_{Dr1}, are shown in Fig. 12, where the ZVS of Q_1 and ZCS of D_{r1} are both realized. The measured maximum output power of class-E RFCs is 1.67 W with a 16.4-Ω resistive load, which is sufficient to supply GD secondary circuits as well as to drive 3.3 kV SiC MOSFET GR40MT33N ($C_{iss} = 10.1$ nF) or 10 kV SiC MOSFET with 4 *Gen-3* dies per switch ($C_{iss} = 24.8$ nF) at $f_{\text{pwm}} =$ 10 ∼ 100 kHz. The efficiency and V_{o} curves of class-E RFCs are given in Fig. 13. These two class-E RFCs can achieve the consistent output characteristics within the whole load range, which ensures a stable V_{o} with the varied PWM duty cycle.

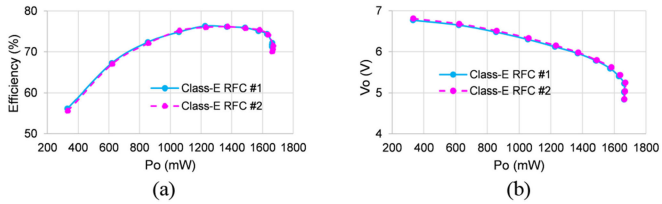


Fig. 13. Efficiency and V_o of RFC$_{1\sim2}$ versus output power. (a) Efficiency versus output power. (b) V_o versus output power.

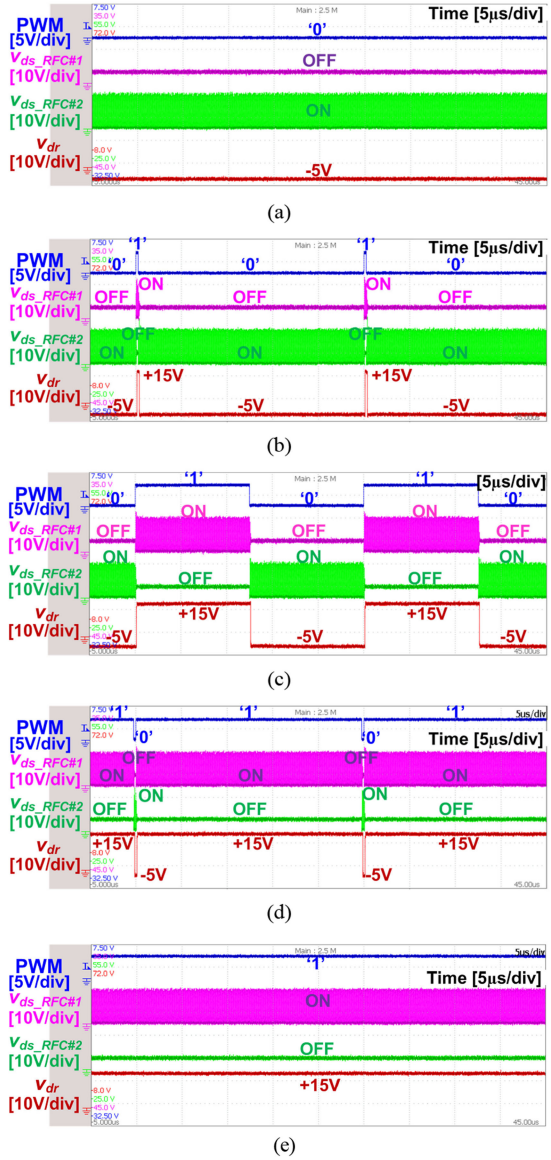


Fig. 14. Complementary operation manners of two class-E RFCs. (a) $D = 0\%$. (b) $D = 1\%$. (c) $D = 50\%$. (d) $D = 99\%$. (e) $D = 100\%$.

B. PWM Duty-Cycle Range and Propagation Delay Time Verification

Fig. 14(a)–(e) shows complementary operation manners of the two class-E RFCs at $D = 0\%$, 1%, 50%, 99%, and 100%, respectively, with $f_{\text{pwm}} = 40$ kHz. At different D, v_{dr} with the desired timing and magnitudes (+15 V/ −5 V) is generated. It is

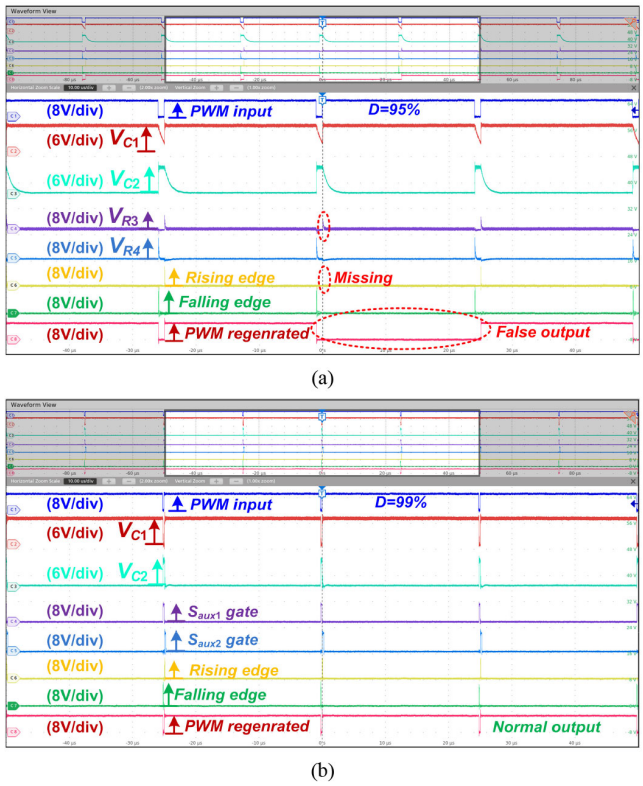


Fig. 15. PWM regeneration waveforms. (a) Active clamping circuit disabled ($D = 95\%$). (b) Active clamping circuit activated ($D = 99\%$).

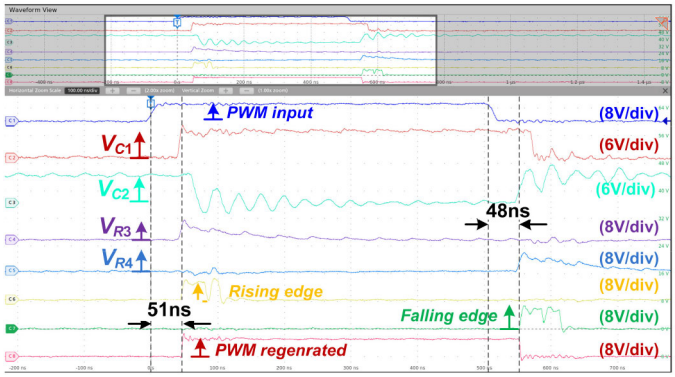


Fig. 16. Measured total propagation delay time of the proposed GD.

demonstrated that the proposed GD achieves the signal-power integrated transmission within the full PWM duty-cycle range.

The full PWM duty-cycle range operation is ensured by the proposed active clamping circuits. The comparison of PWM regeneration waveforms with the active clamping circuits disabled and activated is given in Fig. 15. As shown in Fig. 15(a), the false PWM regeneration occurs when $D = 95\%$ with active clamping circuits disabled. Instead, with active clamping circuit activated, there is no false PWM signal regenerated even when $D = 99\%$ as shown in Fig. 15(b).

The typical propagation delay time of the proposed GD is measured in Fig. 16. The measured total propagation delay times from low to high and from high to low are 51 and 48 ns,

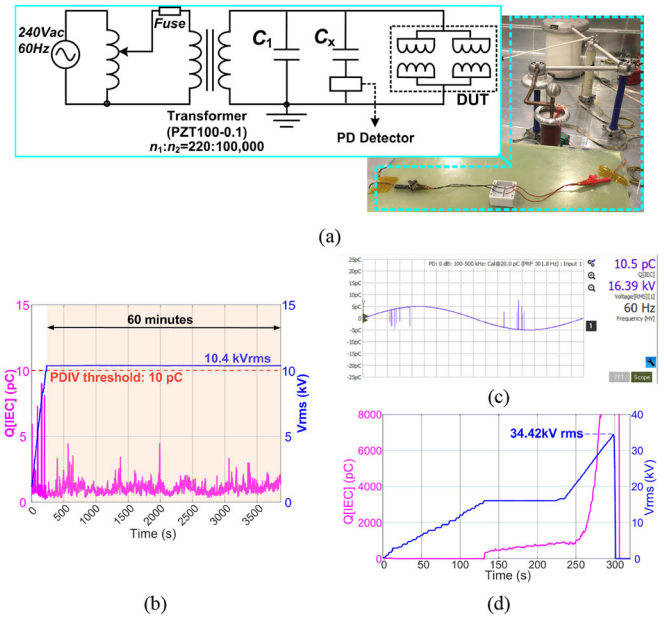


Fig. 17. HV insulation test results for GD transformer. (a) Circuit schematic and photograph of HV insulation test setup. (b) Stress test result at 10.4 kV rms for 60 min. (c) PDIV result. (d) Breakdown test result.

respectively, which matches well with the theoretical range of 36.5–74 ns (asynchronized mode). Therefore, the proposed GD can provide a low total propagation delay time and thus is suitable for SiC MOSFETs with a high switching frequency.

C. High-Voltage Insulation Verification of GD Transformer

The high-voltage (HV) insulation of GD transformer is verified using the HV test setup shown in Fig. 17(a). A 60-Hz ac voltage is applied across the primary and secondary side of transformer. The partial discharge (PD) test is first conducted at ac voltage of 10.4 kV_{RMS} (14.7 kVpk) for 60 min. The recorded PD data are shown in Fig. 17(b), which is free of PD or breakdown failure. The PD inception voltage (PDIV) is also characterized by increasing the ac voltage until the PD reaches the threshold 10 pC. As shown in Fig. 17(c), the measured PDIV is 16.4 kV_{RMS}. The breakdown test is conducted by increasing the ac voltage until electric breakdown occurs. As shown in Fig. 17(d), the measured breakdown voltage is 34.4 kV_{RMS}. These test results demonstrate that the GD transformer can withstand an insulation voltage higher than 10 kV_{RMS}.

D. CMTI Characterization and Verification

To evaluate the robustness of proposed GD to high *dv/dt*, the CMTI of proposed GD is characterized experimentally based on the method of [33]. The CMTI test setup is shown in Fig. 18 where a SiC-based half-bridge circuit is built to generate CM voltage pulses with a 2-kV magnitude, 50% duty cycle and a $dv/dt > 100$ V/ns. The v_{dr} of proposed GD is measured by Tektronix IsoVu Probe TIVH08L; the v_{cm} across the primary and secondary side of the proposed GD is measured by Tektronix HV differential probe THDP0100; the CM current through

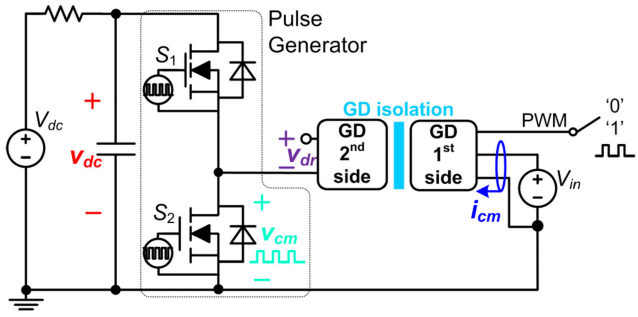


Fig. 18. CMTI test setup.

proposed GD i_{cm} is measured by Pearson Electronics current monitor 2877.

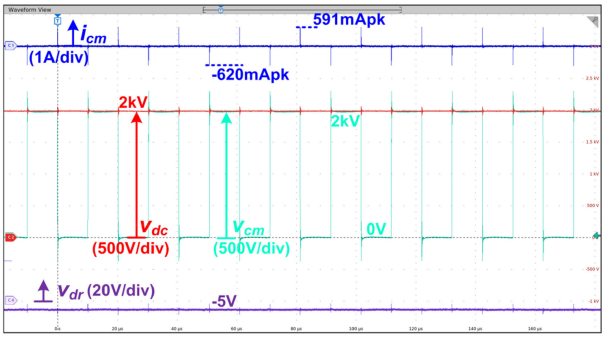
Fig. 19(a)–(c) shows CMTI testing waveforms. The static CMTI testing waveforms with PWM signal tied to logic low ($D = 0\%$) and logic high ($D = 100\%$) are shown in Fig. 19(a) and (b), respectively. The dynamic CMTI testing waveform with $D = 50\%$ and 40 kHz PWM frequency is shown in Fig. 19(c). It is important to note that no CM choke is added into the proposed GD during CMTI tests, the proposed GD operates normally without false-triggering or missing pulses. Transient waveforms during rising and falling intervals of v_{cm} are shown in Fig. 19(d) and (e), respectively. The maximum rising and falling *dv/dt* of v_{cm} are 106 V/ns and 101 V/ns, respectively, but v_{dr} of the proposed GD still remains clear and stable during transients. Therefore, it is concluded that the proposed GD has a CMTI $>$ 100 V/ns, which is qualified for MV SiC MOSFET applications. With the measured peak i_{cm} and maximum rising and falling *dv/dt*, the C_{cp} of the proposed GD is extracted as 5.85 pF. This result is slightly larger than *Q3D* simulation result (i.e., 5 pF), which may be caused by the coupling effect of different PCBs. In the real application, CM chokes can be further utilized to suppress the CM noise current to enhance the GD's robustness.

E. Switching Performance Verifications for 3.3 and 10 kV SiC MOSFETs

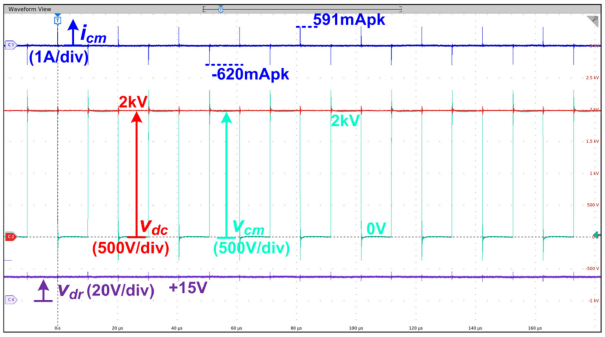
The multiple pulse test (MPT) is first conducted on 3.3 kV discrete SiC MOSFET and 10 kV SiC MOSFET half-bridge power module, respectively, to demonstrate their dynamic switching performance with proposed GD. The continuous operation of proposed GD is then verified on 10 kV SiC MOSFET half-bridge power module.

The MPT testbed schematic is shown in Fig. 20(a). The photos of MPT testbed for 3.3 kV SiC MOSFET GR40MT33N and 10 kV SiC MOSFET half-bridge power module are shown in Fig. 20(b) and (c), respectively. The proposed GD is used to drive the upper switch S_1, where the galvanic isolation and CMTI to the high *dv/dt* is more challenging.

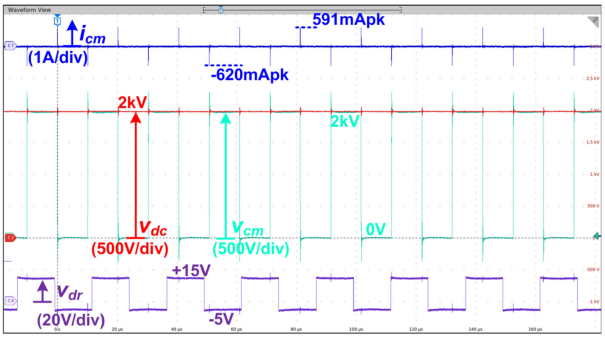
MPT waveform for 3.3 kV SiC MOSFET is shown in Fig. 21(a), where $V_{dc} = 2$ kV, $i_{d\_S1,\max} = 45$ A, $R_{\text{gon}} = 2.5\ \Omega$, $R_{\text{goff}} = 3.3\ \Omega$, $L_{\text{load}} = 1.3$ mH, $C_{\text{bus}} = 80\ \mu$F, and $C_{\text{dec}} = 940$ nF. Zoomed switching transients are shown in Fig. 21(b) and (c). The maximum turn-ON *dv/dt* of S_1 is 92 V/ns occurring at zero load current, and the maximum turn-OFF *dv/dt* of S_1 is



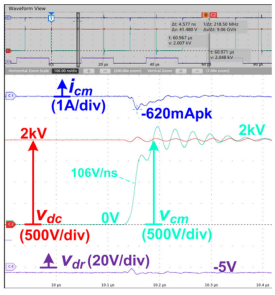
(a)



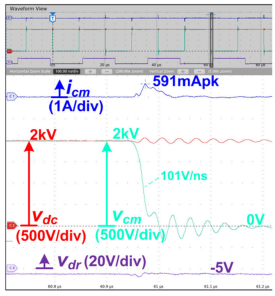
(b)



(c)



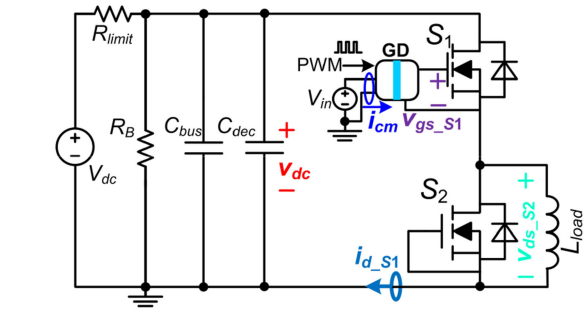
(d)



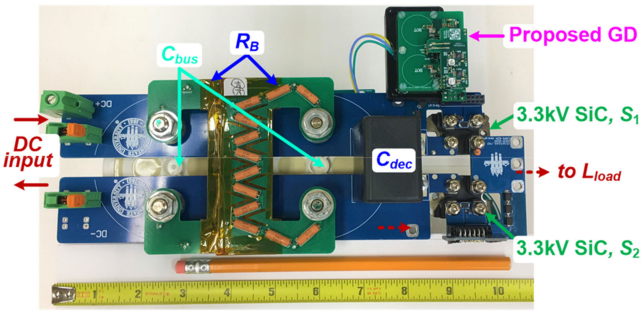
(e)

Fig. 19. CMTI experimental waveforms. (a) PWM = "0." (b) PWM = "1." (c) $D = 50\%$, PWM frequency = 40 kHz. (d) During $v_{\rm cm}$ rising. (e) During $v_{\rm cm}$ falling.

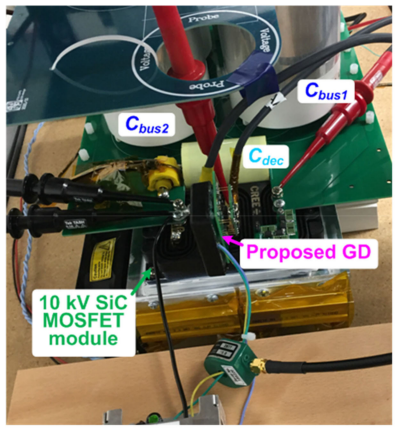
134 V/ns occurring at the maximum load current (i.e., 45 A). MPT waveform for 10 kV SiC MOSFET power module is shown in Fig. 22(a), where $V_{\rm dc} = 5$ kV, $i_{d\_S1,\max} = 60$ A, $R_{gon} = R_{goff} = 3.3\ \Omega$, $L_{\rm load} = 1.3$ mH, $C_{\rm bus} = 40\ \mu$F, and $C_{\rm dec} = 15$ nF. The switching transients are shown in Fig. 22(b) and (c).



(a)



(b)



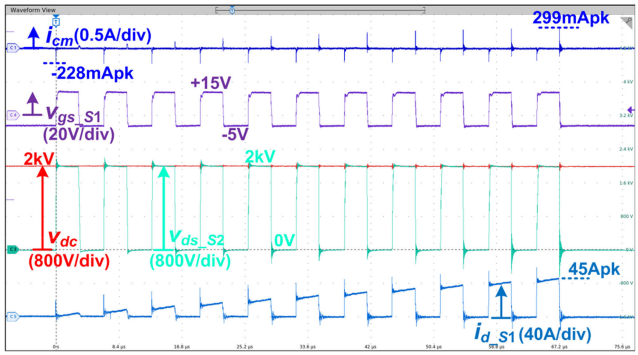
(c)

Fig. 20. MPT testbed for MV SiC MOSFETs. (a) Schematic. (b) MPT testbed hardware for 3.3 kV SiC MOSFET discrete devices. (c) MPT testbed hardware for 10 kV SiC MOSFET half-bridge power module.

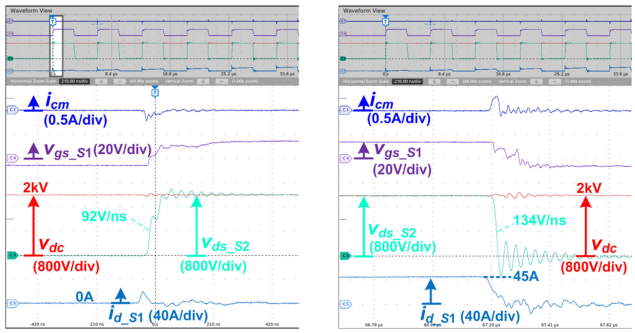
The maximum turn-ON *dv/dt* of S_1 occurs at zero load current and it can reach 55 V/ns. The maximum turn-OFF *dv/dt* of S_1 occurs at the maximum load current (i.e., 60 A) and it can reach 80 V/ns. Figs. 21 and 22 have demonstrated that the proposed GD is free of false-triggering, missing pulse or undesired delay when driving 3.3 kV and 10 kV SiC MOSFETs under high *dv/dt*.

The existing DESAT protection method for 10 kV SiC MOSFET is applied to the proposed GD. Using MPT testbed of Fig. 20(c), an overcurrent (OC) fault is tested on the upper switch S_1 at 5-kV dc-link voltage. The experimental waveform is presented in Fig. 23. The DESAT protection is activated when S_1 current reaches OC protection threshold 75 A. Then, S_1 starts soft-turning-OFF after a response time of 430 ns.

In addition to MPT and DESAT protection tests, the continuous operation of the proposed GD for 10 kV SiC MOSFET

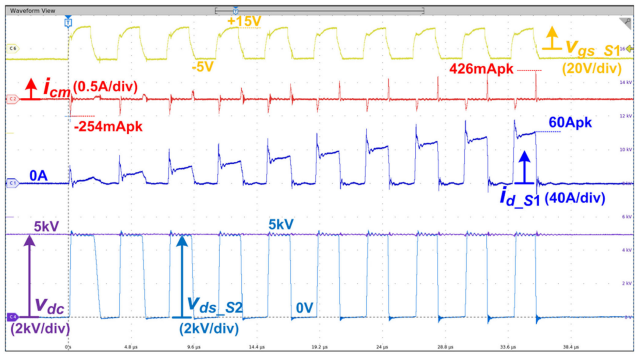


(a)

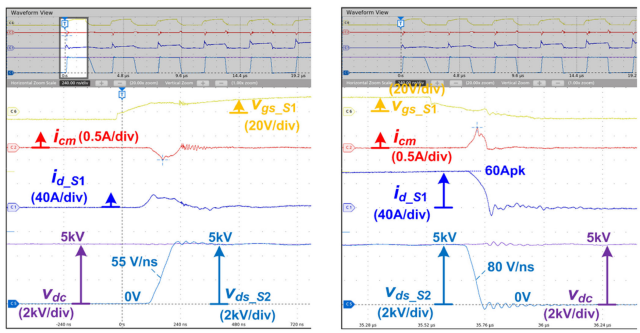


(b) (c)

Fig. 21. MPT results for 3.3 kV SiC MOSFETs. (a) MPT waveform at $V_{\rm dc}$ = 2 kV, $I_{d\_S1\rm max}$ = 45 A, $L_{\rm load}$ = 1.3 mH, R_{gon} = 2.5 Ω, and R_{goff} = 3.3 Ω. (b) Turn-ON transients during the first pulse. (c) Turn-OFF transients during the last pulse.



(a)



(b) (c)

Fig. 22. MPT results for 10 kV SiC MOSFET module. (a) MPT waveform at $V_{\rm dc}$ = 5 kV, $I_{d\_S1\rm max}$ = 60 A, $L_{\rm load}$ = 1.3 mH, and R_{gon} = R_{goff} = 3.3 Ω. (b) Turn-ON transients during the first pulse. (c) Turn-OFF transients during the last pulse.

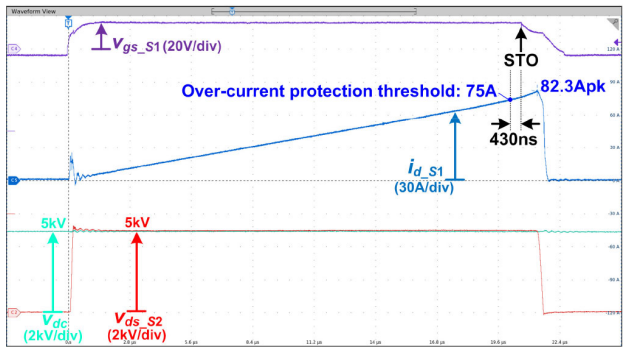
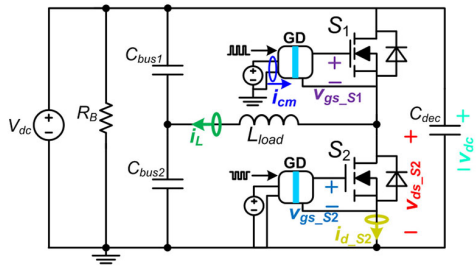
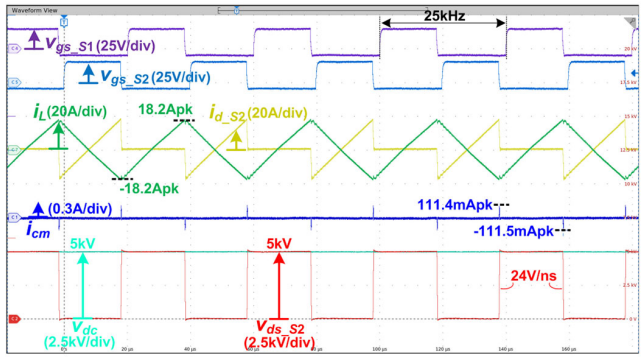


Fig. 23. Experimental waveform of DESAT protection of 10 kV SiC MOSFET module at 5-kV dc voltage.



(a)



(b)

Fig. 24. Continuous test results for 10 kV SiC MOSFET module. (a) Testbed circuit schematic. (b) Experimental waveform at $V_{\rm dc}$ = 5 kV, $I_{L,\rm peak\text{-}to\text{-}peak}$ = 36.4 A, $L_{\rm load}$ = 1.3 mH, and R_{gon} = R_{goff} = 3.3 Ω.

half-bridge module is also verified using the circuit shown in Fig. 24(a). The experimental waveform is illustrated in Fig. 24(b), where $V_{\rm dc}$ = 5 kV, peak-to-peak inductor current $I_{L,\ \rm peak\text{-}to\text{-}peak}$ = 36.4 A, $L_{\rm load}$ = 1.3 mH, R_{gon} = R_{goff} = 3.3 Ω, and $C_{\rm bus1}$ = $C_{\rm bus2}$ = 80μF. The upper and lower switches are turned ON/OFF complementarily with 25 kHz frequency. The output of the proposed GD has the desired timing and magnitude. The CM current flowing through the upper GD reaches 111.5 mA when the *dv/dt* is 24 V/ns. Fig. 24 demonstrates that the proposed GD can continuously drive the 10 kV SiC MOSFET with a 5-kV dc-link voltage and *dv/dt* of 24 V/ns.

V. Conclusion

This article presents a 20 MHz-pulse-transformer isolated GD with the signal-power integrated transmission for MV SiC

MOSFETs. The proposed GD transmits both the PWM signal and GD power simultaneously, so isolated GDPSs and FOs are not required, which reduces the size and cost of GD for MV SiC MOSFETs. The proposed GD utilizes two 20 MHz class-E RFCs in the IPOP architecture and complementary operation manners to transmit a constant GD power with varied PWM duty cycle. The proposed GD can achieve a total propagation delay time $<$ 75 ns, which is enabled by 20 MHz operation and edge-based signal-processing circuits. The active clamping circuit is proposed to avoid the false PWM regeneration, which ensures the proposed GD operate within full PWM duty-cycle range. The PCB-based coreless transformer is integrated into the proposed GD with an insulating voltage higher than 10 $\mathrm{kV_{RMS}}$ and a low C_{cp} of 5.85 pF. A prototype of the proposed GD has been developed in laboratory with a small footprint (51 mm $\times$ 36 mm). The CMTI of proposed GD is characterized as $>$ 100 V/ns at 2 kV CM voltage. The proposed GD can drive MV SiC devices with the desired timing and driving voltage of $+15$ V/ -5 V. The experimental results have verified the validity of proposed GD for 3.3 kV and 10 kV SiC MOSFETs. The proposed GD can also be applied to other voltage (e.g., 6.5 kV) rated MV SiC MOSFET.

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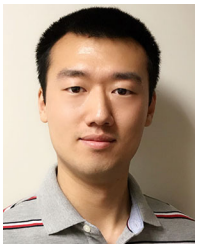

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