Circuit-Based Electrothermal Modeling of SiC Power Modules With Nonlinear Thermal Models

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***Abstract*—Silicon carbide (SiC) power devices have the potential to operate at high temperatures beyond the capabilities of silicon power devices. At increased temperatures, the temperature-dependent material properties of the SiC die and the package multilayer structure can influence the electrothermal (ET) device performance. In this article, a new step-back-correction technique implemented in a finite-difference-method-based thermal modeling tool is proposed to reduce the computational cost while maintaining a good accuracy of ET simulations for multichip power modules. The simulations take the temperature dependence of the thermal conductivity $k(T)$ and both conduction and switching losses into account. The importance of considering $k(T)$ for the accurate temperature prediction of SiC power devices is demonstrated for thermal impedance evaluations characterized by high-temperature swings, as well as for a 100-kHz boost converter with low device temperature amplitudes in the steady state. The proposed ET modeling is validated by COMSOL simulations and infrared camera measurements on an example of a custom-designed and custom-manufactured half-bridge SiC power module.**

***Index Terms*—Electrothermal (ET) modeling, heat capacitance, power module (PM), silicon carbide (SiC), thermal conductivity.**

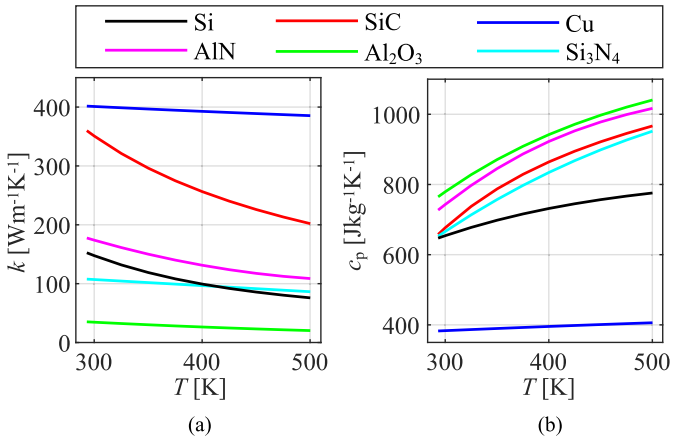

Fig. 1. Temperature dependence of material thermal parameters for the commonly used package materials in PE applications in the temperature range of 293–500 K. (a) Thermal conductivity $k(T)$ of SiC [26], Cu [27], AlN [28], Al_2O_3 [29], Si_3N_4 [30], Si [27]. (b) Specific heat capacity $c_p(T)$ of SiC [26], Cu [31], AlN [28], Al_2O_3 [32], Si_3N_4 [30], and Si [33].

I. Introduction

EMERGING silicon carbide (SiC) power semiconductor devices have pushed the performance limits of power electronic (PE) systems, allowing faster device switching and higher device operational temperatures. System optimization and advanced packaging are necessary in order to utilize SiC power semiconductor devices in the most efficient way in PE applications [1]. Besides enhanced electromagnetic performance, advanced packaging technologies strive toward increasing the operational temperature range of SiC power devices in the applications beyond $T_{\max} = 150$–175 °C [2]. For higher operating temperature range and with large temperature variations, temperature-dependent thermal properties of package materials can have a high impact on the overall electrothermal (ET) package performance. For example, due to its high thermal conductivity, aluminum nitride (AlN) ceramic substrates have been employed in power modules (PMs) designed for high-temperature and/or high-voltage applications [3]–[5]. The thermal conductivities of SiC and AlN feature more pronounced temperature dependence than other materials as copper (Cu), aluminum oxide (Al_3O_2), and silicon nitride (Si_3N_4) (cf. Fig. 1). As temperature of power devices is a crucial design parameter for system performance and reliability, great efforts are made in the direction of evaluating temperature development inside of power semiconductor packages under application conditions, by means of real-time device temperature measurements and/or ET modeling [6]. The main focus of this article is placed on efficient ET modeling of multichip PMs, taking into account temperature-dependent thermal properties of multilayer package structures. This provides a highly valuable input for accurate temperature prediction of SiC power devices operating with higher temperature amplitudes and levels, i.e., $T_{\max} = 200$–225 °C.

In the state-of-the-art literature, ET modeling has been mainly performed using linear and time-invariant thermal models [7]–[14], i.e., neglecting temperature-dependent material properties. Nonlinearity can be taken into account by fully numerical two-way ET modeling using the well-known multiphysics tools, such as COMSOL [15] and ANSYS [16]. However, modeling the device switching losses within such two-way coupled ET modeling environments is not straightforward, and circuit

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simulators implementing temperature-dependent device models are required to calculate switching losses, which are further used as input to determine the temperature of the respective devices. Furthermore, Spice-like circuit simulators specialized for computationally extensive simulations of device switching behavior and handling various Spice models of power semiconductor devices typically provided by device manufacturers are preferred for PE applications.

The thermal time constant of PE converter design with large heat sinks is in the range of seconds so that the device temperature variation under nominal operation is rather small for most PE applications. Neglecting small temperature swings allows the application of iterative approaches for evaluating the steady-state device temperature in operation [17], [18]. On the other hand, estimating the time-dependent temperature of power semiconductor devices has to be performed using fully coupled ET modeling, which, in turn, can be achieved by either simulating PE converter circuits simultaneously with (non)linear thermal models or directly coupling a circuit simulator with a thermal modeling tool. While the former approach is expensive with respect to computational time and memory storage since device temperature is updated in every time step of the circuit simulation, which can be in the range of picoseconds, the weak point of the latter approach is data exchange between two simulators, which can contribute to longer simulation time.

Typically, in the commercial circuit-based ET modeling environments, such as, e.g., ANSYS Icepak-Simplorer [19], only temperature-invariant thermal models can be used. Extracting nonlinear thermal models is not straightforward. A nonlinear thermal model can be imported in the circuit domain in the form of either equivalent Cauer-type networks [20], [21] and Foster-type networks [22] or reduced-order equivalent circuit models [23], [24]. Cauer- and Foster-type networks are obtained typically by performing finite-element method (FEM) simulations or thermal transient measurements at different power levels, while specialized model-order reduction (MOR) techniques as presented in, e.g., [23] are required for extracting reduced-order nonlinear equivalent circuit models. For both methods, the computational cost significantly increases with a higher number of heat sources, i.e., higher number of power semiconductor dies. To avoid thermal modeling requiring insurmountable memory storage and extensive FEM simulations, an ET modeling method considering nonlinear thermal conductivity was proposed in [24], employing the so-called Kirchhoff transformation. Namely, the effect of temperature-dependent thermal conductivity of SiC dies was approximated from an equivalent linear model using a single correction factor derived from a smaller number of steady-state FEM thermal simulations. As tuning the correction factor is based on steady-state FEM simulations, this approach is not suitable for modeling transients of multichip PMs taking into account temperature-dependent thermal conductivities of a multilayer package structure. Consequently, the temperature-dependent thermal properties of packaging materials are commonly neglected in conventional ET simulations based on reduced-order thermal models [12]–[14].

A PSpice-COMSOL-based 3-D ET modeling with a MATLAB script used as an interface link between the PSpice and COMSOL simulations was presented in [25], on an example of an insulated-gate bipolar transistor PM operating under short-circuit conditions. The package material layers below the baseplate, such as thermal interface material (TIM) and heat sink, were not modeled, in order to improve the simulation efficiency. Namely, the circuit-based ET simulations of PMs with large heat sinks are computationally challenging due to few orders of difference between their electrical and thermal time constants. By not modeling the material layers contributing to a larger thermal time constant, such as TIM and heat sink, existing in the actual power converters, the steady-state solution of the ET simulation can be reached at lower computational cost. Furthermore, the computational complexity is increasing by using third software as MATLAB for the interface link between the thermal and circuit simulators, as well as for modeling multichip PMs, which was not addressed in [25].

This article presents a finite-difference-method (FDM)-based thermal modeling tool with a built-in interface link to the LTSpice circuit simulator, allowing computationally feasible circuit-based ET simulations of multichip PMs with temperature-dependent thermal conductivity of package materials. Moreover, the proposed ET modeling approach allows us to control the tradeoff between accuracy and computational cost when simulating fast electrical transients.

In comparison to FEM-based thermal modeling, the FDM uses a structured mesh and leads to an equivalent 3-D RC thermal network. The advantages using the FDM for thermal modeling of PMs are described as well as in [10], [12], [13], [34], and [35]; however, the computational cost when modeling nonlinear thermal systems due to temperature-dependent material properties and the importance of considering temperature-dependent material properties have not been addressed up to now. FDM-based thermal solvers presented in [34] and [35] addressed modeling of temperature-dependent package material properties. The presented modeling approaches require a high-order system matrix to be updated and solved in every simulation step, which significantly slows down the simulation and makes it less attractive for ET simulations. The FDM-based thermal modeling tool developed in-house is, therefore, extended in this article by a new modeling approach, which allows decreasing computational cost of FDM-based thermal modeling with temperature-dependent thermal conductivities.

The rest of this article is organized as follows. In Section II, the effects of temperature-dependent thermal conductivity and specific heat capacity are analyzed on an example of a SiC half-bridge (HB) PM designed in-house. In Section III, the proposed FDM-based thermal modeling approach is presented and compared to COMSOL FEM thermal simulations. In Section IV, fully coupled circuit-based ET simulations of the developed HB SiC PM are performed for different current pulses using a commercial circuit simulator, LTSpice, and the improved FDM thermal tool, showing a higher modeling error when employing constant thermal conductivities. The verification is performed by using infrared (IR) camera measurements and COMSOL FEM-ET simulations for the case of power semiconductor devices operating in the conduction mode. Challenges and perspectives of fully coupled circuit-based ET modeling when both conduction and switching losses have to be taken into account are discussed in Section V. Namely, the advantage of ET simulation based

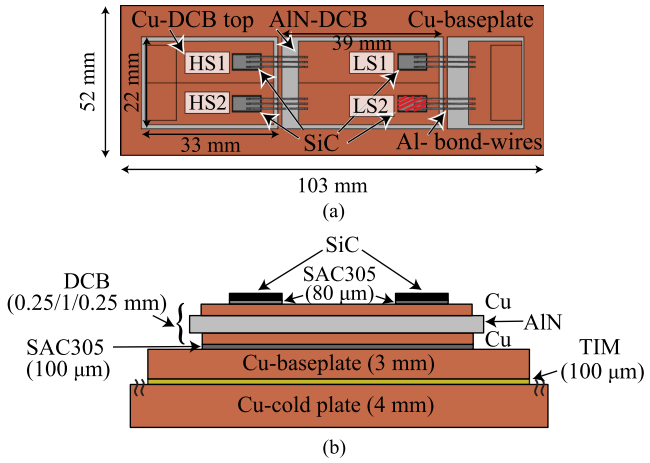

Fig. 2. HB PM used for the analysis of temperature-dependent material thermal properties. (a) Top view. (b) Cross section. The four dies are labeled as high side (HS) and low side (LS).

on an iterative approach over coupling thermal and electrical domains by means of a circuit simulator is demonstrated for a 1.2-kV HB SiC PM employed in a high-frequency (100-kHz) boost converter.

II. Analysis of Temperature-Dependent Material Thermal Properties

In this section, the impact of temperature-dependent thermal conductivity $k(T)$ and specific heat capacity $c_\mathrm{p}(T)$ on the temperature development of SiC power devices is investigated using the structure of an HB PM designed and manufactured in-house [36]. The PM contains four SiC dies [37], soldered with SAC305 on Cu–AlN–Cu direct copper bonded (DCB) substrates [see Fig. 2(a)]. The DCBs are, in turn, soldered to a Cu baseplate, which is thermally connected to the 4-mm-thick Cu cold-plate by the TIM [cf. Fig. 2(b)]. Electrolube silicone heat transfer compound plus (HTSP) thermal paste is used as TIM layer. The package was not optimized for high-temperature operation; therefore, all experiments and simulations performed to validate the proposed modeling approach were designed to keep the junction and solder layer temperature below $T_\mathrm{max} = 210$ °C. In the simulations, the temperature of the cold-plate's bottom surface is set to a constant value, which models the cooling system of the Mentor Graphics Power Tester 1500A used for thermal characterization. As the heat is mainly generated in the channel during the nominal device operation of SiC power MOSFETs, the heat sources are placed at the top surface of the power semiconductor dies. The chip Al metallization and bond wires are neglected in the analysis, since they do not have a significant impact on the dominant heat flow toward the heat sink. Table I presents the analytical formulas used for modeling the temperature-dependent thermal conductivity k and specific heat capacity c_p of the package materials, Cu, SiC, and AlN. Constant thermal properties for the solder (SAC305) ($k = 55$ Wm^{-1}K^{-1}, $c_\mathrm{p} = 218$ J kg^{-1}K^{-1}, and mass density $\rho = 7800$ kg m^{-3}) and TIM layers ($k = 1.09$ W m^{-1}K^{-1}, $c_\mathrm{p} = 1090$ J kg^{-1}K^{-1}, and $\rho = 1470$ kg m^{-3}) are used due to a lack of information about

TABLE I
Analytical Expression of Temperature-Dependent Thermal Properties of Materials of Fig. 1 and Used for the DUT of Fig. 2

Mat.	k and c_p
Cu	$k(T) = 437.6 - 0.165 \cdot T + 1.825 \cdot 10^{-4} \cdot T^2$ $-1.427 \cdot 10^{-7} \cdot T^3 + 3.979 \cdot 10^{-11} \cdot T^4$ $c_\mathrm{p}(T) = 342.8 + 0.134 \cdot T + 5.535 \cdot 10^{-5} \cdot T^2$ $-1.971 \cdot 10^{-7} \cdot T^3 + 1.141 \cdot 10^{-10} \cdot T^4$
SiC	$k(T) = 1/(-0.0003 + 1.05 \cdot 10^{-5} \cdot T)$ $c_\mathrm{p}(T) = 925.7 + 0.377 \cdot T - 7.926 \cdot 10^{-5} \cdot T^2 - 3.195 \cdot 10^{7} \cdot T^{-2}$
AlN	$k(T) = 421.7867 - 1.1262 \cdot T + 0.001 \cdot T^2$ $c_\mathrm{p}(T) = 170.2 - 2.018 \cdot T + 0.032 \cdot T^2$ $-8.957 \cdot 10^{-5} \cdot T^3 + 1.032 \cdot 10^{-7} \cdot T^4 - 4.352 \cdot 10^{-11} \cdot T^5$

the temperature-dependent behavior of these materials. The assumption of die attach layer with a weak temperature dependence of thermal conductivity is typically justified for PMs with silver sinter joints [38] designed for high-temperature operation. Accordingly, the presented analysis based on a die attach layer with a constant thermal conductivity leads to accurate conclusions on the importance of considering nonlinear thermal conductivities of PM's materials for high-temperature applications. In the following analysis, a single device marked in Fig. 2 as LS2 is used as the heat source, without loss of generality. Four simulation types with respect to k and c_p of SiC, Cu, and AlN are performed in COMSOL Multiphysics: (SIM1) both c_p and k temperature dependent, (SIM2) $c_\mathrm{p} = c_\mathrm{p}(T_\mathrm{amb})$ and k temperature dependent, (SIM3) c_p temperature dependent and $k = k(T_\mathrm{amb})$, and (SIM4) $c_\mathrm{p} = c_\mathrm{p}(T_\mathrm{amb})$ and $k = k(T_\mathrm{amb})$, with $T_\mathrm{amb} = 100$ °C. Throughout this article, except when specified, the thermal impedance matrix $\mathbf{Z}_\mathrm{th}$ is calculated from the junction temperatures T_j evaluated as the average temperature at the active area of the dies, which, in turn, corresponds to the temperature evaluated by temperature sensitive electrical parameter (TSEP) measurements [16].

Both self, Z_th11, and mutual thermal impedance, Z_th21, are evaluated for two input power steps of 100 and 200 W, as shown in Fig. 3(a), (b) and (c), (d), respectively.

For both power levels, overlapping thermal impedances are obtained in SIM3 and SIM4, demonstrating a negligible impact of $c_\mathrm{p}(T)$ on the device temperature evaluation in the temperature range up to ≈ 225 °C, i.e., $T_\mathrm{j,max} = 151.5$ °C for $P_\mathrm{heat} = 100$ W [cf. Fig. 3(a)] and $T_\mathrm{jmax} = 207$ °C for $P_\mathrm{heat} = 200$ W [cf. Fig. 3(c)]. The matching between self-impedances evaluated in SIM1 and SIM2 furthermore confirms that the temperature dependence of the heat capacity of SiC can be neglected in the temperature range up to ≈ 225 °C. It is worth mentioning that for fast and large temperature changes, i.e., $\Delta T > 800$ K in few microseconds, also $c_\mathrm{p}(T)$ plays an important role as demonstrated for short-circuit operation of a SiC power MOSFET in [39]. The modeling error made by neglecting $k(T)$ is still acceptable for a lower input power of $P_\mathrm{heat} = 100$ W, where the absolute difference for Z_th11 is only 0.02 K/W and a junction temperature difference of $\Delta T_\mathrm{j,max} = 2$ °C, i.e., 1.3%, whereas for $P_\mathrm{heat} = 200$ W, Z_th11 is underestimated by 0.04 K/W leading to $\Delta T_\mathrm{j,max} = 8$ °C, i.e., $\approx 3.9\%$. The mutual impedance

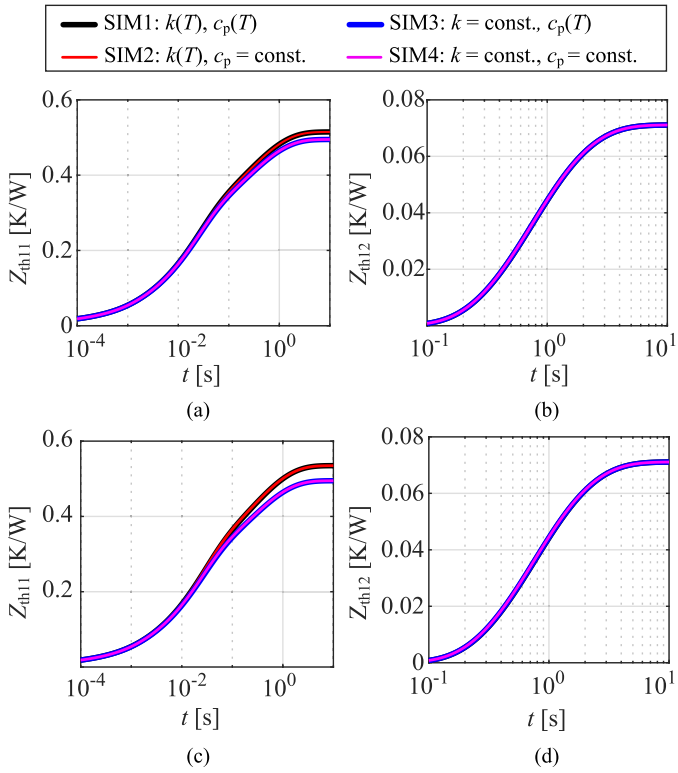

Fig. 3. Power step response of the LS2 die soldered in the HB PM shown in Fig. 2 for four different sets of material properties: (SIM1) temperature dependent $k(T)$ and $c_\mathrm{p}(T)$, (SIM2) $k(T)$ and c_p = const., (SIM3) $c_\mathrm{p}(T)$ and k = const., and (SIM4) k = const. and c_p = const. (a) Self-impedance $Z_{\mathrm{th}11}$ for $P_\mathrm{heat} = 100\,\mathrm{W}$. (b) Mutual impedance $Z_{\mathrm{th}21}$ for $P_\mathrm{heat} = 100\,\mathrm{W}$. (c) $Z_{\mathrm{th}11}$ for $P_\mathrm{heat} = 200\,\mathrm{W}$. (d) $Z_{\mathrm{th}21}$ for $P_\mathrm{heat} = 200\,\mathrm{W}$.

$Z_{\mathrm{th}21}$ is not influenced by the temperature dependence of material properties [cf. Fig. 3(b) and (d)], as the thermal coupling between the two dies is mainly determined by the heat path via the top Cu layer of the DBC substrate with almost constant thermal properties (cf. Fig. 1).

III. Proposed FDM-Based Thermal Modeling Tool

In this section, an FDM tool developed in-house [40] is further improved in order to model the temperature dependence of thermal conductivity in a computationally more efficient way and, hence, to alleviate the coupling between the electrical and thermal domains. This allows temperature profiles of power devices carrying variable currents to be estimated more accurately.

A. Modeling Method Implementation

An FDM thermal model describes the 3-D geometry in the form of a 3-D equivalent electrical network. Each element of the structured mesh is associated with an mth FDM node, with a thermal capacitor $C_{\mathrm{th},m}$ connected to the ground node, representing the heat storage, and thermal resistors $R_{\mathrm{th},mk}$ connected to the neighbor kth node, modeling thermal conduction paths in a Cartesian coordinate system. The values $C_{\mathrm{th},m}$ and $R_{\mathrm{th},mk}$ are determined based on the elemental cell geometry and material properties [41]. Then, the equivalent network can be expressed in a matrix form described by

$$\mathbf{G}_\mathrm{th} \cdot T(t) + \mathbf{C}_\mathrm{th} \cdot \frac{dT}{dt} = Q(t) \tag{1}$$

where $\mathbf{G}_\mathrm{th}$ is the symmetric conductance matrix containing the information about $R_{\mathrm{th},ij}$, $\mathbf{C}_\mathrm{th}$ is the diagonal capacitance matrix, $Q(t)$ is the input vector modeling heat sources in the time domain, and $T(t)$ is the temperature vector representing the unknown temperature distribution to be calculated. The system of linear equations (SLE) given by (1) of order n, where n is the number of nodes, is solved in the developed FDM-based thermal tool using the Gear–Schichman integration method [42], which leads to (2a)

$$\left(\mathbf{G}_\mathrm{th} + \frac{3}{2} \cdot \frac{\mathbf{C}_\mathrm{th}}{\Delta t}\right) \cdot T^i = Q^i + \frac{\mathbf{C}_\mathrm{th}}{\Delta t} \cdot 2 \cdot T^{i-1} - \frac{1}{2} \cdot T^{i-2} \tag{2a}$$

$$\mathbf{S}_\mathrm{th} \cdot T^i = \hat{Q}^i \tag{2b}$$

where the superscript indicates the ith time step and Δt is a discretization time step. The matrix on the left-hand side of eq:GearSchichman is the so-called system matrix $\mathbf{S}_\mathrm{th}$, whereas the right-hand side is denoted as a modified input vector $\hat{Q}^i$, thus leading to (2b). As $\mathbf{G}_\mathrm{th}$ is symmetric and very sparse and $\mathbf{C}_\mathrm{th}$ is a diagonal matrix, the matrix $\mathbf{S}_\mathrm{th}$ is a sparse matrix; hence, it can be efficiently reduced with a MOR approach. Considering that the discretization of PM geometries can lead to a very high number of nodes n, typically $n > 10^4$, a reduction of system complexity is highly recommended to speed up the calculation time at each time step. The MOR technique used in this article is the passive reduced-order interconnect macromodeling algorithm (PRIMA) [43], which guarantees a very accurate reduced model of an RLC network. Applying the MOR transformation to (2b) leads to a reduced system defined by

$$\mathbf{S}_\mathrm{thRed} \cdot T^i_\mathrm{Red} = \hat{Q}^i_\mathrm{Red}. \tag{3}$$

The size of the new reduced-order system matrix $\mathbf{S}_\mathrm{thRed}$ is $n_\mathrm{red} \times n_\mathrm{red}$, where $n_\mathrm{red} \ll n$. The reduced size n_red and accuracy is controlled by an expansion-order parameter, i.e., a high expansion order leads to a more accurate model with a higher number of nodes. The selection of a suitable expansion order strongly depends on the number of ports. The node temperature vector T^i_Red is then calculated using a direct solver based on the lower–upper decomposition.

In order to include the temperature dependence of the thermal conductivity k, the conductance matrix $\mathbf{G}_\mathrm{th}$ containing the information about $k(T^i)$ and, hence, the system matrix $\mathbf{S}_\mathrm{th}$ have to be updated in each simulation step [34], which complicates the implementation of MOR techniques for nonlinear systems. A modeling approach named step-back correction (SBC) is proposed in this article with the aim to avoid a recalculation of $\mathbf{S}_\mathrm{th}$ in each time step and make an FDM thermal simulation with temperature-dependent thermal conductivity computationally more efficient. The idea of the SBC method is that the modeling error made when using a temperature-independent conductivity is corrected retroactively in the next time step, which is realized by a correction term introduced in the modified right-hand-side

Procedure: Step-Back-Correction Algorithm
1 **Input calculated at** t_0**:** $\mathbf{G}_{\mathrm{th}}^{\mathrm{Tid}}$, $\mathbf{C}_{\mathrm{th}}$, $\mathbf{S}_{\mathrm{thRed}}$, $Q(t)$
2 Initialize $T_{\mathrm{Red}}^{0} = T_{\mathrm{init}}$, $T^{0} = T_{\mathrm{init}}$
3 Solve SLE (3) for T_{Red}^{1}
4 **for** $i = 1 : N_{\mathrm{t}}$
5 Reconstruct temperature vector T^{i} from T_{Red}^{i}
6 Update thermal conductivities of nodes $k(T^{i})$
7 Update G-matrix $\rightarrow \mathbf{G}_{\mathrm{th}}^{\mathrm{Td}}$
8 Calculate $\hat{Q}^{i+1}$ (2a) using $\mathbf{C}_{\mathrm{th}}$, Δt and T^{i}
9 Construct the corrected RHS:
10 $\hat{Q}_{\mathrm{mod}}^{i+1} = \hat{Q}^{i+1} + (\mathbf{G}_{\mathrm{th}}^{\mathrm{Td}} - \mathbf{G}_{\mathrm{th}}^{\mathrm{Tid}}) \cdot T^{i}$
11 Apply MOR $\hat{Q}_{\mathrm{mod}}^{i+1} \rightarrow \hat{Q}_{\mathrm{cRed}}^{i+1}$
12 Calculate T_{Red}^{i+1} from (3) with $\hat{Q}_{\mathrm{cRed}}^{i+1}$ and $\mathbf{S}_{\mathrm{thRed}}$
13 **end**

Fig. 4. Procedure of the proposed SBC method.

input vector. In this way, $\mathbf{S}_{\mathrm{th}}$ is calculated only once at the beginning of the simulation. The reduced SLE (3) at the $(i+1)$th time step, t_{i+1}, is modified according to the procedure described in Fig. 4. The two introduced matrices $\mathbf{G}_{\mathrm{th}}^{\mathrm{Tid}}$ and $\mathbf{G}_{\mathrm{th}}^{\mathrm{Td}}$ are the temperature-independent and temperature-dependent thermal conductance matrix, respectively. While $\mathbf{G}_{\mathrm{th}}^{\mathrm{Tid}}$ is defined once during the model initialization and then used to fill out $\mathbf{S}_{\mathrm{th}}$, $\mathbf{G}_{\mathrm{th}}^{\mathrm{Td}}$ is constructed in each time step based on the actual $k(T^{i})$. In line 5 of Fig. 4, a reverse MOR transformation is applied to evaluate the original temperature vector, which is multiplied by the difference $(\mathbf{G}_{\mathrm{th}}^{\mathrm{Tid}} - \mathbf{G}_{\mathrm{th}}^{\mathrm{Td}})$, as specified in line 10, in order to calculate the correction term. This step is necessary, as a direct link between the physical nodes and the reduced model does not exist. The correction term is combined with the updated input vector, and applying a MOR transformation to the right-hand-side expression, as given by line 11, leads to a corrected reduced input vector $\hat{Q}_{\mathrm{cRed}}^{i+1}$. The modified SLE is then solved for the unknown vector T_{Red}^{i+1}, containing the information about the temperature of the selected nodes, i.e., ports. Here, it should be pointed out that the SBC method requires a reconstruction of the temperature vector in each time step, instead of the reconstruction of the whole system matrix. Accordingly, the additional computational cost of FDM-SBC is mainly determined by the calculation of $\mathbf{G}_{\mathrm{th}}^{\mathrm{Td}}$ and the correction term. However, in each time step, not only the average temperature across the active die area but also the temperature of all FDM nodes can be calculated. Accordingly, the temperature distribution of the whole package defined by mesh nodes can be extracted.

B. Thermal Modeling Verification

In this section, the accuracy of the developed FDM-SBC method is verified with COMSOL Multiphysics, i.e., a well-known FEM-based modeling tool, on the example of the HB PM shown in Fig. 2. Five ports, i.e., four for the junction temperatures and one for the boundary to the ambient, are defined in the model. The thermal conductivities of die attach and DCB solder layers are properly calibrated to match T_{j} obtained from IR camera measurements [36]. The bottom boundary temperature is fixed to 100 °C.

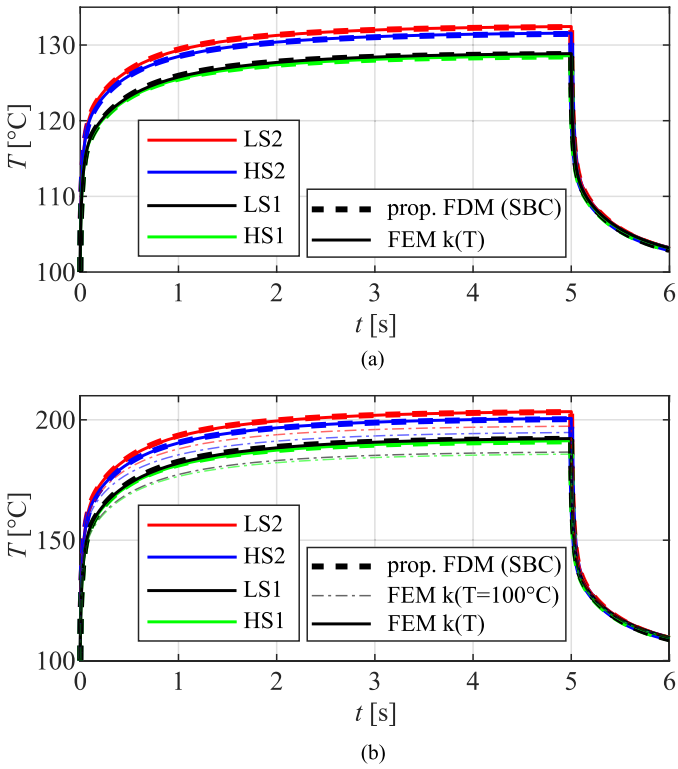

Fig. 5. Comparison of the proposed FDM-SBC approach with a commercial FEM tool, power pulse response of the HB PM (see Fig. 2) for (a) 50 W and (b) 150 W applied to the four dies. In (b), the response for $k(T = 100\ °\mathrm{C})$ is shown for comparison.

In the proposed FDM tool, the geometry is discretized in ≈37 500 nodes and a PRIMA-MOR of order 12 is selected to simulate the temperature response to a power pulse P_{in}. A mesh with ≈ 35 000 elements is used for the COMSOL simulations. Two temperature responses are evaluated for input power $P_{\mathrm{in}} = 50\,\mathrm{W}$ and $P_{\mathrm{in}} = 150\,\mathrm{W}$ applied for 5 s to the four dies, as shown in Fig. 5.

The comparison between the simulation results demonstrates good matching between the COMSOL FEM-based and the proposed FDM-based thermal model. The relative error between the two modeling approaches is below 0.5% for the entire transient simulation of the virtual junction temperature, which is mainly ascribed to the different meshing and modeling approaches. Namely, the maximum difference between the two approaches is 0.1 K for 50 W and 0.3 K for 150 W. In order to quantify the relevance of $k(T)$ for this specific test case, the temperature responses of all four dies are evaluated assuming constant $k(T = 100\ °\mathrm{C})$, as shown in Fig. 5(b), i.e., T_{j} of LS2 die is underestimated by 6.1 K.

The simulations are performed on a machine with eight cores of an Intel(R) Xeon(R) Gold 6254 processor, 3.10 GHz, 96-GB RAM. In the proposed FDM-SBC-based modeling, the simulation time depends on the number of time steps, as shown in Table II.

Large time steps lead to inaccuracies during fast transients; however, the steady-state temperature is not affected, as shown in Fig. 6.

TABLE II
SIMULATION TIMES OF THE PROPOSED FDM-SBC APPROACH (MODEL WITH 37 500 FDM NODES) FOR DIFFERENT TIME STEPS

Steps no.	5001	2501	1501	501	51
$\Delta \mathbf{t}_{\mathrm{th}}$	1 ms	2 ms	3.33 ms	10 ms	0.1 s
Sim. time	9 h 40 min	2 h 20 min	58 min	15 min	5.5 min

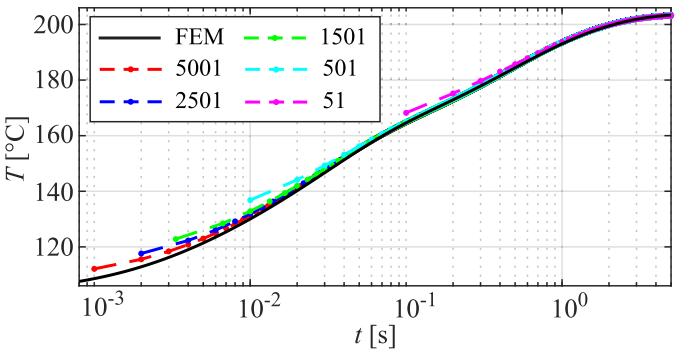

Fig. 6. Impact of the number of time steps (see Table II) on the temperature profile of LS2 simulated with the proposed FDM-SBC approach for $P_{\mathrm{in}} = 150\,\mathrm{W}$ applied to the four devices. The nonlinear FEM simulation from COMSOL is shown as reference.

This proves that the error of the steady-state solution does not increase with larger time steps, when using the proposed FDM-SBC approach, and furthermore, it allows controlling the tradeoff between the simulation time and accuracy, which is highly important for ET simulations of power converters, i.e., the average device temperature during a longer electrical transient is rather of interest. Namely, the selection of a proper thermal time step is crucial to ensure a steady-state solution in a reasonable time, especially when the thermal tool is coupled with a circuit simulator.

Similarly, the number of FDM nodes n impacts the simulation time, as the SBC requires in each time step to reconstruct T^i, to update $\mathbf{G}_{\mathrm{th}}^{\mathrm{Td}}$, and to apply the MOR to the corrected RHS vector. The simulation time for 5001 time steps and the meshes of 28 400 and 47 700 elements is 4 h 20 min and 17 h 20 min, respectively. However, with an optimized structured mesh of a multichip PM, the high number of FDM nodes is not necessary to achieve an accurate solution, i.e., the number of $\approx$ 37 500 elements used in Fig. 5 can be further reduced. An implementation of an automated optimized structured meshing in the developed FDM thermal tool will be addressed in the course of future work. It should be noted that the FDM simulation with temperature-dependent thermal conductivities based on the proposed SBC approach is ≈ 5 times slower than the FDM simulation with temperature-invariant thermal conductivities. However, this increase in calculation time is necessary to obtain an accurate thermal model. With the aim to validate the effectiveness of the SBC approach, the same simulation is performed in the FDM thermal tool by updating the system matrix $\mathbf{S}_{\mathrm{th}}$ in each time step using the corresponding time-changing thermal conductivity $k(T^i)$. The simulation time lasted more than 48 h on the same machine for 37 500 mesh nodes and 5001 time steps. Updating $\mathbf{S}_{\mathrm{th}}$ in each time step prohibits using the MOR approach, as the MOR preprocessing would have to be performed in each time step, which would lead to an even longer simulation time.

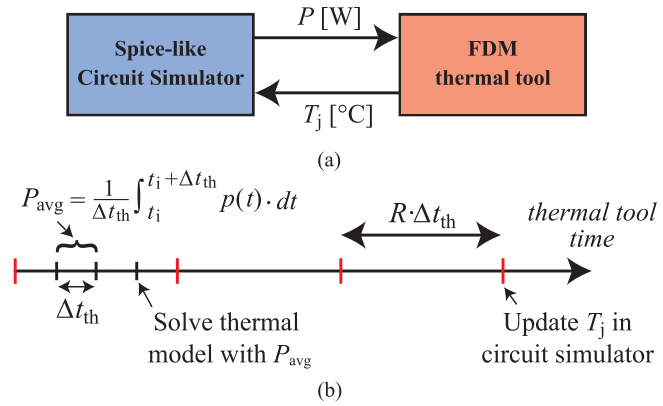

Fig. 7. Coupling of the proposed FDM thermal tool with a commercial circuit simulator. (a) Data transfer between the tools. (b) Example of time steps for the proposed FDM thermal tool; T_{j} is updated in the circuit netlist every $R \cdot \Delta t_{\mathrm{th}}$.

The simulation time in COMSOL on the same machine for a nonlinear model with 38 139 domain elements and 2501 time steps is 3 h 20 min, when using a fixed time-stepping algorithm defined in the same way as in the FDM simulation. It should be noted that COMSOL implements adaptive time-stepping strategies, with time steps automatically determined during the simulation to satisfy a desired error tolerance, which can improve the simulation time. The output values at the time points defined by the user are then calculated by interpolation. For the loads abruptly changing in time as it is the case of a power pulse experiment, the so-called *events interface* have to be used in COMSOL to accurately calculate the temperature response. Accordingly, explicit time events corresponding to fast transitions in the input have to be set at the beginning of a COMSOL simulation so that the algorithm selects fine enough time steps around the transition points. A similar modeling approach is to be implemented in the developed FDM thermal model in the course of its further development.

IV. PROPOSED FDM-THERMAL-TOOL-LTSPICE ET MODELING APPROACH

This section presents an ET modeling based on coupling a circuit simulator and the developed FDM thermal tool, which allows the time step in the thermal domain Δt_{th} to be selected independently from the time step in the circuit domain Δt_{el}. LTSpice is selected as a free commercial circuit simulator. The coupling is accomplished in an automatized way by updating an LTSpice netlist with the latest junction temperature calculated in the FDM thermal tool and by providing the average dissipated power, calculated from the LTSpice simulation during a thermal time step, to the FDM thermal tool, as shown in Fig. 7(a). As the device temperature is represented as a single parameter in the circuit domain, the average junction temperature is used as an output parameter T_{j} from the thermal simulation (cf. Fig. 7). Considering the junction temperature as the maximum temperature at the top of the die would result in an overestimation of the temperature for most of the active region of a power device. The

average temperature T_{avg} is calculated by means of a boundary surface port, with a cross-sectional area equal to the die active area, which selects the corresponding surface FDM nodes. In circuit-based ET simulations, only this single temperature value T_{avg} is forwarded to the circuit simulator, and hence, it is directly available, while the temperature distribution defined by the other FDM nodes can be extracted in a postprocessing step.

Δt_{el} is defined in LTspice with an adaptive time-stepping algorithm, i.e., Δt_{el} varies according to the electrical dynamic. An integer parameter R is introduced to define how frequently the device junction temperatures are updated in LTSpice. Namely, each LTSpice simulation is run with fixed device temperatures for $t_{\mathrm{el,sim}} = R \cdot \Delta t_{\mathrm{th}}$ [see Fig. 7(b)]. The R parameter further decouples the circuit and thermal domains, which is beneficial in the cases when a small Δt_{th} is needed to sample the exact temperature profiles, but the temperature change is negligible for the device electrical behavior, which is shown in more detail in Section V. The simulation time period t_{end}, the thermal time step Δt_{th}, and the parameter R are defined by the user at the beginning of an ET coupled simulation.

A. *Verification by COMSOL ET Modeling: Conduction Mode*

The accuracy of the proposed ET-FDM modeling approach is first verified with a fully coupled COMSOL ET-FEM simulation of the HB PM shown in Fig. 2 and IR camera measurements. In this example, dc power losses, i.e., the conduction losses, are the dominant heat source. The ON-state resistances $R_{\mathrm{ds,ON}}(T)$ of four SiC MOSFET dies were first characterized in the wide temperature range [25 °C, 225 °C] using a wafer prober MPI TS2000-HP and a Keithley curve tracer 2600-PCT-4B. The current- and temperature-dependent $R_{\mathrm{ds,ON}}$ behavior implemented in the LTSpice compact device model provided by the manufacturer was modified to consider the measured $R_{\mathrm{ds,ON}}(T)$ variability between four SiC power MOSFET dies soldered in the PM. Polynomial curve fitting was used to analytically model $R_{\mathrm{ds,ON}}(T,\ I)$ characteristics in COMSOL in the considered temperature and current ranges. As the temperature (T) dependence is much stronger, a polynomial expression of fourth order is used for temperature dependence and the current (I) dependence is modeled by a first-order polynomial function. The thermal conductivity of solder layers was adjusted according to X-ray inspection of the solder voids formed during the soldering process and the IR camera measurements, which is explained in more detail in [36]. The IR measurements were performed with a FLIR A655sc camera using a spatial resolution of 0.14 mm and a maximum available image frequency of 200 Hz. The IR measurements were verified by comparison with the virtual junction temperature T_{vj} measured via a TSEP [36]. In the simulations, each of two DCB solder layers was separated in two regions, as shown in Fig. 2(a), resulting in a total of eight modeling regions for the die attaches and baseplate solder layer.

The ET modeling in COMSOL is based on the multiphysics coupling of the partial differential equations for heat conduction and electrical currents, i.e., Joule heating [15]. Namely, in comparison to the proposed ET-FDM modeling with heat sources uniformly located in the active die area, for the fully coupled ET-FEM modeling, the heat sources are distributed in general in all elementary volumes with current conduction. Another substantial difference between the two approaches is a higher mesh density in COMSOL since the electric current spreading requires a finer mesh than the heat equation, thus leading to a much more computational expensive model. Accordingly, for the comparison between the proposed ET modeling approach and the ET COMSOL modeling, the temperature- and current-dependent electrical conductivity $\sigma_{\mathrm{el}}(T, I_{\mathrm{DS}})$ of four individual SiC MOSFETs was calibrated to match $R_{\mathrm{ds,ON}}(T, I_{\mathrm{DS}})$ implemented in LTSpice and then assigned on the top surface boundary of the SiC dies. A 4-μm-thick aluminum layer representing the top metalization was implemented in the COMSOL model to enable the current spreading from the bond wires to the entire MOSFET's active area. The same thermal material properties were used in both modeling tools.

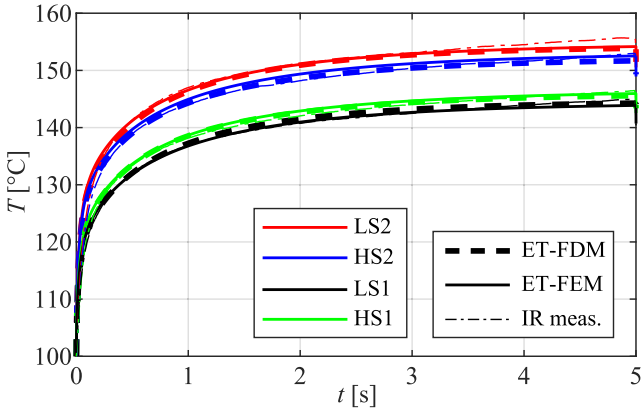

Fig. 8. HB PM temperature response to a current pulse of 57.8 A. Comparison between the proposed ET-FDM approach, the ET-FEM model, and IR measurements.

The temperature responses calculated by the proposed ET-FDM model, the ET COMSOL model, and the IR measurements for a total heating current of 57.8 A applied for 5 s are presented in Fig. 8. The maximum difference between the proposed ET-FDM-LTSpice simulations and COMSOL is 0.85 K, while the maximum difference to the IR camera measurements is 1.4 K at $t = 5$ s. Namely, the IR-temperatures shows a temperature increase after 5 s, which can be explained by a nonideal silicone oil cooling system of the measurement equipment [36], neglected in the simulations. This effect is even more pronounced at higher temperatures, i.e., higher load currents, and hence, a more detailed thermal model should be implemented in both COMSOL and the proposed FDM tool to represent the actual behavior of the measurement system with a higher accuracy, which was not in the focus of this article. The two ET models give close results also for a higher current pulse of 69.8 A, where the nonlinearity of the thermal package model becomes relevant. A maximum temperature difference of 1.48 K is found for the entire transient [cf. Fig. 9(a)], while the simulated current sharing between SiC power MOSFETs is shown in Fig. 9(b). The small relative difference $\epsilon < 1\%$ between the temperature simulation results with the proposed FDM-LTspice tool and COMSOL can be further explained by the intrinsic modeling differences of the two modeling approaches. The simulation time required to obtain the results shown in Fig. 9 using the

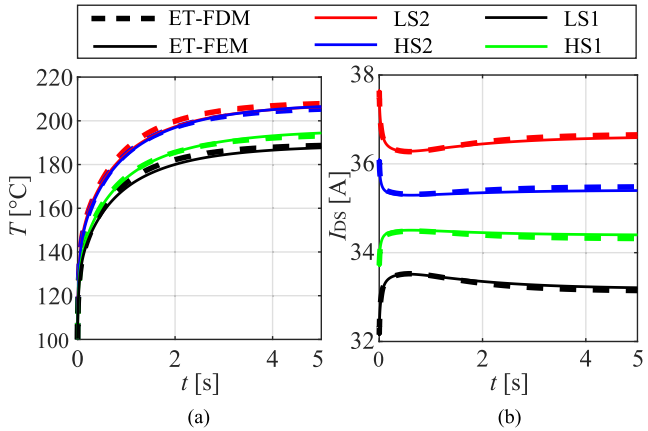

Fig. 9. ET simulation of the HB PM for a current pulse of 69.8 A. Comparison between the proposed ET-FDM approach and the ET-FEM model. (a) Temperature and (b) current profiles.

FDM-LTSPice tool is 2.5 h with a thermal time step of 2.5 ms, updating the LTSpice circuit simulation with a new temperature input after $R = 4$ time steps in the thermal simulation.

V. Circuit-Based ET Modeling With Switching Losses

A large difference between the electrical time constants $\tau_{\rm el}$ in the range of nanoseconds and thermal time constants $\tau_{\rm th}$ from milliseconds to seconds of PE systems [13], [21], [41], [44] makes the numerical coupling between electrical and thermal aspects more challenging in terms of computational efficiency. In addition, including ac power losses, i.e., the switching losses, in a fully numerical ET simulation is not straightforward, as the switching losses depend on both device and circuit and, hence, have to be calculated externally.

When considering fast switching transients, both direct simulations via equivalent thermal networks characterized by a common electrical and thermal time step, and the ET simulations with decoupling $\Delta t_{\rm el}$ and $\Delta t_{\rm th}$ lead to computationally cumbersome simulations. Accordingly, for the design optimization of PE converters, an iterative approach is preferable to evaluate the junction temperature of power devices in steady-state operation. In an iterative approach, a PE circuit is simulated for a longer time period in order to ensure steady-state system behavior, using fixed junction temperatures of power devices. The steady-state power losses are then calculated and used in the thermal simulation to find the next set of device junction temperatures to be used in the following circuit simulation. This iterative procedure is repeated until the difference between the temperature values in subsequent iterations is smaller than a specified relative error tolerance. The iterative modeling approach is, on the other hand, only accurate if the device temperature oscillations in the steady-state system operation are small, so that temperature-dependent parameters in both the thermal and electrical domains can be treated as constant. It should be noted that even the iterative procedure is frequently skipped in the design optimization of power converters [18], [34], [45].

An example of a 100-kHz synchronous boost converter shown in Fig. 10 is used to evaluate the aforementioned challenges

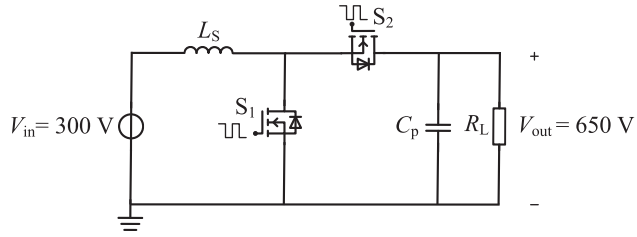

Fig. 10. Circuit schematic of the simulated 100-kHz synchronous boost converter with the output power $P_{\rm out} = 13.5$ kW, the dead time $t_{\rm dead} = 200$ ns, input voltage $V_{\rm in} = 300$ V, and output voltage $V_{\rm in} = 650$ V. S1 and S2 are 1.2-kV 40-mΩ SiC MOSFETs.

of ET modeling and to show the importance of taking into account temperature dependence of thermal conductivity of package materials when estimating the junction temperature of SiC power MOSFETs during a fast switching operation. The analysis is performed by comparing an iterative procedure, an ET simulation using ANSYS Electronics Desktop (EDT), and the proposed FDM-LTspice ET approach. The 1.2-kV HB PM design presented in [46] housing a single die per HS/LS switch is used in the boost converter. For the purpose of evaluating temperature dependence of package material properties, AlN ceramic (cf. Fig. 1) was used for the DCB substrate in the ET simulations. The switches S1 and S2 are modeled as two 1.2-kV SiC power MOSFETs [47]. Switch S1 operates with a duty cycle of 0.542. The behavioral LTSpice device models provided by the vendor and the thermal model of the HB PM are used for the ET modeling of the boost converter. The accuracy of ET simulations depends on both compact (Spice-) device models and thermal models. However, the development and/or verification of temperature-dependent Spice models developed by device manufacturers was not in the scope of this article. Therefore, the proposed FDM thermal tool-LTSpice modeling approach was verified by the ANSYS EDT simulations using the same Spice models in both environments.

A. Direct ET Modeling

As ANSYS EDT can only handle temperature-invariant thermal models, the ET analysis of the boost converter was performed in the proposed FDM thermal tool-LTSpice modeling environment and ANSYS EDT with constant material thermal properties.

1) ET Modeling $\tau_{\rm el} = \tau_{\rm th}$: ET modeling in the ANSYS EDT employs two simulation environments: a circuit simulator, Simplorer, and a thermal modeling tool, Icepak. A thermal model of the HB PM is first developed in Icepak, leading to the extraction of the thermal matrix, $\mathbf{Z}_{\rm ths} = [Z_{\rm ths,11}, Z_{\rm ths,12}; Z_{\rm ths,21}, Z_{\rm ths,22}]$, representing thermal responses of SiC power MOSFETs S1 and S2 to a power step pulse [48]. The ambient temperature and the initial temperature of all package layers are set to $T_1 = 80$ °C. The temperature T_1 was also used to calculate the package thermal material properties. In the next step, a linear temperature-invariant reduced-order model (ROM) of the package is built using the ANSYS EDT and imported in the ANSYS Simplorer. However, this modeling technique does

TABLE III
DEFINITIONS OF THERMAL TIME STEPS IN THE PROPOSED FDM THERMAL TOOL LTSPICE COUPLED SIMULATIONS

Sim. no.	Δt_{th}	R	SIM. time
ET-SIM1	0.67 μs ($T_{\mathrm{sw}}/15$)	15	5h20min
ET-SIM2	10 μs (T_{sw})	1	2.5h
ET-SIM3	1.25 ms ($125\,T_{\mathrm{sw}}$)	1	4min50s
ET-SIM4	0.67 μs ($T_{\mathrm{sw}}/15$)	60	40min
ET-SIM5	0.67 μs ($T_{\mathrm{sw}}/15$)	7500	22min

not allow to model temperature-dependent material properties and to keep a direct link between the extracted thermal ROM and all physical features of the 3-D package thermal model in ANSYS Icepak. Therefore, a change in the PM structure requires a re-extraction of the thermal ROM, which makes this modeling approach less attractive for a converter design process. In the ANSYS Simplorer, the thermal model is solved in each simulation time step; therefore, the simulated temperature response corresponds to the instantaneous power dissipation.

In the HB PM example, the TIM layer contributes to a thermal time constant of several seconds so that reaching the steady-state temperature in the ET simulations was not feasible with the available resources in terms of memory. Therefore, the ET simulation in the ANSYS Simplorer was performed for the initial $t_{\mathrm{end}} = 5$ ms of the boost converter operation (cf. Fig. 11), and the total simulation time was 26 min. Neglecting the effects of the actual cooling system and low thermally conductive interface layers has been exploited in the literature [25], [49] to avoid long transients in ET simulations. Performing thermal simulations in every time step of the electrical domain is not required in practice, since the temperature change during a time step in the circuit domain can be regarded as negligible. Instead, the overall average temperature change during a longer electrical transient is rather of interest for PE applications. Accordingly, the number of thermal simulations should be kept as small as possible in order to speed up the ET simulations, which is shown in more detail on the example of ET simulations using the proposed FDM thermal tool-LTspice coupled modeling environment.

2) ET Modeling $\tau_{\mathrm{el}} \neq \tau_{\mathrm{th}}$: In the proposed FDM thermal tool-LTSpice modeling environment, thermal simulation was performed using the PRIMA-MOR of order eight. The boost converter was simulated starting from T_1. The ET simulations were performed for $t_{\mathrm{end}} = 5$ ms and different sets of thermal time steps Δt_{th} and parameter R, as summarized in Table III and shown in Fig. 11(a). Each LTSpice simulation is run with fixed device temperatures for $t_{\mathrm{el,sim1}} = R \cdot \Delta t_{\mathrm{th}}$. The effect of the instantaneous power dissipation on the junction temperature is observed in ET-SIM1 performing 15 thermal steps in a switching cycle of 10 μs, i.e., $\Delta t_{\mathrm{th}} = 0.67$ μs, and updating the device temperature in LTSpice simulation once per switching cycle ($R = 15$). The results are comparable with the ANSYS modeling approach, as shown in Fig. 11(b). The temperature difference between the ANSYS ET simulation and the proposed coupled ET simulation ET-SIM1 is less than 1 °C, i.e., $< 1.25\%$, which can be mainly explained by the differences of thermal models and the mesh.

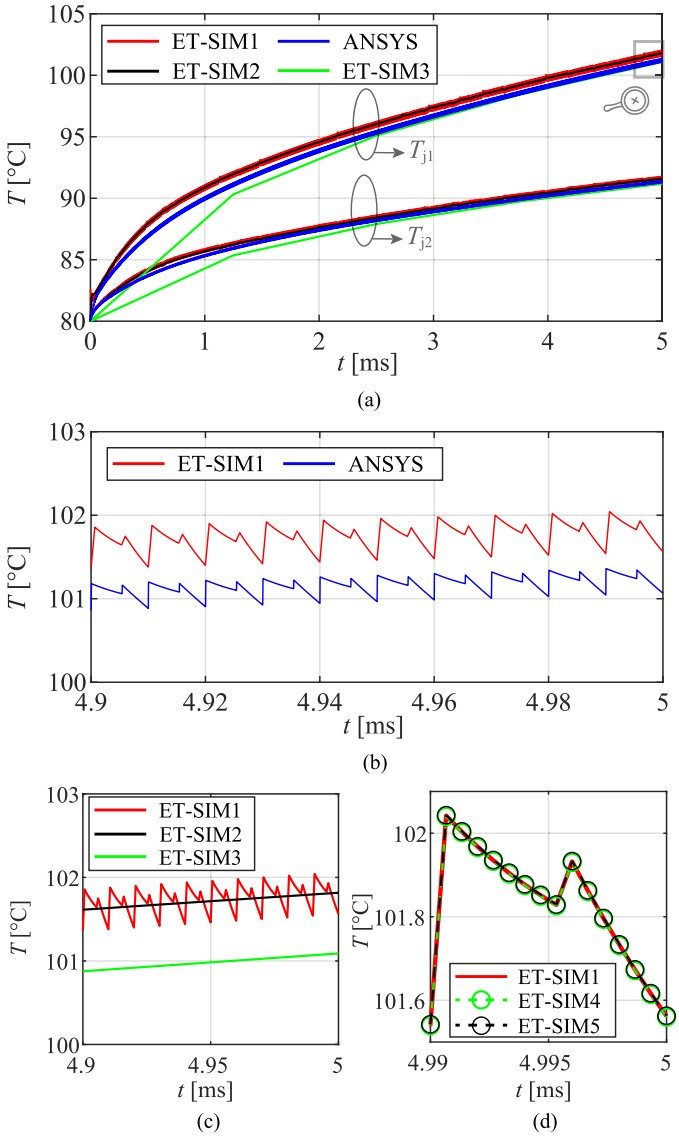

Fig. 11. Simulation results for the junction temperatures of S1 and S2 switches in the 100-kHz synchronous boost converter. (a) Temperature profiles obtained by the ET modeling using the ANSYS EDT and the proposed modeling approach based on FDM thermal tool-LTSpice coupling. Comparison between (a) ET-SIM1–3 and ANSYS for the first 500 switching periods (5 ms); (b) ET-SIM1 and ANSYS and (c) ET-SIM1, ET-SIM2, and ET-SIM3 for the last ten switching periods (100 μs); and (d) ET-SIM1, ET-SIM4, and ET-SIM5 for the last switching period (10 μs). The simulations settings in the FDM-LTSpice modeling approach of ET-SIM1–5 are described in Table III.

A longer Δt_{th} implies that power losses used as the input for each thermal simulation step are calculated by averaging instantaneous power losses over a longer time interval. In Fig. 11(c), the simulation results of ET-SIM 1–3 are compared for the last ten switching periods. This comparison demonstrates the impact of averaging power dissipation during a single switching cycle (ET-SIM2) and 125 switching cycles (ET-SIM3), which corresponds to $R = 1$ and $\Delta t_{\mathrm{th}} = 10$ μs and 1.25 ms, respectively. As shown in Fig. 11(c), the information about fast temperature oscillations is lost for a longer Δt_{th} and the modeling error slightly increases. The simulation times presented in Table III point out, however, that the computational

cost decreases significantly by increasing $\Delta t_{\rm th}$. The temperature swing within a switching period of the simulated boost converter is very low, i.e., < 1 °C. Accordingly, if this small temperature dynamics is not of interest for the design of the power converter, the computation time of ET analysis can be decreased from several hours to ≈ 5 min by using a longer $\Delta t_{\rm th}$ equal to 125 switching cycles, i.e., $\Delta t_{\rm th} = 1.25$ ms.

Another way to reduce the computation time is to run the LTSpice simulation after performing R thermal time steps in the FDM thermal tool. The ET simulations, ET-SIM4 and ET-SIM5, were performed with $\Delta t_{\rm th} = 250$ μs, and $R = 60$ and $R = 7500$, respectively. In Fig. 11(d), an almost perfect matching between the simulation results of ET-SIM1, ET-SIM4, and ET-SIM5 points out that even running only the LTSpice simulation once during 5 ms is acceptable for evaluating the average junction temperature for the first 5 ms. Namely, the change of the converter's electrical behavior in the temperature range 80–102 °C does not affect significantly the temperature response.

The coupling between LTSpice and the FDM tool contributes significantly to a longer simulation time. Particularly, the computational cost of coupling is mainly determined by data exchange between the simulators and slow circuit simulations of mission profiles containing a large number of fast switching transients. LTSpice as a Spice-based simulator allows modeling device switching behavior more accurately than the circuit simulators dedicated to PE applications. A less computationally expensive interface link between the two simulators is needed to further improve the coupling. Accordingly, for the design of power converters, the simplifications of device models can be adopted, controlling the tradeoff between the accuracy and simulation time more precisely. The presented analysis shows the capabilities of the proposed FDM-LTspice modeling, while also indicating the main challenges of efficiently coupling the circuit and thermal domains.

B. Iterative ET Modeling Approach

As the steady-state device temperatures $T_{\rm j1,ss}$ and $T_{\rm j2,ss}$ could not be calculated in practice by the fully coupled ET simulations described in the previous section, an iterative approach was employed to find $T_{\rm j1,ss}$ and $T_{\rm j2,ss}$ taking into account the temperature-dependent thermal parameters of package and device materials. The electrical simulation in LTSpice was initialized with the specified values of inductor current and output voltage in order to skip the electrical transient. During the iterative approach, 500 switching cycles (5 ms) are simulated in every circuit simulation with fixed temperatures of S1 and S2. The steady-state power losses are calculated as an average over the last 50 switching cycles (0.5 ms) and then imported in the proposed FDM thermal tool to calculate $T_{\rm j1,ss}$ and $T_{\rm j2,ss}$ for the given power inputs. The iterative analysis was conducted with two initial temperatures of 80 and 225 °C. The steady-state temperature was reached after four iterations, as shown in Fig. 12. In this article, three different sets of thermal conductivities were used: 1) temperature-dependent thermal conductivity $k(T)$ [see Fig. 12(a)]; 2) constant thermal conductivity $k(T = 80$ °C) [see Fig. 12(b)]; and 3) constant thermal conductivity $k(T = 225$ °C) [see Fig. 12(c)]. The steady-state temperatures of S1 and S2 were determined with an error tolerance of less than 1 K. The steady-state temperatures estimated by using $k(T = 80$ °C), $k(T = 225$ °C), and $k(T)$ are 194.5, 211, and 205 °C, respectively, for S1 and 150, 156, and 152.5 °C, respectively, for S2. Accordingly, by using a constant thermal conductivity, the temperature of S1 is either underestimated by 5.1% or overestimated by 3%. Eight electrical and eight thermal simulations, i.e., four iterations for each initial condition, were performed to calculate the steady-state temperatures in the observed example. The electrical simulation in LTSpice took ≈ 1 min, while the thermal simulation in the FDM tool ≈ 6 s.

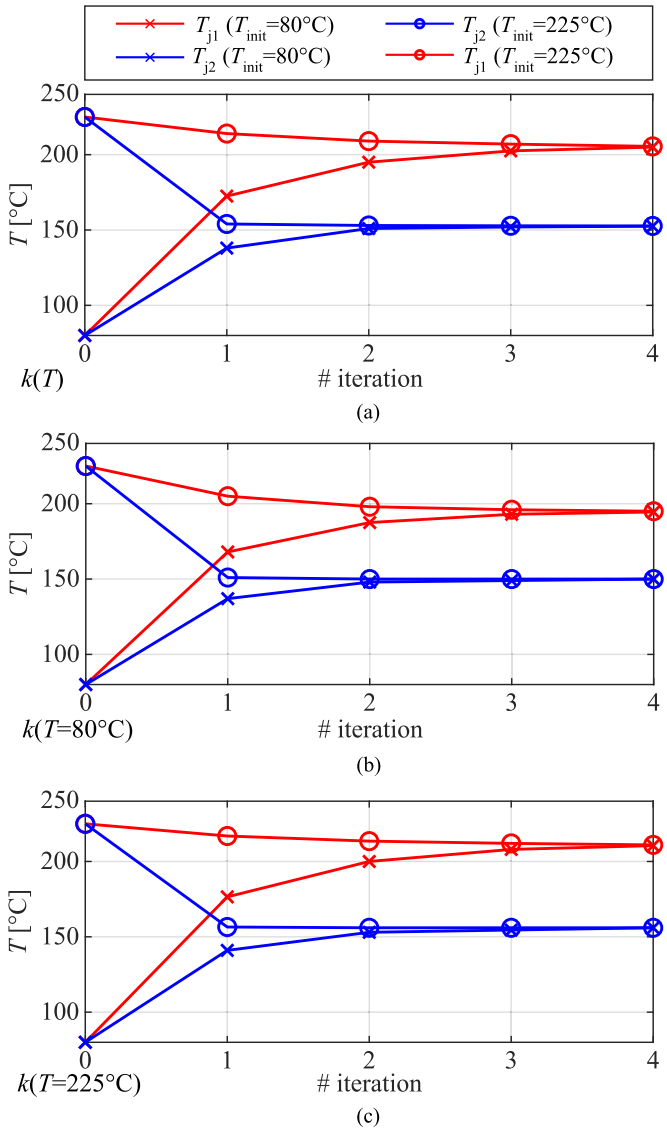

Fig. 12. Iterative coupling of LTspice and the proposed FDM thermal tool for calculating the steady-state thermal behavior of a 100-kHz synchronous boost converter with two initial junction temperatures of 80 and 225 °C and three sets of thermal conductivities: (a) $k(T)$, (b) $k(T = 80$ °C), and (c) $k(T = 225$ °C).

This analysis shows the importance of considering temperature-dependent thermal conductivities for the temperature estimation of fast switching power devices operating in

a higher temperature range, which, in turn, impacts the design optimization of the cooling system. Moreover, it shows that an iterative approach is more efficient for estimating the temperature of power devices than a fully coupled ET circuit-based simulation. However, it is applicable only for small oscillations of device junction temperature under steady-state conditions. Power semiconductor devices can experience temperature oscillations with higher amplitudes in steady-state operation in power cycling tests, inverters for aircraft internal distribution systems, low-speed motor drives, or induction motors [45], [50], [51]. For these applications, the ET modeling approach based on the developed FDM thermal tool and a circuit simulator is highly beneficial for accurate prediction of device temperatures and, hence, accurate virtual prototyping.

VI. Conclusion

This article verified the importance of including the temperature dependence of the thermal conductivity of power semiconductor and package materials for an accurate temperature prediction of SiC power devices operating in a wide temperature range. The temperature prediction becomes less accurate by assuming temperature-invariant material properties. A fully coupled circuit-based ET modeling method using the developed FDM thermal tool and LTSpice was implemented to enable the prediction of the temperature and current distribution of power devices within multichip PMs in a computationally efficient way, while including temperature-dependent thermal conductivity. An example of a SiC power MOSFET HB PM was used to verify the modeling capabilities of the FDM-LTSpice simulations in comparison to the well-known commercial thermal modeling tools of COMSOL and ANSYS, and IR camera measurements. The computational complexity of fully coupled circuit-based ET simulations was compared to an iterative ET modeling approach for a more accurate temperature prediction of SiC power devices with dominant switching losses.

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