A Resonant Push–Pull DC–DC Converter With an Intrinsic Current Source Behavior for Radio Frequency Power Conversion

Nikolai Weitz, Samuel Utzelmann, Stefan Ditze, and Martin März

***Abstract*—In this article, a resonant push–pull dc–dc converter suitable for switching frequencies in the MHz-range is investigated. Despite a simple design procedure with no need of multiresonant tuning, the converter topology is capable of providing a constant output current over a wide output voltage range in unregulated operation. Based on an analytical solution of steady-state operation, normalized dependencies of converter behavior are determined and used to formulate generalized design considerations. In order to verify the theoretical analysis, the design procedure of a 300-W prototype operating at a switching frequency of 6.78 MHz is described considering the impact of circuit parasitics on converter operation. The prototype provides a stable operation within the full output voltage range of 0–150 V and reaches a peak efficiency of 93% at the nominal output voltage. A rapid transient response of the converter is demonstrated by applying a closed-loop ON/OFF-control to the prototype.**

***Index Terms*—Class E dc–dc converter, high-frequency power converters, radio frequency, resonant dc–dc converter, zero voltage switching.**

I. Introduction

THE research effort regarding dc–dc converters that operate at switching frequencies of several MHz is mainly motivated by increasing the power density [1]–[13] and improving the transient response [8]–[12] of future power electronic systems. The dc–dc converters studied in this context typically base on a radio frequency (RF) power amplifier, frequently realized by the class E inverter [5]–[7], [14] or the class Φ_2 inverter [3], [8], [9], [15]–[17], in connection with a resonant rectifier stage [7]–[13], [18]. Another converter topology also basing on the mentioned combination is the quasi-resonant single-ended primary-inductor converter (SEPIC) [1], [10]. A common approach is to design the inverter and the rectifier as two separate subsystems based on fundamental frequency assumptions [3], [11]–[13]. As a consequence, the mutual effects of power amplifier and rectifier are not fully taken into account in the first design step and a subsequent tuning step may be necessary, to meet the required specification. Since the proper operation of high-efficiency power amplifiers is strongly bound to their nominal operating point [2], [17], [19], a popular method to adjust the amount of transmitted power is the ON/OFF control [3]–[5], [9], [11]. Although this approach allows a high-efficiency operation over a wide load range, the output voltage range of typical RF dc–dc converters is limited [2], [17]. However, it has been shown that the flexibility of the converters can be increased by additional circuit effort [13], [19], [20].

The resonant push–pull converter and related topologies have been intensively investigated, analyzed, and continuously improved in the last decades due to the advantages regarding the capability of high switching frequencies, simple design, and low losses [21]–[36]. Thereby, the applied push–pull topologies and the necessary resonant circuits have been adapted to the individual requirements of various applications [21]–[26]. Commonly, the push–pull topology is used in a current-fed configuration, but the dc inductor requires considerable space and also slows down the transient response of the converter, hampering the implementation of an ON/OFF-control [36]. The investigations in [37] and [38] have proved that a primary-side voltage-fed configuration with no need of a dc inductor can be attained by replacing the generally used parallel resonant tank by two series resonant circuits on the primary side of the converter. However, to the best known of the authors, previous work on resonant push–pull converters in a voltage-fed configuration has only considered operation at switching frequencies of several tens of kHz. Moreover, a detailed analysis of steady-state operation has not yet been carried out.

In this article, a resonant push–pull dc–dc converter suitable for operation at RF switching frequencies is investigated. The converter provides a current source behavior on secondary side in unregulated operation that is maintained over a wide output voltage range. This characteristic enables the converter, e.g., to precharge even a large dc link capacitance with no threat of significantly thermal issues caused by varying output voltage levels or any need of additional measures to counteract a short-circuit at the output. Due to a primary-side voltage-fed configuration, all

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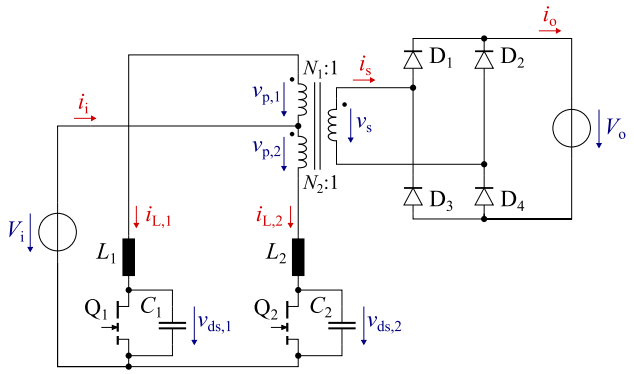

Fig. 1. Schematic of the resonant push–pull dc–dc converter.

passive components act as resonant elements and consequently no bulk energy storing components are required in the circuit. This enables a fast transient response of the converter, which is useful for implementing an ON/OFF control. The proposed topology features a simple design, since only two symmetrical resonant tanks have to be adapted in the tuning process. In addition, the potential inaccuracy arising from a separate analysis of inverter and rectifier is reduced by considering the converter as a whole in the theoretical studies.

The rest of this article is organized as follows. In Section II, typical waveforms and the analysis of steady-state operation are discussed. The results of parameter studies leading to design considerations of the converter are presented in Section III. In order to provide a proof of concept, the design procedure and measurement results of a 300-W prototype operating at a switching frequency of 6.78 MHz are described in Section IV. Finally, Section V concludes this article.

II. Theoretical Analysis

The topology of the resonant push–pull converter is presented in Fig. 1. It contains two switches Q_1 and Q_2, a transformer with a center-tapped primary winding with the turns ratio $N_1 : N_2 : 1$, two resonant tanks on primary side formed by $L_{1/2}$ and $C_{1/2}$, and a bridge rectifier at the output.

Within the theoretical analysis several assumptions are applied. The switches Q_1 and Q_2, their intrinsic reverse diodes, and the rectifier diodes are considered ideal with zero forward voltage and infinite OFF resistance. Any intrinsic junction capacitance of the semiconductors is neglected. The transformer also is assumed as ideal with no leakage inductance and infinite magnetizing inductance. All passive components are considered as linear with zero series resistance. The primary side is fully symmetrical besides the polarity of the transformer windings, leading to the terms $N_{1/2} = N$ ($v_{p,1/2} = v_p$, respectively), $L_{1/2} = L$, and $C_{1/2} = C$. In the considered operation mode, the switches are driven inversely with a duty cycle of 50%.

A. Key Waveforms

Typical current and voltage waveforms, normalized to the mean values of the input and output quantities V_i, I_i, V_o, and I_o, as well as the logical gate signals s_G in steady-state operation, are depicted in Fig. 2. Equivalent circuits, which illustrate the effects at the resonant tanks during the individual time intervals are presented in Fig. 3. Depending on the direction of

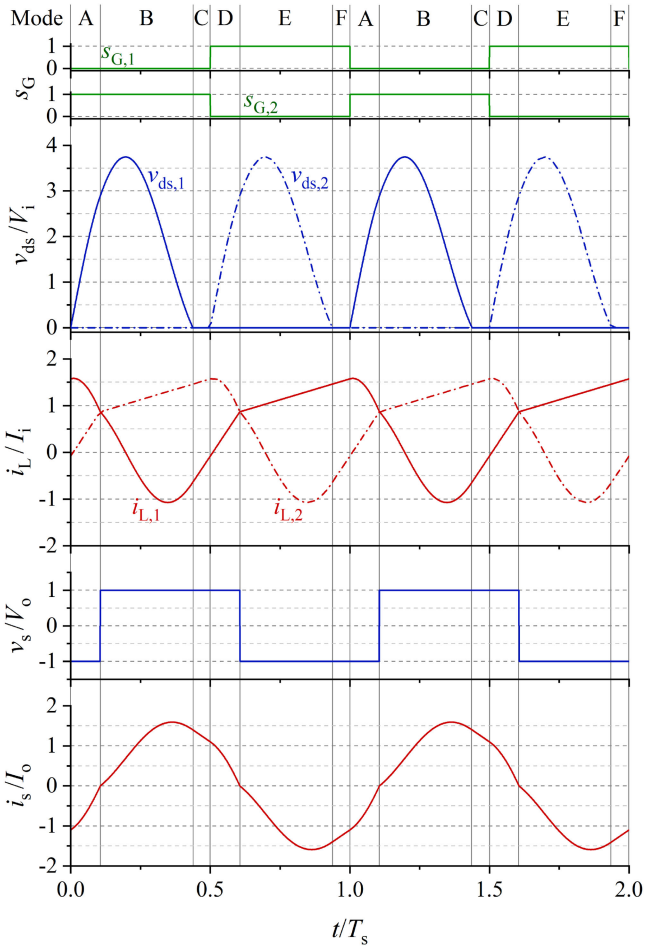

Fig. 2. Typical current and voltage waveforms in steady-state operation.

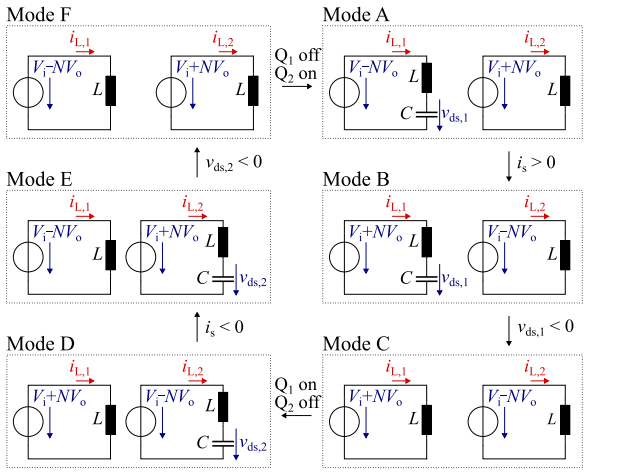

Fig. 3. Equivalent circuits and sequence of modes in steady-state operation.

TABLE I
OVERVIEW OF CONSIDERED TIME INTERVALS, DIFFERENTIAL EQUATIONS, AND GENERAL SOLUTIONS

Mode	Time Interval	Differential Equations	General Solutions	
A	$0 < t < d_\mathrm{A} T_\mathrm{s}$	$\frac{\mathrm{d}^2 i_{\mathrm{L},1}}{\mathrm{d}t^2} = -\frac{1}{LC} i_{\mathrm{L},1}$	$i_{\mathrm{L},1} = I_{\mathrm{A}1} \cdot \sin(\omega t) + I_{\mathrm{A}2} \cdot \cos(\omega t)$	(1)
		$\frac{\mathrm{d}i_{\mathrm{L},2}}{\mathrm{d}t} = \frac{V_\mathrm{i} + NV_\mathrm{o}}{L}$	$i_{\mathrm{L},2} = I_{0,2} + \frac{V_\mathrm{i} + NV_\mathrm{o}}{L} t$	(2)
B	$d_\mathrm{A} T_\mathrm{s} < t < (d_\mathrm{A} + d_\mathrm{B}) T_\mathrm{s}$	$\frac{\mathrm{d}^2 i_{\mathrm{L},1}}{\mathrm{d}t^2} = -\frac{1}{LC} i_{\mathrm{L},1}$	$i_{\mathrm{L},1} = I_{\mathrm{B}1} \cdot \sin\Big(\omega(t - (d_\mathrm{A} + d_\mathrm{B})T_\mathrm{s})\Big) + I_{\mathrm{B}2} \cdot \cos\Big(\omega(t - (d_\mathrm{A} + d_\mathrm{B})T_\mathrm{s})\Big)$	(3)
		$\frac{\mathrm{d}i_{\mathrm{L},2}}{\mathrm{d}t} = \frac{V_\mathrm{i} - NV_\mathrm{o}}{L}$	$i_{\mathrm{L},2} = i_{\mathrm{L},2}\Big\vert_{t=d_\mathrm{A}T_\mathrm{s}} + \frac{V_\mathrm{i} - NV_\mathrm{o}}{L}(t - d_\mathrm{A} T_\mathrm{s})$	(4)
C	$(d_\mathrm{A} + d_\mathrm{B}) T_\mathrm{s} < t < 0.5 \cdot T_\mathrm{s}$	$\frac{\mathrm{d}i_{\mathrm{L},1}}{\mathrm{d}t} = \frac{V_\mathrm{i} + NV_\mathrm{o}}{L}$	$i_{\mathrm{L},1} = I_{\mathrm{B}2} + \frac{V_\mathrm{i} + NV_\mathrm{o}}{L}\Big(t - (d_\mathrm{A} + d_\mathrm{B})T_\mathrm{s}\Big)$	(5)
		$\frac{\mathrm{d}i_{\mathrm{L},2}}{\mathrm{d}t} = \frac{V_\mathrm{i} - NV_\mathrm{o}}{L}$	$i_{\mathrm{L},2} = i_{\mathrm{L},2}\Big\vert_{t=(d_\mathrm{A}+d_\mathrm{B})T_\mathrm{s}} + \frac{V_\mathrm{i} - NV_\mathrm{o}}{L}\Big(t - (d_\mathrm{A} + d_\mathrm{B})T_\mathrm{s}\Big)$	(6)

the secondary-side current i_s, the voltage applied to the secondary winding can be evaluated as $v_\mathrm{s} = \pm V_\mathrm{o}$. Since the magnitude of v_s is constant regardless the value of i_s, the primary-side windings act as constant voltage sources with an applied voltage of $v_\mathrm{p} = \pm NV_\mathrm{o}$. As a consequence, a constant voltage is applied to the primary-side resonant tanks for the duration of each time interval. While the switches or their intrinsic reverse diodes, are conducting, the corresponding resonant capacitors are shorted and the applied drain–source voltage v_ds is zero. Based on the relationships of an ideal transformer, the currents circulating in the transformer are linked by

$$i_\mathrm{s} = N \cdot (i_{\mathrm{L},2} - i_{\mathrm{L},1}). \tag{7}$$

At the beginning of the switching period at $t = 0$ in mode A, Q_1 is turned OFF,while simultaneously Q_2 is turned ON. The voltage applied to the secondary winding is clamped to $v_\mathrm{s} = -V_\mathrm{o}$ due to the negative current i_s. Caused by the resonant tank formed by L_1 and C_1, the progressions of $i_{\mathrm{L},1}$ and $v_{\mathrm{ds},1}$ follow a sinusoidal shape. In contrast, Q_2 is bypassing C_2, which, therefore, is not participating in the resonant process. As a result of the constant voltage across L_2, the current $i_{\mathrm{L},2}$ increases linearly. The transition into mode B is triggered by the zero crossing of i_s. This causes the diode rectifier to commutate and the voltage applied to the secondary winding changes into $v_\mathrm{s} = V_\mathrm{o}$, leading to a voltage step at the resonant tanks on the primary side. At the zero crossing of $v_{\mathrm{ds},1}$, the converter changes into mode C. Since the intrinsic reverse diode of Q_1 prevents the voltage from going negative, both capacitances C_1 and C_2 are shorted, leading to a linear rise of $i_{\mathrm{L},1}$ and $i_{\mathrm{L},2}$. After Q_1 and Q_2 are switched again, the circuit operates in mode D. Due to the assumptions concerning the symmetry of the circuit, the remaining transitions can be derived from the descriptions above.

B. Mathematical Analysis

Based on the equivalent circuits and the sequence of modes discussed above, an analytical solution of steady-state operation is carried out. Due to the symmetry of the waveforms depicted in Fig. 2 regarding half of a switching period T_s, including the switching states from mode A to mode C is sufficient. In Table I the mathematical definition of the time intervals during which the considered modes occur, the differential equations of $i_{\mathrm{L},1}$ and $i_{\mathrm{L},2}$, and the corresponding general solutions are summarized. The linearly independent unknown currents $I_{\mathrm{A}1}$, $I_{\mathrm{A}2}$, $I_{\mathrm{B}1}$, $I_{\mathrm{B}2}$, and $I_{0,2}$ as well as the normalized mode durations d_A and d_B can be determined by applying seven boundary conditions, which are derived in the following.

As Q_1 is turned ON, immediately before the circuit changes into mode A, the voltage applied to C_1 is zero at $t = 0$, which leads to the condition

$$\left.\frac{\mathrm{d}i_{\mathrm{L},1}}{\mathrm{d}t}\right|_{t=0} = \frac{V_\mathrm{i} - NV_\mathrm{o}}{L} = \omega I_{\mathrm{A}1} \tag{8}$$

with the circular frequency $\omega = (\sqrt{LC})^{-1}$. Mode B ends, as soon as $v_{\mathrm{ds},1}$ crosses zero, resulting in

$$\left.\frac{\mathrm{d}i_{\mathrm{L},1}}{\mathrm{d}t}\right|_{t=(d_\mathrm{A}+d_\mathrm{B})T_\mathrm{s}} = \frac{V_\mathrm{i} + NV_\mathrm{o}}{L} = \omega I_{\mathrm{B}1}. \tag{9}$$

Since the total charge of C_1 does not change during the first two time intervals, the equation

$$0 = \int_0^{(d_\mathrm{A}+d_\mathrm{B})T_\mathrm{s}} i_{\mathrm{L},1} \mathrm{d}t \tag{10}$$

can be derived. By inserting the general solutions (1) and (3) in (10), this leads to

$$0 = \frac{1}{\omega}\Bigg(I_{\mathrm{A}1}\big(1 - \cos(\omega d_\mathrm{A} T_\mathrm{s})\big) + I_{\mathrm{A}2}\sin(\omega d_\mathrm{A} T_\mathrm{s}) + I_{\mathrm{B}1}\big(\cos(\omega d_\mathrm{B} T_\mathrm{s}) - 1\big) + I_{\mathrm{B}2}\sin(\omega d_\mathrm{B} T_\mathrm{s})\Bigg). \tag{11}$$

The zero crossing of i_s occurs at $t = d_\mathrm{A} T_\mathrm{s}$. According to (7), $i_{\mathrm{L},1}$ and $i_{\mathrm{L},2}$ have to be equal at this moment, which can be expressed by

$$i_{\mathrm{L},1}\Big\vert_{t=d_\mathrm{A}T_\mathrm{s}} = i_{\mathrm{L},2}\Big\vert_{t=d_\mathrm{A}T_\mathrm{s}} \tag{12}$$

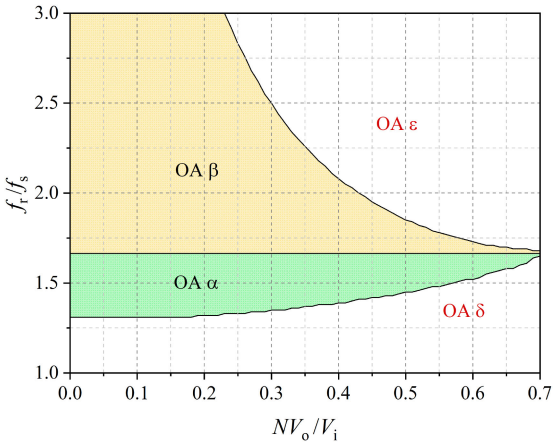

Fig. 4. Definition of operation areas specified by characteristic shapes of v_{ds}.

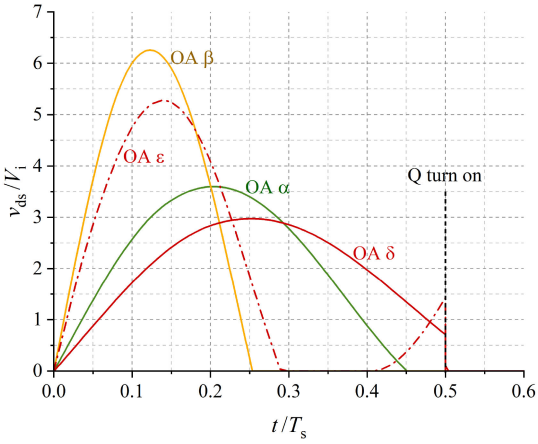

Fig. 5. Typical shapes of the drain-source voltage corresponding with the operation areas.

$$I_{A1}\sin(\omega d_A T_s) + I_{A2}\cos(\omega d_A T_s) = I_{0,2} + \frac{V_i + NV_o}{L} d_A T_s. \tag{13}$$

As $i_{L,1}$ is steady at $t = d_A T_s$, the general solutions also have to match the condition

$$I_{A1}\sin(\omega d_A T_s) + I_{A2}\cos(\omega d_A T_s) = -I_{B1}\sin(\omega d_B T_s) + I_{B2}\cos(\omega d_B T_s). \tag{14}$$

The remaining two boundary conditions base on the symmetry of $i_{L,1}$ and $i_{L,2}$ within one switching period. As they have a time shift of $T_s/2$, the resulting equations are

$$i_{L,1}\Big|_{t=0} = i_{L,2}\Big|_{t=\frac{T_s}{2}} \tag{15}$$

$$I_{A2} = I_{0,2} + \frac{V_i T_s}{2L} - \frac{NV_o T_s}{L}\left(\frac{1}{2} - 2d_A\right) \tag{16}$$

and

$$i_{L,2}\Big|_{t=0} = i_{L,1}\Big|_{t=\frac{T_s}{2}} \tag{17}$$

$$I_{0,2} = I_{B2} + \frac{V_i + NV_o}{L}\left(\frac{1}{2} - d_A - d_B\right)T_s. \tag{18}$$

With the derived boundary conditions, the unknown parameters I_{A1}, I_{A2}, I_{B1}, I_{B2}, and $I_{0,2}$ can be solved in dependence of d_A and d_B

$$I_{A1} = \frac{V_i - NV_o}{\omega L} \tag{19}$$

$$I_{B1} = \frac{V_i + NV_o}{\omega L} \tag{20}$$

$$I_{A2} = \frac{V_i - NV_o}{\omega L} \cdot \frac{\sin(\omega d_A T_s) + (\frac{1}{2} - d_A)\omega T_s}{1 - \cos(\omega d_A T_s)} \tag{21}$$

$$I_{B2} = \frac{V_i - NV_o}{\omega L}\left(\frac{\sin(\omega d_A T_s) + (\frac{1}{2} - d_A)\omega T_s}{1 - \cos(\omega d_A T_s)} \cdot \cos(\omega d_A T_s) + \sin(\omega d_A T_s)\right) - \frac{V_i + NV_o}{L}\left(\frac{1}{2} - d_B\right)T_s \tag{22}$$

$$I_{0,2} = \frac{V_i - NV_o}{\omega L}\left(\frac{\sin(\omega d_A T_s) + (\frac{1}{2} - d_A)\omega T_s}{1 - \cos(\omega d_A T_s)} \cdot \cos(\omega d_A T_s) + \sin(\omega d_A T_s)\right) - \frac{V_i + NV_o}{L} d_A T_s. \tag{23}$$

In order to determine d_A and d_B, the terms

$$0 = (V_i - NV_o)\Big(1 - \cos(\omega d_A T_s) + \sin(\omega d_A T_s)\sin(\omega d_B T_s) + \frac{\sin(\omega d_A T_s) + (\frac{1}{2} - d_A)\omega T_s}{1 - \cos(\omega d_A T_s)}(\cos(\omega d_A T_s)\sin(\omega d_B T_s) + \sin(\omega d_A T_s))\Big) - (V_i + NV_o)\Big(1 - \cos(\omega d_B T_s) + \left(\frac{1}{2} - d_B\right)\sin(\omega d_B T_s)\omega T_s\Big) \tag{24}$$

and

$$0 = (V_i - NV_o)\cdot(1 - \cos(\omega d_B T_s))\Big(\sin(\omega d_A T_s) + \frac{\sin(\omega d_A T_s) + (\frac{1}{2} - d_A)\omega T_s}{1 - \cos(\omega d_A T_s)} \cdot \cos(\omega d_A T_s)\Big) + (V_i + NV_o)\Big(\sin(\omega d_B T_s) + \left(\frac{1}{2} - d_B\right)\cos(\omega d_B T_s)\omega T_s\Big) \tag{25}$$

are further derived by the boundary conditions. For given parameters, d_A and d_B can be solved numerically using (24) and (25).

III. Design Considerations

The analytical solution of steady-state operation is used for the derivation of normalized considerations to describe the converter behavior in a broad parameter range and to facilitate the design process. In this context, the resonant circuit quantities such as resonance frequency $f_r = (2\pi\sqrt{LC})^{-1}$ and the impedance of the resonant circuit $Z_0 = \sqrt{L/C}$ are defined. As a result of normalization, the considerations presented in the following are independent of specific design parameters and vary only with

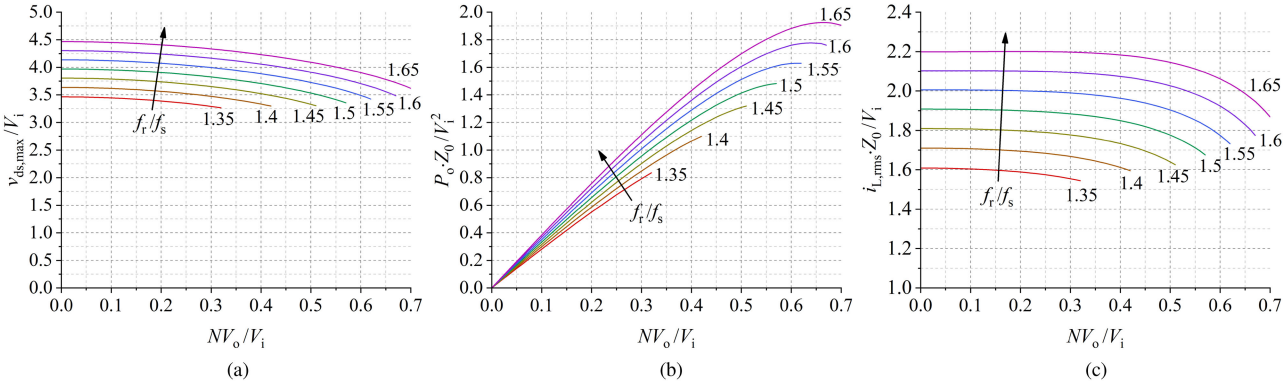

Fig. 6. Normalized progressions of relevant circuit quantities. (a) Voltage stress at the power transistors. (b) Output power of the converter. (c) Current stress on primary side.

the variables indicated in the diagrams. The studies presented in this section all correspond to an unregulated operation with the input and output voltage being clamped to fixed values and the key waveforms during operation resulting from a specific tuning of $f_\mathrm{r}/f_\mathrm{s}$ and Z_0.

Since the achievement of soft-switching and the voltage stress across the power transistors are crucial aspects regarding the proper design of RF dc–dc converters, the description of the converter behavior starts with the definition of operation areas (OAs) that differ in these aspects. In Fig. 4, four OAs are defined depending on the voltage ratio $NV_\mathrm{o}/V_\mathrm{i}$ and the normalized resonance frequency $f_\mathrm{r}/f_\mathrm{s}$, with the corresponding typical waveforms of the drain–source voltages depicted in Fig. 5. While the converter operates within OA α and OA β, the switches are turned ON at zero voltage. Major differences between the named OAs are the significantly higher peak voltage at the transistors and the longer duration of mode C and mode F in OA β. In OA δ and OA ε, the drain–source voltage differs from zero at the switching transition, resulting in switching losses. The sequence of modes defined in Fig. 3 is violated in these OAs. While mode C and mode F are skipped in OA δ, in OA ε the drain–source voltage rises again after the zero crossing, before the switching transition occurs. Since the sequence of modes is assumed in the calculation of steady-state operation presented in Section II-B, the derived equations for converter analysis are only valid for OA α and OA β.

As mentioned above, soft switching is considered as a mandatory prerequisite for pushing the switching frequency into the MHz-range and, therefore, OA δ and OA ε are to be avoided during operation. According to this condition, the feasible range of $NV_\mathrm{o}/V_\mathrm{i}$ depending on $f_\mathrm{r}/f_\mathrm{s}$ can be obtained directly from Fig. 4. The transition between OA α and OA β is marked by the ratio $f_\mathrm{r}/f_\mathrm{s} = 1.65$ providing the widest range of $NV_\mathrm{o}/V_\mathrm{i}$ within soft-switching is achieved. Increasing $f_\mathrm{r}/f_\mathrm{s}$ beyond this point leads to a decrease of the voltage transfer ratio, while the peak voltage across the transistors rises. Due to the advantageous operating characteristics in OA α, the following investigations are limited to this operation area.

Based on the diagrams shown in Fig. 6, further aspects regarding the design of the converter are discussed. All considered quantities resulting from different values of $f_\mathrm{r}/f_\mathrm{s}$ are plotted depending on $NV_\mathrm{o}/V_\mathrm{i}$. Due to the limitation of the operation area, the depicted lines end at the transition to OA δ. In Fig. 6(a), the maximum value of the occurring drain–source voltage $v_\mathrm{ds,max}$ related to the input voltage V_i is plotted. Due to the shape of v_ds, which is reminiscent of the class E inverter with a maximum drain–source voltage of $3.6 \cdot V_\mathrm{i}$ in ideal operation [2], [12], $v_\mathrm{ds,max}$ also ranges close to this value. Assuming a fixed ratio $f_\mathrm{r}/f_\mathrm{s}$ during operation, the utilization of a large range of $NV_\mathrm{o}/V_\mathrm{i}$ leads to a slight increase in the voltage stress of the power transistors. Considering a given input voltage and a desired range of $NV_\mathrm{o}/V_\mathrm{i}$, the required breakdown voltage of the power transistors can be determined by means of the results depicted in Fig. 6(a). As known of the class E inverter, providing a significant share of C by the nonlinear output capacitance of the power transistors leads to a further increase of $v_\mathrm{ds,max}$ [39].

After ensuring soft-switching and the observance of the breakdown voltage of the power transistors, further considerations toward the output power of the converter are to be done. The normalized output power P_o for different frequency ratios $f_\mathrm{r}/f_\mathrm{s}$ is plotted in Fig. 6(b). From the approximately linear progression of the output characteristics for $NV_\mathrm{o}/V_\mathrm{i} < 0.5$, it can be concluded that within this range the input current of the rectifier i_s is only slightly dependent on the voltage transfer ratio, entailing the current source behavior of the converter. Adjusting the remaining parameter Z_0 allows to set P_o without any impact on the aspects discussed so far. Thus, the estimation of the resonant tank parameters at a given switching frequency can be summarized as f_r being chosen by the desired range of $NV_\mathrm{o}/V_\mathrm{i}$, while Z_0 defines the output current at a given input voltage of the converter. Depending on the extent of the influence caused by neglected circuit parasitics, further tuning steps may be necessary. In this case, the presented considerations provide a starting point with regard to a more detailed converter design.

In the previous considerations, the design criteria toward a high-efficiency operation have not yet been taken into account. Despite the power dissipation during operation does strongly depend on the specific characteristics of the deployed semiconductors and passive components, some generalized studies regarding the current stress of the converter are described below.

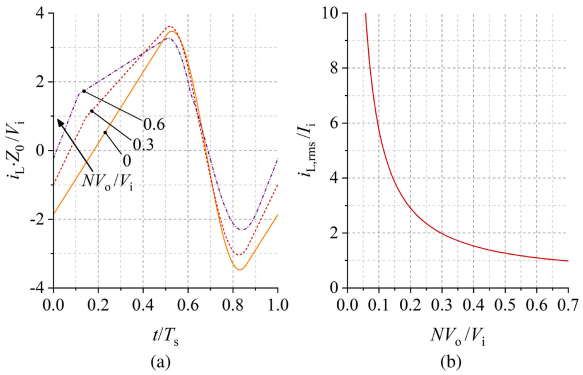

Fig. 7. (a) Current shapes on primary side at $f_r/f_s = 1.65$. (b) Current stress on primary side related to the dc component of the input current.

TABLE II
ELECTRICAL SPECIFICATION OF THE PROTOTYPE

Nominal input voltage	$V_i = 120$ V
Nominal output voltage	$V_o = 150$ V
Nominal output power	$P = 300$ W
Switching frequency	6.78 MHz

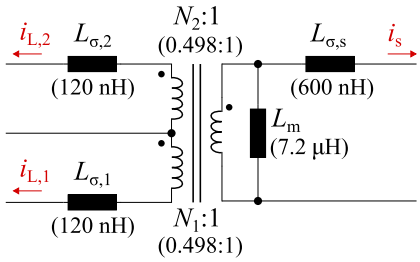

Fig. 8. Equivalent circuit of the transformer including measurement results of the deployed component.

Assuming V_o and P_o as being given by the application, the possibilities to positively affect the secondary-side current i_s are limited. Hence, the following considerations focus on the primary side. Due to the symmetry of $i_{L,1}$ and $i_{L,2}$, their rms value can be expressed by a single variable $i_{L,rms}$, of which normalized progressions are depicted in Fig. 6(c). At a given f_r/f_s, they barely vary within a wide range of NV_o/V_i and close to the transition from OA α to OA δ, they slightly decrease. In order to convey an understanding of the shown lines, the underlying current waveforms at $f_r/f_s = 1.65$ are depicted in Fig. 7(a). The main difference between the waveforms shown is their dc component, which is a result from the varying output power caused by feeding a similar output current into a changing output voltage. At $NV_o/V_i = 0.6$, the amplitude of i_L is reduced, which explains the smaller rms value. Due to the high amount of output power and the reduced current stress, the potential of high efficiency is mostly expected at the transition from OA α to OA δ. At a low NV_o/V_i, the efficiency may suffer, but since there is only a slight increase of $i_{L,rms}$, it is assumed that crucial thermal problems are not to be expected. Although Fig. 6(c) allows to estimate the occurring current stress at a given operating point, since there is a huge variation of output power within the examined parameter range, they are not suitable for making a comparison regarding the efficiency of the converter. To counter this issue, a further abstracted consideration is made. Adjusting the normalization of $i_{L,rms}$ by relating each value to the dc component of the input current I_i at the respective operating points yields the progression shown in Fig. 7(b). Since I_i defines P_o at a given input voltage, $i_{L,rms}/I_i$ forms the ratio of current stress to output power, and, thus, allows to be interpreted as a measure of potential converter efficiency. The results state that there is no dependence on the value of f_r/f_s in this consideration. It is obtained that there is a steady reduction of $i_{L,rms}/I_i$ with increasing values of NV_o/V_i and consequently a high NV_o/V_i is assumed to be beneficial for the converter efficiency.

IV. EXPERIMENTAL VERIFICATION

Based on the generalized design considerations presented in Section III, the design process and the measurement results of a prototype operating at a switching frequency of 6.78 MHz is described in the following. The targeted specification of the prototype is summarized in Table II.

A. Prototype Design

At first, a suitable turns ratio N of the transformer is estimated. Regarding the nominal values of V_i and V_o, the term

$$N < 0.7 \cdot \frac{V_i}{V_o} \tag{26}$$

gives the maximum value of N at which the converter can be operated in OA α. Since significantly lower values of N than given by (26) lead to an increased current stress on primary side, the turns ratio is chosen to $N = 0.5$. After all necessary quantities are known at this point, the resonant elements can be determined according to the descriptions in Section III. To achieve an operating point in OA α, the resonance frequency is selected to $f_r = 1.65 f_s$. Evaluating the corresponding progression in Fig. 6(b) leads to

$$Z_0 = 1.9 \cdot \frac{V_i^2}{P_o}. \tag{27}$$

Applying the specifications, given in Table II, the nominal values of the components of the resonant tanks can be determined with $L = 1.3$ µH and $C = 156$ pF, which serves as a starting point for the further design.

In a next step, a more detailed modeling of the transformer is gained by applying the equivalent circuit depicted in Fig. 8 [40], [41]. The stray inductances $L_{\sigma,1}$ and $L_{\sigma,2}$ are absorbed by L_1 and L_2. As a result, they have no effect on the converter operation discussed in Section III, while they are taken into account during the design. The inductance L_m does not have a significant impact on the operation either, as long as the magnetization current is negligible compared to i_s. A more detailed discussion is carried out toward the influence of the stray inductance $L_{\sigma,s}$ on the secondary side. As it is not in series with any inductance considered in the idealized analysis, it cannot be absorbed by other circuit components. The

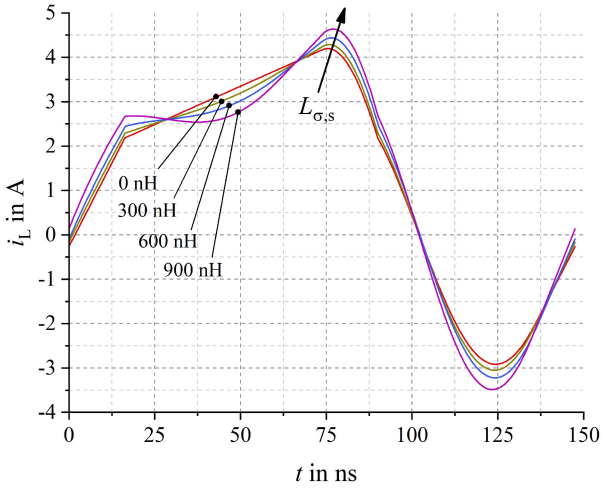

Fig. 9. Waveforms of i_L at different values of $L_{\sigma,s}$.

TABLE III
SET OF RESONANT PARAMETERS

$L_{\sigma,s}$	Z_0	f_r/f_s	L	C
0	91.2 Ω	1.65	1.30 µH	156 pF
300 nH	85 Ω	1.72	1.16 µH	161 pF
600 nH	76.5 Ω	1.79	1.00 µH	171 pF
900 nH	70 Ω	1.89	869 nH	177 pF

resulting waveforms of i_L at different values of $L_{\sigma,s}$ are shown in Fig. 9. To create a basis for comparison, the tuning of the resonant components on the primary side is adjusted to meet the specification of Table II. Additional required constraints are the achievement of soft switching and a shape of v_{ds}, which is similar to the results of the reference set of parameters with zero stray inductance on secondary side. The resulting values of the resonant tanks after the tuning process are summarized in Table III. As it gets visible by the current waveforms depicted in Fig. 9, there is a rise of the current stress on primary side with an increasing value of $L_{\sigma,s}$. The impact of $L_{\sigma,s}$ on the tuning of the resonant elements shows a remarkable aspect. To reach the aimed operating point, $L_{\sigma,s}$ makes a higher value of C and a lower value of L necessary. This context could be exploited to reduce the fraction of total capacitance represented by the switch's nonlinear output capacitance, thus limiting its influence on the transistor's voltage stress. Alternatively, a larger die size could be used to achieve a lower ON-resistance, which counteracts the increase of losses during the ON-state of the transistors caused by the higher current stress.

The contribution of $L_{\sigma,1}$ and $L_{\sigma,2}$ to the required resonant inductances may motivate to solely realize L_1 and L_2 by transformer parasitics. While this approach appears to be feasible, some mandatory demands have to be addressed in the transformer design. If a deviation between $L_{\sigma,1}$ and $L_{\sigma,2}$ cannot be compensated by external inductors, to prevent an asymmetrical voltage and current stress at the power transistors, a fully symmetrical transformer assembly needs to be ensured. In addition, to reduce its impact on converter behavior, the secondary-side leakage $L_{\sigma,s}$ should not exceed reasonably high values, which

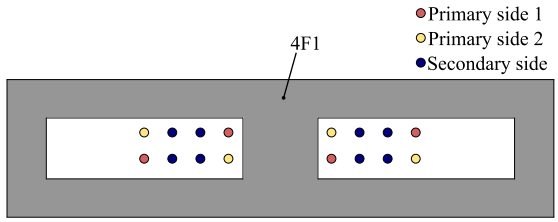

Fig. 10. Outlined winding setup of the deployed transformer.

entails further challenges regarding feasible winding arrangements. In case ferrite materials are used, variations in magnetic properties due to manufacturing tolerances and temperature dependence must be taken into account as well. While these effects can be limited by applying an air gap to the magnetic core, a sufficiently high value of L_m still needs to be maintained.

Considering the transformer design of the prototype, which is intended to serve as a proof of concept, the approach of implementing resonant inductors by transformer parasitics is not being followed. In order to obtain a high value of L_m, an ungapped core assembled by the combination of a E58/11/38 and a PLT58/38/4 core of the NiZn ferrite material 4F1 is deployed. This core may appear to be oversized for the aimed specification, but only few core shapes of ferrites suitable for power electronics applications at the rated switching frequency are commercially available. In order to simplify the design of the resonant elements, the transformer is realized as symmetrical as possible on primary side, which explains the winding arrangement of the deployed transformer outlined in Fig. 10. The measured equivalent circuit parameters of the applied component can be found in Fig. 8.

To realize the power transistors of the prototype, the GS66504B 100-mΩ GaN E-HEMT is selected. With the aim of reducing the conduction losses, the ON-resistance of the transistors should be as low as possible. At a given breakdown voltage of the power transistor, this issue entails a high output capacitance, the influence of which is discussed in advance. An additional relevant aspect are the C_{oss}-losses that occur by charging and discharging the output capacitance. These losses increase with enlarging die sizes, and, therefore, counteract with the losses occurring during ON-state [42]–[46]. In [47], the equation

$$\frac{P_{Coss}}{W} = 7.1 \cdot 10^{-16} \cdot \left(\frac{f_s}{Hz}\right)^{1.6} \cdot \left(\frac{3.56 V_i}{V}\right)^{1.6} \tag{28}$$

for estimating the C_{oss}-losses of the applied transistor in the operation of a class E inverter is given. Since a similar voltage waveform occurs as with the class E inverter, (28) allows to roughly estimate the C_{oss}-losses of about 1-W per transistor in nominal operation.

Considering the current stress on the secondary side, the C6D06065E Schottky diode with a forward voltage drop of about 1.4 V at rated current, a breakdown voltage of 650 V, and a junction capacitance of 44 pF at a reverse voltage of 200 V is used to realize the bridge rectifier. Since the junction capacitance of the diodes must be recharged each time the rectifier is switched, additional operation modes occur, in which all rectifier diodes

TABLE IV
SELECTED COMPONENTS

Power transistors	650 V, 100 mΩ GaN E-HEMT, GS66504B
Gate driver	LM5114
Rectifier diodes	650 V, 6 A SiC schottky diode, C6D06065E
Transformer	E58/11/38 and PLT58/38/4 4F1 cores, $2:2:4$, 1 mm wire, $L_{\rm m} = 7.2$ µH, $L_{\sigma,1} = 120$ nH, $L_{\sigma,2} = 120$ nH, $L_{\sigma,\rm s} = 600$ nH, $N_1 = 0.498$, $N_2 = 0.498$
Air coils	2 x ∼820 nH, each 6 turns 1 mm wire
Resonant capacitors	2 x 47 pF, 1000 V, C0G, ceramic 2 x 100 pF, 1000 V, C0G ceramic

are in blocking state. As reported for other topologies of resonant dc–dc converters, the resulting deviation of the mode sequence from idealized considerations can have a remarkable impact on the output power, which also should be investigated during converter design [48].

The aforementioned parasitics are not taken into account in the theoretical investigations, therefore, their effects on the required tuning still have to be addressed. In order to provide a more realistic view on converter operation, a detailed SPICE simulation in steady-state operation is applied, with the semiconductors modeled by the level 3 SPICE models provided by the manufacturers. Using the SPICE simulation, an iterative adjustment of the resonant tanks is carried out to estimate the final tuning of the converter. Since only two symmetrical resonant tanks need to be adapted, the final design with the components listed in Table IV emerges after few iterations. The simulation results of the proposed design at the nominal input and output voltage given in Table II are depicted in Fig. 11. Comparing the simulated waveforms with the idealized analysis depicted in Fig. 2, the impact of the nonlinear output capacitance of the power transistors on the shape of $v_{\rm ds}$, the effect of the parasitic inductance $L_{\sigma,\rm s}$ on $i_{\rm L}$, as well as the additional modes caused by the junction capacitance of the rectifier diodes are getting visible. At the rated operating point, the simulated output power is $P_{\rm o} = 332$ W, which meets the specification defined in Table II. A photography of the prototype, which is assembled based on the considerations above using the components listed in Table IV is shown in Fig. 12.

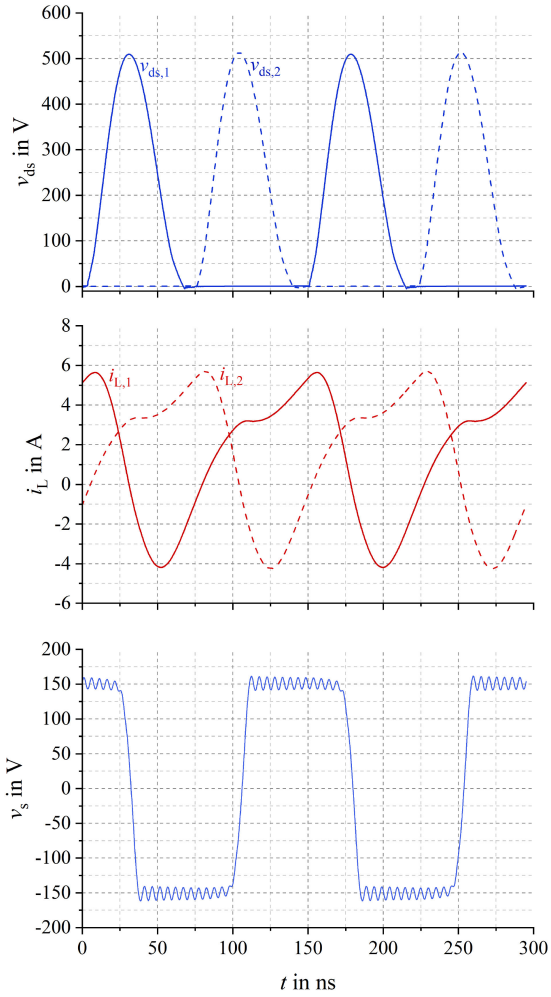

Fig. 11. Simulated voltage and current waveforms of the prototype at the nominal operating point.

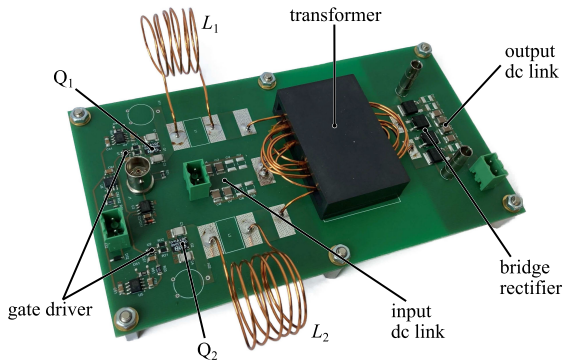

Fig. 12. Photography of the prototype.

B. Control Strategy

To verify the feasibility of an ON/OFF control, a closed-loop control of the output voltage is applied for the prototype. This method has been frequently used to adjust the transmitted output power of RF dc–dc converters and in the majority of publications, it was realized as a hysteretic control with higher and lower voltage thresholds of the output voltage triggering the startup and shutdown of the power stage [4], [5], [9].

The control algorithm, which is used for the prototype, is outlined in Fig. 13. Similar to the approach presented in [10], the power stage is switched at a fixed modulation frequency of $f_{\rm mod} = 113$ kHz. Based on the feedback signal $v_{\rm fb}$ of the monitored output voltage and the reference input variable $v_{\rm ref}$, a PI controller calculates the required duty cycle of the enable signal used to drive the power stage.

C. Measurement Results

The setup applied for the measurements consists of separate power supplies providing the input voltage of the converter and the supply of the gate drivers, a clock signal to trigger the

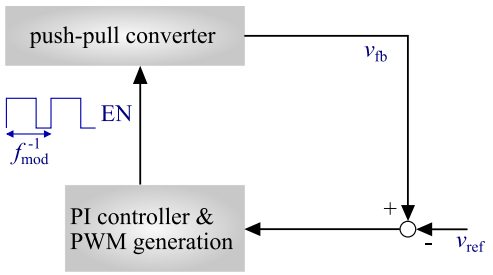

Fig. 13. Block diagram of the control algorithm applied.

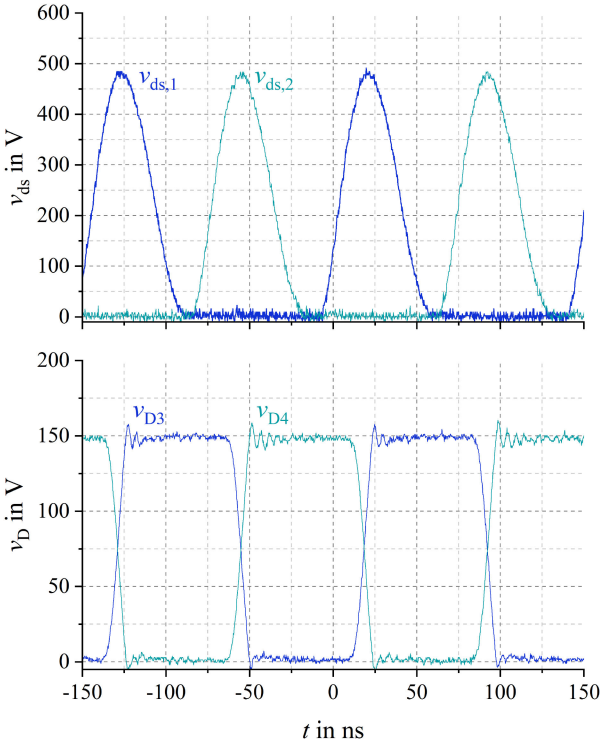

Fig. 14. Measurement results of the drain–source voltage of the power transistors and the blocking voltage of the bridge rectifier at the nominal operating point.

switching transitions, and an electronic load that operates in constant voltage mode. This configuration of the measurement setup allows the same general conditions as in the theoretical studies, meaning unregulated operation with fixed voltages at the input and output of the converter. To estimate the output power and the efficiency, a ZES Zimmer LMG310 precision power analyzer is used.

In Fig. 14, the measured waveforms of the transistor drain–source voltages and the blocking voltages of the lowside rectifier diodes at the nominal operating point are shown. Since they show a sufficiently close accuracy with the simulation results depicted in Fig. 11, it is concluded, that the most relevant influences are respected in the simulations. In order to examine the output voltage range and the efficiency of the prototype, the output

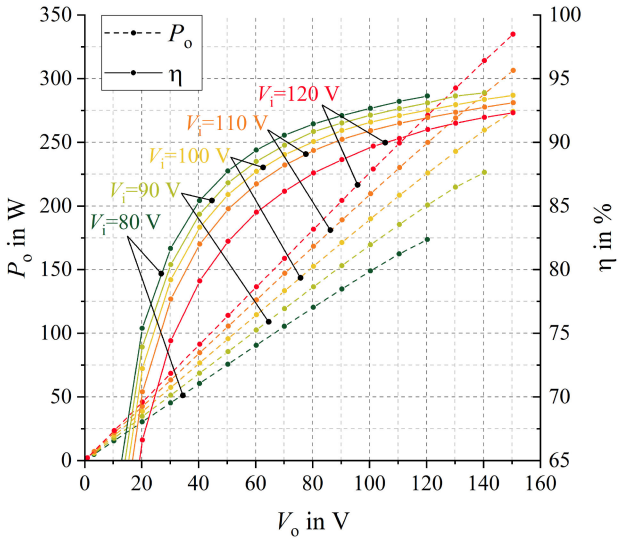

Fig. 15. Measured output power and efficiency within the full output voltage range.

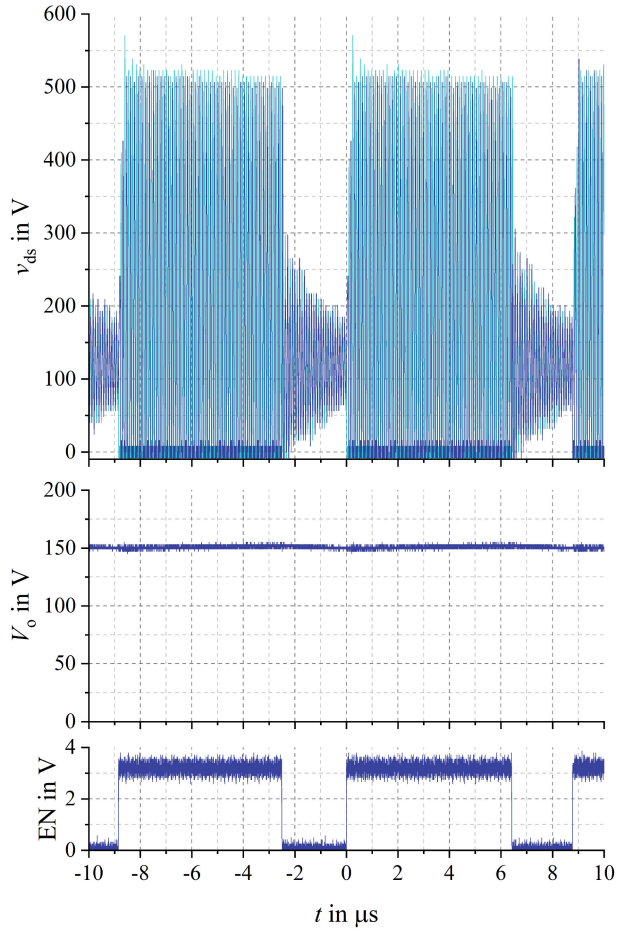

Fig. 16. Measurement results of the drain–source voltages v_{ds}, the output voltage V_o, and the enable signal EN under closed-loop control at a resistive load of $R_{load} = 85\,\Omega$.

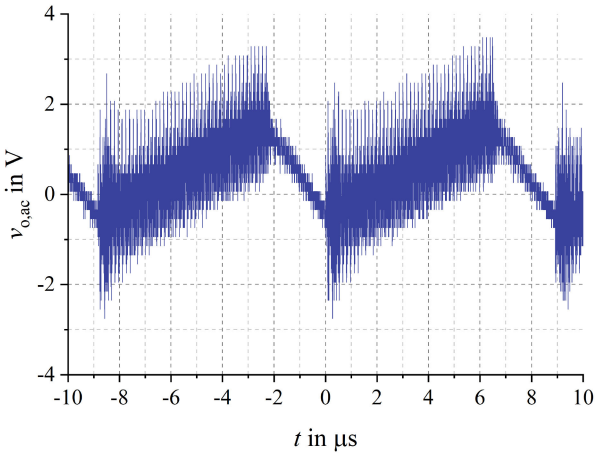

Fig. 17. Measurement results of the output voltage ripple $v_{\mathrm{o,ac}}$ under closed-loop control at a resistive load of $R_{\mathrm{load}} = 85\,\Omega$.

voltage is varied by adjusting the settings of the electronic load. It is mentioned, that the power consumption of the gate drivers is covered by a separate power supply, and, thus, is not included in the measurements of the efficiency. The measurement results of output power and converter efficiency in unregulated operation at several input voltage levels up to the nominal input voltage of $V_{\mathrm{i}} = 120\,\mathrm{V}$ are depicted in Fig. 15. In the measurements, the upper limit of the covered output voltage range is defined either by the transition into hard switching operation or the nominal output voltage of $V_{\mathrm{o}} = 150\,\mathrm{V}$. Key aspects of the theoretical investigations regarding the intrinsic current source behavior in unregulated operation, leading toward a linear dependence of the output power on the output voltage, as well as a steady increase of the converter efficiency at growing output voltages are confirmed. It gets visible that the peak efficiency is not reached at the nominal input voltage of $V_{\mathrm{i}} = 120\,\mathrm{V}$. Since both current stress and C_{oss}-losses increase with rising values of V_{i}, the overall power losses correlate strongly with the applied input voltage of the converter. However, at all input voltages, the converter achieves high efficiency of beyond 90% within an output voltage range of several tens of volts, and a peak efficiency of greater than 93% is measured at lower input voltage levels.

For the measurements of the converter under closed-loop control, the electronic load is replaced by a passive resistive load of $R_{\mathrm{load}} = 85\,\Omega$. In Fig. 16, the measured progressions of the drain–source voltages, the output voltage, and the enable signal are shown. A more detailed depiction of the output voltage ripple $v_{\mathrm{o,ac}}$ at the corresponding operating point is presented in Fig. 17. The measurement results illustrate the rapid transient response both at startup and shutdown of the converter. During startup, a voltage overshoot at the power transistors occurs, but it remains within an acceptable range.

V. Conclusion

This article investigates a resonant push–pull converter suitable for operation at switching frequencies in the MHz-range. Based on an analytical analysis of steady-state operation, normalized design considerations are derived. At the dimensioning of a 6.78-MHz prototype, the impact of circuit parasitics on the operation are discussed. A high accuracy of circuit simulations with the measurement results proves the validity of the theoretical analysis. The prototype presented in this article demonstrates that despite its simple structure, a high peak efficiency beyond 90% is achievable. Further, the converter provides a constant output current over a wide output voltage range. Measurements of the prototype under closed-loop ON/OFF-control prove the fast transient response at startup and shutdown of the converter.

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