Pulsewidth Modulated Three-Level Buck Converter Based on Stacking Switch-Cells for High Power Envelope Tracking Applications

Juan Rodríguez, *Member, IEEE*, Juan R. García-Meré, *Student Member, IEEE*, Daniel G. Aller, *Student Member, IEEE*, and Javier Sebastián, *Senior Member, IEEE*

***Abstract*—Envelope tracking is a well-known RF technique that alleviates the efficiency problem of linear power amplifiers used in wireless communication transmitters. It consists in varying the supply voltage of the amplifier, which is commonly constant, according to the envelope of the communication signal. Therefore, a switching-mode power converter with a bandwidth of several megahertz is required to perform the fast voltage changes needed for tracking the envelope properly. Another important requirement is that the converter needs to be able to achieve high efficiency not only at peak output power, but also at low output power because it operates in that power range most of the time due to the characteristics of modern communication signals. Taking into account these requirements, the design of the converter is very challenging, especially in the case of base stations, where higher power levels are reached by means of higher voltage levels. As a result, transistors with low breakdown voltages (20–30 V), which offer the highest speed, cannot be used in the converter. In this article, a novel multilevel converter able to use transistors with low breakdown voltages is proposed to alleviate that problem. Moreover, it shows a better switching behavior than the previously proposed multilevel converters, thus reducing the switching losses and, consequently, increasing the efficiency. In order to experimentally validate the proposed topology, a 73-W prototype with a switching frequency of 8 MHz was built. The efficiency is 94% and 81.7% at peak output power and at one-tenth of peak output power, respectively.**

***Index Terms*—DC–DC power converters, envelope tracking (ET), multilevel converters, pulsewidth modulation, radiofrequency amplifiers.**

I. Introduction

NOWADAYS, wireless communication systems need to achieve very high data rates to enable the massive connectivity demand. In order to meet such a challenging requirement, the complexity of the communication signals is being increased, which is translated into larger bandwidths and higher peak-to-average power ratios (PAPRs). The amplification of these sophisticated signals requires high linearity and, consequently, linear power amplifiers (LPAs) are the preferred approach. However, the high linearity of LPAs is achieved at the expense of poor efficiency, which falls dramatically with the voltage difference between the supply voltage and the amplified communication signal. Unfortunately, the high PAPR of modern communication signals forces the LPA to operate most of the time with output voltage levels far below the supply voltage, thus damaging the efficiency.

In order to achieve both high linearity and high efficiency during the amplification process, several well-known RF techniques have been proposed, such as Envelope Elimination and Restoration, Outphasing, and Doherty [1]. Envelope Tracking (ET) is one of the most promising approaches which, in fact, is already used in handsets [2]–[7]. In particular, ET consists in varying the LPA supply voltage according to the envelope of the communication signal (see Fig. 1). In this way, the amplifier is always close to its maximum efficiency operating point, thus leading to lower power losses. In ET, the variable supply voltage is provided by a switching-mode power converter (SMPC), which is typically referred to as an envelope amplifier. The fast envelope variations demand an SMPC with a bandwidth of several megahertz. Unfortunately, the higher the SMPC bandwidth, the higher the required switching frequency (f_S) and, consequently, the higher the switching losses. Furthermore, the SMPC needs to be able to achieve high efficiency not only at peak output power, but also at low output power. The reason is that the high PAPR of modern communication signals leads to envelopes whose average values are far below the peak values, which forces the SMPC to operate in the low-power range most of the time. These requirements make the design of the SMPC very challenging, especially in the case of base stations. In this scenario, the power rise is reached by increasing the peak voltage of the envelope, which typically ranges between 28 and 48 V [2], [8]. These voltage specifications force us to use transistors with higher breakdown voltages, thus making the design very difficult due to the worst switching performance of these devices [2], [9].

Several fast SMPCs have been explored in order to meet the challenging requirements of envelope amplifiers, such as buck

Manuscript received April 23, 2021; revised July 19, 2021 and September 28, 2021; accepted November 20, 2021. Date of publication November 30, 2021; date of current version January 19, 2022. This work was supported in part by the Spanish Government under Project MCI-20-PID2019-110483RB-I00 and in part by the Principality of Asturias under Severo Ochoa Program under Grant BP20-181. Recommended for publication by Associate Editor D. Maksimovic. *(Corresponding author: Juan Rodríguez.)*

The authors are with the University of Oviedo, 33003 Oviedo, Spain (e-mail: rodriguezmjuan@uniovi.es; garciamjuan@uniovi.es; garciaadaniel@uniovi.es; sebas@uniovi.es).

Color versions of one or more figures in this article are available at https://doi.org/10.1109/TPEL.2021.3131215.

Digital Object Identifier 10.1109/TPEL.2021.3131215

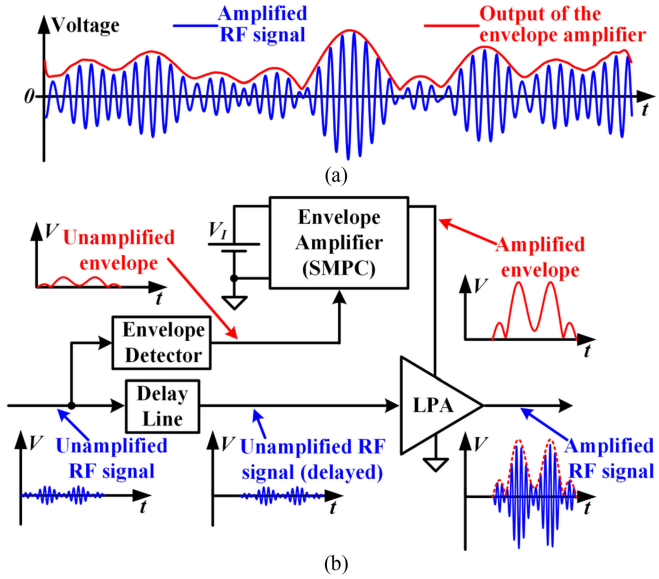


Fig. 1. Overview of an ET system. (a) Key waveforms. (b) General scheme.

converters with high-order filters [10]–[12], linear-assisted SMPCs [13], [14], pulsewidth modulated (PWM) multilevel buck converters [15]–[19], linear-assisted discrete-output multilevel buck converters [20]–[30], class-G modulators [31]–[33], multiphase buck converters [34]–[37], and combinations of them [38]–[51]. In particular, the solutions based on PWM multilevel buck converters are one of the most promising approaches due to their well-known benefits: low voltage stresses across the switches, low output voltage ripple, and low switching losses.

Aiming to combine the main advantages of previously proposed PWM multilevel buck converters, a novel topology specially conceived for high-power ET applications is introduced in this article. In this scenario, the topology achieves high bandwidth and reaches high efficiency not only at peak output power, but also in the low output power range. Three key features allow the topology to achieve low switching losses, which, in turn, explain the previously mentioned benefits.

1) A switching behavior that minimizes the number of parasitic capacitors involved in the switching process.
2) Reduced voltage stress across the switches, which enables the use of transistors with higher speed.
3) Capability to accurately track references with frequencies close to f_S, thus maximizing the bandwidth.

The rest of this article is organized as follows. The main envelope amplifiers based on PWM multilevel buck converters are reviewed in Section II. The proposed topology is described in detail in Section III. The experimental results are given in Section IV. Finally, Section V concludes this article.

II. Envelope Amplifiers Based on PWM Multilevel Buck Converters

PWM multilevel buck converters for ET are based on generating a PWM multilevel voltage (v_S) that is subsequently filtered

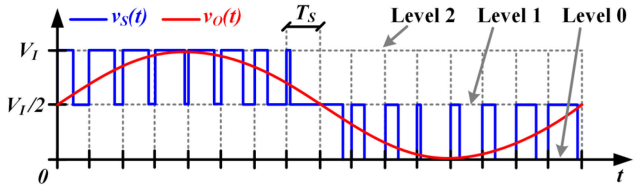


Fig. 2. Operating principle of an envelope amplifier based on a PWM three-level buck converter (note that T_S is the switching period).

to provide the desired output voltage waveform (v_O). In the case of a PWM three-level buck converter (see Fig. 2), v_S switches between half the input voltage ($V_I/2$) and the input voltage (V_I) when v_O is higher than voltage $V_I/2$ and lower than voltage V_I and, otherwise, it switches between 0V and voltage $V_I/2$ when v_O is lower than voltage $V_I/2$. It is important to note that increasing the number of levels leads to a reduction of the voltage difference between adjacent levels. As a result, the harmonics of v_S are lowered and, consequently, the output voltage ripple is reduced.

To the authors' knowledge, the first PWM multilevel buck converter for ET was proposed by Yousefzadeh *et al.* [15], where a PWM three-level buck converter implemented with a flying capacitor (FC) was used as an envelope amplifier. In this topology, two pairs of switches operate complementarily to generate a three-level PWM voltage (i.e., v_S) whose frequency is equal to twice the switching frequency. It is important to note that the switching losses of those two pairs of switches are equivalent to that of a single switch-pair with twice the switching frequency and with a voltage stress of voltage $V_I/2$. Two great benefits of that topology are, first, that it only needs a single input voltage source, and second, that the voltage stress across the switches is equal to voltage $V_I/2$. As a result, this approach has been widely adopted, especially in low-power applications implemented with CMOS technology [16], [50], [51]. Unfortunately, the topology does not have the capability to accurately track references with frequencies close to f_S due to the need of maintaining the same duty cycle (d) for two periods of v_S. This control constraint, which is mandatory in order to properly balance the FC charge, leads to a signal distortion that limits the bandwidth. The drawback becomes noticeable once the frequency of v_S (f_{PWM}) is around 15 times the maximum frequency of the reference signal (f_{Ref}) and it worsens as the ratio falls (see Fig. 3).

Rodriguez *et al.* [17] presented a PWM multiple-input (MI) buck converter, which is based on having several input voltage and a set of switches (two per input voltage source). In this case, the duty cycle can be updated in each period of v_S, thus avoiding the bandwidth limitation caused by the FC of [15]. The PWM MI buck converter requires a previous stage in charge of generating the different voltage levels. It is important to note that although this stage is not as challenging as the PWM MI buck converter because it does not need to operate with high f_S, its complexity rises with the number of levels. The main benefits of the PWM MI buck converter (i.e., low switching losses and low output voltage ripple) have been widely recognized. In general, the PWM MI buck converter has

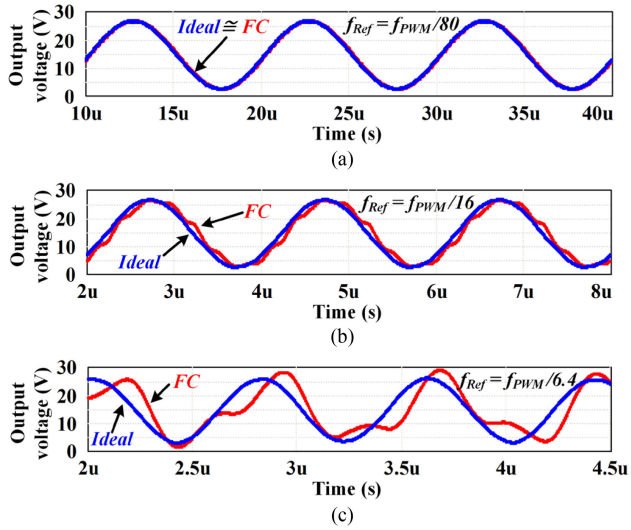


Fig. 3. Simulation of the output voltage obtained when filtering an 8-MHz PWM voltage (i.e., v_S) that tracks a sinusoidal waveform. The waveforms in blue (ideal) correspond to an ideal three-level pulsewidth modulator that updates the duty cycle in each period. The waveforms in red (FC) correspond to a quasi-ideal three-level pulsewidth modulator that maintains the same duty cycle for two periods, thus representing an FC buck converter. A fourth-order filter with a cutoff frequency of 3 MHz is applied in both cases. The frequency of the reference (i.e., f_{Ref}) is increased to show the limited capability of the three-level FC buck converter to accurately track references with frequencies close to f_{PWM}. (a) $f_{\mathrm{Ref}} = 100$ kHz. (b) $f_{\mathrm{Ref}} = 500$ kHz. (c) $f_{\mathrm{Ref}} = 1.25$ MHz.

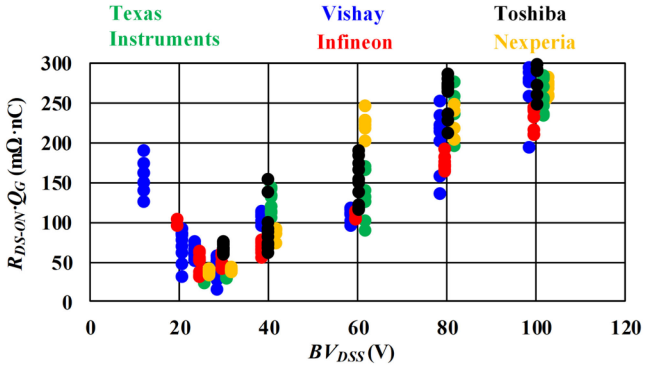


Fig. 4. Impact of voltage rating on transistors performance: power MOSFETs figure-of-merit ($R_{DS\text{-}ON}{\cdot}Q_G$) versus breakdown voltage (BV_{DSS}) for different manufacturers. Note that $R_{DS\text{-}ON}$ and Q_G are the on-resistance and the gate charge, respectively.

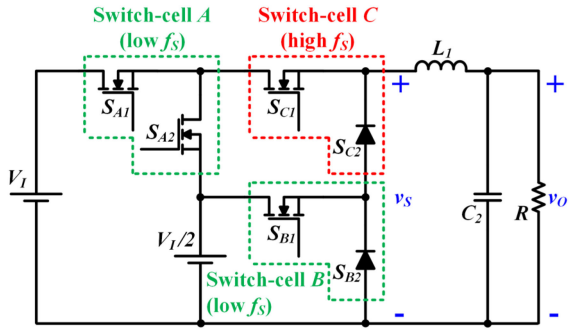


Fig. 5. Proposed PWM three-level buck converter.

been implemented with four levels or more and, although the original idea was presented with a f_S up to 4.6 MHz and a peak output power up to 90 W (the peak output voltage was 15 V) [17], the tendency during the last years has been to increase f_S up to 8 MHz to reach the higher bandwidths demanded by modern communication signals. Unfortunately, the bandwidth increase has been reached at the expense of reducing the output power or increasing the topology complexity by combining it with several of the previously mentioned approaches (i.e., multiphase buck converters, linear-assisted SMPCs, etc.) [19], [43]–[46]. The reason is that despite the outstanding results reached by the PWM MI buck converter, some drawbacks arise when higher power levels and higher switching frequencies are addressed.

The first one is that the turn-ON of a switch not only involves that switch and the one that turns-OFF, but also other switches that stay in OFF-state. The reason is that the voltage withstood by the switches depends on the switch that is activated. As a result, the turn-ON of a switch induces the parasitic capacitors of other switches that stay in OFF-state to be charged/discharged, thus increasing the switching losses. This negative aspect of the switching behavior was already reported and modeled in more detail in [21] and [52].

The second drawback is that the maximum voltage stress across the switches is V_I and, consequently, the voltage rating of the switches cannot be reduced by increasing the number of levels. Hence, the topology is not able to take advantage of the better performance offered by the transistors with lower breakdown voltages (see Fig. 4), thus losing one of the main benefits of the PWM three-level FC buck converter.

III. Proposed PWM Three-Level Buck Converter

A. Topology Description

In contrast to the PWM MI buck converter, the proposed PWM three-level buck converter (see Fig. 5) is based on stacking switch-cells, thus generating different switch-nodes instead of connecting each input voltage source to a common switch-node through a single associated switch (or a bidirectional switch). Taking into account that point, the proposed topology is noted as PWM stacked switch-cells MI (SSC-MI) buck converter. The topology avoids several drawbacks of both the PWM three-level FC buck converter and the PWM MI buck converter at the expense of increasing the number of switches. In particular, it has three key features that allow the converter to maximize the bandwidth and to reduce the switching losses.

1) There is no charge/discharge of the parasitic capacitors of those switches that stay in the OFF-state.
2) The voltage stress across the switches is voltage $V_I/2$.
3) It is able to accurately track references with frequencies close to f_S.

The topology is made up of three pairs of switches that operate complementarily (transistors S_{A1} and S_{A2}, transistor S_{B1} and diode S_{B2}, and transistor S_{C1} and diode S_{C2}), a low-pass LC filter, and two input voltage sources (V_I and $V_I/2$). As in the case of a PWM MI buck converter, a first stage is mandatory to generate the voltage source $V_I/2$ from voltage source V_I. The three pairs of switches (i.e., the three SSCs) can be classified

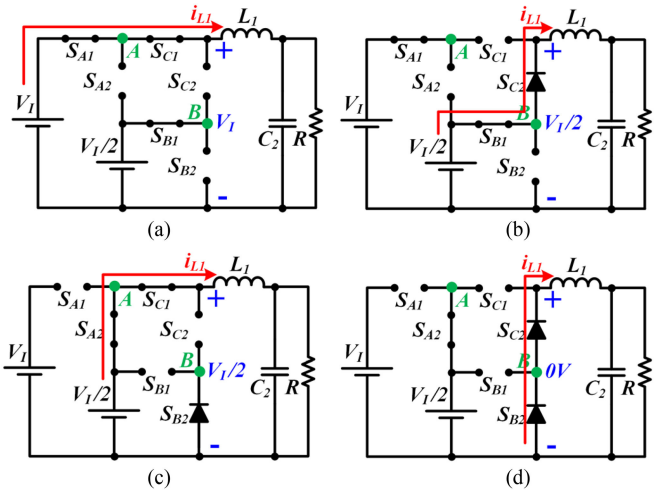


Fig. 6. Different operating modes of a PWM three-level SSC-MI buck converter. (a) High mode with $v_S=V_I$. (b) High mode with $v_S=V_I/2$. (c) Low mode with $v_S=V_I/2$. (d) Low mode with v_S=0V.

into two different categories considering their functionality and their f_S.

High f_S switch-cell: This category is made up of switch-cell *C*, which is responsible for generating the PWM voltage by switching with high f_S between the two voltage levels selected by switch-cells *A* and *B*.

Low f_S switch-cells: This category is made up of switch-cells *A* and *B*, which are responsible for selecting the voltage levels involved in the generation of the PWM voltage. They operate with low f_S because they only switch when the voltage levels of the PWM voltage have to be changed. Note that switch-cells *A* and *B* determine the high-voltage level and the low-voltage level of the PWM voltage, respectively.

B. Operating Modes

The converter can operate in two different modes depending on the output voltage level that it has to generate.

High mode: The converter provides an output voltage that ranges between voltages $V_I/2$ and V_I [see Fig. 6(a) and (b)]. In this mode, S_{A1} and S_{B1} are ON, and S_{A2} and S_{B2} are OFF. As a consequence, the voltage difference between point *A* and ground (v_A) is equal to voltage V_I. Furthermore, the voltage difference between point *B* and ground (v_B) is equal to voltage $V_I/2$. Therefore, both S_{A2} and S_{B2} withstand voltage $V_I/2$. Moreover, S_{C1} and S_{C2} switch complementarily to generate a PWM voltage (i.e., v_S) between voltages $V_I/2$ and V_I. It is important to note that when S_{C1} is ON and S_{C2} is OFF, v_S is equal to voltage V_I and the inductor current (i_{L1}) is delivered by the source V_I and flows through both S_{A1} and S_{C1} [see Fig. 6(a)]. Furthermore, when S_{C1} is OFF, i_{L1} forward biases S_{C2} and, consequently, v_S is equal to voltage $V_I/2$. Note that in this case, i_{L1} is delivered by the source $V_I/2$ and flows through both S_{B1} and S_{C2} [see Fig. 6(b)]. It can be seen that the maximum voltage withstood by both S_{C1} and S_{C2} is voltage $V_I/2$. In addition, the voltage withstood by S_{A2} and S_{B2} (i.e., voltage $V_I/2$) does not change when S_{C1} and S_{C2} switch.

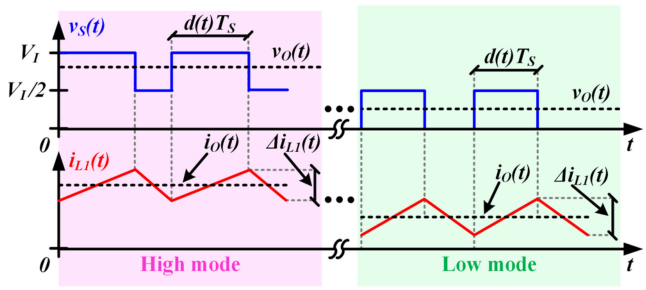


Fig. 7. Main voltage and current waveforms during both operating modes assuming quasi-steady-state conditions.

Low mode: The converter provides an output voltage that ranges between 0 V and voltage $V_I/2$ [see Fig. 6(c) and (d)]. In this mode, S_{A2} is ON, and S_{A1} and S_{B1} are OFF. In this situation, diode S_{B2} withstands approximately 0V due to its activation in part of the mode [see Fig. 6(d)] and due to its lower parasitic capacitance in comparison to the output capacitance of transistor S_{B1} (replacing diode S_{B2} with a transistor could be done to perfectly clamp that voltage to 0 V, but no remarkable benefit would be achieved). In any case, v_A is equal to voltage $V_I/2$ and v_B is equal to 0 V. Hence, both S_{A1} and S_{B1} withstand voltage $V_I/2$. As in high mode, S_{C1} and S_{C2} generate a PWM voltage (i.e., v_S) by switching complementarily. In particular, v_S is between 0 V and voltage $V_I/2$ in low mode. In this case, when S_{C1} is ON and S_{C2} is OFF, v_S is equal to voltage $V_I/2$ and i_{L1} is delivered by the source $V_I/2$ and flows through both S_{A2} and S_{C1} [see Fig. 6(c)]. As in the previous mode, i_{L1} forward biases S_{C2} when S_{C1} is OFF. Note that in this situation, v_S is equal to 0 V and i_{L1} flows through both S_{B2} and S_{C2} [see Fig. 6(d)]. As in the previous mode, S_{C1} and S_{C2} need to be able to withstand voltage $V_I/2$. Furthermore, the voltage withstood by S_{A1} and S_{B1} (i.e., voltage $V_I/2$) does not change when S_{C1} and S_{C2} switch.

In summary, S_{C1} and S_{C2} are the only devices that are switching in both modes to generate a PWM voltage (S_{A1}, S_{A2}, S_{B1}, and S_{B2} only switch when the operating mode changes in order to modify both V_A and V_B). In comparison to a PWM MI buck converter, the maximum voltage that the switches need to be able to withstand is reduced from voltage V_I (i.e., the peak voltage of the envelope approximately) to voltage $V_I/2$. In this way, the proposed topology enables the use of transistors with lower BV_{DSS} and, consequently, better performance. Another important benefit is that, as previously explained, the switching of S_{C1} and S_{C2} does not affect the voltage withstood by the rest of the switches. Therefore, the proposed converter avoids the extra switching losses that appear in a PWM MI buck converter for charging and discharging the parasitic capacitors of the switches that stay in the OFF-state.

C. Conversion Ratio

Although the output voltage of envelope amplifiers varies continuously, steady-state conditions can be assumed during one switching cycle because f_S is several times higher than the envelope bandwidth. Fig. 7 shows the switch-node voltage

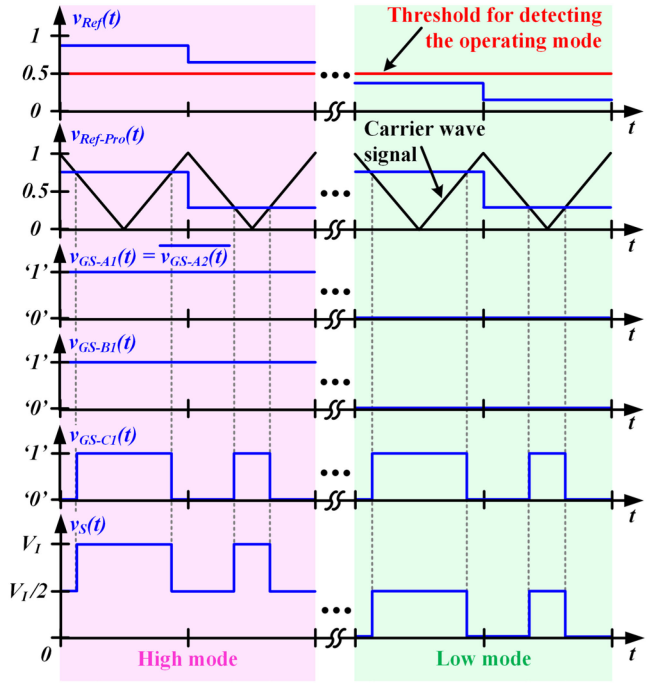


Fig. 8. Main signals of the control system in both operating modes.

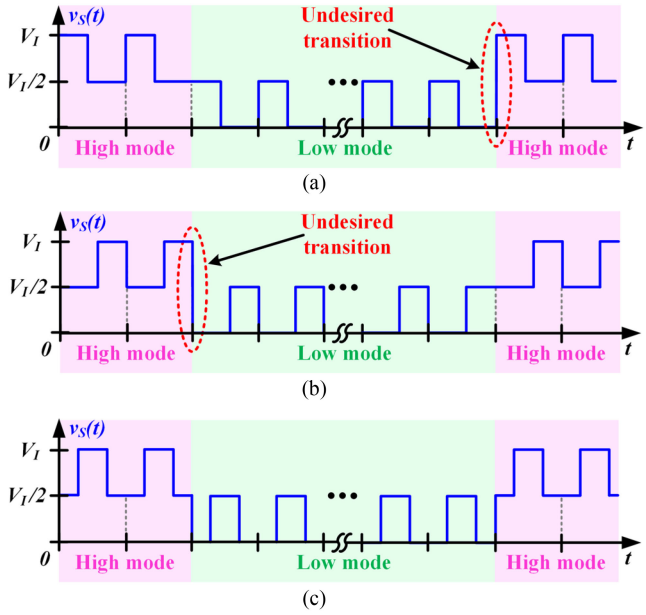


Fig. 9. Transitions between operating modes for different PWM strategies. (a) Trailing-edge. (b) Leading-edge. (c) Dual-edge.

(i.e., v_S), the output voltage (i.e., v_O), the inductor current (i.e., i_{L1}), and its ripple (Δi_{L1}), and the output current (i_O) assuming quasi-steady-state conditions. The relationship between v_O and d depends on the operating mode as follows:

$$v_O = \begin{cases} (1+d)\,\frac{V_I}{2}, & \text{in high mode} \\ d\,\frac{V_I}{2}, & \text{in low mode.} \end{cases} \tag{1}$$

The linear relationship between v_O and d facilitates the converter control for tracking an envelope. However, that linear relationship only remains valid if continuous conduction mode (CCM) is ensured. According to the analysis carried out in [17], the minimum inductor that guarantees CCM is

$$L_{1-\text{Min}} = \frac{R}{2f_S} \tag{2}$$

where R models the supplied LPA.

D. Control System

Fig. 8 shows the main signals of the control system when an envelope is tracked. As can be seen, the reference signal is sampled (v_{Ref}) and compared with a threshold that allows the control system to identify the required operating mode. That comparison determines the gate signals of transistors S_{A1} ($v_{GS\text{-}A1}$), S_{A2} ($v_{GS\text{-}A2}$), and S_{B1} ($v_{GS\text{-}B1}$) according to the explanation given in Section III-B. Note that hysteresis in the comparison between v_{Ref} and the threshold could be necessary to prevent problems caused by the noise of the sampling system. In order to modulate the pulse width of v_S by properly driving S_{C1}, the control system generates a processed reference signal ($v_{Ref\text{-}Pro}$) considering (1)

$$v_{Ref\text{-}Pro} = \begin{cases} 2\,(v_{Ref} - 0.5)\,, & \text{in high mode} \\ 2v_{Ref}, & \text{in low mode.} \end{cases} \tag{3}$$

As Fig. 8 shows, the comparison between $v_{Ref\text{-}Pro}$ and a dual-edge carrier allows the control system to generate the high-frequency gate signal of S_{C1}.

Another important point that should be addressed is the transitions between modes, which take place when the voltage levels involved in the PWM voltage generation need to be changed by switching both low f_S switch-cells. The transitions need to be performed carefully to ensure that no switch withstands voltage V_I during the transition interval. At this point, it is important to note that dual-edge PWM strategy (i.e., the pulse center is fixed in the center of the switching cycle) is more convenient than trailing-edge (i.e., the pulse is placed at the beginning of the switching cycle) and leading-edge (i.e., the pulse is placed at the end of the switching cycle) PWM strategies. The reason is that the dual-edge PWM strategy avoids voltage steps of voltage $\pm V_I$ during the transitions between modes. In trailing-edge PWM strategy, v_S changes from 0 V to voltage V_I when the transition from low mode to high mode is performed [see Fig. 9(a)]. Moreover, v_S changes from voltage V_I to 0 V when the transition from high mode to low mode is performed in the leading-edge PWM strategy [see Fig. 9(b)]. As Fig. 9(c) shows, the voltage steps are always equal to voltage $\pm V_I/2$ in the double-edge PWM strategy. This point facilitates the voltage balancing of the switches during the transitions between modes and, consequently, it was the chosen PWM strategy for implementing the control system.

Two different stages can be identified in each transition (see Fig. 10). As will be explained below, these two stages appear during both transitions, but in a different order. In stage X, transistors S_{A1} and S_{A2} are OFF, and transistors S_{B1} and S_{C1} are

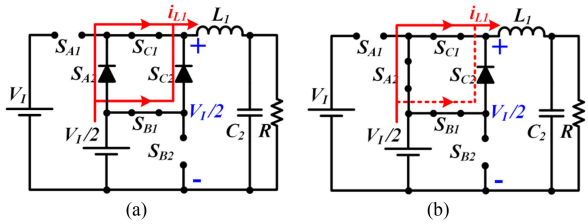


Fig. 10. Equivalent circuits for the different stages of a transition between operating modes. (a) Stage *X*. (b) Stage *Y*.

ON. In this scenario, v_S is equal to voltage $V_I/2$ and i_{L1} forward biases both the diode S_{C2} and the body-diode of transistor S_{A2}, thus generating two current paths. As will be explained below, stage *X* is a dead time period between the turn-ON/OFF of S_{A1} and the turn-OFF/ON of S_{A2}. Regarding stage *Y*, it is very similar to Stage *X*. The main difference is that S_{A2} is ON and, as a result, the upper current path carries most of i_{L1}. It is important to note that no switch withstands voltage V_I during these stages: S_{A1} and S_{B2} withstand voltage $V_I/2$.

Transition from high mode to low mode: This transition starts in the last switching cycle in low mode [see Fig. 11(a)]. In particular, the first difference with respect to the conventional operation in high mode appears when v_S needs to change from voltage V_I to voltage $V_I/2$. Just before that instant, the converter is operating in low mode according to the circuit depicted in Fig. 6(a): v_S is equal to voltage V_I and source V_I delivers i_{L1}, which flows through both S_{A1} and S_{C1}. The transition starts by turning-OFF S_{A1} instead of S_{C1} to perform the fall of v_S from voltage V_I to voltage $V_I/2$, thus reaching stage *X* [see Fig. 10(a)]. A dead time interval later, stage *Y* begins with the turn-ON of S_{A2} under zero-voltage-switching conditions. Finally, the transition ends when both S_{C1} and S_{B1} are turned OFF to perform the fall of v_S from voltage $V_I/2$ to 0 V, thus reaching the circuit operation depicted in Fig. 6(d). It is important to note that perfect synchronization for turning OFF both transistors is not mandatory. If one of them were turned OFF slightly earlier than the other one, there would be a short period of time in which only one of the two current paths depicted in Fig. 10(b) would exist. However, it would not have any remarkable impact on the converter performance.

Transition from low mode to high mode: This transition starts in the first switching cycle in high mode, just when v_S changes from 0 V to voltage $V_I/2$ [see Fig. 11(b)].) Before that instant, the converter is operating in low mode according to the circuit depicted in Fig. 6(d): v_S is equal to 0 V and i_{L1} is flowing through both S_{C2} and S_{B2}. The transition starts with the turn-ON of both S_{B1} and S_{C1} to perform the rise of v_S from 0 V to voltage $V_I/2$, thus reaching stage *Y* [see Fig. 10(b)].) As in the previous transition, the nonperfect synchronization in the turn-ON of both transistors does not have critical consequences. After that, stage *X* starts with the turn-OFF of S_{A2} a dead time interval before the rise of v_S from voltage $V_I/2$ to voltage V_I. Finally, the transition ends with the turn-ON of S_{A1} in order to perform the aforementioned rise of v_S, thus reaching the circuit operation depicted in Fig. 6(a).

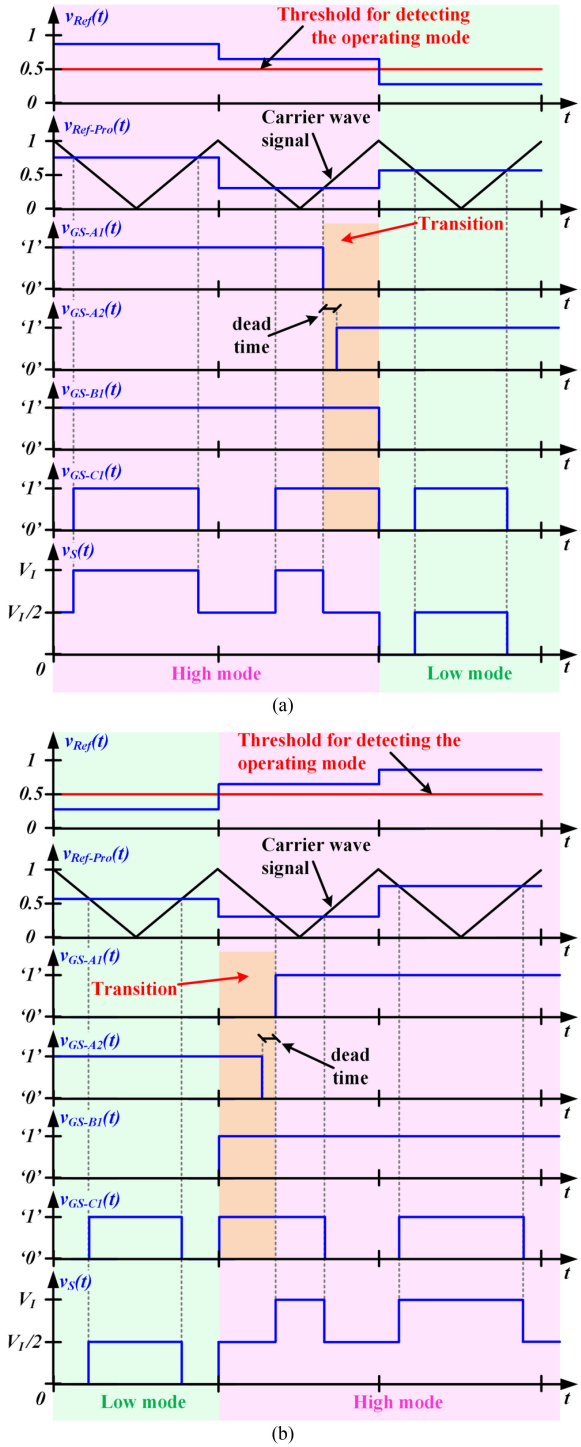


Fig. 11. Switch-node voltage and control signals when the transitions are performed. (a) Transition from high mode to low mode. (b) Transition from low mode to high mode.

E. Design Guidelines

This section is focused on providing a design procedure for selecting the output filter and f_S. Both design points have to be addressed at the same time because both determine the bandwidth and the output voltage ripple. Note that since the converter operates in open loop, the cutoff frequency of the output

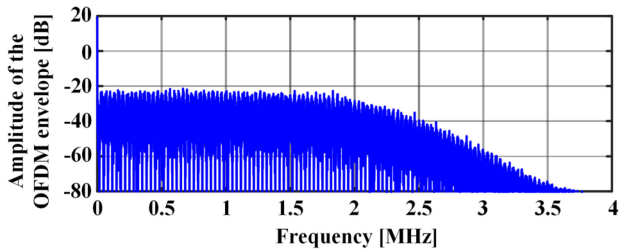


Fig. 12. Spectrum of the envelope to be tracked.

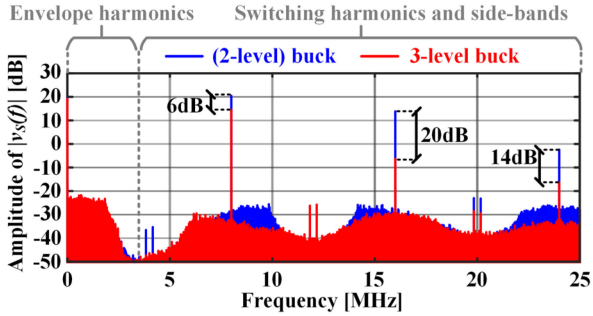


Fig. 13. Spectrum of the PWM voltage (i.e., v_S) of a conventional buck converter and a three-level buck converter with a f_S of 8 MHz when they track the envelope depicted in Fig. 12.

filter (f_C) mainly determines the bandwidth and, consequently, the speed of the envelopes that can be tracked. It is important to note that the design used in the experimental section (see Section IV) is used here as an example of the design procedure.

The first step of this design procedure is the characterization of the envelope to be tracked in the frequency domain. As an example, Fig. 12 shows the spectrum magnitude of the envelope that will be tracked by the prototype reported in Section IV. This characterization allows us to estimate the envelope bandwidth, which is around 2 MHz in our particular case.

The second step is to select f_S taking into account that it needs to be higher than twice the envelope bandwidth according to the Nyquist–Shannon sampling theorem. At this point, the general tradeoff of PWM buck-derived converters between bandwidth and output voltage ripple arises. Basically, f_S needs to be as far as possible from that boundary condition in order to reduce the output voltage ripple. However, f_S cannot be increased excessively because switching losses would become unacceptable. It should be noted that switching losses would be already the main source of power lost in the converter even if f_S is equal to twice the bandwidth. Fortunately, PWM three-level buck converters and, consequently, the proposed topology, alleviate this tradeoff because they achieve both lower switching losses and lower output voltage ripple due to the reduction of the PWM pulses amplitude from voltage V_I to voltage $V_I/2$. As Fig. 13 shows, PWM three-level buck converters achieve a remarkable reduction of the switching harmonics at the input of the filter in comparison to their conventional two-level counterpart. As a first approach, the selected f_S could be ten times higher than the envelope bandwidth. In general, that rule would lead to an excessively high f_S considering current envelope bandwidths.

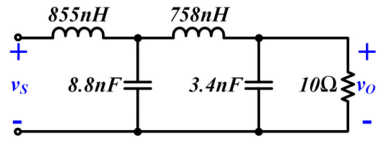


Fig. 14. High order filter chosen for tracking a 2 MHz envelope with a f_S of 8 MHz: fourth-order Legendre-Papoulis output filter.

TABLE I
MINIMUM RATIO BETWEEN THE SWITCHING FREQUENCY AND THE CUTOFF FREQUENCY OF A LEGENDRE-PAPOULIS LOW-PASS FILTER TO ENSURE CCM

Filter order	1	2	3	4	5	6
Minimum f_S/f_C	3.14	2.22	1.97	1.95	1.92	1.92

For instance, f_S would be 20 MHz if that rule is applied in our case. Following the design that will be presented in Section IV, the selected f_S is reduced to 8 MHz (i.e., four times higher than the envelope bandwidth) at the expense of increasing the output filter order.

The third step is the design of that output filter taking into account that it needs to ensure enough switching harmonics rejection to achieve an affordable output voltage ripple. In this sense, f_C should be slightly higher than the envelope bandwidth in order to achieve maximum rejection of the switching harmonics and their side-bands without distorting the envelope harmonics. A conventional second-order low-pass filter does not achieve enough rejection of the switching harmonics if f_S is below ten times the envelope bandwidth. Therefore, the filter order should be increased if that condition is not satisfied in order to achieve an affordable output voltage ripple. This is the most common situation nowadays due to the high bandwidth of modern envelopes. The guidelines for properly designing a high-order output filter can be found in [11] and [42]. In the case of the previously mentioned example, where the envelope bandwidth is 2 MHz and f_S is 8 MHz, a fourth-order Legendre-Papoulis filter with an f_C of 3 MHz was chosen following those guidelines. Fig. 14 shows the particular values of the filter components including the supplied LPA, which can be modeled as a 10-Ω load.

Another important point that should be addressed when using standardized filters is the conduction mode. As previously explained, CCM is desirable in order to operate in open loop ensuring a linear relationship between v_O and d. According to [11], the voltage ripple across the first capacitor of high-order output filters is negligible, especially for filters up to fourth order. Therefore, the first inductor of the high-order filter mainly determines the conduction mode as in a conventional second-order filter. Taking into account that the first inductor depends on the standardized filter family that is chosen for the design, the ratio between f_S and f_C determines the operating mode. Considering (2) and following the guidelines of [11], a minimum ratio can be calculated to ensure CCM for each filter family and each order. As an example, Table I presents the minimum ratio between f_S and f_C that is needed for ensuring CCM in the case of Legendre-Papoulis filters up to sixth order. It can be seen that a ratio equal or higher than 2 is enough when considering filters

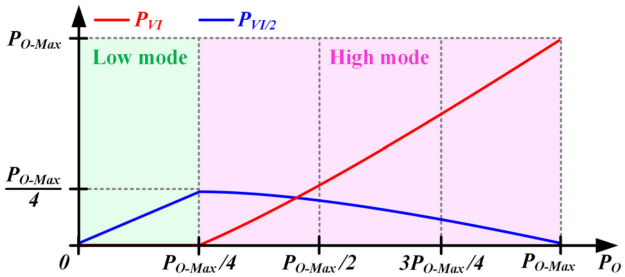


Fig. 15. Power delivered by each input voltage source.

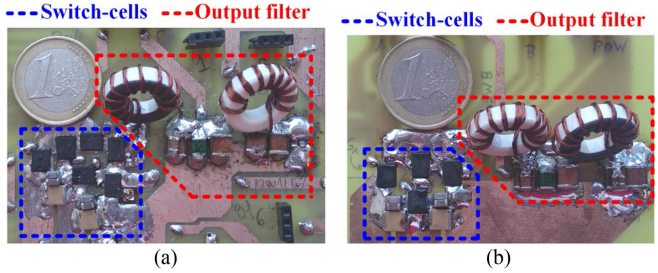


Fig. 16. Prototypes of PWM three-level topologies. (a) SSC-MI buck converter (prototype 1). (b) MI buck converter (prototype 2).

with orders higher than the third one. The ratio between f_S and f_C is equal to 2.67 in the case of the design example discussed in this section, thus satisfying the CCM condition.

F. First Stage

As indicated in Section III-A, the proposed SSC-MI buck converter requires a previous stage in charge of generating voltage $V_I/2$ from voltage source V_I. Fortunately, the design is not as challenging as that of the PWM SSC-MI buck converter because high bandwidth is not required and, consequently, the switching frequency can be low to increase the efficiency. Moreover, it is simpler than the first stage of previously proposed MI buck converters, which require more input voltage sources [17], [19], [41] and, in some cases, isolation [45]. Therefore, a conventional buck converter with a switching frequency in the range of 100 kHz fulfills the first stage requirements and, as will be shown in the experimental section, has little impact on the overall efficiency. Obviously, more complex topologies could be explored to further minimize that impact.

Studying the power delivered by each input voltage source of the PWM SSC-MI buck converter is important in order to properly address the first stage design. In low mode, voltage source $V_I/2$ delivers all output power (P_O), while in high mode, each voltage source processes part of P_O. In particular, the power delivered by voltage source $V_I/2$ can be expressed as follows:

$$P_{VI/2} = \begin{cases} P_O\left(\sqrt{\frac{P_{O-Max}}{P_O}} - 1\right), \text{ in high mode} \\ P_O, \text{ in low mode} \end{cases} \quad (4)$$

where $P_{O\text{-}Max}$ is the maximum power that the SSC-MI buck converter can deliver

$$P_{O-Max} = \frac{{V_I}^2}{R}. \quad (5)$$

It is important to note that the output power threshold between both operating modes is equal to $P_{O\text{-}Max}/4$. Fig. 15 shows both $P_{VI/2}$ and the power delivered by voltage source V_I (P_{VI}) versus P_O neglecting the power losses of the PWM SSC-MI buck converter. It can be seen that P_{VI} quickly overcomes $P_{VI/2}$ in high mode as P_O rises. Furthermore, Fig. 15 allows us to see that the maximum power delivered by the first stage is equal to $P_{O\text{-}Max}/4$ and it takes place in the threshold between both operating modes.

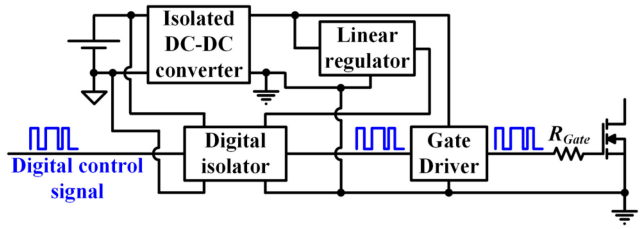


Fig. 17. MOSFETs driving system.

IV. Experimental Section

A. Description of Prototype 1

A prototype of the proposed PWM three-level SSC-MI buck converter was built to evaluate its operation as an envelope amplifier [see Fig. 16(a)]. Since more prototypes will appear along the rest of the experimental section, this one will be noted as prototype 1. The specifications of the envelope amplifier are as follows.

1) v_O ranges between 0 and 27 V.
2) The supplied LPA can be modeled as a 10-Ω load.
3) The maximum instantaneous power ($P_{O\text{-}Peak}$) is 73 W.
4) The envelope of a 64-QAM-OFDM signal with a PAPR of 12 dB is used as a reference signal. The bandwidth and the average power of the envelope are around 2 MHz (see Fig. 12) and 9.2 W, respectively.

In order to fulfill those requirements, the implemented prototype has the following design specifications.

1) Voltage V_I is 30 V and, consequently, voltage $V_I/2$ is 15 V.
2) f_S is 8 MHz.
3) A fourth-order Legendre-Papoulis filter with f_C equal to 3 MHz (i.e., the design reported in Fig. 14) is used as an output filter.

Since the maximum voltage stress across the switches is 15 V, the prototype is implemented with CSD17527Q5A 30V-MOSFETs and SS8P3L-M3/86A 30V-schottky diodes. As the transistors are not in a common source configuration, the high-frequency floating driver depicted in Fig. 17 is used for controlling each MOSFET. The circuit includes EL7156 gate drivers and I8610BC-B-IS digital isolators. The digital control signals are generated by a field programmable gate array (FPGA). In particular, the Nexys 4 DDR, which includes an Artix-7 FPGA, is the platform used for controlling the prototype. Regarding the

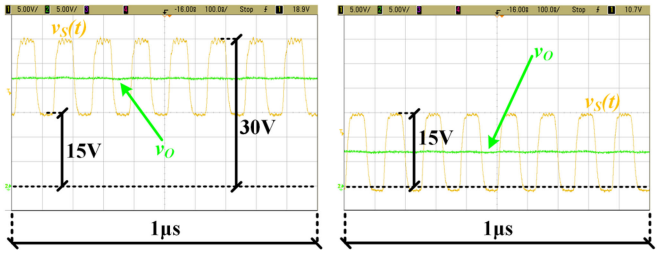


Fig. 18. Switch-node voltage and output voltage when prototype 1 operates under steady-state conditions. (a) High mode. (b) Low mode.

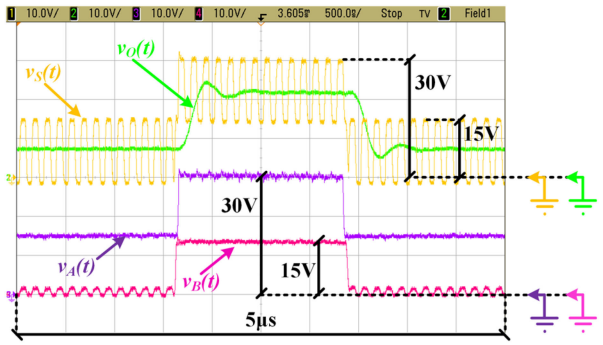


Fig. 19. Switch-node voltage, output voltage, and voltage at points A and B when prototype 1 tracks a pulse waveform that involves both operating modes.

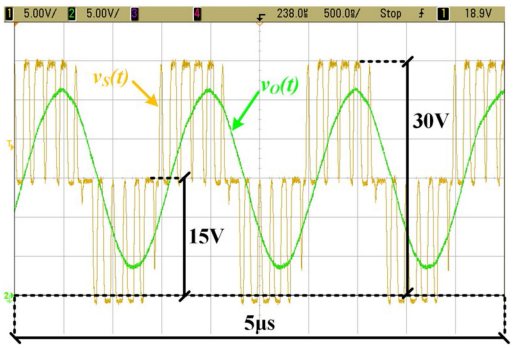


Fig. 20. Switch-node voltage and output voltage when prototype 1 tracks a 660 kHz sinusoidal test waveform with an offset of 15 V.

components of the fourth-order Legendre-Papoulis filter, T68-7 iron powder cores from Micrometals and mica capacitors from the MC(M) series of Cornell Dublier were used for implementing the inductors and the capacitors, respectively.

B. Static and Dynamic Operation

The behavior of prototype 1 was first tested under steady-state conditions (i.e., tracking a constant reference). As Fig. 18 shows, the SMPC is able to properly generate and filter both a PWM voltage between 15 and 30 V in high mode and a PWM voltage between 0 and 15 V in low mode.

After that, the dynamic behavior of the prototype was first evaluated by tracking different test signals, such as triangular, square, and sinusoidal waveforms. As an example, Figs. 19 and 20 show the results when the SMPC tracks a pulse that involves

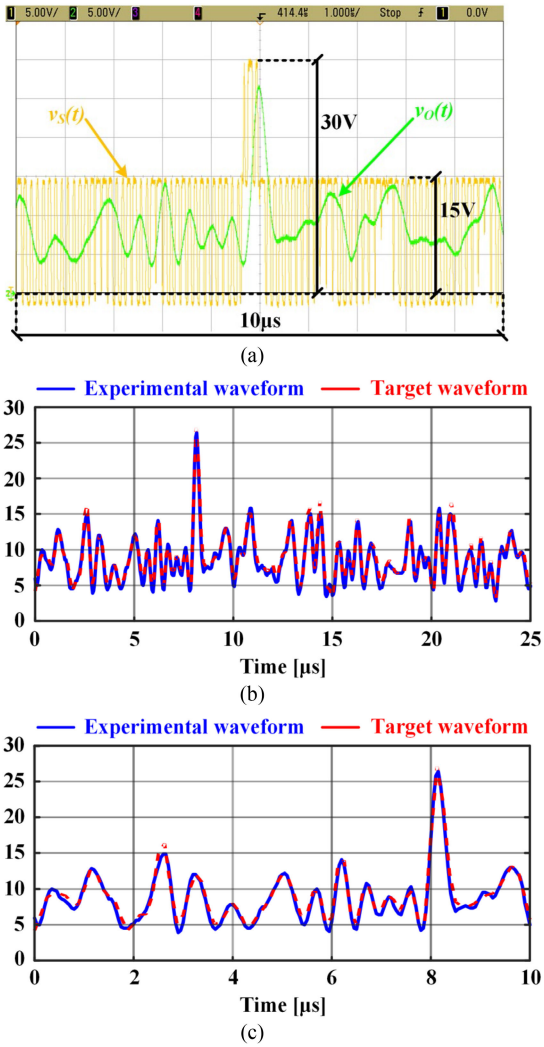


Fig. 21. Prototype 1 operating as an envelope amplifier. (a) Switch-node voltage and output voltage. (b) Comparison between the experimental output voltage and the target waveform. (c) Detail of the previous comparison.

both operating modes and a 660 kHz sinusoidal waveform with an offset of 15 V, respectively.

Finally, the dynamic behavior was completely evaluated by using the prototype as an envelope amplifier. Fig. 21 shows the results of tracking the envelope that was previously introduced in the specifications definition. The target signal is offline processed in MATLAB to determine the duty cycle sequence that must be used to properly drive S_{C1} and to identify the transitions between operating modes. After that, this information is stored in the FPGA, which generates the gate signals of the transistors according to the explanation given in Section III-D. The high PAPR of the communication signal (12 dB) leads to a peak output power around ten times higher than the average output power, which is translated into a peak output voltage around three times higher than the average output voltage [see Fig. 21(a)]. As a result, the converter operates most of the time in low mode and switches between operating modes a few times in comparison to f_S. Although the switching frequency of switch-cells A and B is variable and cannot be easily predetermined due to the arbitrary

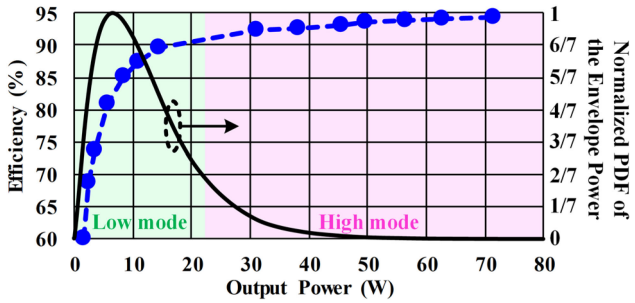


Fig. 22. Measured efficiency of the PWM three-level SSC-MI buck converter.

nature of the envelope, the results shown in Fig. 21(a) can be used to estimate that switching frequency. In this way, the estimated switching frequency of switch-cells A and B is in the range of 100 kHz. This result matches with the explanation given in Section III-A, where it was told that f_S of switch-cell *C* is much higher than that of switch-cells A and B. Fig. 21(b) and (c) shows the results when the experimental output voltage was compared with the reference. It can be concluded that the target envelope is accurately tracked. Moreover, it is observed that peaks and valleys are the points that cause the highest errors, which is a reasonable result because the highest speed is demanded in those moments.

C. Efficiency Evaluation

The efficiency (η) of the implemented prototype was evaluated under static operation for different output voltages, which was translated into different power levels, thus testing the different operating points that appear when an envelope is tracked. Fig. 22 shows both the measured efficiency and the normalized probability density function (PDF) of the envelope power detailed in the specifications. Note that the normalized PDF indicates, as concluded in the previous section, that the SMPC operates most of the time in low mode delivering around 7 W, which is approximately one-tenth of $P_{O\text{-}Peak}$. It is important to note that the efficiency results shown in Fig. 22 include the penalization caused by gate-drive losses of the MOSFETs, which were estimated from the datasheets. It can be seen that the efficiency is above 90% when the output power is higher than 15 W (i.e., around 20.5% of $P_{O\text{-}Peak}$), reaching a peak efficiency of 94.4%. The expected efficiency when the prototype tracks a particular envelope can be estimated as follows:

$$E\left[\eta\left(P_O\right)\right] = \int_{P_O=0W}^{P_{O-Peak}} \eta\left(P_O\right) \cdot f\left(P_O\right) dP_O \qquad (6)$$

where $f(P_O)$ is the PDF of the envelope power. Taking into account the PDF of the envelope power considered in the specifications, the efficiency measured around 10% of $P_{O\text{-}Peak}$ has a major impact on the expected efficiency. In fact, the expected efficiency of the prototype is 84.5% when (6) is evaluated with the information given in Fig. 22, and that result is close to the efficiency reached by the SMPC when the output power is 7 W.

TABLE II
MAIN CHARACTERISTICS OF THE MOSFETS USED IN THE THREE PWM THREE-LEVEL PROTOTYPES

MOSFET	BV_{DSS}(V)	$R_{DS\text{-}ON}$(mΩ) at 4.5V/10V	Q_G(nC) at 4.5V/10V	FOM(mΩ·nC) at 4.5V/10V
CSD17527Q5A	30	12.5/9.3	2.8/6	35/55.8
CSD18534Q5A	60	9.9/7.8	8/17	79.2/132.6
CSD18537NQ5A	60	-/10	-/14	-/140

D. Efficiency Improvement

In order to evaluate the achieved efficiency improvement with respect to a PWM three-level MI buck converter, two prototypes of this topology were implemented [prototypes 2 and 3, see Fig. 16(b)]. These new prototypes have exactly the same specifications as the first one in order to carry out a fair comparison. Furthermore, they include the same fourth order Legendre-Papoulis output filter and it is implemented with the same inductors and capacitors. The only difference between the prototypes in terms of components are the switches: 60 V switches were chosen for prototypes 2 and 3 because the maximum voltage stress across them is 30 V instead of 15 V, thus following the same safety margin rule as in the case of prototype 1. In particular, V8PM6-M3/H 60V-Schottky diodes are used in both prototypes 2 and 3. Regarding the transistors, MOSFETs that belong to the series of those used in prototype 1 were chosen (NexFET family of Texas Instruments): CSD18534Q5A 60V-MOSFETs were the ones selected for prototype 2, while CSD18537NQ5A 60V-MOSFETs were chosen for implementing prototype 3. Both 60V-MOSFETs have an $R_{DS\text{-}ON}$ close to that of the 30V-MOSFETs used in prototype 1 (see Table II). However, the higher BV_{DSS} of these 60V-MOSFETs damages the $R_{DS\text{-}ON}{\cdot}Q_G$ figure-of-merit, which is translated into higher parasitic capacitances. It is important to note that the circuit in charge of driving the MOSFETs is the same for all prototypes: the one reported in Section IV-A.

The experimental results shown in Fig. 23 allow us to evaluate the efficiency improvement. In order to facilitate the comparison, Fig. 23(b) is focused on the results at low power (from 0 to 20 W), while Fig. 23(c) highlights the differences in the high-power range (from 20 to 73 W). It can be seen that the results of both prototypes 2 and 3 are very similar, thus indicating that the small difference in terms of $R_{DS\text{-}ON}$ and Q_G between both 60V-MOSFETs candidates does not have a remarkable impact on the efficiency. Another important point is that the output power needs to be above 45 W (i.e., around 61.6% of $P_{O\text{-}Peak}$) to reach an efficiency higher than 90%, which is around three times more power than in the case of the PWM three-level SSC-MI buck converter. Moreover, the peak efficiency reached by the PWM three-level MI-buck converter prototypes is 92.4%, which is two points lower than in the case of the proposed topology. The improvement is especially remarkable in the low-power range [see Fig. 23(b)], where the efficiency-difference between the two topologies is around 10 points, reaching a peak difference close to 15 points when the output power is 5 W. Regarding the expected efficiency, it is 72.9% and 72.5% in the cases of prototypes 2 and 3, respectively. Note that these

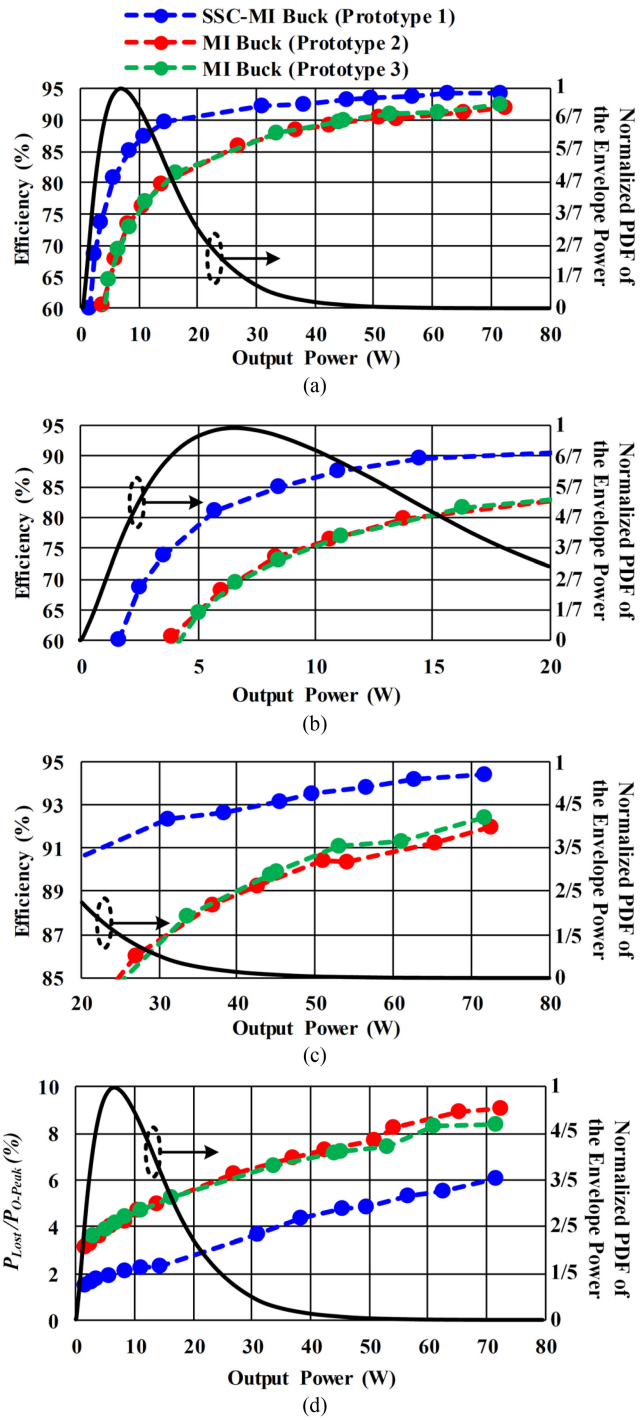


Fig. 23. Comparison between the PWM three-level SSC-MI buck converter (prototype 1) and the PWM three-level MI buck converter (prototypes 2 and 3). (a) Efficiency comparison. (b) Efficiency comparison focused on the low-power range. (c) Efficiency comparison focused on the high-power range. (d) Ratio between the lost power and $P_{O\text{-}Peak}$ for the three prototypes.

results are approximately 12 points lower than in the case of the proposed topology. Fig. 23(d) provides an insight into how these results are translated into power lost. In particular, it shows the ratio between the power lost (P_{Lost}) and $P_{O\text{-}Max}$ for the three prototypes. It can be seen that the PWM three-level MI buck converter prototypes lose around 1.4–2.2 times more power

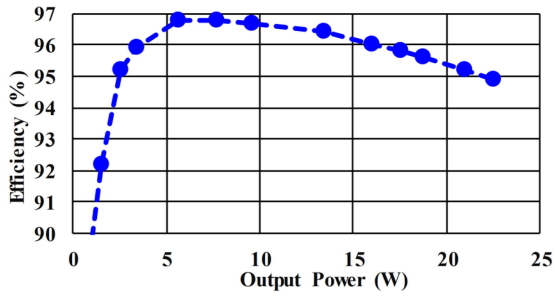


Fig. 24. Measured efficiency of the synchronous buck converter prototype.

than the PWM three-level SSC-MI buck converter. The expected value of the lost power when the prototype tracks a particular envelope can be calculated as follows:

$$E\left[P_{Lost}\left(P_O\right)\right] = \int_{P_O=0}^{P_{O-Peak}} P_{Lost}\left(P_O\right) \cdot f\left(P_O\right) dP_O. \qquad (7)$$

Evaluating (7) with the information given in Fig. 23(d) leads to expected lost powers of 2.15, 4.28, and 4.45 W in the cases of prototypes 1, 2, and 3, respectively. Therefore, the lost power in the case of the PWM three-level MI buck converter prototypes is approximately twice that of the PWM three-level SSC-MI buck converter prototype.

E. First-Stage Impact

A 25 W synchronous buck converter with a switching frequency of 100 kHz was implemented to generate voltage $V_I/2$ (i.e., 15 V) from voltage source V_I (i.e., 30 V). CSD88539ND 60V-MOSFETs are used controlled by an ISL6700IBZ bootstrap driver. The second-order low-pass filter has an inductance of 49 μH (T90-8 iron powder cores from Micrometals) and a capacitance of 10 μF, which leads to a cutoff frequency of around 7 kHz. The FPGA in charge of generating the gate control signals of the PWM three-level SSC-MI buck converter also controls this power stage.

As Fig. 24 shows, the peak efficiency of the first stage is close to 97% and it takes place when the output power is around 7 W. Moreover, the efficiency is above 95% if the output power is higher than 2.5 W. Fig. 25 shows the efficiency reduction of both the PWM three-level SSC-MI buck converter and the PWM three-level MI buck converter caused by the first stage. In both cases, the highest efficiency drop appears when the output power ranges between 10 and 40 W, reaching a maximum reduction of around 3.5 points. As a result, the expected efficiency is reduced from 84.5% to 82% and from 72.9% to 70.3% in the case of the PWM three-level SSC-MI buck converter and the PWM three-level MI buck converter, respectively.

F. Comparison to Other Approaches

Comparing the efficiency of the proposed converter with respect to previously proposed envelope amplifiers is particularly difficult because there is not a standardized method for evaluating the efficiency in this application. In some works, the efficiency is evaluated dynamically by tracking typical common

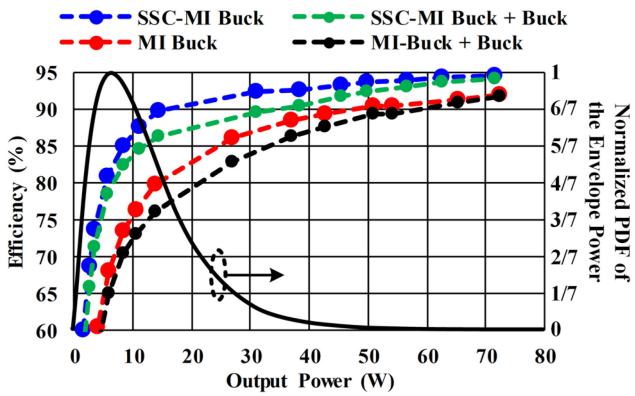


Fig. 25. Evaluation of the impact of the first stage on the efficiency of both the PWM three-level SSC-MI buck converter and the PWM three-level MI buck converter.

signals, such as sinusoidal waveforms with a certain offset or rectified sinusoidal waveforms. In other cases, the tracked waveform is the envelope of a particular communication signal that, consequently, has a particular bandwidth and a particular PAPR. Unfortunately, the PAPR of a communication signal has a high impact on the efficiency measurement and, as a consequence, the results cannot be directly compared. As in our case, other works show the efficiency measurements under steady-state conditions for different output voltage levels. These measurements in combination with the PDF of the specific envelope that has to be tracked allow us to estimate the expected dynamic efficiency by applying (6). Moreover, this method facilitates the comparison between different envelope amplifier approaches.

Table III presents the comparison to the state-of-the-art of PWM envelope amplifiers. It includes the efficiency not only at $P_{O\text{-}Peak}$, but also at $P_{O\text{-}Peak}/2$ and at $P_{O\text{-}Peak}/10$. As explained in Section IV-C, the last one is particularly interesting due to its high impact on the expected efficiency when the converter tracks the envelope of a modern communication signal. In general, previous PWM envelope amplifiers can be classified into three categories: multilevel approaches [17], [41], [46], multiphase approaches [42], [45], [47], [48], and combinations of them [45], [49]. Moreover, each category can be subdivided considering the transistor technology: silicon MOSFETs or Gallium Nitride (GaN) HEMTs.

The PWM five-level MI buck converter with a fourth-order filter reported in [46] can be considered the best-in-class result of the multilevel approaches based on silicon MOSFETs. Focusing on its results when f_S is set to 5 or 10 MHz, the topology achieves an overall efficiency that ranges between 78.4% and 86.7%. However, it should be pointed out that these results are obtained when the converter is tracking the envelope of a 64-QAM signal whose PAPR is quite lower than that of current communication signals (the average output power is $P_{O\text{-}Peak}/4$). Therefore, that efficiency would probably be lower if envelopes similar to the one considered in this article were tested.

Regarding the multiphase approaches based on silicon MOSFETs, the two-phase buck converter with a fourth-order filter reported in [42] can be considered the best-in-class approach of this category. The multiphase stage is implemented with RF MOSFETs and does not require a previous stage to generate different input voltage sources. Focusing on the results when f_S is set to 6–10 MHz, the topology achieves a peak efficiency that ranges between 91% and 92%. Moreover, the efficiency is 72%–75% when the envelope amplifier operates at $P_{O\text{-}Peak}/10$. However, it should be noted that the control in charge of balancing the inductor currents may reduce the converter bandwidth [37].

During the last years, the use of GaN HEMTs in envelope amplifiers has been explored due to the higher speed reached by these devices. The two-phase synchronous buck converter reported in [47] operates with the highest switching frequency (i.e., 50 MHz) at the expense of reducing $P_{O\text{-}Peak}$ (10 W). Despite the high switching frequency, the converter is able to reach very high efficiency (94%) at $P_{O\text{-}Peak}$. However, the switching losses cause the efficiency to fall rapidly as P_O decreases. Increasing the number of phases [48] or combining multiphase approaches with multilevel structures [49] allows the GaN-based envelope amplifier to reach high f_S (25 MHz) with high $P_{O\text{-}Peak}$ (115–140 W) and high expected efficiency (88%–91%) when tracking the envelope of modern communication signals. However, it should be mentioned that the improvement is reached at the expense of increasing the number of high-frequency transistors (eight GaN HEMTs).

As Table III presents, the PWM three-level SSC-MI buck converter achieves the highest efficiencies at $P_{O\text{-}Peak}$ and $P_{O\text{-}Peak}/10$ of the envelope amplifiers based on silicon MOSFETs. In comparison to the two-phase approaches, it can be concluded that the proposed topology achieves a remarkable increase in terms of expected efficiency (i.e., when P_O is around $P_{O\text{-}Peak}/10$) when tracking the envelope of modern communication signals at the expense of slightly increasing the complexity of the envelope amplifier. Regarding the comparison with respect to the other multilevel approaches based on silicon MOSFETs, the proposed topology not only increases the efficiency, but also reduces the complexity of both the multilevel stage and the previous stage due to the reduced number of input voltage sources. Furthermore, considering the improvement achieved with respect to the previous approaches based on silicon MOSFETs and the benefits of GaN devices reported in [48] and [49], the proposed topology could be a good candidate for reaching a bandwidth in the range of 10–20 MHz and an expected efficiency close to 85%–90% by using only a single GaN transistor (i.e., S_{C1}) that operates with high switching frequency.

Finally, a brief comparison should be made with respect to linear-assisted discrete-output multilevel buck converters [20]–[30], [38]–[40], due to the high attention that this approach has caught during the past decade. In this case, the envelope amplifier includes its own LPA supplied by a multilevel buck converter that, in general, does not have an output filter. In this way, the required f_S is reduced because the multilevel converter only switches for changing the active voltage level and, after that, the LPA makes the step-down conversion between that active voltage level and the tracked waveform. However, comparing that f_S with respect to that of the PWM envelope amplifiers shown in Table III is not very useful because the LPA of linear-assisted discrete-output multilevel buck converters constitutes the main

TABLE III
COMPARISON BETWEEN PWM SMPCS USED AS ENVELOPE AMPLIFIERS

Ref.	PWM topology	f_S(MHz)	v_O range (V)	$P_{O\text{-}Peak}$(W)	$\eta(P_{O\text{-}Peak})$	$\eta(P_{O\text{-}Peak}/2)$	$\eta(P_{O\text{-}Peak}/10)$	Are gate-drive losses considered?	Switches	Transistors technology	Input voltage sources
[17]	4-level MI buck converter	4.6	[0, 15]	90	-[*1]	-[*1]	-[*1]	No	6	Silicon	3
[41]	4-level MI buck converter with a 4th order filter	4.5	[2.5, 10]	20	-[*2]	-[*2]	-[*2]	No	8	Silicon	4
[46]	5-level MI buck converter with a 4th order filter	5	[0, 24]	40	-[*3]	-[*3]	-[*3]	Not mentioned	8	Silicon	4
		10	[0, 24]	40	-[*4]	-[*4]	-[*4]	Not mentioned	8	Silicon	4
		15	[0, 24]	40	-[*5]	-[*5]	-[*5]	Not mentioned	8	Silicon	4
[42]	Two-phase buck converter with a 4th order filter	6	[0, 28]	97	92%	90%	75%	Yes	4	Silicon-RF	1
		10	[0, 28]	97	91%	88%	72%	Yes	4	Silicon-RF	1
		14	[0, 28]	97	90%	86%	62%	Yes	4	Silicon-RF	1
		18	[0, 28]	97	90%	84%	60%	Yes	4	Silicon-RF	1
[45]	Two-phase buck converter with a 4th order filter	8	[0, 19]	50	90%	83%	52%	No	4	GaN	1
	Floating two-phase buck converter with a 4th order filter	8	[0, 24.5]	77.7	93%[*6]	88%[*6]	74%[*6]	No	8	GaN and silicon	3
[12]	Synchronous buck converter with a 4th order filter	20	[0, 20]	10	95.5%	93%	<88%	Not mentioned	2	GaN	1
[47]	Two-phase synchronous buck converter with a 4th order filter	10	[0, 20]	10	96.5%	95%	84%	Not mentioned	4	GaN	1
		50	[0, 20]	10	94%	92%	80%	Not mentioned	4	GaN	1
[48]	Four-phase synchronous buck converter with a 4th order filter	25	[0, 30]	140	94%	94%	91%	Yes	8	GaN	1
[49]	Two-phase 3-level FC synchronous buck converter with a 4th order filter	25	[0, 30]	115	97.5%	96%	88%	Yes	8	GaN	1
This work	3-level MI buck converter with a 4th order filter	8	[0, 30]	73	92.4%[*7]/ 92%[*8]	88%[*7]/ 86%[*8]	72.5%[*7]/ 69.7%[*8]	Yes	4	Silicon	2
	Proposed 3-level SSC-MI buck converter with a 4th order filter	8	[0, 30]	73	94.4%[*7]/ 94%[*8]	92.6%[*7]/ 90.5%[*8]	84%[*7]/ 81.7%[*8]	Yes	6	Silicon	2

[1] η ranges between 90.5% and 92.5% when is measured while the envelope amplifier tracks the 10 kHz envelope of two-tone signals with mean powers between 15 and 35 W (i.e., between 16.7% and 38.9% of $P_{O\text{-}Max}$). First stage impact on the efficiency is not considered.
[*2] η ranges between 83% and 88% when is measured while the envelope amplifier tracks the 100 kHz envelopes of two-tone signals with mean powers between 2.5 and 8.5W (i.e., between 12.5% and 42.5% of $P_{O\text{-}Max}$). First stage impact on the efficiency is not considered.
[*3] η is 86.7% when the envelope amplifier tracks the envelope of a 400 kHz 64-QAM signal and the average output power is equal to 10 W (i.e., 25% of $P_{O\text{-}Max}$).
[*4] η is 83.7% when the envelope amplifier tracks the envelope of a 1.6 MHz 64-QAM signal and the average output power is equal to 10 W (i.e., 25% of $P_{O\text{-}Max}$).
[*5] η is 78.4% when the envelope amplifier tracks the envelope of a 2.5 MHz 64-QAM signal and the average output power is equal to 10 W (i.e., 25% of $P_{O\text{-}Max}$).
[*6] First stage impact on the efficiency is not considered. It should be noted that one of the input voltage source must be isolated.
[*7] Without considering the first stage impact on the efficiency.
[*8] Considering the first stage impact on the efficiency.

source of power losses. As a result, the reached efficiency ranges between 50% and 80%, and it strongly depends on a lot of aspects, such as the envelope bandwidth, the PAPR of the communication signal, the number of voltage levels, or the complexity of the digital control system.

V. CONCLUSION

A novel PWM three-level buck converter for ET applications has been proposed in order to achieve both high bandwidth and high efficiency. The topology has the well-known benefits of multilevel structures: low voltage stresse across the switches, low output voltage ripple, and low switching losses. In comparison with PWM three-level FC buck converters, the proposed topology avoids the distortion caused by the need of balancing the FC charge. As a result, the converter is able to operate with a switching frequency close to the maximum frequency of the tracked reference, thus reducing the switching losses (critical in this application). Moreover, it achieves a remarkable improvement in terms of efficiency in comparison to previously proposed PWM MI buck converters due to two key features. The first one is that the proposed topology minimizes the number of parasitic capacitors involved in the switching process, thus reducing the switching losses. The second one is that the voltage stresses across the switches are reduced. Hence, transistors with lower breakdown voltages and, consequently, better performance can be used, which also leads to lower switching losses.

The proposed topology has been satisfactorily evaluated by means of a 73-W prototype with a f_S of 8 MHz. The peak efficiency is 94% and the expected efficiency is 82% (considering the first stage impact) when tracking the envelope of modern communication signals with PAPR values in the range of 12 dB. In comparison to other approaches based on silicon MOSFETs with similar f_S, the proposed topology achieves the highest efficiency not only at high output power, but also at low output power, where the major improvement is reached. This result is

particularly interesting because envelope amplifiers work most of the time at low output power due to the high PAPR of modern communication signals.

REFERENCES

[1] F. H. Raab *et al.*, "Power amplifiers and transmitters for RF and microwave," *IEEE Trans. Microw. Theory Techn.*, vol. 50, no. 3, pp. 814–826, Mar. 2002.

[2] P. Asbeck and Z. Popovic, "ET comes of age: Envelope tracking for higher-efficiency power amplifiers," *IEEE Microw. Mag.*, vol. 17, no. 3, pp. 16–25, Mar. 2016.

[3] L. K. Mathe, T. D. Marra, and T. R. Sutton, "Low-voltage power-efficient envelope tracker," U.S. Patent 8 698 558, Apr. 2014.

[4] L. K. Mathe and Y. Shi, "Envelope tracker with variable boosted supply voltage," U.S. Patent 9 837 962, Dec. 2017.

[5] Z. Popovic, "Amping up the PA for 5G: Efficient GaN power amplifiers with dynamic supplies," *IEEE Microw. Mag.*, vol. 18, no. 3, pp. 137–149, May 2017.

[6] G. T. Watkins and K. Mimis, "How not to rely on moore's law alone: Low-complexity envelope-tracking amplifiers," *IEEE Microw. Mag.*, vol. 19, no. 4, pp. 84–94, Jun. 2018.

[7] B. Kim *et al.*, "Push the envelope: Design concepts for envelope-tracking power amplifiers," *IEEE Microw. Mag.*, vol. 14, no. 3, pp. 68–81, May 2013.

[8] Z. Whang, *Envelope Tracking Power Amplifiers for Wireless Communications*. Norwood, MA, USA: Artech House Publishers, 2014.

[9] B. J. Baliga, "Power semiconductor device figure of merit for high-frequency applications," *IEEE Electron Device Lett.*, vol. 10, no. 10, pp. 455–457, Oct. 1989.

[10] M. C. W. Hoyerby and M. A. E. Andersen, "Ultrafast tracking power supply with fourth-order output filter and fixed-frequency hysteretic control," *IEEE Trans. Power Electron.*, vol. 23, no. 5, pp. 2387–2398, Sep. 2008.

[11] J. Sebastián, P. Fernández-Miaja, A. Rodríguez, and M. Rodríguez, "Analysis and design of the output filter for buck envelope amplifiers," *IEEE Trans. Power Electron.*, vol. 29, no. 1, pp. 213–233, Jan. 2014.

[12] M. Rodríguez, Y. Zhang, and D. Maksimović, "High-frequency PWM buck converters using GaN-on-SiC HEMTs," *IEEE Trans. Power Electron.*, vol. 29, no. 5, pp. 2462–2473, May 2014.

[13] F. H. Raab, "Split-band modulator for Kahn-technique transmitters," in *Proc. IEEE MTT-S Int. Microw. Symp. Dig.*, 2004, vol. 2, pp. 887–890.

[14] V. Yousefzadeh, E. Alarcon, and D. Maksimović, "Band separation and efficiency optimization in linear-assisted switching power amplifiers," in *Proc. 37th IEEE Power Electron. Spec. Conf.*, 2006, pp. 1–7.

[15] V. Yousefzadeh, E. Alarcon, and D. Maksimovic, "Three-level buck converter for envelope tracking applications," *IEEE Trans. Power Electron.*, vol. 21, no. 2, pp. 549–552, Mar. 2006.

[16] X. Liu, C. Huang, and P. K. T. Mok, "A high-frequency three-level buck converter with real-time calibration and wide output range for fast-DVS," *IEEE J. Solid-State Circuits*, vol. 53, no. 2, pp. 582–595, Feb. 2018.

[17] M. Rodriguez, P. Fernandez-Miaja, A. Rodriguez, and J. Sebastian, "A multiple-input digitally controlled buck converter for envelope tracking applications in radiofrequency power amplifiers," *IEEE Trans. Power Electron.*, vol. 25, no. 2, pp. 369–381, Feb. 2010.

[18] A. Garcia i Tormo, A. Poveda, E. Alarcón, and F. Guinjoan, "A study on multi-level PWM and asynchronous /spl Sigma//spl delta/ modulations for enhanced bandlimited signal tracking in switching power amplifiers," *IEEE Trans. Circuits Syst. I, Reg. Papers*, vol. 60, no. 6, pp. 1621–1634, Jun. 2013.

[19] A. Villarruel-Parra and A. Forsyth, "75 MHz discrete GaN based multi-level buck converter for envelope tracking applications," in *Proc. IEEE Appl. Power Electron. Conf. Expo.*, 2019, pp. 1553–1560.

[20] M. Vasic, O. Garcia, J. A. Oliver, P. Alou, D. Diaz, and J. A. Cobos, "Multilevel power supply for high-efficiency RF amplifiers," *IEEE Trans. Power Electron.*, vol. 25, no. 4, pp. 1078–1089, Apr. 2010.

[21] M. Vasić *et al.*, "Envelope amplifier based on switching capacitors for high-efficiency RF amplifiers," *IEEE Trans. Power Electron.*, vol. 27, no. 3, pp. 1359–1368, Mar. 2012.

[22] D. Diaz *et al.*, "Three-level cell topology for a multilevel power supply to achieve high efficiency envelope amplifier," *IEEE Trans. Circuits Syst. I, Reg. Papers*, vol. 59, no. 9, pp. 2147–2160, Sep. 2012.

[23] H. Xi, Q. Jin, and X. Ruan, "Feed-forward scheme considering bandwidth limitation of operational amplifiers for envelope tracking power supply using series-connected composite configuration," *IEEE Trans. Ind. Electron.*, vol. 60, no. 9, pp. 3915–3926, Sep. 2013.

[24] M. Vasić, O. García, J. A. Oliver, P. Alou, and J. A. Cobos, "Theoretical efficiency limits of a serial and parallel linear-assisted switching converter as an envelope amplifier," *IEEE Trans. Power Electron.*, vol. 29, no. 2, pp. 719–728, Feb. 2014.

[25] Q. Jin, X. Ruan, X. Ren, and H. Xi, "High-efficiency switch-linear-hybrid envelope-tracking power supply with step-wave approach," *IEEE Trans. Ind. Electron.*, vol. 62, no. 9, pp. 5411–5421, Sep. 2015.

[26] M. Liu, D. Zhang, and Z. Zhou, "Linear regulator design considerations of the serial linear-assisted switching converter used as envelope amplifier," *IEEE Trans. Power Electron.*, vol. 31, no. 5, pp. 3673–3689, May 2016.

[27] Y. Wang, Q. Jin, and X. Ruan, "Optimized design of the multilevel converter in series-form switch-linear hybrid envelope-tracking power supply," *IEEE Trans. Ind. Electron.*, vol. 63, no. 9, pp. 5451–5460, Sep. 2016.

[28] H. Xi, J. Cao, N. Liu, X. Ruan, Z. Fang, and B. Ji, "High bandwidth envelope tracking power supply with pulse edge independent distribution method," *IEEE Trans. Ind. Electron.*, vol. 66, no. 8, pp. 5907–5917, Aug. 2019.

[29] Y. Li, X. Ruan, Y. Wang, and C. Zhang, "Hysteresis voltage prediction control for multilevel converter in the series-form switch-linear hybrid envelope tracking power supply," *IEEE Trans. Power Electron.*, vol. 35, no. 12, pp. 13663–13672, Dec. 2020.

[30] H. Xi, N. Liu, Y. Xu, Y. Zhu, J. Cao, and X. Ruan, "Switched capacitor based high bandwidth envelope tracking power supply," *IEEE Trans. Ind. Electron.*, vol. 68, no. 5, pp. 4541–4546, May 2021.

[31] C. Florian, T. Cappello, R. P. Paganelli, D. Niessen, and F. Filicori, "Envelope tracking of an RF high power amplifier with an 8-level digitally controlled GaN-on-Si supply modulator," *IEEE Trans. Microw. Theory Techn.*, vol. 63, no. 8, pp. 2589–2602, Aug. 2015.

[32] N. Wolff, W. Heinrich, and O. Bengtsson, "Highly efficient 1.8-GHz amplifier with 120-MHz Class-G supply modulation," *IEEE Trans. Microw. Theory Techn.*, vol. 65, no. 12, pp. 5223–5230, Dec. 2017.

[33] T. Cappello, C. Florian, D. Niessen, R. P. Paganelli, S. Schafer, and Z. Popovic, "Efficient X-band transmitter with integrated GaN power amplifier and supply modulator," *IEEE Trans. Microw. Theory Techn.*, vol. 67, no. 4, pp. 1601–1614, Apr. 2019.

[34] A. Soto, J. A. Oliver, J. A. Cobos, J. Cezon, and F. Arevalo, "Power supply for a radio transmitter with modulated supply voltage," in *Proc. 19th Annu. IEEE Appl. Power Electron. Conf. Expo.*, 2004, vol. 1, pp. 392–398.

[35] M. Norris and D. Maksimovic, "10 MHz large signal bandwidth, 95% efficient power supply for 3G-4G cell phone base stations," in *Proc. 27th Annu. IEEE Appl. Power Electron. Conf. Expo.*, 2012, pp. 7–13.

[36] M. Rodriguez, P. F. Miaja, J. Sebastián, and D. Maksimovic, "Mismatch-error shaping-based digital multiphase modulator," *IEEE Trans. Power Electron.*, vol. 27, no. 4, pp. 2055–2066, Apr. 2012.

[37] P. Cheng, M. Vasić, O. García, J. Á. Oliver, P. Alou, and J. A. Cobos, "Minimum time control for multiphase buck converter: Analysis and application," *IEEE Trans. Power Electron.*, vol. 29, no. 2, pp. 958–967, Feb. 2014.

[38] Q. Jin, X. Ruan, X. Ren, Y. Wang, Y. Leng, and C. K. Tse, "Series–parallel-form switch-linear hybrid envelope-tracking power supply to achieve high efficiency," *IEEE Trans. Ind. Electron.*, vol. 64, no. 1, pp. 244–252, Jan. 2017.

[39] Y. Wang, X. Ruan, Q. Jin, Y. Leng, F. Meng, and X. Zhu, "Quasi-interleaved current control for switch-linear hybrid envelope-tracking power supply," *IEEE Trans. Power Electron.*, vol. 33, no. 6, pp. 5415–5425, Jun. 2018.

[40] Y. Wang, X. Ruan, Y. Leng, and Y. Li, "Hysteresis current control for multilevel converter in parallel-form switch-linear hybrid envelope tracking power supply," *IEEE Trans. Power Electron.*, vol. 34, no. 2, pp. 1950–1959, Feb. 2019.

[41] H. Huang, J. Bao, and L. Zhang, "A MASH-controlled multilevel power converter for high-efficiency RF transmitters," *IEEE Trans. Power Electron.*, vol. 26, no. 4, pp. 1205–1214, Apr. 2011.

[42] J. Sebastián, P. Fernández-Miaja, F. J. Ortega-González, M. Patiño, and M. Rodríguez, "Design of a two-phase buck converter with fourth-order output filter for envelope amplifiers of limited bandwidth," *IEEE Trans. Power Electron.*, vol. 29, no. 11, pp. 5933–5948, Nov. 2014.

[43] P. F. Miaja, M. Rodriguez, A. Rodriguez, and J. Sebastian, "A linear assisted DC/DC converter for envelope tracking and envelope elimination and restoration applications," *IEEE Trans. Power Electron.*, vol. 27, no. 7, pp. 3302–3309, Jul. 2012.

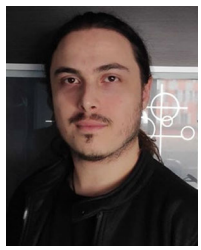
[44] P. F. Miaja, J. Sebastián, R. Marante, and J. A. García, "A linear assisted switching envelope amplifier for a UHF polar transmitter," *IEEE Trans. Power Electron.*, vol. 29, no. 4, pp. 1850–1861, Apr. 2014.
[45] P. F. Miaja, A. Rodríguez, and J. Sebastián, "Buck-derived converters based on gallium nitride devices for envelope tracking applications," *IEEE Trans. Power Electron.*, vol. 30, no. 4, pp. 2084–2095, Apr. 2015.
[46] V. Ž. Lazarević *et al.*, "A comparative analysis of two approaches in EER based envelope tracking power supplies," in *Proc. IEEE Appl. Power Electron. Conf. Expo.*, 2017, pp. 3252–3258.
[47] Y. Zhang, M. Rodríguez, and D. Maksimović, "Output filter design in high-efficiency wide-bandwidth multi-phase buck envelope amplifiers," in *Proc. IEEE Appl. Power Electron. Conf. Expo.*, 2015, pp. 2026–2032.
[48] Y. Zhang, J. Strydom, M. de Rooij, and D. Maksimović, "Envelope tracking GaN power supply for 4G cell phone base stations," in *Proc. IEEE Appl. Power Electron. Conf. Expo.*, 2016, pp. 2292–2297.
[49] S. Yerra and H. Krishnamoorthy, "Multi-phase three-level buck converter with current self-balancing for high bandwidth envelope tracking power supply," in *Proc. IEEE Appl. Power Electron. Conf. Expo.*, 2020, pp. 1872–1877.
[50] P. Mahmoudidaryan, D. Mandal, B. Bakkaloglu, and S. Kiaei, "Wideband hybrid envelope tracking modulator with hysteretic-controlled three-level switching converter and slew-rate enhanced linear amplifier," *IEEE J. Solid-State Circuits*, vol. 54, no. 12, pp. 3336–3347, Dec. 2019.
[51] X. Liu, H. Zhang, P. K. T. Mok, and H. C. Luong, "A multi-loop-controlled AC-coupling supply modulator with a mode-switching CMOS PA in an EER system with envelope shaping," *IEEE J. Solid-State Circuits*, vol. 54, no. 6, pp. 1553–1563, Jun. 2019.
[52] M. Vasic, "Wide bandwidth high efficiency power converter for RF amplifiers," Ph.D. Dissertation, Departamento de Automática, Ingeniería Eléctrica y Electrónica e Informática Industrial, Universidad Politécnica de Madrid, Madrid, Spain, 2021.

Juan Rodríguez (Member, IEEE) was born in Avilés, Spain, in 1991. He received the M.Sc. degree in telecommunication engineering and the Ph.D. degree in electrical engineering from the University of Oviedo, Oviedo, Spain, in 2014 and 2018, respectively.

From 2015 to 2019, he was a Researcher with the Power Supply System Group of the University of Oviedo. From 2019 to 2020, he was an Assistant Professor with the Technical University of Madrid (UPM). Since 2020, he has been with the University of Oviedo, where he is currently an Assistant Professor and a member of Power Supply System Group. His research interests include switching-mode power converters, the use of wide bandgap semiconductors in power converters, LED drivers for visible light communication, and techniques to increase the efficiency of RF power amplifiers.

Juan R. García-Meré (Student Member, IEEE) was born in Gijón, Spain, in 1997. He received the M.Sc. degree in telecommunication engineering in 2021 from the University of Oviedo, Oviedo, Spain, where he is currently working toward the Ph.D. degree in electrical engineering.

His research interests include high-frequency dc–dc power converters, LED drivers for visible light communication, and techniques to increase the efficiency of RF power amplifiers.



Daniel G. Aller (Student Member, IEEE) was born in Oviedo, Spain, in 1992. He received the M.Sc. degree in telecommunication engineering and the Ph.D. degree in electrical engineering from the University of Oviedo, Oviedo, Spain, in 2016 and 2021, respectively.

Since 2016, he has been working as a Researcher of the Power Supply System Group with the University of Oviedo. From 2017 to 2018, he was an Adjunct Professor with the University of Oviedo. His research interests include LED drivers for visible light communication, high-frequency dc–dc converters, and wide band-gap semiconductors.

Javier Sebastián (Senior Member, IEEE) was born in Madrid, Spain, in 1958. He received the M.Sc. degree from the Technical University of Madrid (UPM), Madrid, Spain, and the Ph.D. degree from the University of Oviedo, Oviedo, Spain, in 1981 and 1985, respectively.

He was an Assistant Professor and an Associate Professor with both the UPM and the University of Oviedo. Since 1992, he has been with the University of Oviedo, where he is currently a Professor. His research interests include switching-mode power supplies, modeling of dc-to-dc converters, single-phase high-power factor rectifiers, LED drivers, dc-to-dc converters for envelope tracking techniques and for visible light communication, and the use of wide band-gap semiconductors in power supplies.