A Comprehensive Review on Rectifiers, Linear Regulators, and Switched-Mode Power Processing Techniques for Biomedical Sensors and Implants Utilizing in-Body Energy Harvesting and External Power Delivery

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***Abstract*—This article reviews the state-of-the-art power conditioning techniques to process harvested energy from the human body and any external environmental sources surrounding the human body for powering biomedical implants and sensors. The fundamental focus of this article is to highlight the necessity of power conditioning circuits to energize implanted biomedical circuits. In addition, the underlying challenges in power conversion modules used in these low-power circuits have been discussed in detail. Power conditioning techniques for biomedical implants heavily rely on the type of sources and implants, thereby we aim to provide an elaborate discussion on the operating principle of individual technique through this review. Besides, we have also explored the suitability of each individual power processing technique inside the human body with great details. Finally, a comprehensive discussion on the limitations of existing power conditioning techniques has been presented, and the scopes to improve or mitigate those limitations have been discussed as well. The goal of this work is to present a complete guideline for future researchers to downselect a compatible power conditioning technique for a specific biomedical application.**

***Index Terms*—AC–DC, biomedical implants, cold-start, control, dc–dc, energy harvesting, linear regulator, maximum power extraction, micro-electromechanical system (MEMS), power converter, rectifiers, sensor, switched capacitor (SC), switched inductor, wireless power delivery.**

I. Introduction

IMPLANTABLE medical devices (IMDs) used for clinically assisting patients using a combination of physiological parameter sensing and varied methods of required stimulus incentives are becoming increasingly popular nowadays [1]. IMDs encompass a diversified class of devices in terms of size and driving power requirement, starting from bulky pacemaker to miniature neural stimulator, and from power-hungry total artificial heart (TAH)/left ventricular assist device (LVAD) to low power bone growth stimulator. The invasive installation nature (i.e., major surgery) and associated health risks of the IMDs often call for prolonged sustainability so that patients do not frequently need to undergo the same surgical process. Traditional energy storage devices (e.g., nonrechargeable battery) has limited energy density [2], and thus, they cannot support power-hungry circuits indefinitely. Therefore, alternative solutions are needed to meet the extended energy requirements of the IMDs to provide a prolonged lifetime. As an in-body application, the implant must not cause any discomfort and interference with the daily activities of the patient, which leads to the miniaturization of its footprint. In order to miniaturize implants and minimize the number of invasive battery-replacement surgeries during a patient's lifetime, autonomous operation of the IMDs facilitated by in-body energy harvesting and/or external power delivery is being widely perceived as an indispensable alternative to the traditional battery-powered operation of these devices. That being said, sporadic availability of some ambient energy harvesting sources on a daily basis requires an intermediate energy storage device incorporated in the IMDs. The potential energy storage devices appropriate for powering the IMDs vary with the intended applications, type of energy sources, and implant location inside a human body. The power requirement of IMDs can vary from as low as few microwatts (e.g., bone growth stimulators, etc.) to as high as ∼30 W (e.g., TAH/LVAD, etc.). A location-based list of several IMDs along with their respective power requirements is illustrated in Table I [3]–[21].

Harvesting energy from the human body and the surrounding include kinetic, triboelectric, thermoelectric (TE), glucose biofuel, photovoltaic (PV), etc. Delivering energy to IMDs from outside the body includes inductive power transfer (IPT), ultrasonic energy transfer (UET), optical link, capacitive link,

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TABLE I
POWER REQUIREMENTS FOR IMDS ALONG WITH THEIR LOCATIONS

IMDs	Bone growth stimulator	Cardiac pacemaker	Drug pump	Body area network	Cochlear implant	Retinal stimulator	Neural stimulator	MCSD-LVAD /TAH*
References	[3], [4]	[5]-[7]	[8], [9]	[10], [11]	[12]-[14]	[15]-[17]	[18], [19]	[20], [21]
Power required	5 μW ~20 μW	<100 μW	100 μW ~2 mW	100 μW~ 5 mW	600 μW ~40 mW	1 mW ~100 mW	10 mW ~200 mW	5-30 W
Power level	Ultra-low	Ultra-low	Ultra-low/low	Ultra-low/low	Low	Low	Low	High
Location in the body	Bones undergoing fractures, and fusions	Right ventricle/ right atrium	Mostly at desired body site	Desired body site	Tympanic duct of the inner ear	Outer/internal surface of the retina	Cerebellum/ epidural space	Left ventricle/ middle mediastinum

Note: *MCSD—mechanical circulatory support device; LVAD—left ventricular assist device; TAH—total artificial heart.

and other technologies yet to be explored. Despite having the advantage of autonomous and regenerative power supply, IMDs that are powered by ambient sources experience numerous challenges during implementation. These challenges arise from the extreme size constraint, limitation of the available energy resources, and unstable power/voltage levels generation from the environment. Moreover, power/voltage level requirements for the IMDs are application-specific. For example, PV cells and electromagnetic (EM) harvesters produce very low voltages (typically less than 1 V), while electrostatic (ES) devices can generate voltages at over 100 V [22]. Various sensor implants and digital complementary metal–oxide–semiconductor (CMOS) based auxiliary electronic circuits operate at or below 1.8 V, while the majority of the functional electrical stimulators and LVAD/TAH implants require higher compliance voltages ranging from 2.5 to 38 V [10], [18]. Therefore, voltage up as well as downconversion may be required depending upon the types of energy harvesters and implants powered by them. In addition, inductive and ultrasonic power delivery and the majority of the energy harvesting sources (e.g., kinetic, triboelectric, etc.) generate ac voltage in general, although a few energy harvesting sources, such as solar/PV, microbial fuel cell (MFC), TE, etc., produce dc voltage as well [1]. The former requires an ac-to-dc as well as dc-to-dc voltage conversion, while the latter only needs dc-to-dc voltage conversion so that the energy-harvesting source can comply with the implant load requirement. Therefore, a stand-alone power management interface is necessary to handle the unpredictable power/voltage levels extracted from the environment, rectify, and/or convert these voltages to proper voltage levels for powering the implantable circuits. The interface should also provide the functionality to extract the maximum possible power from the harvesting source. In addition, the power management circuit should have a low-voltage cold-start functionality when the harvester voltage levels fall below the circuit threshold values. Therefore, the basic power electronics topology for such a power management interface system between the energy harvester and the implant load electronics generally follows the architecture that is shown in Fig. 1 [22].

Any power conversion circuit used in biomedical applications is subjected to design tradeoffs. However, these specifications are somewhat different in higher power circuits than ultralow and low-power circuits. This topic has been discussed in Section II. Fig. 2 shows the classification of the power conditioning

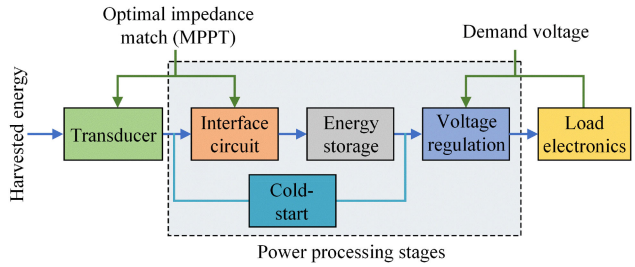


Fig. 1. Power electronics topology for energy harvesting system of IMDs [22].

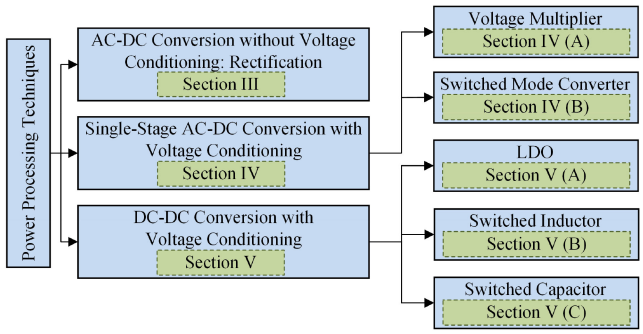


Fig. 2. Families of power conditioning techniques used in IMDs.

techniques used in IMDs. The power conversion circuit can be a simple rectifier, a single-stage direct ac–dc converter, or a dc–dc converter. The general category of a rectifier that performs ac-to-dc voltage conversion without any voltage conditioning varies from simple passive rectifiers to active rectifiers. A passive full-wave rectifier can be made from junction-based diodes (p–n/Schottky) or diode-connected MOSFETs, whereas an active rectifier uses comparator-controlled MOSFETs in place of diodes/diode-connected MOSFETs [23], [24]. A brief review of these rectifier circuits is provided in Section III. In addition, rectification as well as voltage conditioning using a single-stage direct ac–dc converter has been discussed in Section IV, which includes self-commutated capacitor-based converters, also known as voltage multipliers (VM), and ac–dc switch-mode converters containing switched inductors. Section V presents a detailed overview of the existing dc–dc voltage converters, such as low drop-out (LDO) regulators and switched-mode regulators involving one or more energy storage components.

LDO has been traditionally used for voltage down-conversion using a continuous-time circuit with a dissipative element [25]. Switched-mode regulators can be configured in both step-down (buck) and step-up (boost) configurations. The energy can be stored either in inductors, yielding to a switched-inductor converter, or in a capacitor, leading to a switched capacitor (SC) converter [26]. Section VI provides an insight into the suitability of different types of power converters based on target applications while highlighting the strengths and weaknesses of each technique. Section VII discusses the start-up issues experienced by the power converter circuits and how these issues are addressed using power electronics. Section VIII explains today's technology gap and future research directions to counteract the weaknesses of power conversion techniques highlighted in this review. Finally, Section IX draws the conclusion.

II. Power Electronic Requirements in Biomedical Applications

Depending on the source, an energy harvesting technique may generate insufficient or incompatible voltage and current levels to the implantable load demand. Hence, further processing is required, which may involve a combination of rectification, voltage conversion, smoothing, and/or regulation depending on the specific application. The aforementioned processing techniques can be different from what is employed in traditional power electronic applications. In general, output voltage harvested from ambient energy resources is typically comparable to the threshold voltage of a semiconductor switch, while the power level required for a typical biomedical application is comparable to the quiescent power consumption in traditional power electronics applications [27]. Therefore, one of the fundamental challenges of incorporating power electronics-based converters in biomedical implants is achieving high efficiency at a low power level while maintaining a small form factor. Keeping that in focus, various passive and active rectification techniques have been developed for IMDs requiring steady (dc) voltage and current. LDOs and switched power converters can provide further voltage regulation for the target implant applications.

Conduction loss associated with LDOs and multiple loss mechanisms (e.g., control loss, leakage loss, switching loss, conduction loss, etc.) associated with the switched power converters in IMDs reduces the efficiency of the converter. To that end, effective loss mitigation schemes should be in place to improve the efficiency of the converter, which in turn ensures reliable operation of low-power devices such as IMDs. At this low power level, leakage and control losses can significantly degrade the overall efficiency of the system. Control losses can be minimized by simplifying the control loops that allow for scaling power consumption with output power. Leakage current can be mitigated through on-chip power gating and voltage scaling [27]. Unlike pulsewidth modulation (PWM), pulse–frequency modulation (PFM) leads to better power efficiency at low power levels since it reduces the switching loss by changing the operating frequency as the power decreases [26]. However, the variable frequency in the PFM technique makes noise-filtering difficult. Moreover, PFM may lead to a greater voltage ripple at the output. In a nutshell, when switching loss mitigation is of concern, it is advantageous to opt for the PFM method at light load conditions, and the PWM method has the edge at heavy load conditions. Therefore, an intelligent switching scheme combining both PWM and PFM techniques depending on the load conditions can offer significant switching loss mitigation capability in biomedical implant applications [26], [28]. A significant mismatch exists between the levels of continuous harvested power and peak instantaneous power consumption of most implantable loads. Therefore, it is essential to design and integrate intermediate energy storage in the power converter interface of the implantable device to store sufficient energy that can be supplied when needed. Moreover, a cold-start/start-up circuit is also required to kick-start the conversion processes of the converter itself if the voltage levels of the low energy ambient sources fall below circuit threshold values.

While designing a power processing circuit for an IMD, the designer must ensure patient safety and security. Human exposures to electric, magnetic, and EM fields are allowed within a frequency range of 0 Hz to 300 GHz given that the thresholds of certain associated parameters specified by the safety standards (i.e., IEEE C95.1-2019/Cor 2-2020) are not violated [29]. A few examples of such parameters are internal electric field strength, specific absorption rate, and so on. According to the IEC-60601-1 standard, the use of galvanic isolation in an implantable circuit governs its maximum voltage limitation [30]. Electromagnetic interference (EMI) must also be considered as part of the power converter design for IMDs since imaging equipment, patient monitors, etc., have detection and signaling components that are very sensitive to EMI.

III. AC–DC Conversion: Rectification

Most of the IMDs require stable regulated dc input voltage, which can be delivered by a voltage converter. Since both the wireless power transfer (WPT) and kinetic energy harvesting techniques generate time-varying voltage, rectification is also needed apart from the voltage conversion. Rectification can be achieved either by passive or active topology.

A. Passive Rectification

The simplest way to achieve rectification is to use four junction-based diodes (p–n or Schottky) or diode-connected MOSFETs in different full-bridge rectifier (FBR) topologies, which are referred to as passive rectification, as shown in Fig. 3(a)–(g). The schematic of a conventional junction diode-based rectifier is depicted in Fig. 3(a) [8], [31]. This type of rectifier suffers from a significant voltage drop ($\sim$0.2 V or higher) in forward-bias mode, which contributes to $\sim$30% power loss of an ac signal with an amplitude of 1 V [24]. This implies that the junction diode-based rectifier is not a feasible choice for low-voltage low-power biomedical applications. Moreover, in the context of integrated circuits, these junction diode-based rectifiers are not available in standard CMOS processes since the required fabrication process to integrate them in the submicrometer level CMOS chips is expensive [32].

To increase the efficiency at ultralow and low-power applications, the junction diodes of conventional rectifiers are usually

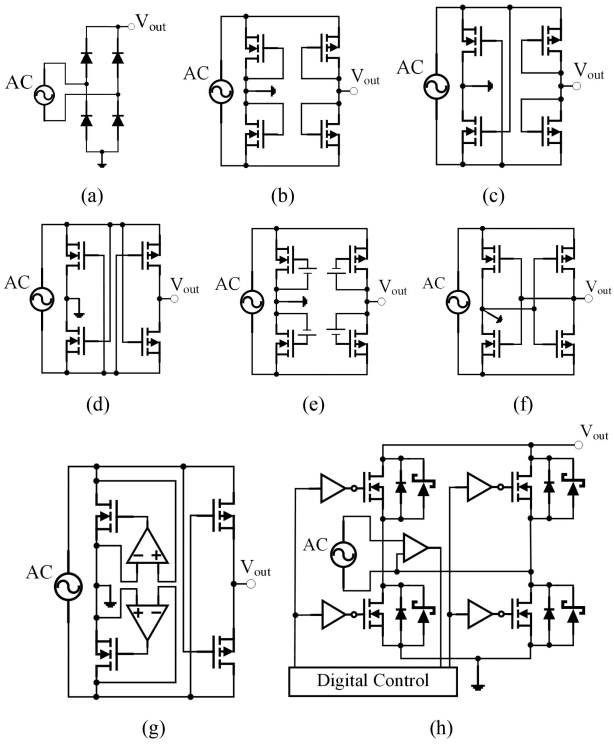


Fig. 3. Conventional ac–dc rectifier topologies. (a) Junction diode-based passive rectifier [8], [31]. (b) Diode-connected MOS passive rectifier [35]. (c) Gate-cross coupled passive rectifier [36]. (d) Differential fully gate-cross coupled passive rectifier [37]–[39]. (e) EVC passive rectifier [41]. (f) SVC passive rectifier [43]. (g) Active rectifier with cross-coupled PMOS switches [62]. (h) Synchronous rectifier using self-driven eGaN FETs [21].

replaced by MOSFETs in a diode-tied configuration using standard CMOS fabrication process [33]–[35]. These CMOS-based bridge rectifiers gained popularity in implantable biomedical applications due to their compatibility with the low-cost CMOS fabrication process, better efficiency at low voltage input signals, and so on. A simple MOSFET-based passive full-wave rectifier where the junction diodes are replaced with diode-connected MOS transistors is shown in Fig. 3(b). Efficiency at low input voltage due to the MOSFET threshold voltage ($V_{\rm th}$) drop, and therefore, the ideal maximum output dc voltage, is limited to $2 \times (V_{\rm in}$-$V_{\rm th})$, $V_{\rm in}$ being the maximum input signal amplitude [32]. That being said, the efficiencies of these MOSFET-based passive rectifiers are sensitive to $V_{\rm th}$. Moreover, this configuration may result in each MOSFET not being fully turned ON or OFF, which can increase the leakage current and voltage drop across the devices significantly [23].

To improve power conversion efficiency (PCE) in an integrated MOSFET-based FBR operation, two forms of gate cross-coupled rectifier technologies, namely gate cross-coupled rectifier and differential fully gate cross-coupled rectifier, are considered as the most popular choices [36]–[39]. In each signal cycle of the gate cross-coupled configurations, $V_{\rm th}$ of one or both of the main pass MOSFETs is replaced with the effective voltage drop across their complementary transistors, as shown in Fig. 3(c) and (d). However, this gate cross-coupled technology operates efficiently within a limited range of input power since it conducts in a reverse direction once the instantaneous value of the input ac signal becomes lower than the output dc voltage in every cycle. This periodic reverse leakage is exacerbated, and therefore, the PCE increases as the input power level grow. To improve the PCE at a higher power level, Ouda *et al.* [40] proposed a modified version of a gate cross-coupled rectifier with a self-biasing mechanism, which controls the conduction of the rectifying MOSFETs by raising their effective turn-ON voltage at high input power levels. This rectifier circuit was able to achieve more than 40% PCE and an input power range extension of more than 50% relative to the conventional gate cross-coupled rectifier.

The effect of $V_{\rm th}$ can also be mitigated by generating the required gate-bias voltage with the help of several $V_{\rm th}$ cancelation techniques, such as external-$V_{\rm th}$-cancelation (EVC), internal-$V_{\rm th}$-cancelation (IVC), and self-$V_{\rm th}$-cancelation (SVC). To generate the required gate-bias voltage, the EVC scheme uses external battery/power sources [41], as shown in Fig. 3(e). In contrast, the IVC scheme utilizes an additional circuit powered by the rectifier itself [10], [42]. Both EVC and IVC schemes suffer from leakage current when the diode-connected MOSFET is reverse-biased. They also require additional hardware leading to additional cost and increased power consumption, which may become unsuitable for low power applications. Fig. 3(f) shows a schematic overview of the SVC rectifier, which can achieve better PCE at low input power conditions compared to EVC and IVC rectifiers [43]. SVC scheme applies the gate bias voltage generated from the output voltage of the rectifier itself, thus reducing the effective $V_{\rm th}$ of the MOS transistors. One potential drawback of using such an SVC scheme may arise when the effective $V_{\rm th}$ of the MOS transistor becomes very small or even negative due to the excessive dc bias voltage, resulting in a large leakage current and, hence, reducing the overall PCE.

In recent years, more focus is being driven into the body-effect compensation technique to mitigate the threshold voltage effect. To counteract the body-effect of the MOSFETs, several recent studies proposed to change their body-source potential using additional circuits [44], auxiliary transistors, and/or separated well transistors [6], [45], [46]. This body-effect elimination method also reduces the substrate leakage current, which is beneficial to the enhancement of the overall PCE of the rectifier circuit, and by incorporating this method, 80% PCE was reported very recently in [46].

Reducing/eliminating the impact of $V_{\rm th}$ is an active area of study in present times, and many new methods are being proposed to improve existing MOSFET-based passive rectification techniques, such as by integrating additional precharged floating gate transistors [47], [48] and bootstrapping circuitry [49], [50]. However, these techniques do not perform satisfactorily at a very low input voltage level and high operating frequency. As a result, more focus is being driven to hybrid type schemes combining two or more $V_{\rm th}$ cancelation schemes in order to increase efficiency at very low input voltage levels and high operating frequencies [42], [51], [52]; 70%–80% PCE is possible even for low input voltages, as shown by Hashemi *et al.* [51].

B. Active and Synchronous Rectification

Active rectification offers another alternative to further increase the efficiency of a rectifier by reducing the conduction

losses of the pass transistors operating as switches in the deep triode region [23], [24]. Fig. 3(g) shows a simplified schematic of a typical active rectifier with cross-coupled PMOS switches. In active rectifier topology, the MOSFET is driven by a comparator and associated control circuitry (e.g., pulse generator, level shifter, etc.). The MOSFET together with its comparator is referred to as "active diode." The comparator continuously monitors the voltage drop across the MOSFET based on the source characteristics and load requirements and turns it ON or OFF in such a way that it can ensure minimal conduction loss and reverse leakage current. However, the comparator and control circuitry of active topologies presents additional power consumption. Fortunately, the overall power consumption is very low ($<1\ \mu$W) and independent of the MOSFET drain current, resulting in excellent PCE at high output power [49].

Several active rectifier topologies are reported in [32], [35], and [53]–[65] and the most basic topology of them includes two active diodes and two gate cross-coupled MOSFETs together with control circuitry and a self-body bias circuit(s). In reality, the delay time of the comparator and the gate-drive buffer limits the highest operating frequency and increases the reverse current of the rectifier, thereby compromising the output signal fidelity as well as the rectifier PCE and voltage conversion efficiency (VCE), especially at low input voltage ($<$1.5 V). To achieve high PCE and VCE by eliminating the reverse current, the power switches should be switched OFF right before the input ac signal goes below the output dc voltage. Comparators with constant/fixed artificial offset [54], [65], dynamic artificial offset [62], switched-offset biasing [57], etc., are used to compensate for the delay and to turn the power switches ON and OFF properly. A similar study by Rozgic *et al.* [53] introduced an adaptive real-time ON/OFF calibration with three adaptive delay compensating comparators that were able to achieve 82%–91% PCE and 92% VCE. In a conventional self-body bias circuit-based rectifier, the transistor parasitic capacitance may couple the ac signal from source to the body, bringing down the overall VCE and PCE. Substituting the self-body bias circuit with an adaptive body bias circuit, Cheng *et al.* were able to achieve PCE up to $\sim$92% and VCE up to 96%, the highest values reported to date. A quadvoltage rectifier suitable for both low and high compliance voltages has been proposed in [17] and [56]. The proposed architecture consists of both HV and LV half-wave active rectifiers with a mixed-voltage gate controller to avoid substrate leakage current at high compliance voltage. This scheme is particularly suitable for implantable applications (e.g., neurostimulator implant) that require a high compliance voltage of around $\pm$12 V to provide biphasic current to the target tissues besides its low-voltage requirements ($\sim\pm$1.8 V) for the digital controller and data telemetry circuits.

The high voltage ($\sim$14 V) and high-power requirements ($\sim$30 W) of LVAD or TAH impose particular challenges in designing the rectifier circuits, especially when the implants are powered by IPT at a high operating frequency [21], [67]. The challenges are mostly related to switching losses, power and volume constraints, propagation delays in the digital control path, the gate drivers and the switches, etc. The self-driven eGaN FETs in a synchronous rectifier configuration [see Fig. 3(g)] could be an optimal choice for these applications due to their high switching speeds, low ON-state resistance, and specifically low total gate charge, as reported in [19]. Employing this scheme, more than 95% PCE at 800 kHz operating frequency and $\sim$30 W of output power was reported in this study.

C. Comparison of Rectifiers in Implant Application

A comprehensive summary of the comparative performances of the published state-of-the-art passive and active rectifiers used in biomedical implant applications is presented in Table II. It is quite evident that passive rectification is usually preferred for low-voltage (less than $\sim$4 V) and ultralow-power implantable applications, such as cardiac pacemakers, vascular stent system, bone growth stimulator, and monitoring and recording system for targeted biological activities. In contrast, active rectifiers are not preferred to be used in ultralow and low-power ($<$1 mW) applications due to their additional power consumptions in associated comparators and MOSFET drivers. Therefore, if proper $V_{\rm th}$ mitigation technique and/or low-voltage threshold process are adopted, MOSFET-based passive rectifiers can offer superior performance compared to active rectifiers at lower power levels (typically less than 1 mW), which is in accordance with the findings of Szarka *et al.* [23] and Lehmann and Moghe [59]. However, some functional electrical stimulator implants (e.g., retinal, neural, and cochlear implants) and TAH/LVAD implants need output compliance voltage of 10–35 V and/or consume power in the range of milliwatt to a maximum of 30 W which, if the passive rectifier is used, may impose challenges in terms of high leakage current and substantial heat generation. In such cases, active or synchronous full-wave rectifier outperforms their passive counterpart, in terms of both PCE and VCE, at relatively high-voltage high-power implant applications. However, wide variations in input (alternating) voltage due to several factors such as human motion (vibration-based harvester), environmental variations (solar, TE generator), and coil misalignments (IPT) may affect the rectifier performance in terms of PCE, cold-start problem, etc. Adaptive reconfigurable rectifier proposed in [68] and [69] can address this issue by automatically changing its operating mode to either a voltage doubler or a rectifier circuit, depending on which one is a better choice for generating the desired output voltage at the highest possible PCE.

IV. AC–DC Conversion With Voltage Conditioning

As mentioned earlier, the output voltage of the power management interface circuitry must comply with the load specifications. The required rectification, conversion, and regulation can be performed by one of the two stages: either by single-stage circuit discussed in this section or by separate rectifier followed by the dc–dc converter circuit reviewed in Section V.

A. Self-Commutated Capacitor-Based Converters/VM

Self-commutated capacitor-based converters can simultaneously provide rectification and voltage multiplication and are often referred to as VM. VM circuits are typically low-cost designs, built for basic voltage conditioning and do not regulate the

TABLE II
SUMMARY AND COMPARISON OF THE STATE-OF-THE-ART RECTIFIER CIRCUITS USED IN BIOMEDICAL APPLICATIONS

Type	Ref	Output voltage (V)	Input signal frequency (MHz)	Power delivered (mW)	Load resistance (kΩ)	Maximum VCE (%)	Maximum PCE (%)	Target implant
Passive	[38][a]	1.2-1.8	13.56	0.005[b]	20	-	66	Vascular graft monitor system
	[16]	1.8	13.56	0.012	-	-	54.9	Body sensor network (BSN)
	[14]	2.5	0.256	0.02	-	80.2	-	Cardiac pacemaker
	[39][a]	0.5-0.84	1100	0.35	2	-	34	Coronary stent system
	[66]	0.2	1860	0.5	0.1	-	55	Drug delivery system
	[46]	2.3-3	13.56	0.632	10	70	70-87	Cardiac pacemaker (stimulation)
	[50][c]	0.39-2.92	13.56	13.72	2	88.6	87	Biomedical implants[d]
	[49]	2.0	10	-	2	78	80	Biomedical implants[d]
Active	[59]	2.88	5	4.15	2	90	80	A/V prosthesis (Stimulations)[e]
	[57]	1.2-3.56	13.56	24.8	0.5-1.8	89-93	82.2-90.1	Biomedical implants[d]
	[58]	1-2.3	1.5	~ 50	0.1-2	84-95	87	A/V prosthesis (Stimulations)[e]
	[60]	2.5	13.56	~ 50	0.1	82	84.82	Epileptic seizure (Stimulations)[e]
	[55]	2-3.46	13.56	89	0.1-1	86-96	88-92	Biomedical implants[d]
	[56]	1.8 (LV) 12 (HV)	2	10 (LV) 99 (HV)	2.3 (LV) 5.4 (HV)	82 (LV) 83.2 (HV)	82-84	Retinal Implants (stimulation)
	[53]	2.4	10	-	-	92	82-91	Neural implant (stimulation)
	[54]	1.3	13.56	-	1	89	81.9	Biomedical implants[d]
	[61]	4.5-18	1.314	-	-	92	71.4	Neural Implant (Stimulations)

Note: References are sorted in ascending order based on their delivered power levels.
[a][38] uses 8 (eight) rectifiers in series. [39] uses 2 (two) rectifiers in series.
[b]Consumed power.
[c]Results are based on simulation.
[d]Did not mention any specific implant.
[e]A/V prosthesis: audio/visual prosthesis

output dc voltage very well. They are fabricated from networks of capacitors, diodes, and switches that can be configured in a number of ways so that the dc output voltage is equal to some odd or even multiples of the peak value of the ac input voltage. Compared to full-wave rectifiers, the VM circuits offer better system efficiency as the maximum achievable power is higher due to the power being extracted at a higher voltage and a lower current, resulting in reduced conduction losses [70].

1) Passive VM: Passive VM circuits provide voltage level shifting at the expense of reduced PCE [23]. Most of the reported VM architectures use either junction-based diodes or other low-voltage drop devices (e.g., BJT, diode-connected MOSFETs, etc.) [71]–[73]. A simple voltage quadrupler circuit is shown in Fig. 4(a), consisting of three junction-based diodes and three capacitors connected in a star configuration [23]. Torah *et al.* reported efficiencies in the range of 65% at 23 μW load for an optimized Schottky-diode voltage quadrupler [72]. Interestingly, optimized Schottky diode-based VM can attain efficiencies 10% higher than the efficiency of those constructed from diode-connected MOSFETs due to the lower forward voltage threshold of the diode and additional leakage current resulting from the diode-connected MOSFETs not turning OFF completely. However, difficulty in the CMOS process fabrication of these junction-based diodes has instigated researchers to employ either diode-connected MOSFETs or active diodes in low-power biomedical applications [73]–[75]. In [73], a passive push–pull type voltage doubler, as shown in Fig. 4 (b), is implemented using diode-connected MOSFETs to power the auxiliary circuits of the implant IC. The authors reported that such devices should consume as low as 2.1% of the overall power (85 μW) consumed by the IC. Although the diode-connected MOSFETs incur more forward voltage drop compared to active diode because of their threshold voltages, they do not significantly impact the overall PCE of the VM circuits given that the load current is small.

2) Active VM: Active diode-based VM can improve the PCE significantly due to the mitigated losses in its associated switches. Lehmann and Moghe [59] reported 15% increased efficiency when active voltage doubler was incorporated in place of the passive doubler at 4 mW of output power. The principles discussed in the active rectifier sections are relevant here since active VM uses the comparator-controlled MOSFET (active diode) as its pass switch. Lee and Ghovanloo [74] proposed an active voltage doubler for functional electrical stimulators, which can provide 2.84 V dc output across 1 kΩ load from a 1.46 V peak ac input at 13.56 MHz. This active topology was able to achieve the highest PCE of 79% ever reported at this high frequency, thanks to its high-speed comparators equipped with external offset control functions that can compensate for both turn-ON and turn-OFF delays, as shown in Fig. 4(c).

3) Comparison of VMs in Implant Application: Implant applications that naturally require ultralow power, such as cardiac pacemaker, bone growth stimulator, monitoring, and recording system for targeted biological activities, usually incorporate passive VMs for rectification since they do not significantly impact the overall PCE in such low power applications. At low excitation frequency (sub-100 Hz), charge-up losses within voltage source–capacitor loops dominate over the MOSFET conduction losses, while at higher frequencies conduction losses become more dominant [23], [76]. Therefore, passive VMs are also preferred to their active counterpart at the low excitation frequency. In contrast, active VM is typically preferred when power is harvested from high-frequency sources (e.g., inductive/UET)

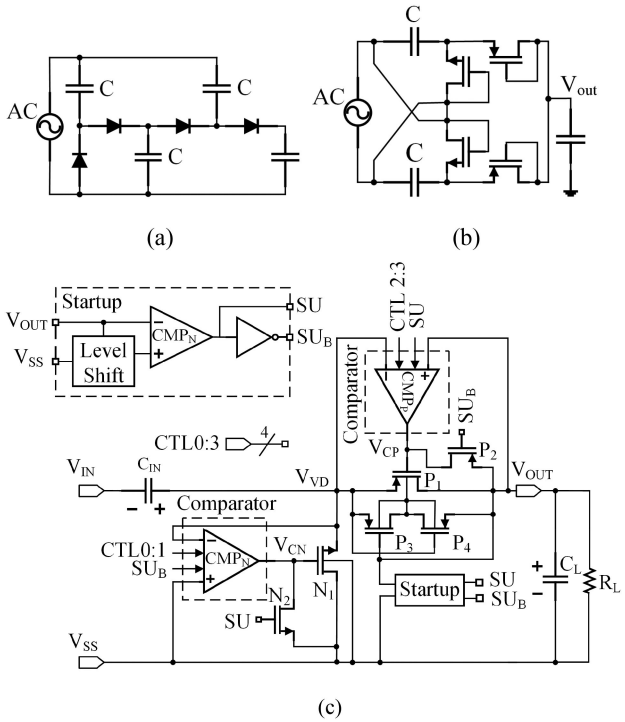


Fig. 4. Various VM circuits. (a) Voltage quadrupler circuit in star configuration [23]. (b) Push–pull voltage doubler described in [73]. (c) Active voltage doubler proposed in [74] . Here, N_2 and P_2 are start-up switches driven by a complementary pair of start-up signals S_{UB} and S_{U}.

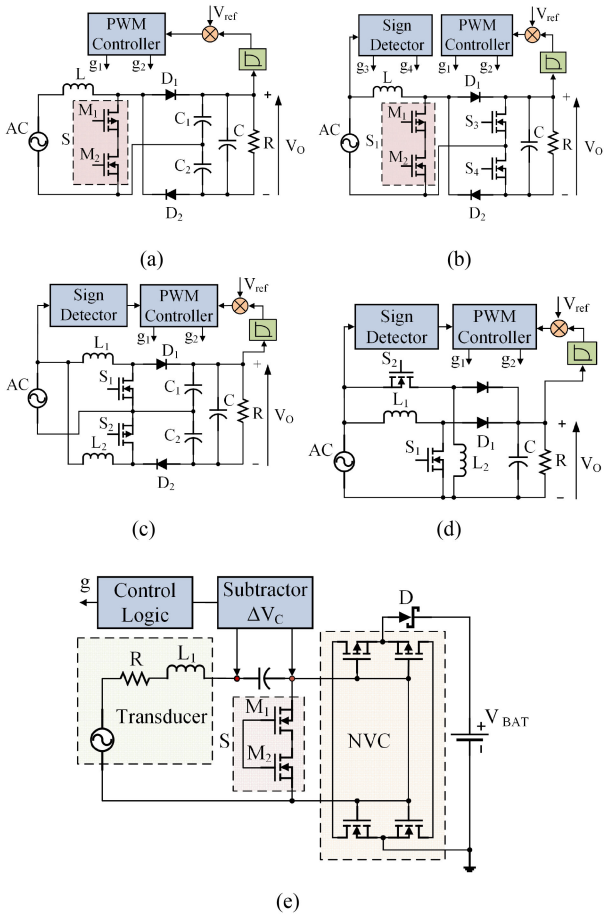


Fig. 5. EM harvester-specific single-stage switched-mode ac–dc converter topologies. (a) Single inductor with split capacitor [81]. (b) Single inductor with secondary-side switches [78]. (c) Dual boost converter [80]. (d) Combined boost and buck–boost converter [79]. (e) AC–DC chopper combined with an NVC [83].

to the implant. In addition, active VM can outperform passive VM to power relatively high-voltage, high-power biomedical implants such as neurostimulators, TAH/LVAD, etc.

4) Harvester-Specific Interactions: VM circuit designed for piezoelectric (PE) generators can use the piezoelement's internal capacitance as part of the circuit. However, VM is unable to apply complex conjugate matching to compensate for the relatively large capacitance in the PE transducer in order to extract maximum power from it [77]. Extremely low-voltage (∼0.1–1 V) and high-current output of EM generators may result in poor PCE in VM circuits (as well as in bridge rectifiers) due to the losses in diodes or diode-tied MOSFETs. Moreover, the bridge rectifiers and VM circuits behave as nonlinear loads making the design extremely difficult to track the maximum power from the energy harvesters [78], [79]. To overcome these issues, timed switching elements in ac–dc converter circuits for kinetic energy harvesters are proposed in the literature and discussed in the following section(s).

B. Direct AC–DC Switch-Mode Converters

Direct ac–dc switch-mode converter does not require a separate rectifier stage and usually incorporates switched inductors to pave the way for extracting maximum energy from the kinetic energy sources besides their regular ac–dc conversion. They can operate with very low input voltages and offer more effective current and voltage regulation than VM topologies [80]. The power profiles of the kinetic energy harvesters vary with human motion, environmental variations, etc., which implies that there exists a maximum power output point. These kinetic energy-based microgenerators are generally spring–mass–damper- based systems, whose damper characteristics (or damping force) need to be optimized to extract maximum energy for powering potential IMDs. The preferred way to achieve this optimal damping force is to adjust the effective output impedance of the EM and PE transducers or electric field between the two electrodes of the ES transducer with the help of direct ac–dc switch-mode power converters [80]. In light of the aforementioned discussion, it is evident that direct ac–dc power converters can extract maximum power from kinetic energy harvesters besides regular voltage conditioning.

1) EM Harvester-Specific Switched-Mode AC–DC Converters: Fig. 5 illustrates the direct ac–dc boost converter topologies proposed in [78] and [80]–[83], and most of them exploit the EM generators as input sources. These converters operate in discontinuous conduction mode (DCM) to reduce the inductor size requirements and MOSFET's power dissipation, making them suitable for exploiting low-voltage low-power EM harvester. Converter topologies shown in Fig. 5(a) and (b) are single inductor topologies, where the dc bus relies on two split capacitors in circuit (a) [81] and two additional MOSFET switches referred to as secondary-side switches in circuit (b) [78]. Both

converters produce a regulated dc output voltage of 3.3 V from an ac input voltage range of 0.2–0.8 V and achieve conversion efficiency in the range of 60% at an input power level of around 100 mW. However, the split-capacitor architecture is simpler since it uses a reduced number of switching devices and requires no additional sensors to detect the polarity of the input voltage. In contrast, direct ac–dc converters equipped with two-stage regulation and input polarity sensors have been proposed in [79] and [80] and are shown in Fig. 5(c) and (d). The positive and negative input voltage cycles are processed by two boost converter stages in circuit (c) [80] and a buck–boost and a boost converter in circuit (d) [79]. The efficiency of the dual boost converter is reported as 50% with an input power of 50 mW, whereas the combination of boost and buck–boost converters achieves an efficiency of 61% with an input power of 100 mW. Since the output dc bus of the dual boost converter is split into two series-connected capacitors that suffer from large voltage drop when connected to the load, it is less efficient compared to the converter comprised of boost and buck–boost topologies. To achieve high conversion efficiency, Bolt *et al.* proposed an ac–dc converter that implements an ac–dc chopper combined with a negative voltage converter (NVC) consisting of rectifying cross-coupled MOSFETs connected in a bridge configuration [see Fig. 5(e)] [83]. Instead of using an external switched inductor, this architecture exploits an EM generator's internal inductance. This converter achieved 88%–90% PCE with a quiescent current of 250 nA.

2) ES Harvester-Specific Switched-Mode AC–DC Converters: It is worth noting that, unlike EM and PE generators, the damping force, being voltage controlled, can be dynamically optimized for ES generators. However, one of the main challenges for designing a converter for an ES generator is to minimize the parasitic capacitance connected to the generator, which will otherwise affect the overall converter efficiency [80]. In addition, a significant amount of voltage down-conversion is needed for powering low-power implant loads because of the high voltage (10–220 V) generated by the ES generator. In [84], a power processing circuit for a constant-charge ES generator was proposed. The design of the power processing circuit includes a buck converter to regulate the high output voltage from the ES generator to suit the power demand of the implant electronics. However, as the generator voltage rises, the depletion layer capacitance of the blocking junction of the high-side MOSFET forms a parasitic capacitance in parallel with the generator capacitor, consequently further reducing the converter efficiency. Mitcheson *et al.* presented a modified fly-back converter as a viable candidate for the power processing of biomedical implants while addressing the above-mentioned issues [80].

3) Piezoelectric (PE) Harvester-Specific Switched-Mode AC–DC Converters: The output impedance of a PE harvester is dominated by capacitive reactance, which becomes prohibitively large at the low operating frequency of such harvester. Therefore, the optimum load for maximum power transfer would require a significantly large inductance, possibly in the order of several tens to hundreds of Henry [23]. A possible solution to the above-mentioned problem is to enhance the conversion efficiency by flipping/reversing the PE voltage at zero-crossing instants of the velocity of the proof mass (i.e., electrical current), as depicted in

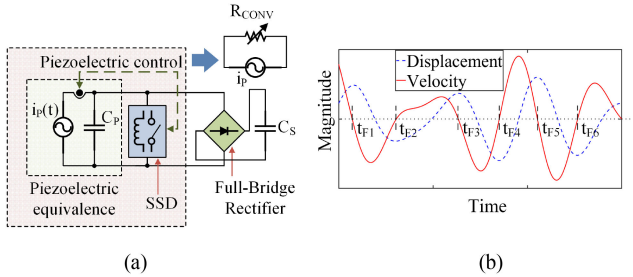


Fig. 6. Voltage flipping solution by implementing the SSD method [85], [86]. Here, t_{Fi} corresponds to the time instants when piezovoltage is induced by the switching process on zero speed values ($i = 1, 2, \ldots$).

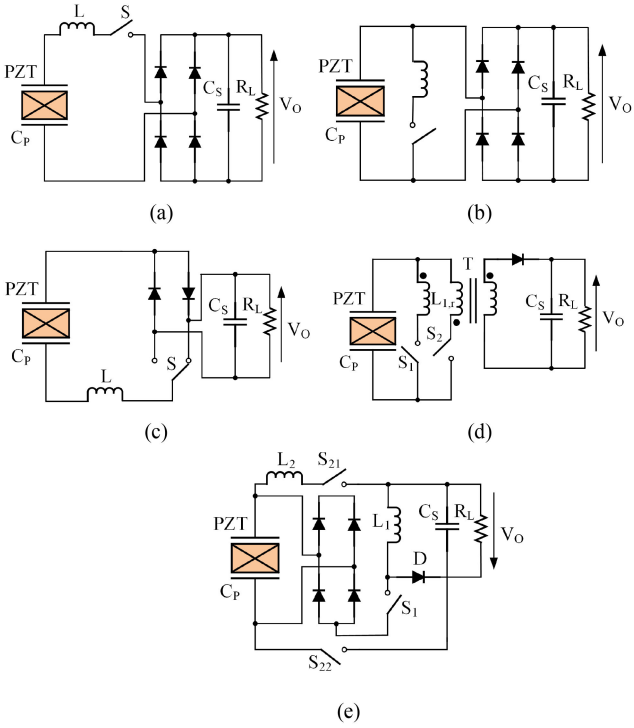


Fig. 7. Different SSHI topologies for PE energy harvesting. (a) Series-SSHI topology [23]. (b) Parallel-SSHI topology [23]. (c) Optimized series-SSHI topology [89]. (d) SSHI-MR topology [90]. (e) Series-SSHI with pulsed energy feedback [92].

Fig. 6 [85], resulting in maximum generated voltage, which exceeds the peak open-circuit voltage. The voltage flipping allows the circuit to maximize the harvested energy by extracting stored charge within the internal capacitances of the PE harvester at the extremes of the displacement cycle; otherwise, this energy would become waste. This voltage flipping can be implemented in a way, namely the synchronized switch damping (SSD) method, where a resonant electrical network is formed by placing an inductor between the harvester device and the rectifier. The combined PE capacitance (C_P) coupled with the rest of the harvesting circuit acts as a tunable resistor (R_{CONV}), as shown in Fig. 6 [86].

a) Synchronized Switch Harvesting on Inductor (SSHI): Voltage flipping using the SSD method can easily be realized by the *LC* resonant loop formed in the SSHI topologies, as shown in Fig. 7 [88]. Such SSHI topologies achieve an increase in the power gain above 4–15 times compared to direct charging

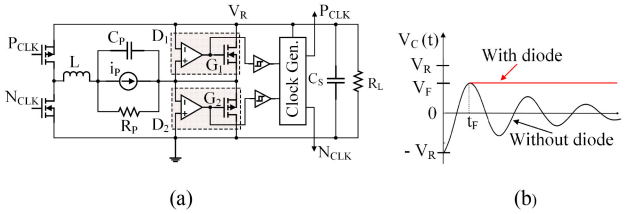


Fig. 8. (a) SSHI circuit incorporating active diode-inserted-resonant-loop [77] and (b) PZT internal capacitor voltage. Here, t_F = the optimal flipping time and V_F = the flipping voltage = V_R-V_D, V_D = diode voltage drop. The additional active diode in each resonant loop holds the capacitor voltage upon reaching its peak in the opposite polarity at t_F.

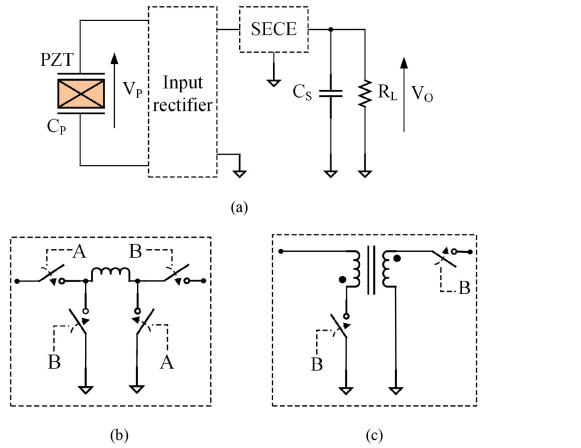


Fig. 9. (a) Structure of a power converter stage based on SECE topology for piezoelectric transducers. (b) Boost topology for SECE. (c) Flyback topology for SECE [99].

through bridge rectifiers only [87], [88]. The most common forms of SSHI circuits are series-SSHI and parallel-SSHI, where series-SSHI uses an inductor in series with a rectifier, whereas a parallel-SSHI configuration uses a parallel inductor, as depicted in Fig. 7(a) and (b), respectively. Optimized series-SSHI shown in Fig. 7(c) provides further efficiency improvement by replacing four diodes of the bridge rectifier with two diodes and a selector switch [89]. The authors reported an increase in harvested energy output as much as 120% of the parallel-SSHI circuit. Garbuio *et al.* proposed a series-SSHI circuit with a transformer called SSHI using magnetic rectifier (SSHI-MR), and the topology is shown in Fig. 7(d) [90]. This SSHI-MR can facilitate start-up and, most importantly, can maintain good efficiency at a very low input voltage level due to having a lower number of energy dissipating discrete components (i.e., diodes). Lallart *et al.* presented a rectifier that can automatically switch between SSHI-MR and parallel-SSHI topology according to the harvester voltage levels [91]. Lallart and Guyomar proposed a series-SSHI with pulsed energy feedback to the PE element [92], as shown in Fig. 7(e), and achieved ten times power gain compared to the conventional SSHI technique presented in [93]. To increase the efficiency of PE energy harvesting over a wide operation range, integration of SSHI and maximum power point tracking (MPPT) is proposed in [94].

A significant amount of research is dedicated to overcoming the design challenges of SSHI that lie in the precise timing control to switch OFF at the peak voltage (voltage flipping) with minimal circuit complexity of the controller. This feature is critical since the efficiency of the circuit is sensitive to the flipping time [77]. For instance, in order to achieve precise timing control, Sanchez *et al.* [95] used an external variable resistor, whereas Ramadass and Chandrakasan [96] introduced an external 8-bit digital module, resulting in 4–5.8 times more power extraction compared to the state-of-the-art standard FBR or voltage doubler with the same displacement amplitude. To avoid external tuning circuits and their associated power consumption, Aktakka *et al.* [97] and Lu and Boussaid [98] proposed a parallel-SSHI topology where an additional p–n junction diode is inserted in the resonant loop followed by an FBR. The additional diode enforces a unidirectional flow of the loop current, which maintains the capacitor voltage upon reaching its peak in the opposite polarity, thereby eliminating the need to tune the switch OFF at the precise time (t_F) of capacitor peak voltage, as shown in Fig. 8(b). Unlike [97], [98], the design approach proposed in [77] inserts an active diode (instead of a p–n junction diode) for each resonant loop and does not require any subcircuit for polarity detection, which further simplifies its controller operation [see Fig. 8(a)]. This active diode-inserted-resonant-loop approach achieves a maximum PCE of 85% and output power of 136 μW in addition to its 210% improvement in the maximum power extraction compared to a conventional rectifier FBR.

b) Synchronous Electrical Charge Extraction (SECE): One of the main drawbacks of the SSHI technique is that the efficiency is bias-dependent and quite low in extreme load conditions [99]. The SECE method is another well-known energy extraction technique for PE harvesters where the generated power is almost load-independent [99]–[108]. Unlike the SSHI technique, in SECE, energy is first transferred from the transducer to an inductor upon detection of the peak voltage. This energy translates to the output through two resonant circuits after that, in a way similar to a boost converter, as shown in Fig. 9 [99]. This unique topology makes the efficiency of an SECE independent of the output bias, while the complete removal of electrical charge at each activation doubles the peak voltage. Lefeuvre *et al.* demonstrated that the SECE circuit achieved a power improvement of 400% compared to the FBR technique [100]. In order to reduce losses on freewheeling diodes, SECE can also be implemented with a flyback topology [107]. To achieve better performance and simplify the enhanced complexity of the control and switching mechanism associated with SECE, several enhancements were made on the basic SECE topology, such as the optimized SECE (OSECE) by Wu *et al.* [101], adaptive pulsed SECE by Hehn *et al.* [108], the self-powered OSECE by Liu *et al.* [102], SECE with residual charge inversion by Dini *et al.* [99], and SECE with rectifier-free, bidirectional converter topology by Shareef *et al.* [103]. Nevertheless, these SECE rectifiers are not suitable for strongly-coupled PE harvesters. For designing an SECE converter in a strongly-coupled PE environment, some guidelines are provided in the tunable SECE by Lefeuvre *et al.* [104], the synchronous electric charge partial extraction by Xia *et al.* [105], and short-circuit synchronous electric charge extraction based on a short-circuit tunable phase by Morel *et al.* [106].

c) Comparison and Implementation of SSD Methods in Implant Applications: Parallel and series-SSHI methods may exhibit outstanding performances under periodic vibrations

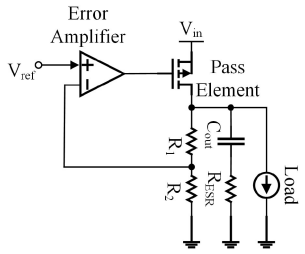


Fig. 10. Schematic of a conventional LDO regulator [117].

from internal organs (lung and cardiac motions, blood circulations, etc.). However, in most of today's implantable applications, kinetic energy is extracted from the movement of skeletal muscle under voluntary control, where the vibrations are not periodic and mechanical stimuli occur at unpredictable rates. The SSHI scheme presents inherent weaknesses of poor impedance matching and voltage regulation while harvesting such sporadic vibrations (i.e., variable amplitude) [109]. In contrast, the SECE scheme outperforms its SSHI counterparts in terms of power gain while harvesting energy from weakly coupled PE harvester systems or PE harvester systems vibrating under OFF-resonant conditions due to the unpredictable mechanical vibrations of the skeletal muscles [110]. However, unlike SSHI methods, the SECE scheme may demonstrate poor performance at harvesting PE energy for ultralow and low power implants because of the power consumption in their complex internal switching and control circuits.

The above-mentioned state-of-the-art direct ac–dc switch-mode converters for kinetic energy harvester require no less than one switched inductor to facilitate the maximum power extraction. The power converters using off-chip inductors not only require more board space but also pose substantial health risks due to the susceptibility of the inductor to EMI [111]. However, since maximum power extraction is of primary importance while harvesting ambient energy sources for powering biomedical implants, converter design and optimization should be carefully accomplished to minimize the size and number of the switched inductor.

V. DC–DC Conversion With Voltage Conditioning

An alternate option to using a direct ac–dc voltage conversion technique is to use a separate rectifier followed by a dc–dc converter circuit. While the rectifier stage can be realized by any of the technologies described in the previous sections, dc–dc converter topologies will be discussed in the following sections.

A. LDO Linear Regulators

LDO regulator provides a stable stepped-down dc output voltage independent of load impedance, input-voltage variations, temperature, and time [112]. Fig. 10 shows the typical configuration of an LDO regulator. An LDO usually comprises three basic functional elements: a pass element (either a BJT or a MOSFET), a reference voltage, and an error amplifier. Typically, the pass element governs the accuracy of the output voltage by being always ON and dissipating continuous power. The error amplifier senses the output voltage continuously, compares it with the reference voltage, and generates a compensated control signal that changes the pass element's voltage drop to maintain a constant output load voltage.

LDO can be classified into two categories based on the presence of an output capacitor in the design: LDO with capacitor [113], [114] or LDO without capacitor [115], [116]. LDO with capacitor has the benefit of simpler circuit architecture to maintain adequate stability over a wide range of loading conditions. However, the relatively large-sized output capacitors in the single microfarad (μF) range required for this type of LDO cannot be realized in the system-on-chip (SoC) approach of the implantable devices. Therefore, an off-chip external capacitor is needed for this type of LDO to maintain stability under all operating conditions [117]. Nevertheless, the equivalent series resistance of the external capacitor reinforces the ripple in the output voltage during load transients [118]. In contrast, capacitorless LDO can reduce the size of the implants significantly since it does not require an external off-chip capacitor. For example, Chen *et al.* proposed a capacitorless LDO design with a high power supply rejection ratio (PSRR) for artificial retina application that can provide a stable output voltage of 3.3 V under the output current variation of 1–5 mA while achieving a PSRR of -46 dB at 10 MHz [119]. However, a robust compensation scheme is required for this kind of LDO to maintain the transient response stability and alternating current stability that otherwise would have been carried out using the presence of an external output capacitor [120].

The biomedical implant systems may require multiple independent regulated voltage sources to power different submodules. In a study presented in [121], a multiple-output LDO (MOLDO) with an off-chip external capacitor has been proposed, where one MOSFET is time-shared by four output legs to produce four individual outputs. These four output terminals are configured with different voltage ratings with a maximum single output voltage of 3 V from an input voltage of 3.3 V. Although the proposed MOLDO can minimize power consumption by providing independent regulated voltage for each submodules of an implant system, it suffers from slow settling time and large ripples in the output voltages arising from a small feedback factor. To overcome this limitation, Mo *et al.* introduced a constant feedback factor-based time-shared technique in MOLDO architecture that reduces the ripples in the output voltages by enhancing the settling time through constant feedback [122].

The frequency stability of the above-mentioned analog LDOs (ALDOs) is highly load-dependent [118]. To address this problem, the error amplifier of the ALDO is replaced by a digital control logic circuit in a digital LDO (DLDO) architecture. In a DLDO, the output voltage is digitized by an analog-to-digital (ADC) converter and fed to a digital controller [123]. A compensation digital code is generated by the digital controller and supplied to a digital-to-analog (DAC) converter to produce the required output voltage. DLDO offers the advantages of a wide range of load variations, lower sensitivity to process variations, scalability, size, and low voltage operation [118], [123]. For instance, A DLDO has been reported in [124] that works at an input voltage as low as 0.5 V at a current efficiency

of 98.1%, thereby making it suitable for powering ultralow-power implant electronics. However, DLDO can suffer from load current-dependent ripple in steady-state condition due to digital loop compensation in discrete steps [118]. Ripple cancelation amplifier can minimize the ripple in the output at the expense of increased circuit complexity.

The quiescent current consumed by the series pass transistor of an LDO in its idle stage contributes to reduced efficiency. Continued research efforts have scaled down the quiescent current consumed by an LDO to a value as low as 0. 062 μA, thereby minimizing power loss [125]. To date, LDOs have been designed to power a wide range of implantable devices operating at a voltage as low as 0.9 V [126] to a voltage as high as 10 V [127].

LDOs are an efficient choice over the switched-mode converters when the current is relatively low or the voltage drop is relatively small. Therefore, LDOs have been extensively used in the power management units (PMUs) of ultralow and low power implantable applications such as wireless intracranial pressure monitoring system [128], artificial retina application [119], spinal cord stimulator [120], neural stimulator [17], [56], blood flow sensor microsystem [38], cardiac microstimulator [14], total knee replacement (TKR) [129], and many more. Other attractive features of LDOs with respect to implantable applications are low-noise output voltage, small size due to fewer external components, low shutdown current, and low cost. In fact, the clean voltage generated by the LDO is an ideal choice for noise-sensitive, high-frequency analog and digital circuits such as phase-locked loops for microprocessors, high-speed communication links, etc., inside PMUs of IMDs. However, voltage up-conversion is not possible by LDO which limits their applications in harvester-driven IMDs.

B. DC–DC Switched-Inductor Converters

A large and growing body of literature has investigated the classic switch-mode inductor-based converter topologies to power IMDs from ambient energy sources. A step-up converter with a cold-start mechanism is needed when considering powering IMDs from extremely low-voltage microenergy sources, such as thermoelectric energy generator (TEG) devices, MFCs, and solar PV energy sources. Moreover, the voltage produced from the kinetic energy harvester needs to be stepped up or down depending on the requirements of the implant electronics. Several studies thus far have evaluated dc–dc switched-inductor converters for harvesting energy from TEG devices [99], [130]–[140], MFCs [140]–[142], and solar PV energy sources [133], [143]. In addition, numerous studies have attempted to focus on combining energy from multiple sources to further improve system reliability and increase power availability [144]–[146].

1) Single-Input Single-Output (SISO) Topology: The most widely used switched-inductor converters are realized on a single output utilizing a single inductor in its direct power transfer path to the load [99], [131]–[136], [140]–[142]. Many of these converters introduce hybrid-type architecture including a separate dedicated circuit for MPPT, cold-start (start-up), additional auxiliary converters, etc., to achieve the requirements for low

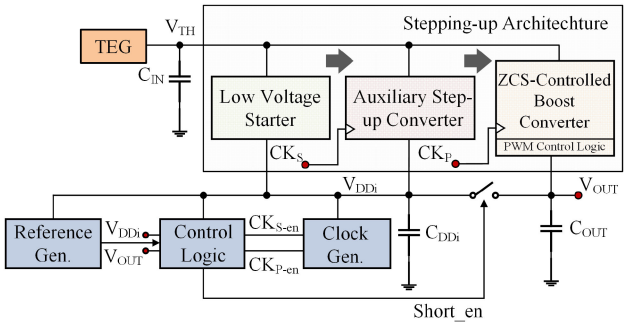


Fig. 11. Single-stage SISO step-up converter as a TEG energy harvesting interface proposed in [130].

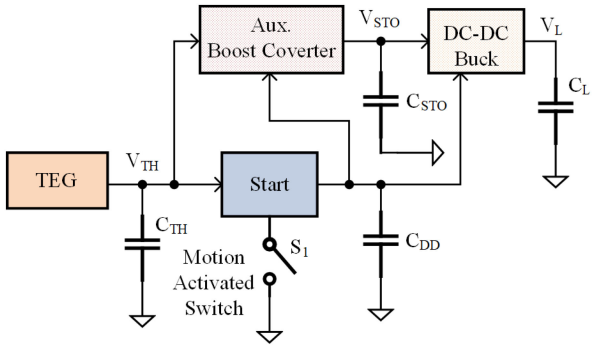


Fig. 12. Cascade-type two-stage SISO switched-inductor dc–dc converter as a TEG energy harvesting interface proposed in [139].

input voltage and high conversion efficiency simultaneously. For instance, Weng *et al.* presented a fully electrical start-up, a batteryless step-up converter that can generate a regulated 1.2 V output voltage from a TEG with a minimum input voltage of 50 mV and maximum efficiency of 73% [130]. The schematic is shown in Fig. 11 that consists of four functional blocks: a low-voltage start-up circuit, an auxiliary step-up converter, a ZCS-controlled boost converter and peripheral controllers. The auxiliary step-up converter acts as an intermediate buffer to prevent the undesirable loading effects during the cold start period. A two-stage topology with a cascaded auxiliary boost converter and dc–dc buck converter for a TE energy harvesting system has been proposed by Ramadass and Chandrakasan [139] (see Fig. 12). This dc–dc converter can operate down to an input voltage of 25 mV and provide a regulated output of 1.8 V with an overall end-to-end efficiency of 58%. A human motion-activated switch-based boost converter acts as a cold-start circuit. The auxiliary boost converter processes and transfers energy from the harvester to the storage capacitor (C_{STO}). The dc–dc buck converter starts powering the load at regulated voltage 1.8 V (V_{L}) when the storage capacitor voltage (V_{STO}) reaches 2.4 V. All these SISO topologies obtain reasonable efficiencies at relatively high input power (mW) levels. However, the efficiencies degrade as the input power decreases and become insufficient at μW power levels. This is due to the fact that the control circuit is usually powered by the converter output whose voltage level is determined by the requirements of the implant load rather than optimized for the low power consumption of the control

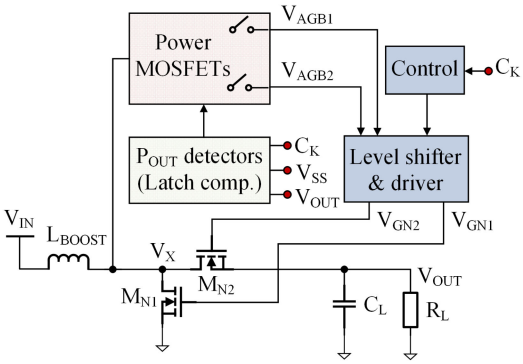


Fig. 13. Single inductor SIMO step-up dc–dc converter topology based on AGB and ERC techniques proposed by Chen *et al.* [137].

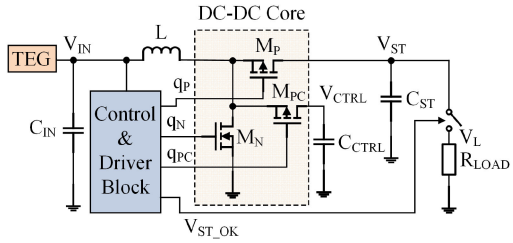


Fig. 14. Single inductor SIDO step-up dc–dc converter topology for harvesting TEG energy proposed by Katic *et al.* [138].

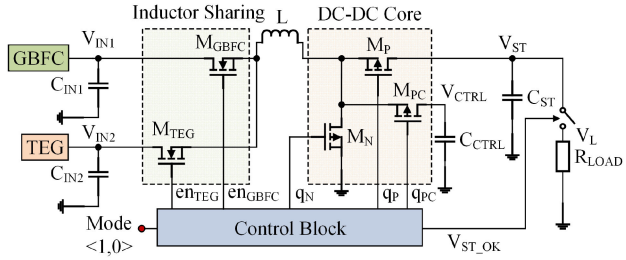


Fig. 15. Single inductor dual-input dual-output (DIDO) boost converter topology proposed by Katic *et al.* [144].

circuit. As described in the following sections, a multiple-output architecture is employed to achieve a high conversion efficiency at μW input power levels by reducing the power consumption of the control circuit to nanowatt level [138].

2) Single-Input Multiple-Output (SIMO) Topology: Time-sharing of a single inductor in DCM allows the switched-inductor converter to add load-independent output(s) that ensures high efficiency over a wide range of power for multiple reasons. First, the additional load-independent output can be optimized for the low power consumption of the control circuit, and second, to start up the converter, instead of charging a large storage load capacitor, a much smaller additional output capacitor(s) can be charged. Last but not the least, by providing multiple outputs through a single inductor, the SIMO converters can meet multiple voltage requirements of the low-power implant electronics with minimal dynamic power consumption and enable a considerable saving in cost, weight, and size with minimum risk of EMI [147]. Chen *et al.* proposed a single inductor SIMO step-up converter for TE energy harvesting with adaptive gate biasing (AGB) and near-threshold voltage energy redistribution control (ERC) technique that can optimize power consumption over a wide range [137]. The schematic of the converter architecture is shown in Fig. 13. The AGB technique produces two load-depended gate driving voltages (V_{AGB1} and V_{AGB2}) for the power switches of the primary boost converter in such a way that it reduces conduction and switching losses under heavy-load and light-load conditions, respectively. The proposed converter can boost an input voltage of 100–500 mV at 25–100 μW of output power and achieved a maximum efficiency of 83.4%, which is the highest efficiency reported to date for a boost converter at this low output voltage level. However, the efficiency of the converter drops drastically beyond the output voltage of 500 mV because of the additional switches in the AGB block along with the large inductor (1 mH) that incur a significant loss at high voltage stress. Another single-input dual-output (SIDO) boost converter is shown in Fig. 14, which together with its ZCS and ZVS switching techniques and additional load-independent output ensures high conversion efficiency at very low input power (microwatt) levels [138]. The boost converter can start working at an input voltage as low as 15 mV and the control circuit consumes only 160 nW of quiescent power. It can boost a thermal input voltage of 45 mV to a regulated output voltage of 1.9 V with a peak conversion efficiency of 86.6% at 30 μW input power.

3) DC–DC Converters for Multisource Energy Harvesting Interface: All the previous switched-inductor converter architectures rely on a single source to power the load electronics. However, microenergy harvesting for biomedical implants from a single source may often experience issues such as inadequate output power and poor reliability due to its unpredictable nature. In contrast, energy harvesting from multiple sources can improve the overall system reliability, robustness, and can increase the attainable output power. Several attempts have been made to investigate multisource platforms that combine the power from GBFC-TEG [144], PV-TEG-piezo [145], PV-RF-piezo [146], and so on. Combining energy from these multiple sources is facilitated by inductor sharing using DCM operation where the inductor is alternatively time-shared with one harvester at a time to deliver power to the output load while the switches correspond to the other harvesters are kept OFF. For instance, Katic *et al.* presented a single-inductor dual-output boost converter topology that combines energy from implanted GBFC and TEG devices, and the architecture is shown in Fig. 15 [144]. The control block is powered from the second output (V_{CTRL}) and the digital signal $V_{\mathrm{ST\_OK}}$ controls the switch that connects the load to the main output provided that enough energy is accumulated in the storage capacitor (C_{ST}). The low quiescent power consumption of the control block together with both ZCS and ZVS switching of the converter enable it to achieve a peak conversion efficiency of 89.5% at 66 μW of combined power delivered by the two harvesters. The converter obtains a peak power efficiency of 85.32% at an output power of 23 μW for the TEG source and 90.4% at 29 μW for the GBFC source. Similarly, Bandyopadhyay and Chandrakasan [145] proposed a

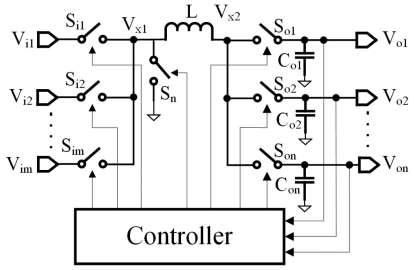


Fig. 16. Inductor sharing scheme in a single inductor MIMO switching converter [148].

multisource platform that combines power from solar, thermal, and PE sources. A boost converter is employed for thermal and PV inputs and a rectifier followed by a buck–boost converter is implemented for the PE input. The system can boost the input voltages from 20 mV to 5 V and achieved a power efficiency in the range of 58% to 83% when using individual harvesters and a peak power efficiency of 96% when considering overall end-to-end efficiency.

4) Inductor Sharing Scheme in Implant Applications: The above-mentioned multiple port dc–dc switched-inductor converters including SIMO, multi-input single-output (MISO), and multi-input multi-output (MIMO) power conditioning architectures allow combining multiple converters into a shared inductor converter by conducting time-sharing of the inductor utilizing the idle time of the DCM operation [147]. Fig. 16 shows a schematic of an exemplary inductor sharing scheme in a single-inductor MIMO buck switching converter [148]. This suffices the need for separate inductors for either additional outputs or inputs in these converter topologies, resulting in significant savings in cost and area for space-constrained implant applications. Reducing the number of required inductors in switched-inductor converters also mitigates the EMI-related health risk. However, at an ultralow-power implant system, the complex control circuit overhead associated with inductor sharing limits the system's overall efficiency. In order to achieve better efficiency in such ultralow-power ranges, greater attention to design optimization is needed that may include power gating, dynamic pulse width control, ZCS and ZVS techniques, and so on [138], [143].

C. DC–DC SC Converters

DC–DC SC converters or charge pumps (CPs) use capacitive energy transfer instead of inductive energy transfer associated with dc–dc switched-inductor converters. These converters are combinations of switches and capacitors where the charge is transferred from one capacitor to another under the control of regulator and switching circuitry [149]. In addition to being more immune to EMI, the inductorless design of SC converters can lead to a drastic reduction in the complexity and cost of the on-chip integration and fabrication process, and consequently, are widely employed in implant applications [150]–[152].

Among various SC topologies, the Dickson, voltage doubler, series–parallel, and Fibonacci topologies are widely used in implantable applications [6], [7], [15], [16], [73], [153], [154].

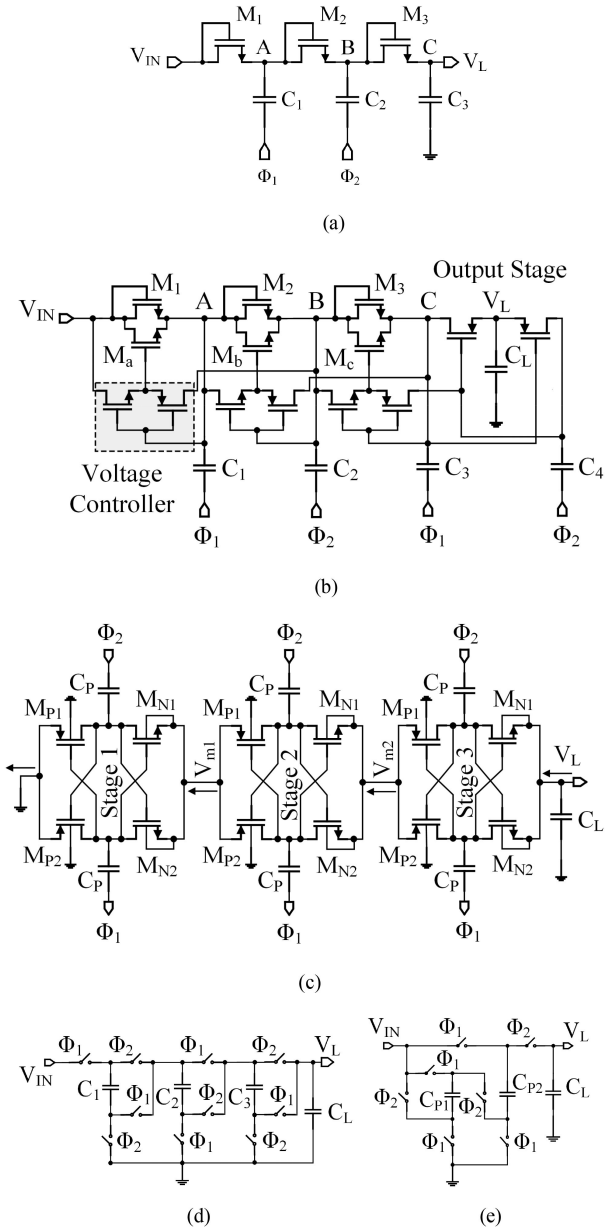


Fig. 17. Schematics of different SC topologies. (a) Conventional Dickson CP [155]. (b) Modified Dickson CP used in [6]. (c) Pelliconi architecture based three-stage negative charge pump used in [16]. (d) Fibonacci 5:1 SC network used in [154]. (e) Series–parallel SC topology used in [7].

Fig. 17(a) shows a basic structure of a Dickson CP topology where capacitors are interrelated by two nonoverlapping clocks and coupled in parallel with diode-connected MOSFETs [155]. However, the voltage pumping gain is limited by reverse-charge-sharing effects and the MOSFET threshold voltage. To overcome these limitations, a modified Dickson CP is adopted, which utilizes additional parallel auxiliary switches as static charge transfer switches and voltage controller consisting of pass transistors [see Fig. 17(b)] [6], [153]. For example, Lee *et al.* designed such a modified CP for a cardiac pacemaker that can generate a stimulation voltage of 3.2 V from a 1.2 V dc supply [6]. Chen *et al.* [156] proposed a four-stage on-chip

Dickson CP with parallel-connected photodiodes for subdermal implant applications. By employing an auxiliary charge pump using zero-threshold voltage (ZVT) devices in parallel with the main charge pump, this system obtained a low-voltage start-up of 0.25 V and an output power of 1.65 μW at 1.06 V from a 0.31 V input.

With the Pelliconi charge pump design, dual-polarity can be achieved, thus making it suitable for biphasic stimulation with small area utilization [15], [16]. Pelliconi [157] CP uses antiphase clock signals to actively operate cross-coupled MOS switches along with two coupling capacitors. Each stage of the Pelliconi CP circuit acts as a voltage doubler, and like the Dickson charge pump circuit, the gain ratio (GR) can be enhanced by cascading multiple stages. For example, Ethier and Sawan proposed two separate charge pumps based on Pelliconi architecture to generate $\pm$9 V driving voltage from 3.3 V dc supply that facilitates biphasic intracortical current-pulse stimulation [16]. The schematic of the proposed three-stage negative charge pump intended to generate –9 V supply is shown in Fig. 17(c).

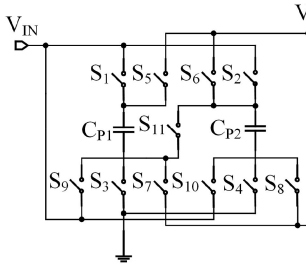
Fibonacci CP proposed by Makowski *et al.* is an *n*-stage charge pump where the voltage gain increases or decreases by the (n+1)th Fibonacci number as opposed to the Dickson or Pelliconi charge pump, where the voltage gain increases linearly [158]. A 5:1 Fibonacci CP, shown in Fig. 17(d), was reported by Wieckowski *et al.* for implantable applications that achieve output voltage one-fifth of input supply of 3.6 V while delivering 250 nW of power [154].

CP with series–parallel topology has the best switch-capacitor utilization among the other basic SC topologies. From an area-cost point of view, it is the most suitable CP to be applied in implant PMUs. Fig. 17(e) shows a schematic of a basic 3X series–parallel SC topology used in a single-chip very-low-power interface IC that delivers a high-voltage stimulation for cardiac pacemakers [7].

1) Regulation of SC Converters: Conventional SC converters suffer from poor efficiency in a wide range of $V_{\rm in}$ and/or $V_{\rm o}$ values [150]. However, the implant PMU must efficiently meet its varying load and different voltage requirements of different functional blocks, as well as various operating modes. Multiratio SC converters (MRSC) with reconfigurable power stages can provide a wide range of output voltages catering to these different voltage requirements, with the added benefit of minimal power consumption [151], [152].

a) Multiratio SC Converters: Several MRSC converter topologies, such as step-up [159], step-down [136], [152], [160]–[163], and both step-up and down converters [151], [164], [165], have been evaluated for ultralow power applications in the literature, where the power stage can be reconfigured into different architectures to achieve multiple GRs. One such reconfigurable SC converter power stage was reported by George *et al.,* which is shown in Fig. 18 [151]. The converter can be reconfigured to achieve five GRs in both step-up and step-down conversion modes and can deliver up to 7.5 mW to the load with maximum 75% efficiency, using an active area of only 0.04 mm^2.

MRSC converter has lower than the expected efficiency due to its inability of providing low output impedance and increased



Gain Ratio	ϕ_1	ϕ_2
1/2	S_1, S_2, S_7, S_8	S_3, S_4, S_5, S_6
2/3	S_1, S_2, S_7, S_8	S_4, S_5, S_{11}
1	S_1, S_2, S_3, S_4	S_3, S_4, S_5, S_6
3/2	S_1, S_4, S_{11}	S_3, S_4, S_9, S_{10}
2	S_1, S_2, S_3, S_4	S_5, S_6, S_9, S_{10}

Fig. 18. Five-GR reconfigurable SC converter power stage along with its different switching schemes [151].

number of switches and control circuitries. The efficiency of the MRSC converter is noticeable at ultralow ($\sim$0.1 μW) to low power ($\sim$1 mW) implantable loads, such as a pacemaker, bone growth stimulator, body area network and cochlear implant [26], [150]. Low power density applications pave the way for operating the converters in relatively lower switching frequencies, thereby reducing the switching losses. Therefore, at this low power level, the efficiency of this MRSC converter becomes substantially dependent on the conduction losses that can be minimized by using increased GRs.

b) Control Strategies Applied in SC Converters: In order to maintain the line and load regulations of the SC converters, various control strategies have been implemented as of now. According to (1), four variables such as GR (M), switching frequency ($f_{\rm sw}$), duty cycle (D), and switch conductance (G) can be changed to control the output voltage of an SC converter [150]. The output of the SC converter can be defined as

$$V_{\rm out} = MV_{\rm in} - I_{\rm out}R_{\rm out}\left(f_{\rm sw},\ D,\ G\right). \tag{1}$$

One of the most common control strategies used in implant applications is conversion ratio control, also known as gear-box control or adaptive gain (AG) control that adjusts the M to provide the required output voltage [151], [152], [160]–[162], [164]. Since conduction loss is directly affected by the number of conversion ratios, it is the only control method that can reduce the conduction loss [26]. The remaining three control variables, $f_{\rm sw}$, D and G, modify the output impedance ($R_{\rm out}$) of the converter for voltage regulation, conceptually similar to the lossy regulation of a series linear regulator. Out of these three control variables, only switching frequency ($f_{\rm sw}$) can be easily varied over the necessary range [150]. Therefore, the efficiency of the SC converters in ultralow-power/low-power implant applications is primarily dependent on minimizing switching losses of this control strategy.

Traditionally, to achieve fine regulation, SC converters adopt PFM in combination with the AG control, as described in [151], [152], [162], and [164]. This is preferred for ultralow-power and low-power implant applications because PFM keeps switching losses proportional to load current, leading to better efficiencies. In general, two types of PFM controllers are reported in biomedical applications, namely, discrete or automatic frequency scaling (DFS) controller [151], [162], [164] and asynchronous controller [152]. The DFS controller scales the switching frequency in several steps to regulate the output voltage. For instance, George *et al.* [151] proposed a step-up/down SC converter using AG and

DFS controller that is capable of regulating the output voltage within a range of 1–2.2 V derived from an input voltage of 1.8 V by scaling the frequency in four steps (1.25/2.5/5/10/20 MHz). It can deliver a load power of 7.5 mW with a reported efficiency of up to 75%. However, the DFS controller requires a constant running clock and frequency divider, thereby increasing the dynamic power consumption of the converter even if the load is not active. In contrast, the asynchronous controller, proposed in [152], is able to turn on the minimum number of switches while keeping the additional switches OFF depending on the load current (event-driven technique). Therefore, it can potentially reduce power consumption during low-load scenarios. PFM control scheme suffers from switching frequency variation with load and input voltage change, thus making it difficult to filter out the unwanted noise from the controlling signal. A delta-sigma closed-loop-based control technique may be useful in suppressing the noise by spreading the generated unwanted tones across a wider frequency spectrum [166].

In biomedical applications, several attempts have been made to carry out the series connection of an LDO voltage regulator with the SC converter [6], [73], [154], [161]. In this scheme, the SC converter is designed to make up most of the voltage gap between the inputs and the expected output voltages (coarse tune), whereas the LDO is designed to fine-tune the output voltage toward the desired target voltage. This hybrid type of converter is preferred when the input to output voltage ratio is high enough to achieve high efficiency using either SC converter or LDO alone. Other advantages of LDO-coupled SC converters include reduced noise at high-frequency operation, low input and/or output voltage ripple, and faster dynamics in the load regulation [26]. Wieckowski *et al.* [154] proposed a hybrid SC converter network consisting of a 5:1 Fibonacci CP cascaded with LDO. The Fibonacci SC converter alone provides 720 mV from a 3.6 V Li-ion battery source and it is further stepped down to 444 mV when connected in series with an LDO. This hybrid configuration achieves an output voltage ripple of less than 50 mV at 56% power efficiency (4.6 $\times$ of an ideal linear regulator) under 5 μW of loading conditions. However, the main drawback of this hybrid approach is that in order to allow for the voltage drop across the LDO, the $I_{\rm out}R_{\rm out}$ drop of the SC converter needs to be even lower, which implies the use of a higher switching frequency, larger switches, higher capacitors, or specific combination of them. Any of these would result in an increase in the switching losses.

c) Multiphase SC Converters: Unwanted noise generated in the SC converter may also be reduced by splitting it into smaller cells in a modular approach. This type of converter is called the multiphase SC converter that has been implemented in many applications reported in [159], [160], [162], [163], and [167]. While the SC converters suffer from large output voltage ripples and input inrush current because of their separate charge-discharge path, the interleaving technique used in multiphase converter minimizes these drawbacks. In the interleaving technique, a part of the converter's charge transfer capacitances can be shared among multiple-stage cells by time multiplexing the evenly distributed clock phases. In addition, the multiphase configuration may allow a significant reduction of the size of the output capacitance resulting in a significant reduction of the size of the converter chip, and thereby decreasing the size of the target biomedical implant as a whole. Fig. 19 shows the architecture of a multiphase SC converter proposed in [167]. The converter obtains two different GRs (1/2 and 2/3) with an efficiency of 81% at a power density of 38.6 mW/mm^2. As expected, the measured output voltage ripple is as low as 3.8 mV, which is less than the ripple produced by the single-phase SC converters having similar output capacitance.

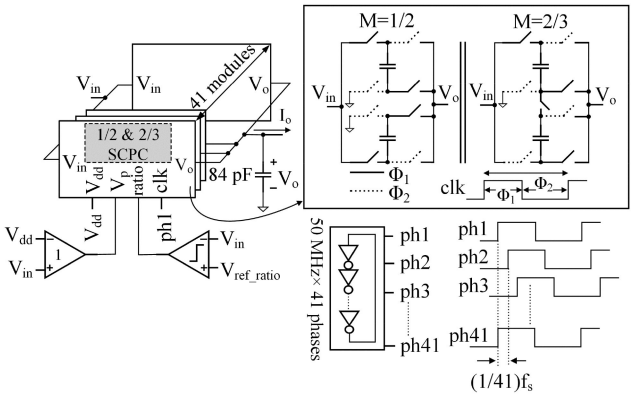


Fig. 19. Multiphase architecture of the SCPC proposed in [167].

VI. Comparisons of Different Power Converters

A. Strengths and Limitations of Different Power Converters

A comprehensive analysis comparing the characteristics of different power converters will be presented in this section. Because the use of IMDs has increased significantly over the years, more research focus is being driven toward improving the efficiency of the power converters that are used as the interface between energy harvesters and implants. Therefore, linear regulators (e.g., LDOs), switched-capacitor power converters (SCPC), and switched-inductor power converters (SIPC) are being predominantly employed as the voltage conversion blocks to condition power for the IMDs [26].

LDO architecture is one of the widely used elements of power management for applications where volume and weight requirements are stringent with marginal voltage overhead [126]. Due to their ability to achieve noise-immune voltage regulation, LDOs are still popular in implant applications where noise isolation and emissions are major system concerns. That being said, in implant applications, the excessive energy dissipation across the LDO can impose a significant health risk, especially where the output voltage of an energy harvester is several orders higher than the load voltage. In addition, a large capacitor is required to stabilize the output of a conventional LDO regulator, which may become challenging in on-chip applications, especially without a substantial tradeoff in the form factor and chip area [117]. Capacitorless LDO regulators have been proposed in several studies with additional control circuits that increase the implementation cost and complexity of the regulator circuit [126], [168]. As a result, designers need to overcome significant design challenges to fully utilize the advantages of capacitorless LDOs. Moreover, LDO can only accomplish down-conversion of the input voltage

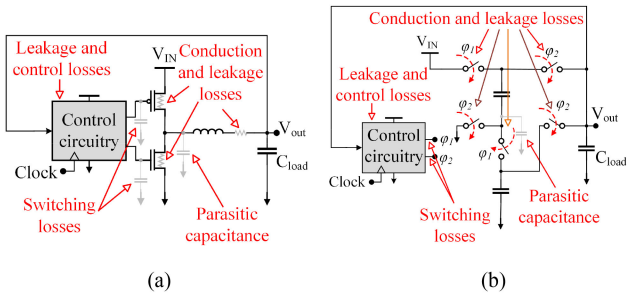


Fig. 20. Circuit implementations of (a) inductor-based and (b) SC-based step-down converters showing key sources of efficiency losses [27].

rendering itself irrelevant in biomedical applications that require voltage up-conversion.

Switching power converters (i.e., SCPC and SIPC) can be configured to accomplish both voltage-up and voltage-down conversion depending on the biomedical application requirements. Moreover, these types of converters can achieve the required voltage conversion at a much higher efficiency (compared to the LDOs) in applications having a substantial mismatch between input and output voltages. The efficiency (η) of a switching converter can be expressed by the following equation [27]:

$$\eta = \frac{E_{\text{load}}}{E_{\text{load}}+E_{\text{conduction}}+E_{\text{switching}}+E_{\text{parasitics}}+E_{\text{control}}+E_{\text{leakage}}} \times 100\%. \quad (2)$$

Here, E_{load} refers to the energy delivered to the load per cycle, and other terms in the denominator refer to different losses incurred during the operation of the switching converter. Simplified designs of the SC and switched-inductor-based converters are illustrated in Fig. 20. These designs are configured in a step-down mechanism, coupled with fundamental sources of efficiency losses.

SCPC operates based on the capacitive energy transfer mechanism. Since SCPC does not have an inductor, it is less affected by EMI and can be used in implants that utilize inductive links. For the same reason, they are ideal for integrated implementation. One of the major advantages of SCPC is the ability to start at lower input voltages when compared with other dc–dc converters, particularly SIPC. This advantage is often exploited during cold-start, which is detailed in Section VII. In some biomedical implant systems, a broad set of implementable conversion ratios may be required to support its different blocks or to meet the voltage differences between the input and the load that may vary substantially from time to time. Multiratio SCPC (MR-SCPC) instead of fixed GR SCPC can meet multiple voltage requirements with minimal dynamic power consumption by adopting dynamic voltage scaling (DVS). However, MR-SCPC suffers from heightened switching and conduction losses that can be attributed to the increased number of switches and capacitors incorporated to realize multiratio architecture. Conduction and switching losses of semiconductor switches and charge-up losses within source–capacitor loops are some of the most prominent loss mechanisms of an SCPC [76]. At low switching frequency, charge-up losses dominate, while at higher switching frequency conduction losses and switching losses dominate [23]. Splitting the flying capacitor into smaller packages and activating the required number of packages depending on the required level of output power can become a viable solution to reduce the charge-up losses [169]. Switching losses within an SCPC can be minimized by opting for PFM at light-load conditions. One drawback of using PFM instead of PWM is the variable frequency associated with PFM that leads to a broad noise spectrum, thereby making the noise filtering process sophisticated and expensive. However, the noise content in the low switching frequency of PFM corresponding to ultralow-power/low-power conditions is less than its PWM-controlled counterpart. At higher switching frequency, PWM-controlled SCPC is more efficient compared to its PFM-controlled counterpart [26].

On-chip integration of capacitors using bulk CMOS technology and subsequent small form factor are two of the most prominent features of SCPC that fuel its widespread use in biomedical applications. Under the bulk CMOS technology, the capacitive density varies from 4 to 12 nF/mm^2, which may not be sufficient in many applications where large output current ripple suppression is needed [26]. Allocating a larger area to implement sufficient on-chip capacitance can solve the issue at the expense of increased implementation cost. Capacitors implemented through *metal–insulator–metal* and *silicon-on-insulator* technology can reduce the bottom-plate parasitic, which in turn can reduce the charge-up losses and increase the capacitive density [154], [170]. Capacitive density can reach up to a maximum of 400 nF/mm^2 by using trench capacitors, as mentioned in [171].

SIPC provides an alternative form of voltage conversion technology that utilizes a magnetic energy transfer mechanism to accomplish the required voltage conversion. Unlike SCPC, the efficiency of this type of converter topology is not limited by a fixed conversion ratio for a specific application, making them suitable for DVS implementation. Besides regular voltage conditioning, switched inductors in direct ac–dc power converters facilitate maximum power extraction from kinetic energy harvesters. The inductor of an SIPC can be integrated either monolithically or can be adopted in a system-in-package (SiP) approach to miniaturize the overall footprint. However, the current ripple stemming from the absence of adequate large inductance gives rise to a large rms current, inducing significant loss. Using ferrite as a substrate for chip-size solenoid inductor [172], incorporating off-chip SMD air-core inductors [173], and realizing reactive components and switches in different dies [174] are some of the SiP approaches that can incorporate the required reactive components at comparatively low cost. Nevertheless, monolithic integration of inductors within a small form factor remains challenging in the standard CMOS process, which is attributed to the cost and technology limitation. However, replacing the inductor with bond wires can improve the form factor compared to conventional SIPC [175]. Increasing ohmic losses with increasing switching frequency, magnetic core losses, hysteresis losses, and eddy current losses associated

TABLE III
ADVANTAGES AND DISADVANTAGES OF VARIOUS POWER CONVERSION SCHEMES USED IN IMPLANTABLE DEVICES

Type	Advantages	Disadvantages
LDO	- One of the simplest forms of voltage conversion technique - Small form-factor - High efficiency step-down operation is possible - Can produce noise free voltage for noise-sensitive electronics.	- Voltage up-conversion is not possible - Can produce heat during regulation which can lead to tissue damage - Is not practical for large V_{in}-V_{out}
SCPC	- Mature on-chip integration can yield smaller footprint - At low input voltage, cold-start circuitry is not typically required - Superior performance compared to LDO when V_{in}-V_{out} is large - PFM ensures negligible switching loss at lighter load and low conversion ratio.	- Voltage conversion ratio is somewhat limited - Limited maximum power handling capability - May require large form factor - May become expensive due to high-density capacitor fabrication - Stepped output voltages, fine tuning is difficult
SIPC	- Suited for high-power, high-efficiency applications -Wide range of voltage conversion possible without sacrificing form-factor - Continuous voltage conversion ratio - AC-DC switched inductor enables maximum power extraction from kinetic harvesters	- Relatively large footprint and EMI susceptibility due to inductor - May result in large RMS current - Fabrication of on-chip inductors may require larger area - May require additional cold-start circuitry, resulting in increasing cost and footprint

with the inductor add to the overall loss profile of a SIPC topology, thereby compromising converter efficiency [176]. At low output powers, moving to DCM over CCM allow the converter to use small-sized inductors leading to improved form factor and increased efficiency, although at the price of higher current ripple and the complex timing of the switch driving signals. DCM operation also facilitates the time-sharing of a single inductor in a multisource and/or multioutput platform, thereby can maintain a comparatively smaller form factor.

As a conclusion to this section, Table III briefly states the advantages and disadvantages of each type of power converters used in implantable devices discussed in this section.

B. Comparison of SCPC and SIPC Based on Key Performance Metrics

In this section, a comparative analysis of SCPC and SIPC suitable for implantable electronics is presented based on their electrical parameters and performances. Since this is a quantitative comparison based on key performance metrics, we reviewed only dc–dc switched-mode converters in order to perform an apple to apple comparison. We compared the peak efficiencies of these two converters with respect to different performance metrics in Fig. 21. Maximum output power, power density, VCR, and input voltage are the selected metrics that are individually plotted against peak efficiency to compare the performance of SIPC and SCPC converters reported in the literature.

Fig. 21(a) illustrates the comparison of peak efficiency versus output power for the two converter topologies. It highlights the widespread use of SCPC in ultralow ($\sim$0.1 μW) to low power ($\sim$1 mW) implantable loads. At relatively high-power levels ($>$1 mW), the required number of flying capacitors significantly increases, resulting in compromised form factor and increased switching loss, thereby hindering the feasibility of utilizing SCPC. In contrast, except single-stage ac–dc SIPC (exists at microwatt level), dc–dc SIPC is limited to a relatively high-power levels ranging from $\sim$1 mW to $\sim$30 W due to the implementation of discrete inductors. SIPC converters are traditionally configured in buck, boost, and/or buck–boost configuration based on a single inductor that allows voltage up/down conversion without significant area penalty compared to SCPC. An SIPC topology reported in [20] has achieved a maximum output power close to 30 W, and it substantiates the superior ability of SIPC to operate at higher output power. Fig. 20(b) illustrates the number of existing SCPCs tailing off as power density increases. The decline in existing SCPC topologies at high power density can be attributed to the low capacitive density of on-chip capacitors realized by standard CMOS technology. However, capacitors implemented by superior technology (e.g., trench capacitors [184]) can reach the high end of the power density spectrum with added implementation cost. Unlike SCPC, SIPC does not exhibit any declining trend with an increased power density as evident from Fig. 21(b). In light of the discussion based on Fig. 21(a) and (b), it is worth mentioning that future research efforts in power converter design tailored for a biomedical application must focus on developing SCPC suited for medium-to-high power levels.

The next performance metric is the VCR. The superiority of SIPCs over SCPCs in terms of VCR is distinguishable from Fig. 21(c). SCPCs can be configured to achieve a higher conversion ratio by adding a large number of flying capacitors. However, the resulting VCR improvement comes at a price of larger footprint, increased switching loss, and increased implementation cost. Therefore, most of the SCPCs discussed here are configured to achieve a low to moderate VCR ranging from 1 to 10. In contrast, SIPCs can attain a high VCR without sacrificing a large die area, as the VCR primarily depends on the duty ratio of the circuit. As shown in Fig. 21(c), an SIPC can achieve a VCR as high as $\sim$100 [186].

The comparison between the two converter topologies in terms of input voltage is illustrated in Fig. 21(d). The majority of the research on SCPC topology is focused on a narrow input voltage range of 0.2–2 V, whereas SIPC can operate at an input voltage as low as 20 mV [131]. Therefore, SIPC is better suited for applications where the generated voltage by an energy harvester is significantly low. Due to the ability to achieve a high conversion ratio with better efficiency and form factor by changing only the duty ratio, a conventional SIPC can be configured to obtain a high voltage output from a low input voltage ($\sim$20 mV) provided that an appropriate cold-start circuit

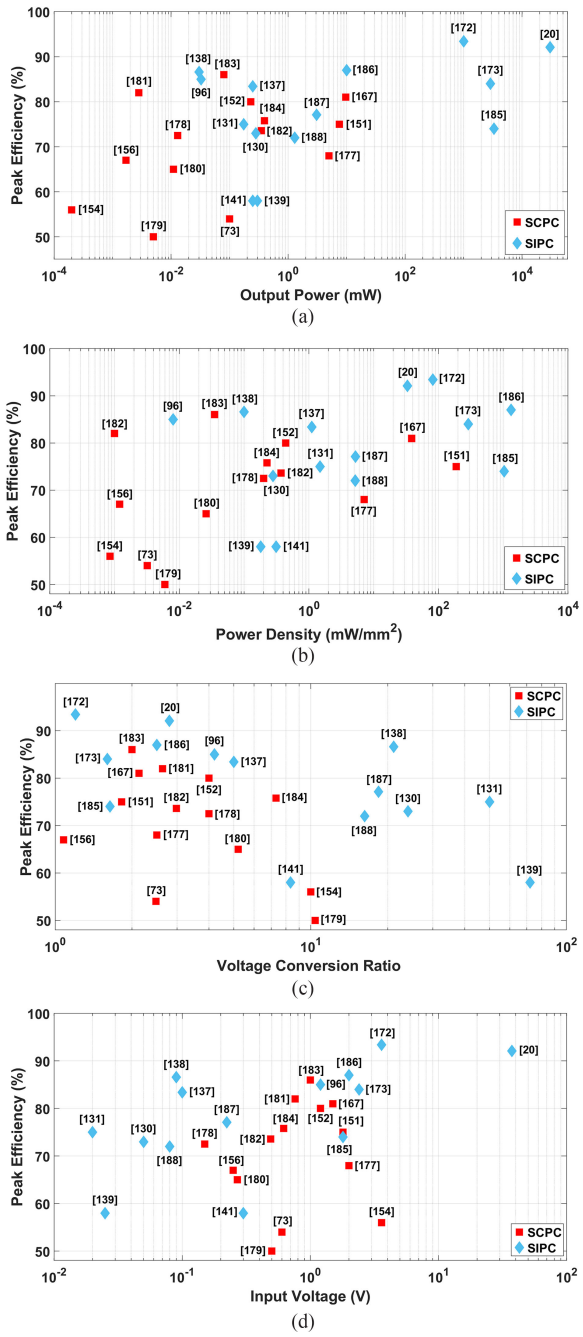


Fig. 21. Existing power converter efficiency versus (a) output power, (b) power density, (c) voltage conversion ratio, and (d) input voltage.

is adopted. However, a conventional SCPC can achieve the same feature by adopting a large number of capacitors, but not without the expense of additional cost, area, and switching loss.

Considering the attributes featured in Fig. 21(a)–(d), we can establish a selection process of power converters suitable for the intended biomedical application with a specific voltage and power requirement as there is no "*one-size-fits-all*" solution. For instance, implants that require a high-efficiency power conversion at high output power may adopt SIPC topology. For implants requiring ultralow to low output power can use both SCPC and SIPC. That being said, conventional SIPC requires

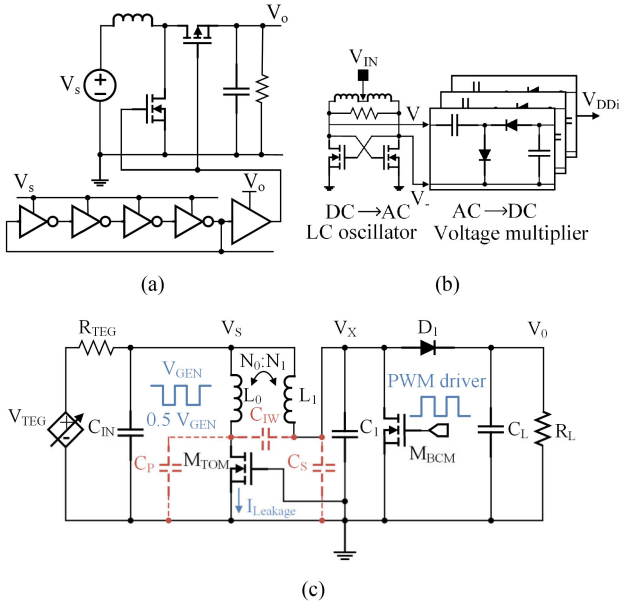


Fig. 22. Oscillator-based cold-start circuit. (a) Conventional CMOS inverter-based oscillator circuit [190]. (b) ILRO circuit [130] and transformer oscillation mode boost converter where low-voltage start-up is achieved by the built-in mutual inductance of the transformer [132].

a larger footprint in comparison to an SCPC. Hence, SCPC would be the appropriate choice of power conversion in in-body implants that must maintain a small form factor.

VII. Start-Up Issues

Many of the energy harvesters discussed so far suffer from the problem of "*cold-start*." This situation occurs when the harvested energy from ambient sources, such as TEGs, MFCs, and solar PV energy sources, yields converted voltage levels that are insufficient to provide ancillary power for the gate drivers and other auxiliary circuits/functional blocks [23], [28].

One approach to achieving start-up is to adopt oscillator-based circuits, where an oscillator is incorporated, usually followed by a VM circuit or a charge pump. The oscillator uses the low input voltage of the harvester to generate a clock signal that is boosted beyond the supply voltage of the VM circuit to facilitate the start-up. The easiest oscillator structure is the conventional CMOS inverter-based oscillator or ring oscillator [133], [189], [190], as shown in Fig. 22(a). The threshold voltage of MOSFETs limits the minimum input voltage of the oscillator, which makes it unattractive for a low-voltage start-up circuit. However, it is possible to reduce the start-up voltage by adopting some postprocessing threshold voltage tuning, which imposes additional processing costs. *LC* tank oscillator and inductive load ring oscillator (ILRO) based cold-start systems can overcome the above-mentioned problem related to MOSFET threshold voltage and can achieve as low as half of the start-up voltage of a classical inverter-based ring oscillator [130], [134], [143]. Fig. 22(b) shows an ILRO-based start-up architecture that obtains oscillation by using two inductors configured in mutual feedback with the help of a cross-coupled transistor pair. Like the ILRO-based start-up scheme, mutual feedback can be realized by the built-in

mutual inductance of a transformer due to the common magnetic core sharing between inductors. Such a transformer-based self-staring boost converter for a TEG harvester is shown in a simplified manner in Fig. 22(c) [132]. This cold-start circuit can achieve a minimum self-start-up voltage of 21 mV through a positive feedback loop formed by a native ZVT MOSFET (M_{TOM}) together with the transformer winding pair, which is triggered by thermal noise. This transformer-based cold-start solution requires a very high turn ratio to achieve direct multiplication of the harvester's low input voltage, which increases the OFF-state leakage current of the native MOSFET. To overcome this issue, Teh and Mok [140] introduced a modified boost converter to initiate the start-up that utilizes a single switch-based unity turns ratio transformer, such as a high inductance pulse transformer. However, both inductor- and transformer-based start-up schemes require additional off-chip magnetic components that limit device miniaturization. Recently, Garcha *et al.* proposed a fully integrated start-up solution using a Meissner Oscillator with an on-chip transformer that could achieve start-up voltage as low as 25 mV [191].

Rather than using an oscillator circuit, some external sources such as a battery or supercapacitor [77], [131], [133], [141] and auxiliary RF energy source [133], [136] were used to carry out one-time precharging of the load/output capacitor [131], [133], [136], [141]. The size of the output/load capacitor is set for comparatively high-power requirements of the load rather than the control circuit. This implies that a comparatively large amount of power is needed to charge it during the start-up period resulting in poor efficiency of the total power conversion system. This issue was addressed by Goeppert and Manoli [135] carrying out one-time precharging on a separate storage capacitor that is much smaller than the output capacitor and is independent of the implant load requirements. Nevertheless, the converter output takes over the power delivery to the control circuit and thus affects the PCE again. To overcome this problem, a separate dedicated output to power the control circuit rather than powering the implant load during the start-up as well as the regular operation is proposed in [61] and [138]. Fig. 14 can be referred for realizing such a start-up scheme that was able to help the boost converter operate with input voltages as low as 15 mV.

Unlike storing sufficient energy by stepping up the source voltage for the cold-start, direct triggering of the active components was reported that include the additional/separate external sources such as battery [113] and mechanical switch [139]. For instance, Ramadass and Chandrakasan designed a mechanically assisted start-up method for a TEG-supplied boost converter, which can achieve start-up at an input voltage as low as 35 mV, and the circuit diagram of the energy harvester is already shown in Fig. 12. However, separate external sources are comparatively expensive and require off-chip components that limit their applications.

The design of the cold-start circuit is application dependent. For example, while designing a cold-start circuit for ultralow-voltage energy sources such as TEG, MFCs, or solar, the design considerations need to be focused on minimizing start-up voltage and the time needed to initialize the start-up, even at the cost of lower efficiency. In contrast, for other energy harvesting applications, the cold-start is considered an inefficient process and is often excluded from published efficiency values due to the event rarely occurring, possibly as little as once over the lifetime of the system [28].

VIII. Existing Research Gap

For any given application, finding the most suitable power converter topology seems to be the biggest hurdle because there is no universal architecture that performs the best for all applications. Many uncertainties exist, and the key factors behind the selection of any converter are type of implant, type of energy source, voltage and current ratings, nature of power—pulsed or dc, allowable volume, EMI and magnetic resonance imaging (MRI) related issues, and so on. With IPT or kinetic energy harvesting, ac–dc conversion is needed. Most of the high-performance ac–dc or dc–dc converters employ inductors—either on-chip or off-chip, and they suffer from EMI issues and start-up problems. With large implanted inductors, patients cannot undergo MRI. LDO-based systems are effective as long as the voltage drop across the converter is small, and they may suffer from heat dissipation within the body once the voltage drop exceeds a limit. Therefore, we can identify the technology gaps in the following way. First, there is a clear disjoint between the biomedical community and the power electronics community—the researchers designing sensors and implanted circuits do not have a clear understanding of the power processing architectures. In many cases, the proposed solution is not the most optimum. Second, because there is no universal solution, researchers are thinking of designing switching power converters without inductive elements. In this way, the VCR of the converters can be controlled very precisely as opposed to SC-based converters. During the last ten years, the coauthors of this article have proposed a MEMS resonator-based power conversion architecture that can achieve high VCR without using inductors [192]–[194]. This type of "system-on-chip" solutions are still in their infancy, and extensive research is needed to come up with a universal solution that could be implanted without any EMI or MRI issues. Because resonators are electromechanical energy storage devices, power converter circuits based around them do not generate EMIs, which could be a key element to decide the optimum power converter topology for any given implantable application.

IX. Conclusion

This review article summarizes a plethora of state-of-the-art power conditioning circuits that can establish end-to-end power conditioning interfaces between in-body energy harvesting sources and target implant applications. Rectification, voltage regulation, and auxiliary circuit for maximum power transfer and cold-start constitute the basic end-to-end power conditioning interface for an implantable system. The uniqueness of each biomedical application creates a unique set of voltage and power requirements. Hence, elaborate knowledge on the strengths and limitations of each power conversion architecture and its working mechanism is of paramount importance. This knowledge can help the researchers to determine the power

conversion block that is the best fit for a specific set of implant load and energy harvesting/power delivery schemes.

With the recent advancements in power electronics technology, researchers are moving away from simple passive topologies toward advanced self-powered switching regulators. The active/synchronous full-wave rectifiers are more efficient than their passive counterparts; however, if a $V_{\rm th}$ mitigation technique and/or low-voltage threshold process is adopted, then passive rectifiers could possibly offer superior performance at lower power levels of implant application. VM are basically rectifying technologies with relatively poor voltage regulation ability. In designs where direct ac–dc conversion with regulated output voltage is required, single-stage direct ac–dc switched-mode converters can become a feasible solution. These single-stage converters are able to provide optimal impedance match to the low-power kinetic energy harvester in order to harvest maximum power. We have also reviewed two-stage power conversion topologies for implant applications, where the rectification stage is separate from the voltage conditioning and/or regulation stage. LDO is found to often offer a better choice compared to switched-mode converters for the circuits that require less than a few hundred milliwatts, provided that $V_{\rm in}$–$V_{\rm out}$ is small, and only voltage down-conversion is needed. Both types of dc–dc switched-mode converters, namely SCs and switched inductors, enable efficient up and down-conversion. Using PFM instead of PWM, SC converters offer better performance at comparatively ultralow ($\sim$0.1 μW) to low power ($\sim$1 mW) implantable loads. Compared to SC converters, switched-inductor converters are generally configured for higher output power IMDs ($>$1 mW) without significant area penalty. However, SC converters offering similar output power in the range of switched-inductor converters are appearing, whereas switched-inductor converters are less suitable for ultralow output powers. Nevertheless, EMI generated from the inductors used in inductor-based converters may pose a substantial health risk to patients hosting the associated IMDs. A micro-electromechanical system (MEMS) resonator-based converter can be an intriguing alternative to such inductor-based converters to mitigate EMI-related health hazards.

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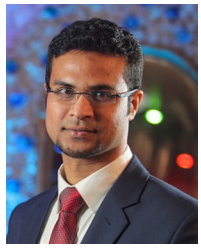

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