High-Efficiency Single-Phase Matrix Converter With Diverse Symmetric Bipolar Buck and Boost Operations

Hafiz Furqan Ahmed, Mohamed Shawky El Moursi, *Senior Member, IEEE*, Bashar Zahawi, *Senior Member, IEEE*, and Khalifa Al Hosani, *Senior Member, IEEE*

***Abstract*—Single-phase matrix converters (MCs) are undergoing rapid developments due to their bipolar voltage gain (as required in dynamic voltage restorers) and step-changed frequency operation (used in high step-up ac–dc rectifiers, and to provide medium frequency isolation in traction and wind turbine converters, etc.). However, existing buck–boost MCs require high-voltage/current rating devices, and suffer from large component voltage/current stresses and ripples, significantly degrading their efficiency. This article proposes a highly efficient single-phase buck–boost MC; consisting of eight IGBTs (implemented using two full-bridge IGBT modules), second-order input and output filters, and a small value film capacitor. Efficient discrete inverting and noninverting buck and boost operations are proposed (same as that of sixteen-switch cascaded buck–boost MC) with significantly lower component voltage/current stresses and ripples. In addition, flexible inverting and noninverting buck–boost operations are proposed with independent control of buck and boost duty ratios. All of the proposed operations are free of commutation issues, compatible with reactive loads, and provide smooth input and output currents. Furthermore, all the switches have same voltage stresses, and all four switches in a full-bridge module experience the same current stresses. A comprehensive description of circuit operation is presented based on a number of proposed switch modulation strategies with a nonunity power factor load, followed by design guidelines, and comparative evaluations with existing topologies. Finally, experimental verification results are presented, using a 400-VA laboratory prototype converter.**

***Index Terms*—AC–AC power conversion, bipolar buck–boost operation, high-efficiency, single-phase matrix converter.**

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I. Introduction

AC–AC power converters are widely used in industrial applications, for example, variable-speed drives; and to solve grid power quality issues, for example, to mitigate utility voltage sags and swells. Indirect ac–dc–ac converters [1], [2] with a constant dc-link can provide flexible control of amplitude, phase, and frequency of the output ac voltage. However, they have two-stage power conversion (ac to dc and dc to ac), while requiring a sizeable, short-life electrolytic capacitor at the dc-link. Direct PWM ac–ac converters [3], [4] and matrix converters (MCs) [5]–[7], on the other hand, can provide single-stage ac power conversion, eliminating the dc-link capacitor.

Single-phase direct ac–ac converters and MCs have been extensively researched for applications requiring various ac voltage operations, such as

1) unipolar voltage operation (direct ac–ac voltage regulators [8]);
2) bipolar voltage operation (dynamic voltage restorers (DVR) [9]);
3) step-changed frequency operation (high-gain ac–dc rectifiers [7], medium frequency isolation in traction, and wind turbine converters [10], [11], etc.).

The basic single-phase direct ac–ac buck, boost, and inverting buck–boost (or Cuk) converters [3], [4] have limited applications, mainly as direct ac voltage regulators, due to their unipolar gain operation. The single-phase Z-source [12]–[14], unified PWM [15], and switching-cell [16] direct ac–ac converters have been proposed with bipolar voltage operations, enabling them to compensate both voltage sag (using positive voltage injection) and voltage swell (using negative voltage injection), in applications such as DVR. However, the Z-source ac–ac converters in [12]–[14] lack noninverting buck operation, making them unable to compensate voltage sags of less than 50% when used as DVR [9]. Whereas, unified PWM [15] and switching-cell [16] ac–ac converters cannot provide noninverting boost operation, limiting their capability to mitigate voltage sags of only less than 50%.

Single-phase MCs [5]–[7] can provide symmetric bipolar gain operation, making them suitable for application as a DVR [17]. In addition, they can provide step-changed frequency output, which although not purely sinusoidal, is still useful for various applications as explored in [7], [10], [11], and [18]. However, the basic buck- and boost-type MCs [5], [7] suffer from a limited

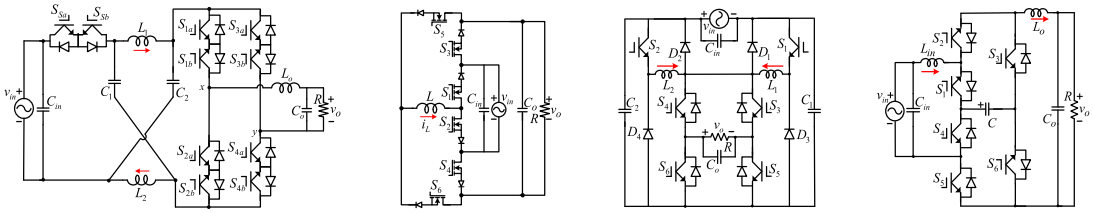

Fig. 1. Existing single-phase buck–boost MCs. (a) Z-source [19]. (b) Current-source type [20]. (c) Switching-cell [21]. (d) Three-switch leg [22].

TABLE I
SEMICONDUCTOR DEVICES REQUIREMENT AND STRESSES COMPARISON

Parameters	Buck MC [5]	Boost MC [7]	ZS buck-boost MC [19]	Current-source type buck-boost MC [20]	Switching-cell buck-boost MC [21, 22]	Three-switch leg buck-boost MC [23]	Proposed high-efficient buck-boost MC
Symmetric voltage gains (G)	$\pm D$	$\pm\frac{1}{1-D}$	$\pm\frac{1-D}{1-2D}$	$\pm\frac{D}{1-D}$	$\pm\frac{D}{1-D}$	$\pm\frac{D}{1-D}$	$\pm D, \pm\frac{1}{1-D}, \pm\frac{D_a}{1-D_b}$
No. of switching devices & Implementation	8 (IGBTs)	8 (IGBTs)	10 (IGBTs)	12 (6 IGBTs, 6 Diodes)/ 6 (RB-IGBTs)	10 (6 IGBTs, 4 Diodes)	6 (IGBTs)	8(IGBTs)/ 2 (commercial full bridge IGBT/MOSFET modules)
Main switches voltage stresses	v_{in}	v_o	$\frac{v_o}{1-D} > v_{in,o}$	$v_{in} + v_o$	$v_{in} + v_o$	$v_{in} + v_o$	v_{in}(Buck), v_o(Boost)
Main switches current stresses	i_o	i_{in}	$2i_{in} + i_o$	$i_{in} + i_o$	$i_{in} + i_o$	$i_{in} + i_o$	i_{in} *or* i_o
Uniform switches voltage/current stresses	Yes	Yes	No	No	No	No	Yes
Switching devices in power loop	4	4	6	6	4	4	4

voltage gain range (only buck or boost), narrowing the magnitude of voltage sags, which can be mitigated. To solve this limited gain range problem, a Z-source buck–boost MC [see Fig. 1(a)] is proposed in [19]. Nevertheless, this requires a large number of active switches and passive components, and is vulnerable to commutation issues, similar to the basic buck- and boost-MCs [5], [7]. A current-source type buck–boost MC [see Fig. 1(b)] is proposed in [20] overcoming the commutation issue, but this requires a large number of switching devices, and suffers from pulsating input and output currents. A switching-cell buck–boost MC [see Fig. 1(c)] is proposed in [21] with quasi-continuous input and output currents and no commutation issues. However, this uses four external diodes in addition to the six active switches, and has lower magnetic utilization. A modification to this circuit has been proposed [22] to make the input current continuous by adding two more inductors. A two three-switch legs buck–boost MC [see Fig. 1(d)] has recently been proposed [23], which has no commutation issue and provides continuous input and output currents.

However, all of the aforementioned existing buck–boost MCs [19]–[23] have common problems of inefficient buck–boost voltage operation with a voltage gain of $D/(1-D)$. To provide discrete buck or boost voltage, both buck and boost operations occur simultaneously, producing voltage gains of D_{bu} and $1/(1-D_{bo})$, respectively, with interdependent duty ratios $D_{bu} = D_{bo} = D$. The resultant voltage gain is therefore $D/(1-D)$, in which the effect of buck operation dominates at lower duty ratios ($D < 0.5$) producing step-down output voltage, and vice-versa. This operation results in large component voltage and current stresses (see Table I) and ripples and lower power conversion efficiency, as explained in the following.

1) The main high-frequency switches in these buck–boost MCs have higher voltage stresses of $v_{in} + v_{\rm o}$ (or similar, as given in Table I), compared to that of only v_{in} and $v_{\rm o}$ for basic buck [5] and boost [7] MCs, respectively. Moreover, the same switches also suffer from higher current stresses of $i_{\rm in} + i_{\rm o}$ (or similar, as given in Table I), compared to that of only $i_{\rm o}$ and $i_{\rm in}$ for basic buck and boost MCs, respectively.
2) These higher voltage and current stresses result in higher switching losses. Moreover, higher switch currents ($i_{\rm s} = i_{in} + i_{\rm o}$) lead to significantly higher conduction losses ($I_s^2 r_{\rm s}$, where $r_{\rm s}$ is the ON resistance of the switch). This increases power losses, reducing the power conversion efficiency.
3) Higher voltage and current rating devices are required increasing their cost; while higher voltage rating IGBTs have higher switching and conduction losses [24]. Moreover, the switches have nonuniform voltage/current stresses and losses, requiring discrete switching devices with complicated heat sink design [25].
4) The inductors suffer from higher current ripples Δi_L (and magnetic flux density swings ΔB), which increase magnetic requirement and losses. Moreover, the buck–boost MCs in [20] and [21] have higher inductor current handing requirement of $i_{\rm in} + i_{\rm o}$, greatly increasing their winding losses ($I_L^2 r_L$).

To solve these above mentioned problems of existing buck–boost MCs [19]–[22], this article proposes a highly efficient single-phase buck–boost MC, consisting of a small film capacitor, input, and output *LC* filters, and eight active switches. The proposed converter can provide very efficient discrete

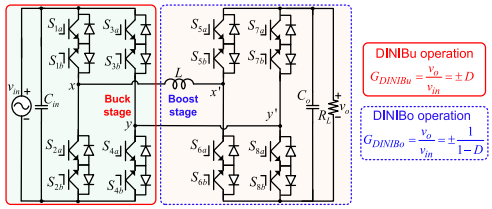

Fig. 2. Conventional single-phase cascaded buck–boost MC.

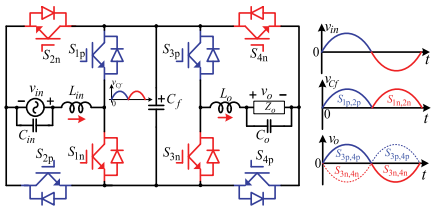

Fig. 3. Proposed high-efficiency buck–boost MC.

inverting and noninverting buck (DINIBu) mode operations with voltage gains of $\pm D_a$, in which the boost stage is completely bypassed. It can also produce very efficient discrete inverting and noninverting boost (DINIBo) mode operations with voltage gains of $\pm 1/(1 - D_a)$, in which the buck stage is bypassed. These operating modes are highly efficient with lower switch voltage stresses (of only v_{in} or v_o), lower switch current stresses (of only i_{in} or i_o), and lower inductor current handling requirements and ripples. Flexible inverting and noninverting buck–boost (fINIBB) operating modes are also proposed, with independent control of buck and boost duty ratios. These operating modes also have lower component stresses and ripples. All of the proposed operations have no commutation issues, provide continuous input and output currents, and work well with nonunity power factor loads. Moreover, the eight switching devices can be implemented using two commercially available industry standard full-bridge IGBT/MOSFET modules (due to uniform stresses as given in Table I), which can simplify the converter design, improve power density, and reduce the cost. Comprehensive circuit operations for all operating modes are presented. Component design and selection guidelines are discussed along with comparisons with existing topologies. Finally, experimental results are provided to verify circuit operations, obtained using a 400-VA laboratory prototype converter.

II. Proposed Single-Phase Buck–Boost MC

To overcome the previously discussed inefficient operation problem of existing buck–boost MCs in [19]–[23], the conventional solution is to cascade a basic buck MC [5] with a boost MC [7], as shown in Fig. 2. This cascaded buck–boost MC can provide DINIBu and DINIBo operations with lower component stresses/ripples. However, it requires 16 active switches, with eight of them being in a power loop at all times. Fig. 3 shows the proposed buck–boost MC, which can be easily put together by connecting a small film capacitor C_f and second-order input and output LC filters ($L_{in}C_{in}$, L_oC_o) with two full-bridge IGBT

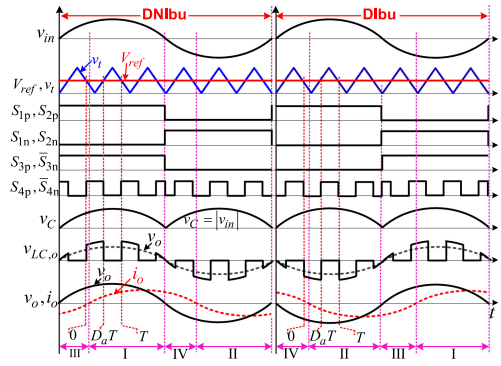

Fig. 4. Switch gate signals and major waveforms for the DINIBu operation.

modules. The circuit structure resembles that of a single-phase back-to-back (B2B) full-bridge ac–dc–ac converter with a dc-link [2]. Nevertheless, the existing converter in [2] is of indirect ac–dc–ac type with two power conversion stages, requiring a high-value dc-link capacitor (>1mF) to maintain a constant dc-link voltage. For this high capacitance requirement, inevitably a bulky electrolytic capacitor is utilized, which decreases the power density of the converter and suffers from a short life span due to its wear-out characteristics [26]. The proposed buck–boost MC, on the other hand, provides single-stage direct ac–ac power conversion with capacitance C_f requirement of only a few microfarads (>1 μF), which is hundreds of times smaller than that in an indirect ac–dc–ac converter [2]. A reliable (long-life), efficient (low ESR loss), and small value film capacitor can therefore can be utilized in the proposed buck–boost MC.

A. Discrete Inverting and Noninverting Buck Operation

From the switch gate signals and key waveforms in Fig. 4, the input bridge switches ($S_{1p,1n} - S_{2p,2n}$) are operated at low (line) frequency. This folds (or converts) the input ac voltage v_{in} into a rectified sinusoidal voltage across the capacitor C_f ($v_{Cf} = |v_{in}|$). Whereas, the output bridge switches ($S_{3p,3n} - S_{4p,4n}$) provide buck operation while unfolding the rectified sinusoidal voltage of C_f into a sinusoidal ac voltage v_o at the output, with the same polarity as that of v_{in} (discrete noninverting buck DNIBu operation), or with the opposite polarity as that of v_{in} (discrete inverting buck DIBu operation).

Circuit operation for $v_{in} > 0$ is explained as follows.

1) Mode-I and II: The equivalent circuits for mode-I ($v_o, i_o > 0$) in DNIBu operation and mode-II ($v_o, i_o < 0$) in the DIBu operation are shown in Figs. 5 and 6, respectively. The switches S_{1p} and S_{2p} are always turned-ON and v_{in} is applied across C_f ($v_{Cf} = v_{in}$).

For the D_aT interval during DNIBu operation [see Fig. 5(a)], the capacitor C_f provides energy to the output inductor L_o and load Z_o, through switches S_{3p} and S_{4p}. Circuit operation is the same as for D_aT interval during DIBu operation, as shown in Fig. 6(a), with the only difference being that switches S_{3n} and S_{4n} are now turned-ON (instead of S_{3p} and S_{4p}), and the polarity of the voltage v_{Cf} is reversed across the output filter

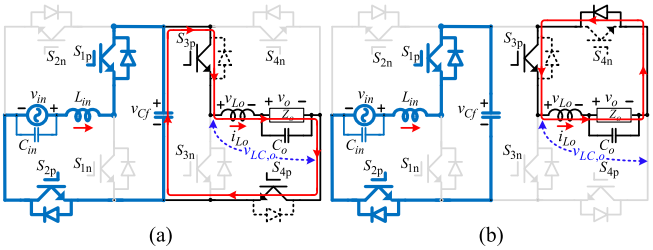

Fig. 5. Equivalent circuits for the DNIBu operation when $v_{in} > 0$, mode-I ($v_o > 0,\ i_o > 0$). (a) D_aT interval. (b) $(1 - D_a)T$ interval.

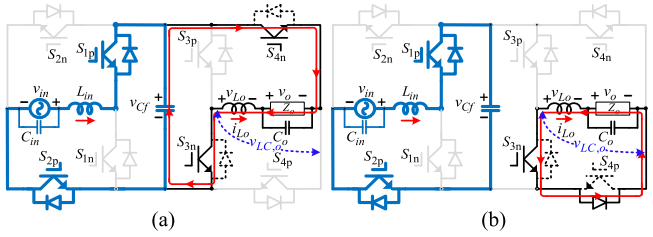

Fig. 6. Equivalent circuits for the DIBu operation when $v_{in} > 0$, mode-II ($v_o < 0,\ i_o < 0$). (a) D_aT interval. (b) $(1 - D_a)T$ interval.

(L_oC_o). Circuit equations are given by

$$\begin{cases} v_{Lo} + v_o = v_{Cf}\ (=v_{in}), & DNIBu \\ v_{Lo} + v_o = -v_{Cf}\ (=v_{in}), & DIBu. \end{cases} \tag{1}$$

For the $(1 - D_a)T$ interval during DNIBu operation [see Fig. 5(b)], S_{4p} is turned-OFF while S_{4n} is turned-ON. The inductor L_o releases its energy to the load Z_o through switches S_{3p} and S_{4n}. Operation is the same as during DIBu operation, as shown in Fig. 6(b), with the only difference being that the inductor L_o current (i_{Lo}) flows through switches S_{3n} and S_{4p}. Circuit equations are given by

$$\begin{cases} v_{Lo} = -v_o, & DNIBu \\ v_{Lo} = -v_o, & DIBu. \end{cases} \tag{2}$$

2) Mode-III and IV: Mode-III ($v_o > 0, i_o < 0$) and mode-IV ($v_o\langle 0, i_o\rangle 0$) are regenerative modes, which occur for reactive loads (inductive), where the direction (or polarity) of i_o is reversed (become opposite to that of v_o), as shown in Fig. 4. Due to the use of bidirectional current switches (IGBTs/MOSFETs with antiparallel diodes), the reversed i_{Lo} current can flow through the same current loops but through the dotted IGBT and antiparallel diodes, as shown in Figs. 5 and 6.

Operation for $v_{in} < 0$ is the same as that explained for $v_{in} > 0$, but with the switching signals and operations of switches S_{xp} and S_{xn} ($x = 1, 2, 3, 4$) interchanged.

Using (1) and (2), the voltage gains G_a for DINIBu operations are given by

$$G_a = \frac{v_o}{v_{in}} = \pm D_a. \tag{3}$$

B. Discrete Inverting and Noninverting Boost Operation

Fig. 7 shows the switch gate signals and key waveforms for the DINIBo operation. The input bridge switches ($S_{1p,1n} - S_{2p,2n}$)

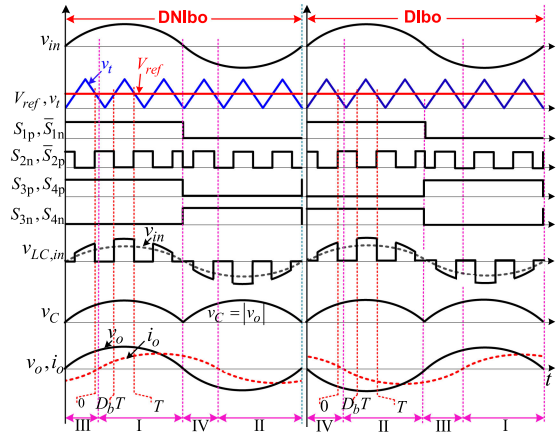

Fig. 7. Switch gate signals and major waveforms for DINIBo operation.

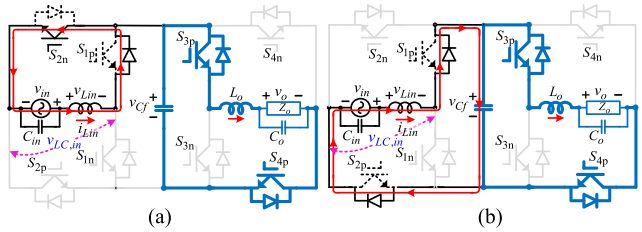

Fig. 8. Equivalent circuits for DNIBo operation when $v_{in} > 0$, mode-I ($v_o > 0,\ i_o > 0$). (a) D_bT interval. (b) $(1 - D_b)T$ interval.

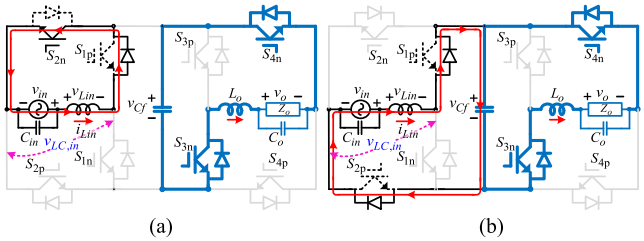

Fig. 9. Equivalent circuits for DIBo operation when $v_{in} > 0$, mode-II ($v_o < 0,\ i_o < 0$). (a) D_bT interval. (b) $(1 - D_b)T$ interval.

now provide boost operation of the ac input voltage v_{in} and fold it into a rectified sinusoidal waveform across capacitor C_f. The output switches ($S_{3p,3n} - S_{4p,4n}$) operate at line frequency to unfold the rectified voltage v_{Cf} into ac voltage v_o at the output.

Circuit operation for $v_{in} > 0$ is explained in the following.

1) Mode-I and II: From Fig. 8 for DNIBo operation, switches S_{3p} and S_{4p} are always turned-ON, applying the positive capacitor voltage v_{Cf} across the load Z_o through the output filter L_oC_o. Whereas, the reverse capacitor voltage $-v_{Cf}$ is applied across Z_o through switches S_{3n} and S_{4n} during DIBo operation, as shown in Fig. 9.

For D_bT interval during DNIBo and DIBo operations, [see Figs. 8(a) and 9(a), respectively], the input inductor L_{in} stores energy from input source v_{in} through switches S_{1p} and S_{2n}. Circuit equations are given by

$$v_{Lin} = v_{in} \quad \text{DINIBo.} \tag{4}$$

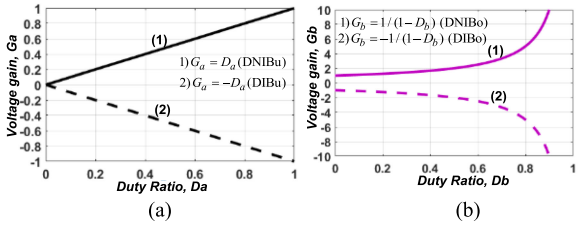

Fig. 10. Voltage gain (G) versus converter duty ratio (D). (a) DINIBu operation. (b) DINIBo operation.

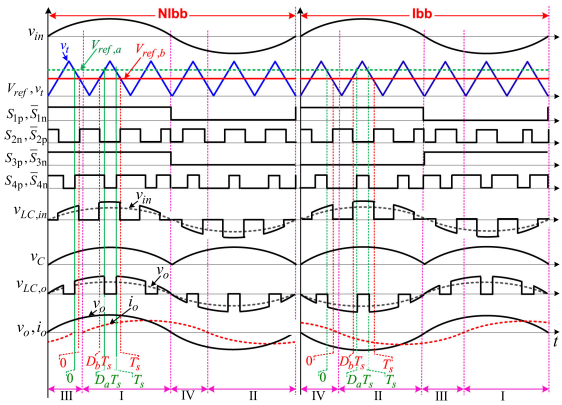

Fig. 11. Switch gate signals and major waveforms for the fINIBB operation.

For the $(1 - D_b)T$ interval during DNIBo and DIBo operations, the input source v_{in} and inductor L_{in} charge capacitor C_f through switches S_{1p} and S_{2p}, as shown in Figs. 8(b) and 9(b), respectively. Circuit equations are given by

$$\begin{cases} v_{in} - v_{Lin} = v_{Cf}\,(=v_o)\,, & DNIBo \\ v_{in} - v_{Lin} = v_{Cf}\,(=-v_o)\,, & DIBo. \end{cases} \tag{5}$$

2) Mode-III and IV: Mode-III ($v_o > 0, i_o < 0$) and mode-IV ($v_o \langle 0, i_o \rangle 0$) occur for nonunity power factor loads. However, the reversal of both input and output inductor currents (i_{Lin}, i_{Lo}) is possible due to bidirectional conducting devices, making these operations compatible with reactive loads.

The voltage gains G_b for DINIBo operations are given by

$$G_b = \frac{v_o}{v_{in}} = \pm\frac{1}{1 - D_b}. \tag{6}$$

The voltage gains (G) are plotted against duty ratio (D) in Fig. 10 for DINIBu and DINIBo operations. The gains are the same as that of the 16 switch cascaded buck–boost MC (see Fig. 2).

C. Flexible Inverting and Noninverting Buck–Boost Operation

Fig. 11 shows switch gate signals and key waveforms for the fINIBB operation when $D_a > D_b$. Compared to existing buck–boost MCs [19]–[22] with dependent buck (D_a) and boost (D_b) duty ratios (i.e., $D_a = D_b$, always), D_a and D_b can be independently adjusted in the proposed fINIBB operation, making it possible to select optimal values of D_a and D_b for more an efficient operation.

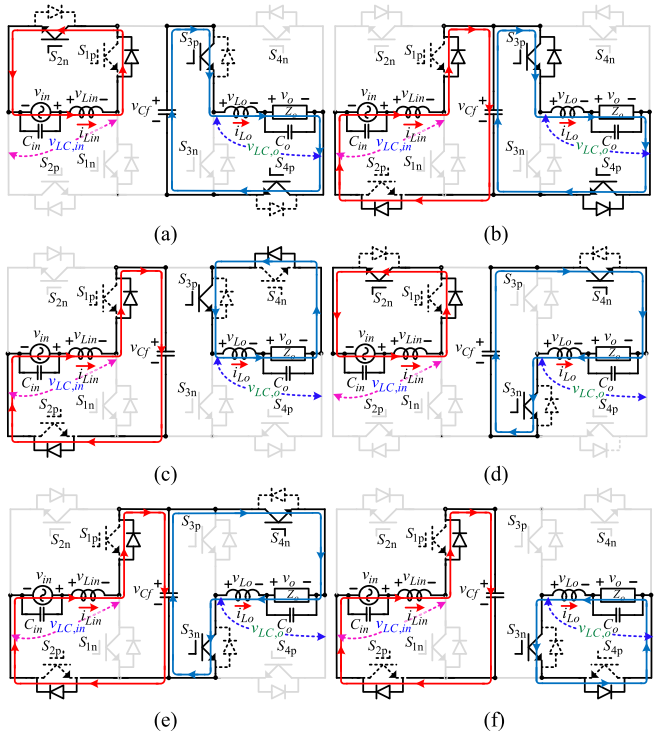

Fig. 12. Equivalent circuits for fINIBB operation when $v_{in} > 0$: (a), (b) and (c) are for fNIBB operation, mode-I ($v_o > 0,\ i_o > 0$); (a) D_aT and D_bT intervals. (b) D_aT and $(1 - D_b)T$ intervals. (c) $(1 - D_a)T$ and $(1 - D_b)T$ intervals. (d), (e), and (f) are for fIBB operation, mode-II ($v_o < 0,\ i_o < 0$); (d) D_aT and D_bT intervals. (e) D_aT and $(1 - D_b)T$ intervals. (f) $(1 - D_a)T$ and $(1 - D_b)T$ intervals.

The input bridge switches $S_{1p,1n} - S_{2p,2n}$ provide boost operation of the input voltage v_{in} and fold it into a rectified sinusoidal voltage across the capacitor C_f. Meanwhile, the output bridge switches $S_{3p,3n} - S_{4p,4n}$ provide buck operation of the voltage across C_f and unfold it into a sinusoidal ac voltage at the load.

Circuit operation for $v_{in} > 0$ is explained in the following.

1) Mode-I and II: From Fig. 12(a) and (d), inductor L_{in} stores energy from the input source v_{in} through switches S_{1p}, S_{2n}, during the D_bT interval for fNIBB and fIBB operations, respectively. Meanwhile, the capacitor C_f discharges and provides energy to L_o and the load Z_o through switches S_{3p}, S_{4p} (fNIBB operation) or S_{3n}, S_{4n} (fIBB operation) during the D_aT interval. Circuit equations are given by

$$\begin{cases} v_{Lin} = v_{in}, & D_bT \\ v_{Lo} + v_o = \pm v_{Cf}, & D_aT. \end{cases} \tag{7}$$

Fig. 12(b) and (e) shows the equivalent circuits for fNIBB and fIBB operations, respectively, when v_{in} and L_{in} charge C_f through S_{1p}, S_{2p} in $(1 - D_b)T$ interval. Whereas C_f still provides energy to L_o and load Z_o in the D_aT interval. Circuit equations are given by

$$\begin{cases} v_{in} - v_{Lin} = v_{Cf}, & (1 - D_b)T \\ v_{Lo} + v_o = \pm v_{Cf}, & D_aT. \end{cases} \tag{8}$$

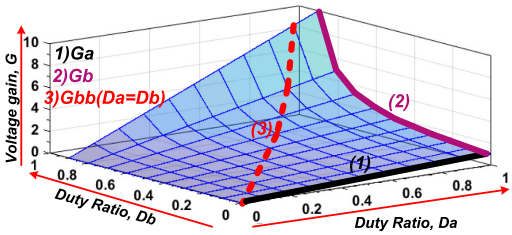

Fig. 13. 3-D plot of voltage gain (G) versus converter duty ratios D_a and D_b for fINIBB operation (only fNIBB operation is plotted).

Fig. 12(c) and (f) shows the equivalent circuits for fNIBB and fIBB operations, respectively, when L_o provides the stored energy to load Z_o through switches S_{3p}, S_{4n} (fNIBB operation) or S_{3n}, S_{4p} (fIBB operation) in the $(1 - D_a)T$ interval. Whereas v_{in} and L_{in} keep charging C_f through S_{1p}, S_{2p} in the $(1 - D_b)T$ interval. Circuit equations become

$$\begin{cases} v_{in} - v_{Lin} = v_{Cf}, & (1 - D_b)T \\ v_{Lo} = -v_o, & (1 - D_a)T. \end{cases} \tag{9}$$

2) Mode-III and IV: These are the same as Mode-I and II, with the only difference being that the current i_{Lo} flows in the reverse direction through the same bidirectional switches.

The voltage gains G_c for fINIBB operations are given by

$$G_c = \frac{v_o}{v_{in}} = \pm\frac{D_a}{1 - D_b}. \tag{10}$$

Fig. 13 shows a 3-D plot of the positive portion of G_c versus buck and boost duty ratios (D_a, D_b). From this figure, the gain curves G_a and G_b (during DINIBu and DINIBo operations, respectively) are special cases of voltage gain G_c during the fINIBB operation, when $D_b = 0$ and $D_a = 1$, respectively. The buck–boost gain curve G_{bb} (=D/(1–D)), as shown in Fig. 13, is obtained when $D_a = D_b$, which is the only achievable gain for existing buck–boost MCs [20]–[22]. For any arbitrary buck–boost voltage gain, operating at $D_a > D_b$ (represented by all the gain curve area enclosed by G_a, G_b, and G_{bb} curves) would provide better operation (lower voltage/current stresses and ripples of the components) than existing buck–boost MCs [20]–[22].

Conventional direct ac–ac/MCs are based on the bidirectional current flow and bidirectional voltage blocking devices, which are deprived of natural free-wheeling paths for inductor current during dead-time, leading to the commutation issues [28], [29]. This commutations problem is illustrated in Fig. 14 for a single-phase buck-type MC. The upper and lower bidirectional switches in each leg (S_{1ab} and S_{2ab} in the first leg) are switched in a complementary manner. However, the delayed responses of gate drive circuits and limited speed of switching devices would result in a small overlap [see Fig. 14(a)] or dead time [see Fig. 14(b)] between complementary devices in each switching transition, leading to current overshoots (*di/dt*) or voltage spikes (*dv/dt*), respectively. To deal with these commutation issues, dedicated safe-commutation switching strategies are required [29] based on the sensing of input voltage polarity, output current directions, or both.

The proposed topology utilizes bidirectional current flow, but unidirectional voltage blocking switching devices (same as dc–ac inverter), each of which implemented with a single IGBT/MOSFET switch. Commutations issues are simply resolved by adding a small dead-time between complementary switches due to the presence of natural inductor current freewheeling paths. Fig. 15 shows the inductors L_{in} and L_o current paths during dead-time when all switches are assumed to be turned-OFF. As evident, both positive and negative inductor currents $(\pm i_{Lin}, \pm i_{Lo})$ have continuous paths to flow through the antiparallel diodes of the switches and the capacitor C_f, eliminating any commutation issues.

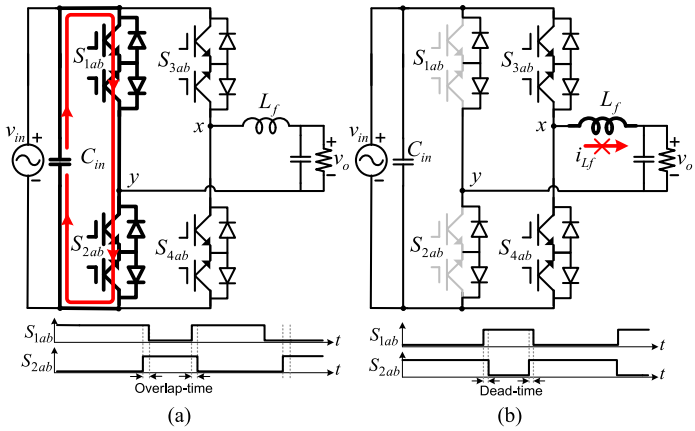

Fig. 14. Commutation problems in the buck-type MC. (a) Overlap time. (b) Dead time.

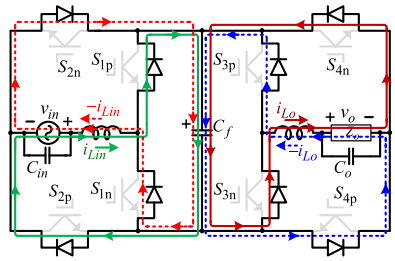

Fig. 15. Inductors L_{in} and L_o current flow paths during dead-time.

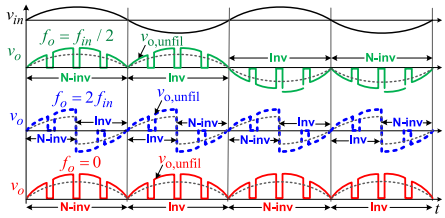

Fig. 16. Step-up/step-down frequency operation and ac-dc rectification.

D. Adjustable Frequency Operation

The proposed buck–boost MC can produce an output voltage with step-changed frequency. This is simply achieved by periodically switching between noninverting and inverting operations [20], as shown in Fig. 16. These step-changed frequency output voltages of the proposed buck–boost MC are not purely sinusoidal, similar to all the single-phase MCs [5]–[7], [19]–[22],

TABLE II
VOLTAGE/CURRENT VALUES AND RIPPLES OF THE PROPOSED BUCK–BOOST MC

Parameter		DINIBu	DINIBo	fINIBB
Switch voltages/ currents	v_{sw}	$v_{S1} - v_{S4} = v_o$	$v_{S1} - v_{S4} = v_{in}$	$v_{S1} - v_{S4} = G_b v_{in}$
	i_{sw}	$i_{S1}, i_{S2} = i_{in}$ $i_{S3}, i_{S4} = i_o$	$i_{S1}, i_{S2} = i_{in}$ $i_{S3}, i_{S4} = i_o$	$i_{S1}, i_{S2} = i_{in}$ $i_{S3}, i_{S4} = i_o$
Inductor current/ ripples	i_L	$i_{Lin} = i_{in}$, $i_{Lo} = i_o$	$i_{Lin} = i_{in}$, $i_{Lo} = i_o$	$i_{Lin} = i_{in}$, $i_{Lo} = i_o$
	Δi_L	$\Delta i_{Lo} = \frac{v_o(1-D_a)T}{L_o}$	$\Delta i_{Lin} = \frac{v_{in}D_bT}{L_{in}}$	$\Delta i_{Lin,DINIBo}$ $\Delta i_{Lo,DINIBu}$
Capacitor voltage/ ripples	v_C	$v_C = v_{in}$	$v_C = v_o$	$v_C = G_b v_{in}$
	Δv_C	$\Delta v_C \approx 0$	$\Delta v_C = \frac{i_o D_b T}{C}$	$\Delta v_C = \frac{i_o D_b T}{C}$

however, they are still well suitable for various applications given in [7], [10], [11], and [18] as mentioned earlier. In addition, the proposed buck–boost MC can also operate as a single-phase ac–dc matrix rectifier (see Fig. 16).

III. COMPONENT DESIGN AND SELECTION OF THE PROPOSED BUCK BOOST MC

The component voltage and current stresses/ripples of the proposed buck–boost MC are given in Table II.

A. Switch Voltage Stresses

Switch voltage stresses v_s are obtained as

$$\begin{cases} v_{S1(p,n)-S4(p,n)} = \frac{v_o}{G}; & DINIBu \\ v_{S1(p,n)-S4(p,n)} = v_o; & DINIBo\,. \end{cases} \tag{11}$$

Maximum switch voltage stresses occur during the DINIBu operation when *G* has a minimum value.

B. Switch Current Stresses

Switch current stresses i_s are determined as follows:

$$\begin{cases} i_{S1(p,n)}, \quad _{S2(p,n)} = i_o G \\ i_{S3(p,n)}, \quad _{S4(p,n)} = v_o. \end{cases} \tag{12}$$

Switches S_1 and S_2 have same current stresses for DINIBu and DINIBo operations. Switches S_3 and S_4 have maximum current stresses during the DINIBo operation when *G* is at maximum value.

C. Inductor Design

The inductors L_{in} and L_o have current handling requirement of i_{in} and i_o, respectively. The inductor current ripples Δi_L (and flux density swings ΔB) can be determined as

$$\begin{cases} \Delta i_{Lin}\,(or\ \Delta B_{Lin}) = \frac{v_o T}{L_{in}\ (or\ NA_e)} \frac{G-1}{G^2}; & DINIBo \\ \Delta i_{Lo}\,(or\ \Delta B_{Lo}) = \frac{v_o T}{L_o or\ (or\ NA_e)}\,(1-G)\,; & DINIBu. \end{cases} \tag{13}$$

Using (13), the minimum inductance values L can be determined to limit inductor current ripple Δi_L to $x\%$ of inductor current I_L; $\Delta i_L = x\%\ I_L$ and $x = 10$ to 50.

D. Capacitor Design

The capacitor *C* has a voltage stress of v_o/G for the DINIBu operation and v_o for the DINIBo operation. Its voltage ripple Δv_C can be found as

$$\Delta v_c = \frac{i_o T}{C}\frac{G-1}{G}; \quad \text{DINIBo.} \tag{14}$$

From (14), the capacitance value *C* can be determined to limit $\Delta v_C = x\%\ v_C$ ($x = 5$ to 20).

IV. COMPARISON OF COMPONENT VOLTAGE AND CURRENT STRESSES AND RIPPLES

To show the reduction in component voltage and current stresses and ripples of the proposed buck–boost MC, this section provides a detail comparison with existing buck–boost MCs [19]–[23].

A. Switching Devices

The proposed buck–boost MC has a simple device configuration with uniform voltage and current stresses unlike existing buck–boost MCs. Thus, it can utilize two industry standard full-bridge IGBT/MOSFET modules.

The voltage stresses v_s of the main high-frequency conducting switches in existing counterpart buck–boost MCs (in terms of v_o and *G*) are given as

$$\begin{cases} v_s^{\text{INIBu}} = \left(2 + \frac{1}{G}\right) v_o, v_s^{\text{INIBo}} = \left(2 - \frac{1}{G}\right) v_o; & [19] \\ v_s^{\text{INIBB}} = \left(1 + \frac{1}{G}\right) v_o; & [20],\ [21],\ [22],\ [23]. \end{cases} \tag{15}$$

Using (11) and (15), the variations of the normalized switch voltage stress (v_s/v_o) versus voltage gain *G* of the proposed and counterpart buck–boost MCs are plotted in Fig. 17(a). Clearly, the proposed buck–boost MC has significantly lower switch voltage stresses for the entire gain (*G*) range.

The current stresses i_s of the main high-frequency conducting switches in the counterpart buck–boost MCs are given by

$$\begin{cases} i_s^{\text{INIBB}} = (2+G)\, i_o; & [19] \\ i_s^{\text{INIBB}} = \left(1 + \frac{1}{G}\right) v_o; & [20],\ [21],\ [22],\ [23]. \end{cases} \tag{16}$$

Using (12) and (16), normalized switch current stresses (i_s/i_o) versus voltage gain *G* are plotted in Fig. 17(b). As observed, switching devices in the proposed buck–boost MC have much lower current stresses.

These higher switch voltage and current stresses of existing buck–boost MCs [19]–[22] increase their switching losses. In addition, they require high-voltage rating IGBTs with relatively poor switching and conduction performances [24]. Their switch conduction ($I_s^2 r_s$) losses are also significantly higher. The total switch conduction losses in the proposed buck–boost MC and existing buck–boost MCs (assuming the same switch

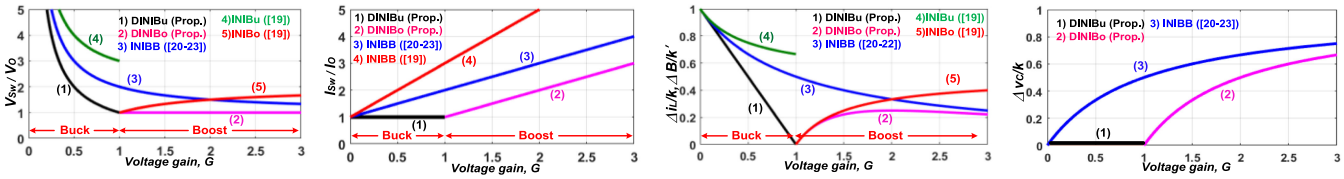

Fig. 17. Comparison plots. (a) Switch voltages. (b) Switch currents. (c) Inductor current ripples or flux density swing. (d) Capacitor voltage ripples.

ON-resistance r_s) are given by

$$\begin{cases} P_{s,\text{cond}} = \left(2I_{in}^2 + 2I_o^2\right) r_s\,; & \text{Proposed} \\ P_{s,\text{cond}} = P_{s,\text{cond}}^{\text{Proposed}} + \left(4I_{in}^2 + 4I_o^2 + 2I_{in}I_o\right) r_s; & [20] \\ P_{s,\text{cond}} = P_{s,\text{cond}}^{\text{Proposed}} + \left(I_o^2 + 2I_{in}I_o\right) r_s; & [21], [22], [23] \end{cases} \tag{17}$$

From (17), all existing buck–boost MCs have higher switch conduction losses than the proposed buck–boost MC.

B. Inductors

The proposed buck–boost MC utilizes two inductors L_{in} and L_o, which ensure the supply of continuous input and output currents.

The inductor current ripples Δi_L (and magnetic flux density swings ΔB) for the existing buck–boost MCs are given by

$$\begin{cases} \Delta i_L\,(or \Delta B\,) = \frac{v_o T}{L_{1,2,o}\ or\ (N_t A_e)} \frac{G+1}{(2G+1)}; & INIBu\ ([19]) \\ \Delta i_L\,(or \Delta B\,) = \frac{v_o T}{L_{1,2,o}\ or\ (N_t A_e)} \frac{G-1}{(2G-1)}; & INIBo\ ([19]) \\ \Delta i_L\,(or \Delta B\,) = \frac{v_o T}{L\ or\ (N_t A_e)} \frac{1}{(1+G)}; & [20],\ [21],\ [22],\ [23] \end{cases} \tag{18}$$

where N_t is the number of turns of the inductor and A_e is the cross-sectional area of the magnetic core. From (13) and (18), the normalized inductor current ripple $\Delta i_L/k$ ($k = v_o\,T/L$) [or magnetic flux density $\Delta B/k'$ ($k' = v_o\,T/N_t A_e$)] for all the buck–boost MCs under comparison are plotted in Fig. 17(c). As observed, the inductors L_{in} and L_o in the proposed buck–boost MC have lower current ripples (less inductance requirement) and flux density swings (lower magnetic core losses).

The inductors L_{in} and L_o in the proposed buck–boost MC have much lower current handling requirement of i_{in} and i_o, respectively, compared to that of $i_{in} + i_o$ for counterpart MCs [20], [21]. Considering the effect of the inductor current ripple Δi_L, the inductor current handling requirements ($i_L + \Delta i_L/2$) of the proposed MC would be smaller than that of counterpart MCs [19], [22], [23].

The total inductor winding conduction losses $P_{L,\text{cond}}$ ($I_L^2 r_L$, where r_L is the winding resistance of the inductor) of the proposed and existing buck–boost MCs [19]–[23] are given by

$$\begin{cases} P_{L,\text{cond}} = \left(I_{in}^2 + I_o^2\right) r_L\,; & Proposed,\ [22],\ [23] \\ P_{L,\text{cond}} = P_{L,\text{cond}}^{\text{Proposed}} + I_{in}^2 r_L\,; & [19] \\ P_{L,cond} = P_{L,\text{cond}}^{\text{Proposed}} + 2I_{in}I_o\, r_L; & [20], [21]. \end{cases} \tag{19}$$

From (19), the inductor winding conduction losses of buck–boost MCs in [19]–[21] are higher than that in the proposed buck–boost MC. Therefore, the proposed buck–boost MC would have smaller total magnetic losses (magnetic core and winding conduction losses).

C. Capacitors

The capacitor voltage ripples Δv_C for the counterpart buck–boost MCs are given by

$$\Delta v_c = \frac{i_o T}{C} \frac{G}{G+1}; \quad \text{DINIBB.} \tag{20}$$

Using (14) and (20), the normalized capacitor voltage ripple $\Delta v_C/k$ ($k = i_o\,T/C$) is plotted in Fig. 17(d) for the proposed and counterpart buck–boost MCs. The capacitor C in the proposed buck–boost MC has a smaller voltage ripple (or less required capacitor value).

The voltage stresses of the capacitor C in the proposed buck–boost MC are v_o/G and v_o for DINIBu and DINIBo operations, respectively, which are much smaller than that of $v_{in} + v_o$ for the capacitors in counterpart buck–boost MCs [20], [21]. The capacitor C voltage stress would also be lower than that in counterpart buck–boost MC in [19] and [22] when capacitor voltage ripple is considered.

To further validate the above-mentioned benefits of the proposed buck–boost MC, the numerical values of component voltage and current stresses and ripples of the proposed and counterpart buck–boost MCs [20]–[23] are listed in Table III for the same practical operating conditions ($v_{in} = 45{\sim}95\ V_{\text{rms}}$, $v_o = 70\ V_{\text{rms}}$, $P_o = 200$ W, $f_{sw} = 25$ kHz) as given in [20]–[23], and the same passive component values ($L = 800\ \mu$H, $C = 6\ \mu$F). Clearly, the components in the proposed buck–boost MC experience much smaller voltage and current stresses and ripples.

V. Comparative Evaluation of Switching Devices Power Ratings/Losses and Passive Component Volumes

The volume of a power converter is contributed by switching devices, heat sinks, and passive components. To compare the volumes of the proposed and counterpart buck–boost MCs [20]–[23], analytical methods in [21], [22], [30], and [31] are adapted to determine the switching devices power ratings and losses (which reflect the sizes of switching devices plus heat sinks) and stored energies of passive components (which reflect the volume of passive components). The buck–boost MC in [19] has already proved to have much higher switching devices power

TABLE III:
COMPARISON OF COMPONENT VOLTAGE AND CURRENT STRESSES AND RIPPLES

Parameters		Z-Source buck-boost MC [19]	Current-source type buck-boost MC [20]	Switching-cell buck-boost MC [21]	Modified Switching-cell buck-boost MC [22]	Three-switch leg buck-boost MC [23]	Proposed high-efficient buck-boost MC
Max. switch voltage stress $V_{s,max}$	Buck	332.3 V	233.3 V	233.3 V	233.3 V	233.3 V	134.4 V
	Boost	134.4 V	162.6 V	162.6 V	162.6 V	162.6 V	99 V
Max. switch current stress $I_{s,max}$	Buck	11.1 A	7.02 A	7.02 A	7.02 A	7.02 A	4.04 A
	Boost	14.3 A	10.33 A	10.33 A	10.33 A	10.33 A	6.3 A
Inductor current ripple Δi_L	Buck	$\Delta i_{L1,L2,Lo}$=3.48 A	Δi_L = 2.85 A	$\Delta i_{L1,L2}$ = 2.85 A	Δi_{L1-L4} = 2.85 A	$\Delta i_{Lin,Lo}$ = 2.85 A	Δi_{Lin} = 0 A, Δi_{Lo} =1.3 A
	Boost	$\Delta i_{L1,L2,Lo}$=1.59 A	Δi_L =1.94 A	$\Delta i_{L1,L2}$ =1.94 A	Δi_{L1-L4} =1.94 A	$\Delta i_{Lin,Lo}$ =1.94 A	Δi_{Lin} = 1.14 A, Δi_{Lo} =0 A
Inductor current handling requirement ($I_L + \Delta i_L/2$)		L_{in1}, L_{in2}: 7.1 A L_o: 5.78 A	L: 11.3 A	L_1, L_2: 11.3 A	L_{in1}, L_{in2} : 7.3 A L_{o3}, L_{o4}: 5.5 A	L_{in}: 7.3 A L_o: 5.5 A	L_{in}: 6.86 A L_o: 4.69 A
Capacitor voltages stresses $v_C + \Delta v_C/2$		240.2 V	NA	239 V	139 V	239 V	134.4 V
Capacitor voltage ripples		10.2 V	NA	16.4 V	16.4 V	16.4 V	9.62 V

ratings/losses and passive component volumes [20], [21] and thus, not included for comparison.

A. Switching Devices Power and Heatsink Requirements

As proposed in [30], the total peak switching device power SDP_{pk} is a direct indicator of current and voltage ratings and cost of switching devices. Whereas, total average switching device power SDP_{avg} is a direct indicator of their power losses and thus, thermal requirement and sizes of heat sinks. The SDP_{pk} and SDP_{avg} are determined as

$$\begin{cases} SDP_{pk} = \sum_{n=1}^{N} V_n^{pk}\, I_n^{pk} \\ SDP_{\text{avg}} = \sum_{n=1}^{N} V_n^{pk}\, I_n^{\text{avg}} \end{cases} \tag{21}$$

where N is the total number of switching devices, V_n^{pk} is the peak voltage stress of the nth switching device, and I_n^{pk} and I_n^{avg} are its peak and average current stresses, respectively.

The SDP_{pk} and SDP_{avg} of the proposed buck–boost MC in terms of voltage gain G are given by

$$\begin{cases} SDP_{pk} = \frac{8+8G}{G} P_o; & DINIBu \\ SDP_{pk} = (8+8G)\, P_o; & DINIBo \end{cases} \tag{22}$$

$$\begin{cases} SDP_{\text{avg}} = \frac{8+4G}{\pi G} P_o; & DINIBu \\ SDP_{\text{avg}} = \frac{8+4G}{\pi} P_o; & DINIBo. \end{cases} \tag{23}$$

The SDP_{pk} and SDP_{avg} (normalized with respect to P_o) of the proposed and counterpart buck–boost MCs [20]–[23] are plotted against G in Fig. 18(a) and (b), respectively. Clearly, the proposed buck–boost MC has much lower SDP_{pk} and SDP_{avg} values, indicating it can utilize lower rating switching devices with less power losses, and require smaller size heat sinks.

B. Stored Energies and Volume Requirements of Passive Components

Passive components are a major contributor to the overall volume of the converter. They are designed to limit the voltage and current ripples within a specific limit. The volumes of inductors and capacitors are directly proportional to the energies

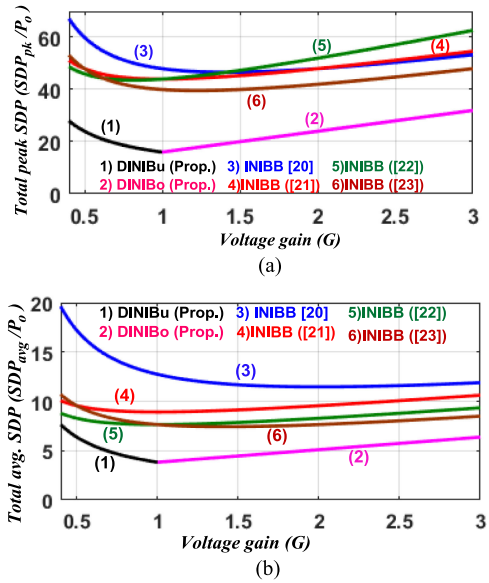

Fig. 18. Total switching device power comparisons. (a) SDP_{pk}. (b) SDP_{avg}.

they store [22], [31], which are given by

$$\begin{cases} W_L^{\text{Ind.}} = \frac{1}{2} L (I_L^{\text{max.}})^2 \\ W_C^{\text{cap.}} = \frac{1}{2} C (V_C^{\text{max.}})^2. \end{cases} \tag{24}$$

The total maximum stored energy $W_L^{\text{tot.}}$ ($=W_{Lin} + W_{Lo}$) of inductors L_{in} and L_o of the proposed buck–boost MC is given by

$$\begin{cases} W_L^{\text{tot.}} = \frac{P_o T}{x} (1-G); & DINIBu \\ W_L^{\text{tot.}} = \frac{P_o T}{x} \frac{G-1}{G}; & DINIBu \end{cases} \tag{25}$$

where x is the percentage maximum allowed inductor current ripple and T is the switching time period.

The normalized $W_L^{\text{tot.}}/k$ (where $k = P_o T/x$) for the proposed and counterpart buck–boost MCs are plotted in Fig. 19(a). As observed, the proposed buck–boost MC has smaller values of total stored energy of inductors, indicating that it requires least magnetic volume.

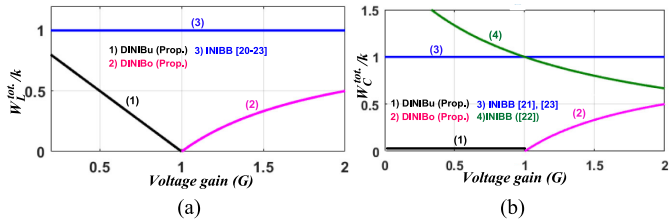

Fig. 19. Comparison of the normalized maximum stored energies of (a) inductors ($W_L^{\text{tot.}}/k$) and (b) capacitors ($W_C^{\text{tot.}}/k$).

TABLE IV
COMPARISON OF SWITCHING DEVICES POWER VALUES

Parameter	[20]	[21]	[22]	[23]	Proposed
$SDP_{pk}(KVA)$	15.187	12.927	13.371	11.523	5.866
$SDP_{avg}(KVA)$	4.183	2.580	2.610	2.134	1.228

TABLE V
COMPARISON OF STORED ENERGIES OF PASSIVE COMPONENTS

Parameter	[20]	[21]	[22]	[23]	Proposed
$W_L^{tot.}$(mH.A^2)	57.73	57.73	65.77	65.77	16.54
$W_C^{tot.}$(mF.V^2)	N/A	164.6	139.5	164.6	52.62

The maximum stored energy of capacitor *C* of the proposed buck–boost MC is given by

$$\begin{cases} W_C^{\text{tot.}} = 0; & DINIBu \\ W_C^{\text{tot.}} = \frac{P_o T}{y}\frac{G-1}{G}; & DINIBo \end{cases} \tag{26}$$

where *y* is the percentage allowed capacitor voltage ripple.

The normalized maximum stored capacitor energies $W_C^{\text{tot.}}/k$ (where $k = P_o T/x$) for the proposed and counterpart buck–boost MCs are plotted in Fig. 19(b). Clearly, the proposed buck–boost MC has smaller capacitor energy storing requirement and, thus, can utilize smaller size capacitors.

To evaluate and compare the quantified values of above discussed volume related parameters, the operating conditions given in previous Section IV are considered and practical SDP_{pk} and SDP_{avg} ratings are calculated using maximum switching device voltage stresses (which occurs when v_{in} is maximum) and maximum switch device peak and average currents (which occurs when v_{in} is minimum). The calculated values of SDP_{pk} and SDP_{avg} are compared in Table IV for the proposed and counterpart buck–boost MCs. Clearly, the proposed buck–boost MC has much smaller values of SDP_{pk}, SDP_{avg} and, thus, require least switching devices plus heatsink sizes. The maximum stored energies of inductors are calculated using the values of minimum required inductance (to limit the maximum allowable current ripple to 30% of inductor current) and maximum inductor current (occurs when v_{in} is minimum). The maximum stored energies of capacitors are also determined based on the values of minimum required capacitance (to limit the allowable ripple to 10% of capacitor voltage) and maximum capacitor voltage stresses (when v_{in} is maximum). These numerical values are listed in Table V. As observed, the proposed buck–boost MC has much smaller inductor and capacitor energy storing requirements. From the above discussion, the proposed buck–boost MC requires smaller switching devices, heatsink sizes, and passive components volumes, indicating its improved power density when compared with counterpart buck–boost MCs.

VI. POWER LOSS ANALYSIS OF THE PROPOSED BUCK–BOOST MC

The discrete noninverting and inverting buck–boost operations are identical and together they form the step-changed frequency operation. Therefore, power losses would remain the same for all proposed operations, as given in the following section.

A. Inductor Losses

The winding conduction losses $P_{Lin-\text{Wind.}}$ and $P_{Lo-\text{Wind.}}$ of inductors L_{in} and L_o for DINIBu and DINIBo operations are determined as

$$\begin{cases} P_{Lin-\text{Wind.}} = \left(\frac{P_o}{V_o}G\right)^2 r_{Lin} \\ P_{Lo-\text{Wind.}} = \left(\frac{P_o}{V_o}\right)^2 r_{Lo} \end{cases} \tag{27}$$

where r_{Lin} and r_{Lo} are winding resistances of inductors L_{in} and L_o, respectively.

The magnetic flux density swings ΔB of inductors L_{in} and L_o are determined as

$$\begin{cases} \Delta B_{Lin} \cong 0; & DINIBu \\ \Delta B_{Lin} = \frac{v_o T}{N_t A_e}\frac{G-1}{G^2}; & DINIBo \end{cases} \tag{28}$$

$$\begin{cases} \Delta B_{Lo} = \frac{v_o T}{N_t A_e}(1-G); & DINIBu \\ \Delta B_{Lin} \cong 0; & DINIBo \end{cases} \tag{29}$$

where N_t is number of turns and A_e is the cross-sectional area of the magnetic core. Using calculated ΔB values from (28) and (29), the inductor core loss P_L can be estimated as

$$P_L \cong a.\ \Delta B^b.\ f_{sw}^c \tag{30}$$

where *a*, *b,* and *c* are constants as determined from operating conditions and the data sheet of the magnetic core.

B. Capacitor Loss

The capacitor C conducts currents i_o and i_{in} during D_bT and $(1-D_b)$T intervals, respectively, for the DINIBo operation. The power loss P_{C-ESR} of capacitor C is given by

$$\begin{cases} P_{C-ESR} \cong 0; & DINIBu \\ P_{C-ESR} \cong \left(\frac{P_o}{V_o}\left(\sqrt{\frac{G-1}{G}}+\sqrt{G}\right)\right)^2 r_{C-ESR}; & DINIBo \end{cases} \tag{31}$$

where $r_{C-\text{ESR}}$ is equivalent series resistance of the capacitor.

C. Switching Devices Losses

The currents flowing through the switching devices along with their conduction time intervals are given in Table VI. Using that information, the rms currents $I_{S-\text{rms}}$ flowing through switching

TABLE VI
SWITCHING DEVICES CURRENTS AND CONDUCTING INTERVALS

Switch	$v_{in} > 0$		$v_{in} < 0$	
	Conducting current	Conducting interval	Conducting current	Conducting interval
DINIBu operation				
$\overline{S_{1n}}, \overline{S_{2n}}$	i_{in}	$D_a T$	0	$D_a T$
S_{1p}, S_{2p}		$(1-D_a)T$		$(1-D_a)T$
$S_{3p}, \overline{S_{3n}}$	i_O	$D_a T$	0	$D_a T$
		$(1-D_a)T$		$(1-D_a)T$
$S_{4n}, \overline{S_{4p}}$	0	$D_a T$	i_O	$D_a T$
	i_O	$(1-D_a)T$	0	$(1-D_a)T$
DINIBo operation				
$S_{1p}, \overline{S_{1n}}$	i_{in}	$D_b T$	0	$D_b T$
		$(1-D_b)T$		$(1-D_b)T$
$S_{2n}, \overline{S_{2p}}$	i_{in}	$D_b T$	0	$D_b T$
	0	$(1-D_b)T$	i_{in}	$(1-D_b)T$
$\overline{S_{3n}}, \overline{S_{4n}}$	i_O	$D_b T$	0	$D_b T$
S_{3p}, S_{4p}		$(1-D_b)T$		$(1-D_b)T$

devices can be determined as

$$\begin{cases} I_{S1(p,n),\ S2(p,n)-\mathrm{rms}} = \frac{P_o}{\sqrt{2}V_o} G; \\ I_{S3(p,n)-\mathrm{rms}} = \frac{P_o}{\sqrt{2}V_o}; \\ I_{S4(p,n)-\mathrm{rms}} = \frac{P_o}{\sqrt{2}V_o}\left(\sqrt{G} + \sqrt{1-G}\right); \end{cases} \quad \text{DINIBu} \quad (32)$$

$$\begin{cases} I_{S1(p,n)-\mathrm{rms}} = \frac{P_o}{\sqrt{2}V_o} G\left(\sqrt{G} + \sqrt{1-G}\right); \\ I_{S2(p,n)-\mathrm{rms}} = \frac{P_o}{\sqrt{2}V_o}; \\ I_{S3(p,n),\ \ S4(p,n)-\mathrm{rms}} = \frac{P_o}{\sqrt{2}V_o}; \end{cases} \quad \text{DINIBo.} \quad (33)$$

The conduction losses $P_{S-\mathrm{Cond.}}$ of switching devices can be determined as

$$P_{S-\mathrm{Cond.}} = {I_{S-\mathrm{rms}}}^2 r_s \quad (34)$$

where r_s is the device ON-state resistance.

Two switches conduct at high frequency in any operating mode, producing the switching losses. The major part of switching losses come from the discharge of junction capacitor C_{oss} as given by

$$\begin{cases} P_{Sw} = f_{sw}.\ E_{oss}.v_{in}; & DINIBu \\ P_{Sw} = f_{sw}.\ E_{oss}.v_o; & DINIBo. \end{cases} \quad (35)$$

The diode reverse recovery loss P_{Drr} is obtained as

$$\begin{cases} P_{Drr} = \left(\frac{1}{4}\right)\ f_{sw}.\ I_{rr}.\ v_{in}.\ t_b; & DINIBu \\ P_{Drr} = \left(\frac{1}{4}\right)\ f_{sw}.\ I_{rr}.\ v_o.\ t_b; & DINIBo \end{cases} \quad (36)$$

where I_{rr} is the reverse recovery current and t_b is the reverse recovery time.

The component power losses are computed for the operating conditions and circuit parameters given in Table VII. Inductor and capacitor losses are theoretically calculated using (27)–(31), and the losses of switching devices are calculated using the thermal module in PSIM [23]. The power loss breakdown for the DINIBu operation ($v_{in} = 150\ V_{\mathrm{rms}}$) and the DINIBo operation ($v_{in} = 70\ V_{\mathrm{rms}}$) are given in Fig. 20(a) and (b), respectively, for $v_o = 110\ V_{\mathrm{rms}}$, $P_o = 400$ W, and $f_{sw} = 25$ kHz.

TABLE VII
EXPERIMENTAL CONDITIONS AND COMPONENT SPECIFICATIONS

Operating Conditions		
Input ac voltage (v_{in})		70~150 V_{rms} (50 Hz)
Output voltage (v_o)		110 V_{rms} (25/50/100 Hz)
Output power (P_o)		400 VA
Load (RL)		29 Ω + 30 mH
Switching frequency (f_s)		25 kHz
Component Specifications		
Switches		47N60CFD
Capacitors (C_{in}, C_o)	Model	B32523Q3225
	Capacitance	(2.2 μF, 2.2 μF)
Capacitor (C_f)	Model	(B32523Q3225)×2
	Inductance	(4.4 μF)
Inductors (L_{in}, L_o)	Core	RM-14, Ferrite
	Core area	200 mm^2
	Inductance	(400 μH, 500 μH)

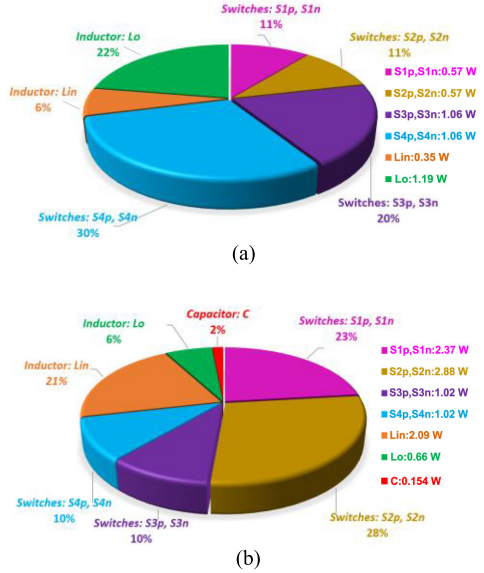

Fig. 20. Power loss breakdown of the proposed buck–boost MC for v_o =110 V_{rms}, P_o =400 W, $f_{sw} = 25$ kHz. (a) DINIBu operation: $v_{in} = 150\ V_{\mathrm{rms}}$. (b) DINIBo operation: $v_{in} = 70\ V_{\mathrm{rms}}$.

VII. CONTROL OF THE PROPOSED BUCK–BOOST MC

The proposed buck–boost MC offers discrete buck, discrete boost, and flexible buck–boost mode operations while producing noninverting, inverting, and step-changed frequency outputs. These different circuit operations find use in various applications such as direct ac–ac voltage regulators [8], DVRs [9], high-gain ac–dc rectifiers [7], traction systems [10], etc. The already developed dedicated controls for each application would also work well with the proposed buck–boost MC; for instance, the same frequency control methods adopted in [7], [10], and [20] can be utilized. This section discusses different control methods of the proposed buck–boost MC, all of which are compatible with nonunity power factor operation, and reactive loads.

A. Control for Noninverting, Inverting, and Step-Changed Frequency Output Voltages

To produce the noninverting and inverting output voltages and adjust the frequency of the output voltage, control can be

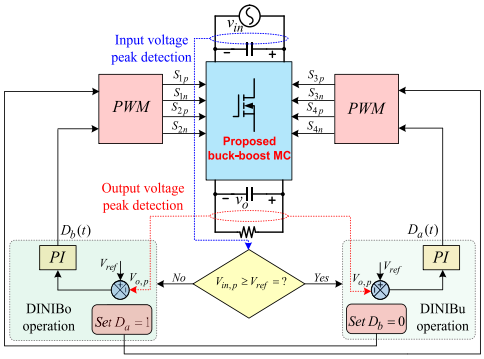

Fig. 21. Control block diagram of the combined DINIBu and DINIBo operation.

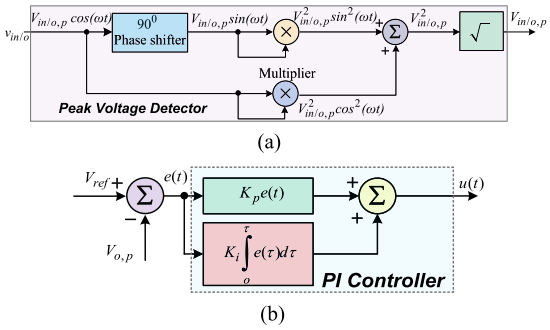

Fig. 22. Block diagrams of (a) peak voltage detector and (b) PI controller.

implemented by varying the switching signal patterns. For this purpose, a square wave control signal $S_{\mathrm{sq-ctrl}}$ can be generated. When $S_{\mathrm{sq-ctrl}}$ =1, switches $S_{3p}$and S_{4p} are turned-ON to produce a positive output voltage (v_o> 0), and vice-versa. By synchronizing $S_{\mathrm{sq-ctrl}} = 1$ with $v_{in} > 0$ and $S_{\mathrm{sq-ctrl}} = 0$ with $v_{in} < 0$, a noninverting output voltage is produced, and vice-versa. The step-changed frequency control of output voltage v_o is also achieved by varying the frequency of the $S_{\mathrm{sq-ctrl}}$ signal and synchronizing it with v_{in} with or without a phase shift. The frequency of $S_{\mathrm{sq-ctrl}}$ and its phase can be decided by predetermining the time intervals (as already provided in [20]) to switch between noninverting and inverting operations, controlling the frequency of the output voltage.

B. Feedback Control for Adjustable Voltage Magnitude

To control the magnitude of the output voltage for noninverting, inverting, and step-changed frequency operations, a proposed discrete buck combined with discrete boost (DINIBu combined DINIBo) or flexible buck–boost (fINIBB) voltage based feedback control is utilized. The control block diagram of the proposed DINIBu combined DINIBo operation is shown in Fig. 21. This control is similar to that of cascaded buck–boost MC (see Fig. 2). The peak values ($V_{in,p}$ and $V_{o,p}$) of input and output voltages (v_{in} and v_o) are obtained using peak voltage detector [32] as shown in Fig. 22(a), through the following

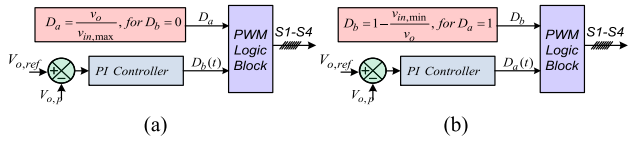

Fig. 23. Control block diagram for the fINIBB operation. (a) When D_a is fixed and D_b is dynamically adjusted. (b) D_b is fixed and D_a is dynamically adjusted.

relation:

$$\sqrt{V_{in/o,p}^2 Sin^2(\omega t) + V_{in/o,p}^2 Cos^2(\omega t)} = V_{in/o,p}. \quad (37)$$

$V_{in,p}$ is compared with a reference output voltage $V_{o,\mathrm{ref}}$. If $V_{in} > V_{\mathrm{ref}}$, discrete buck (DINIBu) mode is activated in which $D_b(t)$ is set to 0, while the PI controller [as shown in Fig. 22(b)] generates the buck control duty signal $D_a(t)$. If $V_{in} < V_{o,\mathrm{ref}}$, discrete boost (DINIBo) mode is activated, $D_a(t)$ is set to 1, while $D_b(t)$ is dynamically adjusted through the PI controller.

In the abovementioned control method for combined discrete buck (DINIBu) and discrete boost (DINIBo) operation, D_a is the main control duty for the buck operation and D_b is the main control duty for the boost operation. However, the proposed fINIBB operation provides various options of varying only D_a or only D_b to provide both buck and boost voltage control, similar to the control of existing buck–boost MCs [19]–[23], but with less device voltage/current stresses (see Table II). Fig. 23 shows the control block diagrams for two such cases. Fig. 23(a) shows the control block diagram when D_a is set to a fix value ($D_a = v_o/v_{in,\max}$) corresponding to regulation of v_o for maximum value of $v_{in,\max}$, by setting $D_b = 0$. Whereas the value of D_b is dynamically adjusted using the PI controller to regulate the output voltage v_o as v_{in} varies between $v_{in,\max}$ and $v_{in,\min}$. Fig. 23(b) shows the control block diagram when D_b is set to a fix value ($D_b = 1 - v_{in,\min}/v_o$) corresponding to regulation of v_o for $v_{in,\min}$, by setting $D_a = 1$. The value of D_a can now be dynamically adjusted using the PI controller to regulate v_o as v_{in} varies between $v_{in,\min}$ and $v_{in,\max}$.

VIII. Experimental Results

A 400-VA laboratory scale hardware prototype of the proposed buck–boost MC was constructed and tested. The experimental conditions and specifications of the power stage components are given in Table VII. As the load is rarely purely resistive in practice, a partial inductive (RL) load (29 Ω + 30 mH) is used for the experiments.

The measured waveforms of input voltage v_{in}, output voltage v_o, capacitor C_f voltage, and output current i_o for DNIBu operation are shown in Fig. 24(a), when $v_{in} = 150\ V_{\mathrm{rms}}$ and $D_a = 0.73$. The practical waveforms of v_{in}, v_o, and i_o along with input current i_{in} for DIBu operation are shown in Fig. 24(b). As can be noted, the input current i_{in} is continuous and sinusoidal due to the presence of the input *LC* filter (L_{in} and C_f). The voltage stresses of switches $S_{1p,1n}$ and $S_{4p,4n}$ are given in Fig. 25 for the DINIBu operation. The peak switch voltage stress is around 212 V (the peak value of v_{in}) with no voltage

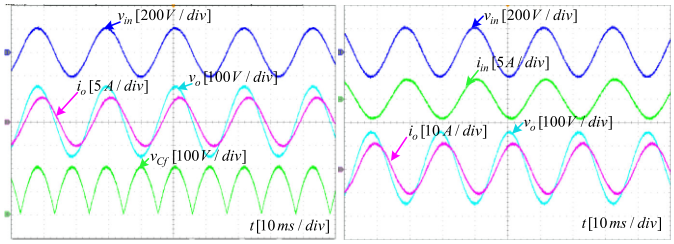

Fig. 24. Experimental results for DINIBu operation when $v_{in} = 150\ V_{\rm rms}$. (a) DNIBu operation. (b) DIBu operation.

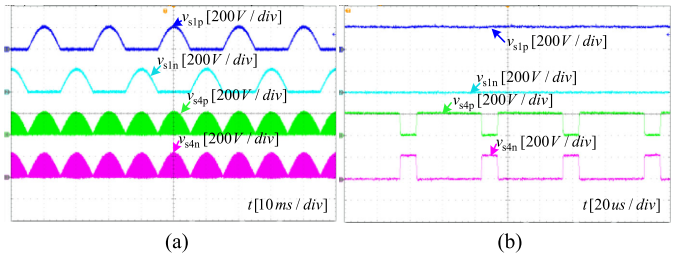

Fig. 25. Experimental results for DINIBu operation when $v_{in} = 150\ V_{\rm rms}$. (a) Switch voltage stresses. (b) Enlarged waveforms of (a).

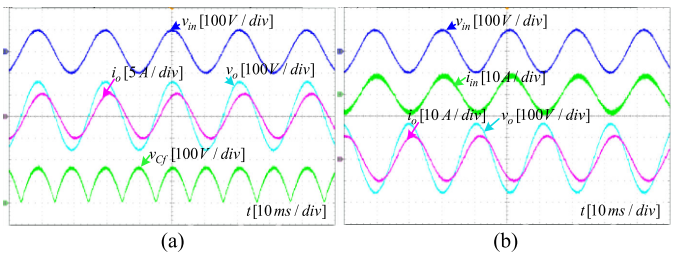

Fig. 26. Experimental results for DINIBo operation when $v_{in} = 70\ V_{\rm rms}$. (a) DNIBo operation. (b) DIBo operation.

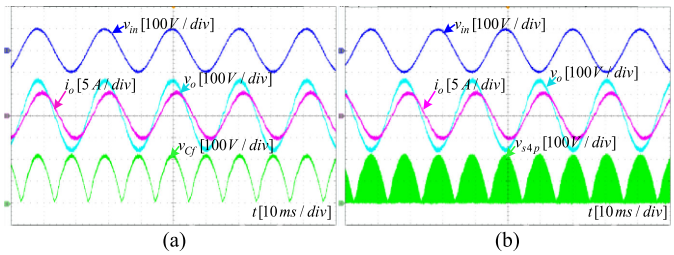

Fig. 27. Experimental results for fINIBo operation when $v_{in} = 70\ V_{\rm rms}$. (a) fNIBo operation. (b) fIBo operation.

overshoot due to the voltage clamping action of C_f. Figs. 26(a) and (b) show the practical waveforms (of v_{in}, v_o, v_{Cf} and i_o) for DNIBo and (of v_{in}, v_o, i_{in} and i_o) for DIBo operations, respectively, when $v_{in} = 70\ V_{\rm rms}$ and $D_b = 0.364$. The practical waveforms of v_{in}, v_o, v_{Cf}, and i_o for the fNIBo operation are shown in Fig. 27(a), when $v_{in} = 70\ V_{\rm rms}$, $D_a = 0.73$, and $D_b = 0.533$. Whereas, the practical waveforms of v_{in}, v_o, i_o and the voltage stress of switch S_{4p} for the fIBo operation

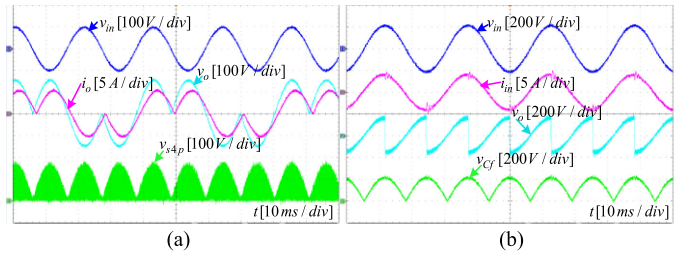

Fig. 28. Experimental results for step-changed frequency operation. (a) Step-down frequency (25 Hz) and boost voltage operation. (b) Step-up frequency (100 Hz) and buck voltage operation.

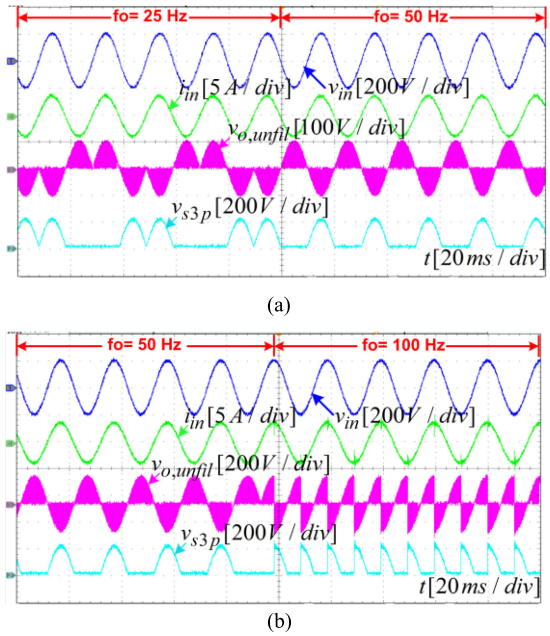

Fig. 29. Experimental results for step-changed frequency control of output voltage. (a) Transition from 25 to 50 Hz. (b) Transition from 50 to 100 Hz.

are shown in Fig. 27(b). The practical waveforms for fINIBu operations are the same as those given in Fig. 24 for DINIBu operations, when $v_{in} = 150\ V_{\rm rms}$, $D_a = 0.73$, and $D_b = 0$. Fig. 28(a) shows the practical waveforms of v_{in}, v_o, v_{Cf}, and i_o for step-down output frequency (25 Hz) and voltage boost operation ($v_{in} = 70\ V_{\rm rms}$). The practical waveforms of v_{in}, i_{in}, v_o, and v_{Cf} for step-up output frequency (100 Hz) and buck voltage operation ($v_{in} = 150\ V_{\rm rms}$) are shown in Fig. 28(b).

Fig. 29 shows the measured waveforms of v_{in}, i_{in}, unfiltered output voltage $v_{o,unfil}$, and the voltage across switch S_{3p} with step-changed frequency control. Fig. 29(a) shows the output voltage frequency change from 25 to 50 Hz, and Fig. 29(b) shows the transition from 50 to 100 Hz. Fig. 30 shows the experimental waveforms of v_{in}, v_o, i_o, and the voltage stress of switch S_{3p} with close-loop voltage control for combined discrete buck (DNIBu) and discrete boost (DNIBo) operation. Fig. 30(a) shows the transition from discrete buck to discrete boost operation when the input voltage has a step-down change from 150 to 70 $V_{\rm rms}$. The output voltage is regulated to 110 $V_{\rm rms}$. The same

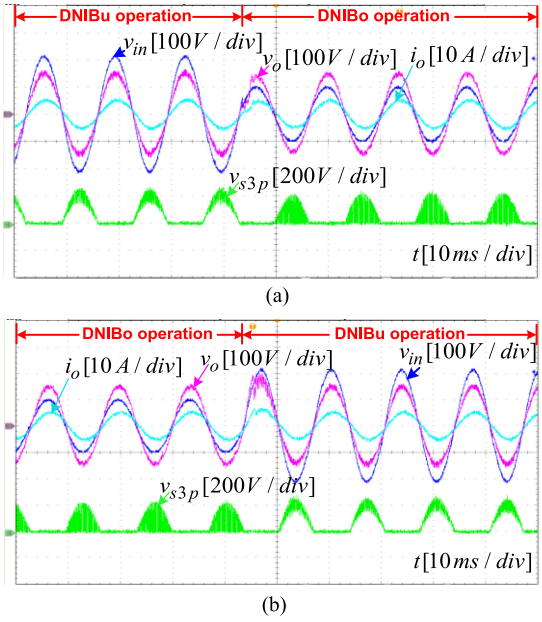

Fig. 30. Experimental results with close loop voltage control for discrete buck (DINIBu) combined discrete boost (DINIBo) operation. (a) Transition from DNIBu to DNIbo operation. (b) Transition from DNIBo to DNIBu operation.

TABLE VIII
POWER FACTOR AND THD VALUES OF THE PROPOSED BUCK–BOOST MC

Output frequency	25 Hz		50 Hz		100 Hz	
Operation mode	Boost	Buck	Boost	Buck	Boost	Buck
Input power factor, PF_{in}	0.984	0.989	0.982	0.988	0.97	0.976
THD of input current (THD_{Iin})	2.6 %	1.6 %	2.8 %	1.73 %	3.9 %	3.5 %
THD of output voltage (THD_{Vo})	57. 1 %	58. 3%	1.5%	2.2%	57. 8%	58. 9%

waveforms for discrete boost to discrete buck mode transition are shown in Fig. 30(b). The input voltage is stepped-up from 70 to 150 $V_{\rm rms}$, the output voltage is again regulated to 110 $V_{\rm rms}$.

The measured input power factor PF_{in} along with THD values of input current THD_{Iin} and output voltage THD_{vo} are given in Table VIII for noninverting, inverting, and step-changed frequency outputs with buck and boost operations. A high-input power factor PF_{in} and very low input current THD (THD_{Iin}) are obtained due to the high-quality sinusoidal input currents in each operating mode, as shown in the experimental waveforms. THD_{Iin} is even lower in buck mode with a further improved power factor due to the *CLC* input filter formed by capacitor C_{in}, inductor L_{in}, and capacitor C_f. The output voltage THD is also very small when output voltage frequency is the same as input voltage frequency ($f_{in} = f_o = 50$ Hz), and the value is even smaller in boost mode due to formation of a *CLC* filter at output by capacitor C_f, output inductor L_o, and output capacitor C_o. THD_{vo} is higher for step-down (25 Hz) and step-up (100 Hz) output frequencies as the output voltages are not purely sinusoidal anymore, the same as the case with existing single-phase MCs [19]–[23]. However, these THD_{vo} values with step-up/step-down frequencies are given for information purposes

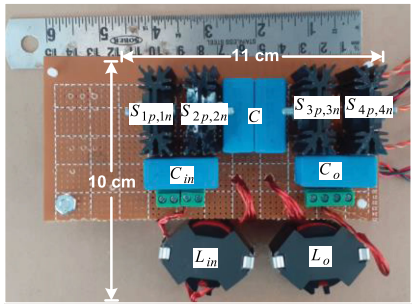

Fig. 31. Photograph of the prototype converter.

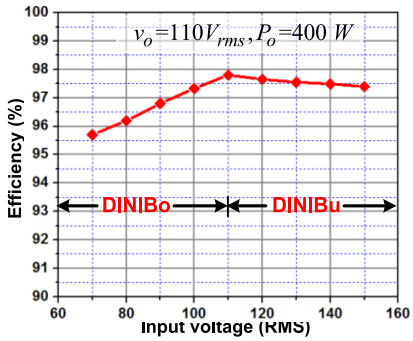

Fig. 32. Experimental efficiency of the proposed buck–boost MC for $v_{in} = 70\sim150$ $V_{\rm rms}$.

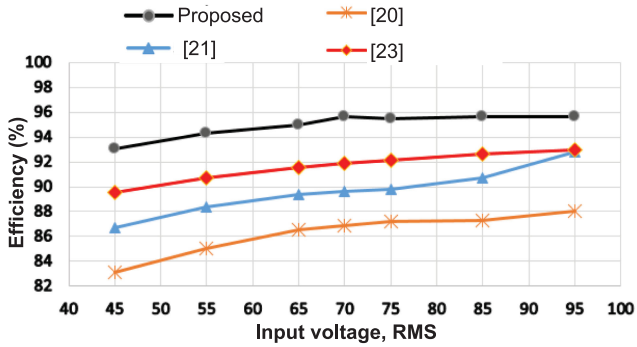

Fig. 33. Power conversion efficiency comparison for $v_{in} = 45\sim95$ $V_{\rm rms}$.

only as in step-changed frequency applications (high-gain ac–dc rectifiers [7], traction systems [10], etc.), the output voltage is eventually rectified into a dc waveform and the THD values become irrelevant. Overall, the obtained power factors are close to unity with THD values limited below 5%.

A photograph of the prototype converter is shown in Fig. 31. Fig. 32 shows the measured efficiency of the proposed buck–boost MC plotted for $v_o = 110$ $V_{\rm rms}$, $P_o = 400$ W, and a wide range of input voltages $v_{in} = 70\sim150$ $V_{\rm rms}$. Fig. 33 compares the plotted measured efficiencies of the proposed buck–boost and counterpart buck–boost MCs [20], [21], [23] for the same operating conditions of $v_o = 70$ $V_{\rm rms}$, $P_o = 200$ W, and a wide range of input voltages $v_{in} = 45\sim95$ $V_{\rm rms}$. The comparative numerical values of measured efficiency for the proposed and

TABLE IX
COMPARISON OF POWER CONVERSION EFFICIENCY WITH EXISTING MCs

Circuit topology	Operating mode (Inverting)	Operating Conditions				Max. Eff. (%)
		v_{IN} (V_{rms})	v_o (V_{rms})	G= v_o/v_{in}	P_o (W)	
[20]	Buck	95	70	0.74	200	88.1
	Boost	45	70	1.55	200	83
[21]	Buck	95	70	0.74	200	92.8
	Boost	45	70	1.55	200	88
[22]	Buck	95	70	0.74	200	93
	Boost	45	70	1.55	200	89.8
[23]	Buck	95	70	0.74	200	93.1
	Boost	45	70	1.55	200	89.6
Proposed	Buck	95	70	0.74	200	95.7
	Boost	45	70	1.55	200	93.6

counterpart buck–boost MCs [20]–[23] are also given in Table IX for buck operation ($v_{in} = 95\ V_{\text{rms}}$) and boost operation ($v_{in} = 45\ V_{\text{rms}}$) when $v_o = 70\ V_{\text{rms}}$ and $P_o = 200$ W. Clearly, the proposed buck–boost MC has significantly higher power conversion efficiency due to its lower switching devices and passive components losses, demonstrating the practical merits of the proposed buck–boost MC.

IX. CONCLUSION

A highly efficient, single-phase, buck–boost MC is proposed. It has a simple construction as achieved by connecting a small film capacitor and input/output *LC* filters to two full-bridge IGBT modules, which also reduces its size. Using only eight switches, the proposed converter combines the operations of basic buck and boost-type MCs (16 switches in total), also called the DINIBu and DINIBo operations, respectively. These operations have lower component voltage/current stresses, ripples, and losses than that of the existing buck–boost MCs. In addition, flexible inverting and noninverting buck–boost operations are proposed offering maximum control flexibility by independently modulating buck and boost duty ratios. The proposed operations have smooth input and output currents, uniform component stresses, no commutation issues; and are completely suitable for nonunity power factor loads.

Circuit operations are explained in details for all the proposed modes of operation. Guidelines for the design and selection of components are given together with comprehensive comparisons with existing buck–boost MCs. Experimental verification is provided for bipolar buck–boost and step-changed frequency operations, proving the usefulness of the proposed buck–boost MC.

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