The Modular Multilevel DC Converter With Inherent Minimization of Arm Current Stresses

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***Abstract*—The modular multilevel dc converter (M2dc) is a partial power processing dc–dc converter that is gaining popularity for medium-voltage and high-voltage dc (HVdc) grid applications. However, internal ac current stresses go up as the step-down dc voltage ratio increases, leading to increased cost and losses, and ultimately renders the M2dc impractical for some applications. The HVdc autotransformer (AT) (HVdc-AT) is another class of the partial power processing dc–dc converter that circumvents this issue by using a transformer for interarm ac voltage matching, although the core must tolerate a very large dc voltage stress between windings that leads to increased magnetics size and weight. Interestingly, the M2dc does not suffer from interwinding dc voltage stresses. This article presents a new class of the partial power processing dc–dc converter that uses an integrated center-tapped transformer to merge the best traits of the M2dc and HVdc-AT. Comparative analysis reveals the proposed converter can minimize ac current stresses at all operating points while also achieving a significant reduction in transformer area product relative to the HVdc-AT. A dynamic controller is proposed that regulates dc power transfer while ensuring balanced capacitor voltages. The converter operation and dynamic controls are validated by simulation and experiment.**

***Index Terms*—DC-DC power conversion, HVdc converters, HVdc transmission.**

NOMENCLATURE

CCL	Circulating current loop.
F2F-MMC	Front-to-front modular multilevel converter.
HVdc	High-voltage dc.
HVdc-AT	High-voltage dc autotransformer.
MMC	Modular multilevel converter.
MVdc	Medium-voltage dc.
M2dc	Modular multilevel dc converter.
M2dc-CT	Modular multilevel dc converter with integrated center-tapped transformer.
P3T	Partial power processing transformer.
SM	Submodule.

I. INTRODUCTION

DC POWER transmission and distribution technology has been garnering increased attention over the last several years [1]. At present, an increasing number of voltage-sourced converter based high-voltage dc (HVdc) transmission systems are being planned and built around the world. Advancements in voltage-sourced converter technology, the rapid adoption of offshore wind power generation, and the low-loss delivery of power from scattered renewable energy resources to high-density urban load centers are some of the main drivers. Looking forward, an evolution from traditional two-terminal HVdc links to more complex multiterminal HVdc grids is anticipated. Indeed, the Zhangbei-1 project will be the first global installation of a multiterminal HVdc grid when completed [2]. The development of medium-voltage dc (MVdc) systems is also gaining momentum, e.g., collector networks for offshore wind power generation [3]. The recently commissioned dc Angle project is one of the first point-to-point MVdc links in Europe for reinforcement of ac distribution systems [4].

DC–DC converters are one of the important building blocks of future dc grids [5]–[7]. They enable interconnection of different dc systems for power flow control, and can be augmented with advanced features such as dc fault blocking. Utilizing classical switched-mode dc–dc converters for HVdc applications is not practical due to the high current and voltage stresses for the semiconductors. The lack of modularity and scalability is another drawback. Much research attention has been focused on the development of dc–dc modular multilevel converters (MMCs) that series-cascade many low-voltage submodules (SMs) to build up to the high operating voltages required. These dc–dc MMCs are inspired by the well-known dc–ac MMC [8] that has gained widespread acceptance for HVdc, MVdc, and flexible ac transmission system applications. The dc–ac MMC enjoys high modularity and scalability, low filtering requirements, and high efficiencies due to low equivalent switching frequency of the semiconductors. The first dc–dc MMCs to arise for HVdc application were based on the dual-active-bridge topology [9]. The generalization of this concept using three-phase MMCs is presented in Fig. 1(a). Primary (p) and secondary (s) MMCs are coupled on their ac sides via a transformer in a manner first proposed in [10]. The p and s arms can be comprised of half-bridge SMs or full-bridge SMs; the latter can be used to accommodate dc link polarity reversals. This topology is sometimes referred to as a front-to-front MMC (F2F-MMC). The F2F-MMC with half-bridge SMs provides galvanic separation between dc terminals and can block dc faults on either terminal due to the use of two separate MMCs. Many works on modeling, control, and topology development of F2F-MMCs have been published, e.g., [11]–[15].

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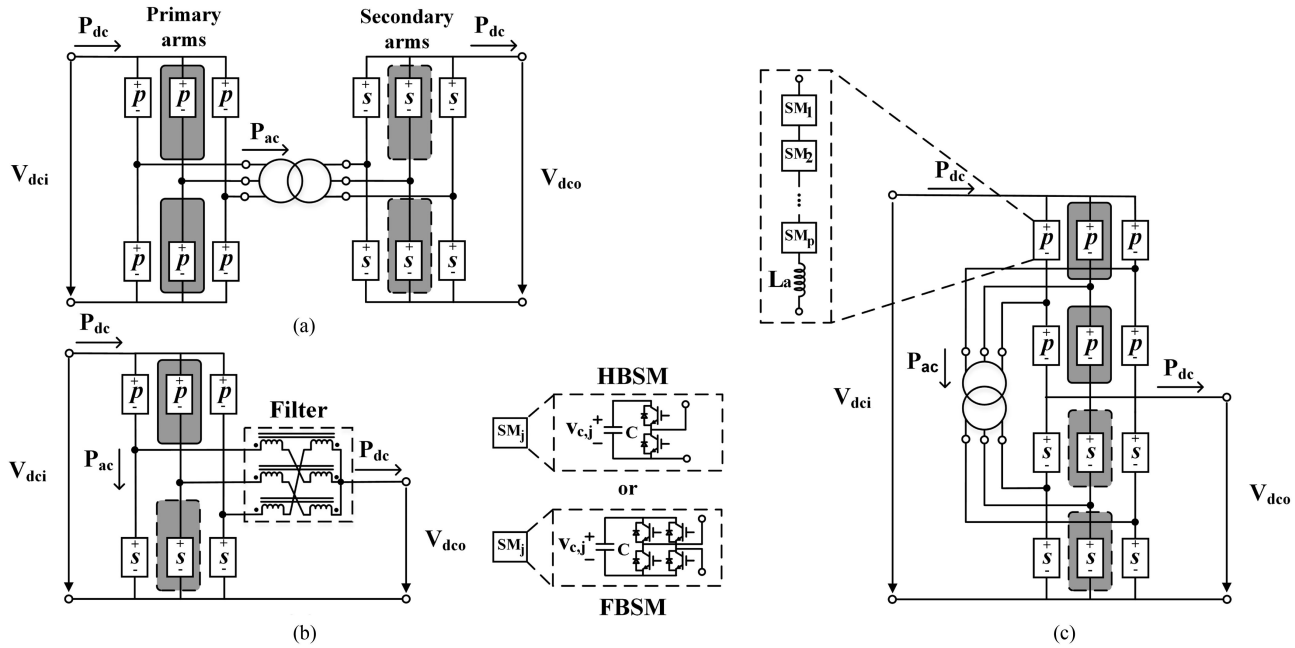

Fig. 1. Exemplar dc–dc converters based on MMC. (a) F2F-MMC. (b) M2dc [16]–[18]. (c) HVdc-AT [19].

Research into dc–dc MMCs other than the F2F-MMC is also taking place. An overview of topologies can be found in [5]–[7]. The modular multilevel dc converter (M2dc) and HVdc-AT are representative examples of the broader classes of circulating current loop (CCL) and partial power processing transformer (P3T) type dc–dc MMCs, respectively [20]. CCL and P3T refer to the different dc–dc power transfer mechanisms being employed. The M2dc [16]–[18], as shown in Fig. 1(b), offers significant potential savings in semiconductor, capacitive energy storage, and magnetics requirements relative to the two-stage F2F-MMC. The savings depend on the dc step ratio, e.g., 2:1 ratio provides a 50% reduction in total number of SMs for the same dc power transfer [21], and come at the expense of relinquishing galvanic separation between dc terminals. DC fault blocking can be achieved by using the requisite number of full-bridge SMs in the p arms [22]. The M2dc is attracting much interest from academia and industry for HVdc systems, e.g., [23], [24]. However, one fundamental limitation of the topology is that it experiences high ac current stresses in the arms when $V_{\rm dco} \ll V_{\rm dci}$ [22], [25], [26]. The ac current stresses go up as the dc input voltage is further stepped down, eventually rendering the topology impractical for certain applications, e.g., HVdc to MVdc interconnects or HVdc power tapping. Some works have focused on control methods to reduce the ac currents needed for a given $P_{\rm dc}$ [27], [28], however, the resulting ac currents will still be inherently large when $V_{\rm dci}$ and $V_{\rm dco}$ are significantly different.

The M2dc facilitates dc–dc conversion by shuttling $P_{\rm ac} = (1 - V_{\rm dco}/V_{\rm dci})P_{\rm dc}$ between p and s arms using internal ac currents. This is a hallmark of the CCL power transfer mechanism [20]. An alternative approach is to instead shuttle this $P_{\rm ac}$ between p and s MMCs that are series-stacked, which leads to the HVdc-autotransformer (AT) (HVdc-AT) structure in Fig. 1(c) [19]. The HVdc-AT relies on the P3T power transfer mechanism [20], and therefore, it uses a partial power processing ac transformer (instead of the filter magnetics in the M2dc) to enable $P_{\rm ac}$ transfer. The transformer also provides a key advantage: it enables independent maximization of ac arm voltages, which circumvents the high ac current stress issue that plagues the M2dc. The caveat, however, is that the transformer core must tolerate large dc voltage stress between primary and second windings [5]. This leads to increased size, weight, and core design complexity for the transformer.

In this article, a new class of the modular multilevel dc–dc converter is proposed that merges the best traits of the HVdc-AT and M2dc, i.e., it offers both the ability to minimize ac currents and semiconductor effort across wide range of dc step ratios, and the avoidance of interwinding dc voltage stresses for the magnetics.

The abovementioned features cannot be simultaneously obtained with the HVdc-AT nor the M2dc. The proposed topology is able to do this by using a novel dc–dc power transfer mechanism that is a hybrid of CCL and P3T types. It is suitable for dc–dc applications requiring high or low dc step ratios, for example,

1) HVdc-to-MVdc grids interconnects;
2) connecting offshore wind MVdc collector networks to offshore HVdc stations;
3) HVdc power tapping with MVdc bus output;
4) interconnecting HVdc systems of similar voltages;
5) dc line power flow controllers where only incremental series dc voltage injection is needed.

II. Derivation of Proposed Topology

A. Motivation

The M2dc and HVdc-AT in Fig. 1 are partial power processing topologies. The amount of ac power processing is $P_{\rm ac} = (1 - G_v)P_{\rm dc}$, where $P_{\rm ac}$ is the average ac power exchanged between p and s arms, $G_v = V_{\rm dco}/V_{\rm dci}$ is the dc step ratio and $P_{\rm dc}$ is the dc power transfer. $P_{\rm ac}$ is needed to satisfy charge balance of the

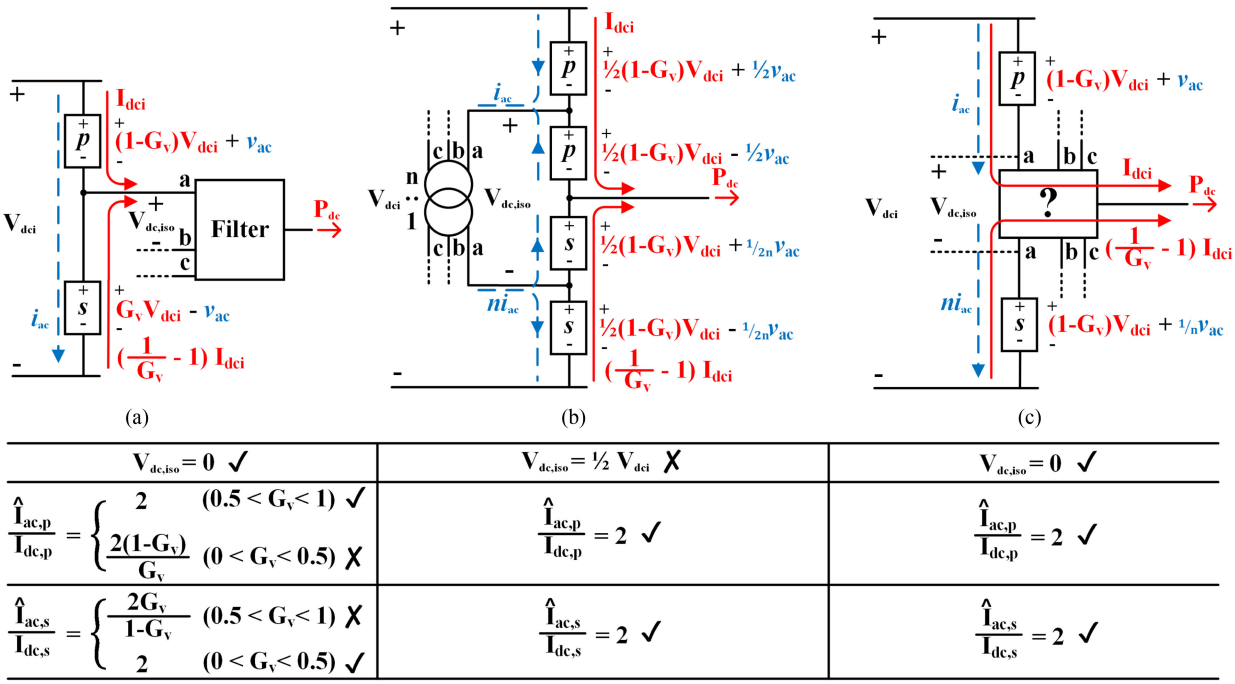

Fig. 2. DC and fundamental frequency quantities for (a) M2dc, (b) HVdc-AT, and (c) conceptualized topology with ideal features.

SM capacitors, and is facilitated by ac currents that flow within the converters [29].

Fig. 2(a) and (b) shows the dc and fundamental frequency components of the arm currents and voltages for a single-phase leg of the M2dc [cf. Fig. 1(b)] and HVdc-AT [cf. Fig. 1(c)], respectively. Higher order harmonics are neglected to focus on the ideal dc–dc conversion process. Each phase leg accommodates $P_{\rm dc} = V_{\rm dci} I_{\rm dci}$. $V_{\rm dc,iso}$ represents the dc isolation required between windings of the M2dc filter (zig-zag transformer) and windings of the HVdc-AT transformer. The HVdc-AT must tolerate interwinding voltage stress $V_{\rm dc,iso} = 0.5 V_{\rm dci}$ at all values of G_v, while the M2dc has no such burden. This onerous requirement will be shown later to significantly increase the size and weight of the HVdc-AT transformer.

Fig. 2(a) and (b) also lend insight into arm current stresses for the M2dc and HVdc-AT. For both topologies, the p arms support dc current $I_{\rm dci}$ while the s arms support $(G_v^{-1} - 1) I_{\rm dci}$. The dc currents are an unavoidable consequence of the $P_{\rm dc}$ demand. $v_{\rm ac}$ and $i_{\rm ac}$ are necessary to transfer average ac power between p and s arms in both the M2dc and HVdc-AT for capacitor charge balancing, i.e., satisfying $P_{\rm ac}$ criteria. However, the arms ac modulation differs between topologies. The HVdc-AT can impose different ac voltages between p and s arms by appropriate selection of transformer turns ratio n. This design parameter can be exploited to minimize ac current stresses of both p and s arms for any value of G_v. As will be shown as follows, the M2dc has no such inherent capability and, therefore, suffers from higher ac current stresses.

Each primary arm (the same as secondary arm) in Fig. 2 must satisfy steady-state power balance criteria

$$V_{{\rm dc},p} I_{{\rm dc},p} + \frac{1}{2} \hat{V}_{{\rm ac},p} \hat{I}_{{\rm ac},p} \cos(\theta_v - \theta_i) = 0 \qquad (1)$$

where $v_p(t) = V_{{\rm dc},p} + \hat{V}_{{\rm ac},p} \cos(\omega t + \theta_v)$ and $i_p(t) = I_{{\rm dc},p} + \hat{I}_{{\rm ac},p} \cos(\omega t + \theta_i)$. For ease of analysis, it is assumed that i) arm chokes and transformer leakage inductance are small, i.e., converter vars consumption is negligible, and therefore, $\cos(\theta_v - \theta_i) \approx -1$, and ii) losses are negligible. Recalling the dc components of p and s arm voltages are $(1 - G_v) V_{\rm dci}$ and $G_v V_{\rm dci}$, respectively, the arms ac current stresses for both the M2dc and HVdc-AT are then

$$\frac{\hat{I}_{{\rm ac},p}}{I_{{\rm dc},p}} \approx 2(1 - G_v) \frac{V_{\rm dci}}{\hat{V}_{{\rm ac},p}} \qquad \frac{\hat{I}_{{\rm ac},s}}{I_{{\rm dc},s}} \approx 2(G_v) \frac{V_{\rm dci}}{\hat{V}_{{\rm ac},s}} \qquad (2)$$

which have been normalized to the dc current of each arm. The per-unit (p.u.) ac current stresses depend on the dc step ratio G_v and also the peak ac voltage magnitude for the arm.

Equation (2) motivates the maximization of ac arm voltages to minimize the ac currents. Assuming use of half-bridge SMs, the simultaneous minimization of ac currents for p and s arms requires $\hat{V}_{{\rm ac},p} = (1 - G_v) V_{\rm dci}$ and $\hat{V}_{{\rm ac},s} = G_v V_{\rm dci}$, yielding 2 p.u. ac current in each arm. However, due to the absence of an internal ac transformer, the M2dc cannot achieve this optimal outcome as both arms must have the same ac voltage magnitude. The largest possible ac voltage for the M2dc arms is limited to the minimum dc voltage of either arm, i.e., $\hat{V}_{{\rm ac},p} = \hat{V}_{{\rm ac},s} = \min\{(1 - G_v) V_{\rm dci}, G_v V_{\rm dci}\}$ [22]. Combining this constraint with (2), the resulting normalized ac currents for p and s arms of the M2dc are given in Fig. 2(a). The optimal minimum 2 p.u. current can only be achieved at $G_v = 0.5$. For $G_v < 0.5$, the p arms exhibit > 2 p.u. ac current stress, while for $G_v > 0.5$, the s arms exhibit > 2 p.u. ac current stress.

Unlike the M2dc, the HVdc-AT in Fig. 2(b) uses an ac transformer to link p and s arms and can independently achieve maximal values $\hat{V}_{{\rm ac},p} = (1 - G_v) V_{\rm dci}$ and $\hat{V}_{{\rm ac},s} = G_v V_{\rm dci}$ in (2) by

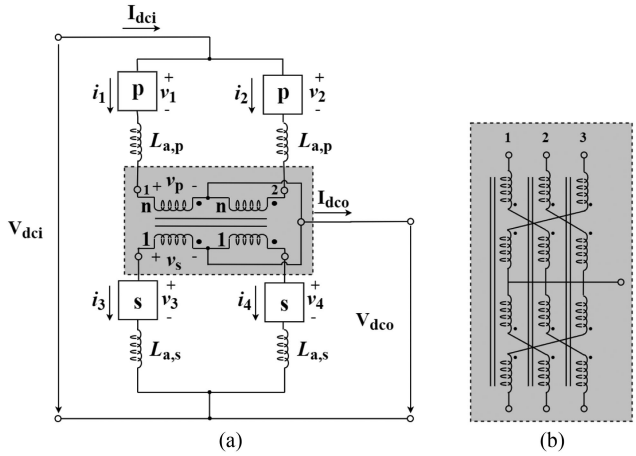

Fig. 3. (a) Proposed two-string M2dc with center-tapped transformer (M2dc-CT). (b) Magnetic structure suitable for three-string M2dc-CT.

setting $n = (1 - G_v)/G_v$. Therefore, the HVdc-AT can achieve the minimum 2 p.u. ac current stress in all arms, across all values of G_v, as indicated in Fig. 2(b).

The preceding analysis offers insight into the fundamental operating characteristics of the M2dc and HVdc-AT. These features are direct consequences of their CCL and P3T power transformer mechanisms. In can be summarized as follows:

1) The HVdc-AT must tolerate large dc voltage stress ($V_{\text{dc,iso}} = 0.5V_{\text{dci}}$) between transformer windings, regardless of dc step ratio, which inevitably leads to increased size and weight of its transformer. However, the HVdc-AT can achieve the ideal minimum 2 p.u. ac current stresses for all arms regardless of G_v value.
2) The M2dc has no dc voltage insulation stress for the filter windings regardless of G_v value. However, it is plagued by increased ac current stresses for $G_v \neq 0.5$, which inevitably leads to increased semiconductor cost and higher conduction losses.

The main contribution of this article is a new dc–dc MMC that merges the best traits of both topologies, i.e., lower ac current stresses for HVdc-AT and lower magnetics size and weight for M2dc. This ideal topology is conceptualized in Fig. 2(c).

B. Proposed DC–DC Converter

Fig. 3(a) proposes a new class of dc–dc MMC that satisfies the desired features of Fig. 2(c) by exploiting a center-tapped multiwinding transformer. Interarm ac voltage matching similar to the HVdc-AT is achieved by placing the transformer windings in series with the p and s arms. The lack of interwinding dc voltage stress similar to the M2dc is achieved by locating the transformer at the converter midpoint, i.e., the transformer is flanked by p and s arms. The windings center-taps are linked together to allow power transfer to the dc output. The dc–dc power transfer mechanism requires the windings to carry both dc and ac currents, however, similar to the M2dc filter, the windings orientation provides core dc flux cancellation. The use of transformers in MMCs that handle dc and ac currents is an area of research interest [15], [30]–[33].

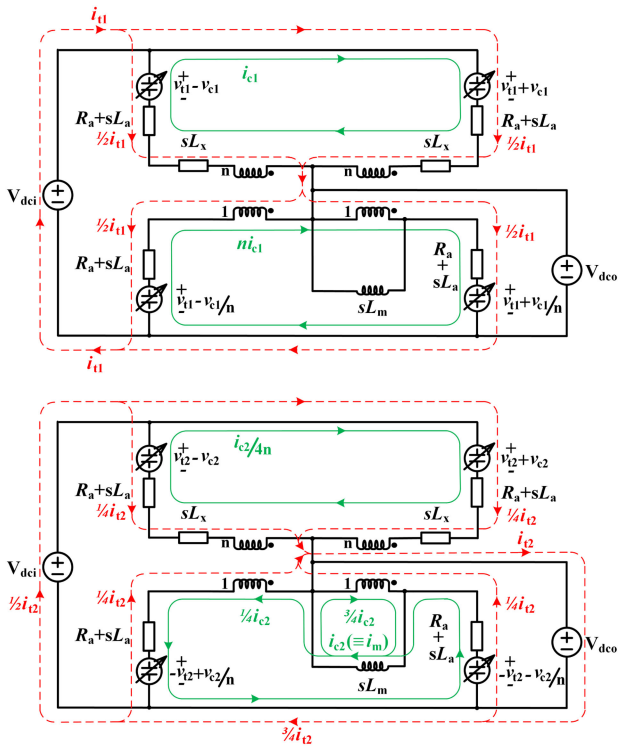

Fig. 4. Time-averaged circuit model for M2dc-CT in Fig. 3(a).

The dc–dc MMC in Fig. 3(a) consists of two interleaved phase legs and utilizes a single-phase ac transformer. The proposed two-string dc–dc MMC can be readily extended to a three-phase implementation by using a suitable magnetic structure that also achieves dc core flux cancellation, for example, as shown in Fig. 3(b), based on zig-zag transformer. Two-string and three-string variants have identical operating principles, and thus, this work focuses on the former. Hereinafter, the topology in Fig. 3(a) is referred to as the M2dc-CT as it utilizes the M2dc structure with an integrated center-tapped transformer.

III. Converter Analysis

A. Principle of Operation and Mathematical Modeling

Similar to the M2dc and HVdc-AT, the M2dc-CT is a partial power processing dc–dc MMC where $(1 - G_v)\%$ of P_{dc} is shuttled between p and s arms as average ac power. The M2dc-CT uses a new power transfer mechanism that is a hybrid of CCL and P3T mechanisms employed by the M2dc and HVdc-AT, respectively. The subsequent modeling and analysis assumes the following:

1) converter voltages and currents comprise dc and fundamental frequency components;
2) energy conversion is lossless; and
3) half-bridge SMs are employed and thus $G_v = V_{\text{dco}}/V_{\text{dci}} \in [0, 1]$.

The dc power throughput is $P_{\text{dc}} = V_{\text{dci}} I_{\text{dci}}$.

Fig. 4 presents a time-averaged circuit model of the M2dc-CT. L_m and L_x are the magnetizing and leakage inductances for the transformer, and L_a and R_a are the arm inductance and

resistance. Arm currents and voltages in Fig. 3(a) are denoted by $[i_1\ i_2\ i_3\ i_4]$ and $[v_1\ v_2\ v_3\ v_4]$, respectively. These physical quantities can be mapped into new abstract variables as illustrated by Fig. 4, by summing and subtracting quantities according to

$$[i_{t1}\ i_{t2}\ i_{c1}\ i_{c2}]^T = \mathbf{T_i}[i_1\ i_2\ i_3\ i_4]^T \tag{3}$$

$$[v_{t1}\ v_{t2}\ v_{c1}\ v_{c2}]^T = \mathbf{T_v}[v_1\ v_2\ v_3\ v_4]^T \tag{4}$$

where

$$\mathbf{T_i} = \frac{1}{4}\begin{bmatrix} 2 & 2 & 2 & 2 \\ 4 & 4 & -4 & -4 \\ -1 & 1 & -\frac{1}{n} & \frac{1}{n} \\ -4n & 4n & 4 & -4 \end{bmatrix}$$

$$\mathbf{T_v} = \frac{1}{4}\begin{bmatrix} 1 & 1 & 1 & 1 \\ 1 & 1 & -1 & -1 \\ -1 & 1 & -n & n \\ -1 & 1 & n & -n \end{bmatrix}. \tag{5}$$

This mapping assigns transformer turns ratio $n = (1 - G_v)/G_v$ because it yields the minimum arm ac current stresses, as explained in Section II-A. Fig. 4 shows the paths of $[i_{t1}\ i_{t2}\ i_{c1}\ i_{c2}]$ where subscripts t and c denote terminal and internal circulating currents, respectively. Each arm voltage is comprised of $[v_{t1}\ v_{t2}\ v_{c1}\ v_{c2}]$ as shown. This mapping is based on previous works [29], [34] where it has been shown to offer decoupling of frequency content for currents and voltages.

The dc terminal currents are shown with the dashed (red) lines while internal circulating currents are represented with the solid (green) lines in Fig. 4. The dc components of i_{t1} and i_{t2} represent power transfer between input and output dc networks, where $i_{t1} = I_{\text{dci}} - I_{\text{dco}}/2$ and $i_{t2} = I_{\text{dco}}$. Ideally, the dc components of i_{t1} and i_{t2} split evenly amongst the four arms. Requesting nonzero I_{dco} (and hence, a P_{dc} demand) will invoke a dc power imbalance between p and s arms, which ultimately causes a deviation in capacitor voltages from their nominal values. The fundamental frequency component of i_{c1} can be regulated to counteract this power imbalance and, thus, ensure balanced capacitor voltages, i.e., i_{c1} is i_{ac} in Fig. 2 responsible for capacitor charge balancing. i_{c2} is a fundamental frequency current that coincides with the transformer magnetizing current, i.e.,

$$i_m \equiv i_{c2}. \tag{6}$$

Magnetizing current i_m only contains a fundamental frequency component due to the windings orientation, i.e., there is dc flux cancellation in the core. i_m is very small in practice assuming the magnetizing inductance L_m is high.

Dynamic equations can be derived from Fig. 4, yielding

$$[(n^2+1)L_a + L_x]\frac{di_{c1}}{dt} = -(n^2+1)R_a i_{c1} - 2v_{c1} \tag{7}$$

$$\left(\frac{nL_m}{2} + \frac{nL_a}{4} + \frac{L_a}{4n} + \frac{L_x}{4n}\right)\frac{di_{c2}}{dt} = -\frac{n^2+1}{4n}R_a i_{c2} - 2v_{c2} \tag{8}$$

$$\left(L_a + \frac{L_x}{2}\right)\frac{di_{t1}}{dt} = -R_a i_{t1} - 2v_{t1} + V_{\text{dci}} \tag{9}$$

$$\left(L_a + \frac{L_x}{2}\right)\frac{di_{t2}}{dt} = -R_a i_{t2} - 4v_{t2} + 4V_{\text{dci}} - 4V_{\text{dco}}. \tag{10}$$

Equations (7)–(10) reveal that arm voltages $[v_{t1}\ v_{t2}\ v_{c1}\ v_{c2}]$ enable control of their respective currents, e.g., v_{t2} drives i_{t2}.

B. Arm Capacitors Power Balancing Process

To transfer dc power from input to output, the M2dc-CT must internally transfer $(1 - V_{\text{dco}}/V_{\text{dci}})$ p.u. of P_{dc} as average ac power between p and s arms. This is similar to the M2dc and HVdc-AT. The ac power processing is needed to satisfy capacitor charge balance for the arm capacitors. To elucidate this process, consider the steady-state power balance criteria for arms 1 and 3 in Fig. 3

$$(V_{\text{dci}} - V_{\text{dco}})\frac{I_{\text{dci}}}{2} + \frac{1}{2}\hat{V}_1\hat{I}_1\cos(\theta_{v1} - \theta_{i1}) = 0 \tag{11}$$

$$V_{\text{dco}}\frac{(I_{\text{dci}} - I_{\text{dco}})}{2} + \frac{1}{2}\hat{V}_3\hat{I}_3\cos(\theta_{v3} - \theta_{i3}) = 0 \tag{12}$$

where $\hat{V}_1$, $\hat{I}_1$ and $\hat{V}_3$, $\hat{I}_3$ are the fundamental frequency peak amplitudes of voltage and current for arms 1 and 3, respectively. As shown in Fig. 4, the ac quantities (those with subscript c) supported by these arms are v_{c1}, v_{c2} and i_{c1}, i_{c2}. However, in practice i) $\hat{V}_{c1} \ll \hat{V}_{c2}$ as a relatively small v_{c1} is needed to drive rated i_{c1} with typical values of arm choke and leakage inductance L_a, L_x [cf. (7)], and ii) $\hat{I}_{c2} \ll \hat{I}_{c1}$ as magnetizing inductance L_m is very large [cf. (8)] that suppresses i_{c2}. These simplifying approximations imply

$$\hat{I}_1 \approx \hat{I}_{c1} \quad \hat{I}_3 \approx n\hat{I}_{c1} \quad \hat{V}_1 \approx \hat{V}_{c2} \quad \hat{V}_3 \approx \frac{\hat{V}_{c2}}{n}. \tag{13}$$

Applying these approximations to (11) and (12), along with lossless relationships $V_{\text{dco}} = G_v V_{\text{dci}}$ and $I_{\text{dci}} = G_v I_{\text{dco}}$, yields

$$(1 - G_v)V_{\text{dci}}\frac{I_{\text{dci}}}{2} + \frac{1}{2}\hat{V}_{c2}\hat{I}_{c1}\cos(\theta_{v1} - \theta_{i1}) = 0 \tag{14}$$

$$-(1 - G_v)V_{\text{dci}}\frac{I_{\text{dci}}}{2} + \frac{1}{2}\hat{V}_{c2}\hat{I}_{c1}\cos(\theta_{v3} - \theta_{i3}) = 0. \tag{15}$$

Equations (14) and (15) confirm arms 1 and 3 must exchange an average ac power equal to $0.5(1 - G_v)P_{\text{dc}}$ for capacitor charge balancing. The key ac quantities responsible for this power transfer are the fundamental frequency components of v_{c2}, i_{c1}.

C. Arms Current Stresses

Based on (14) and (15), the peak ac current seen by p and s arms assuming converter internal vars consumption is small in

$$\hat{I}_{c1} \approx \frac{P_{\text{dc}}(1 - G_v)}{\hat{V}_{c2}}. \tag{16}$$

$\hat{I}_{c1}$ can be minimized by maximizing ac arm voltage $\hat{V}_{c2}$, which is consistent with (2). For the M2dc-CT with half-bridge SMs, the maximal value of $\hat{V}_{c2}$ is limited to the minimum dc voltage

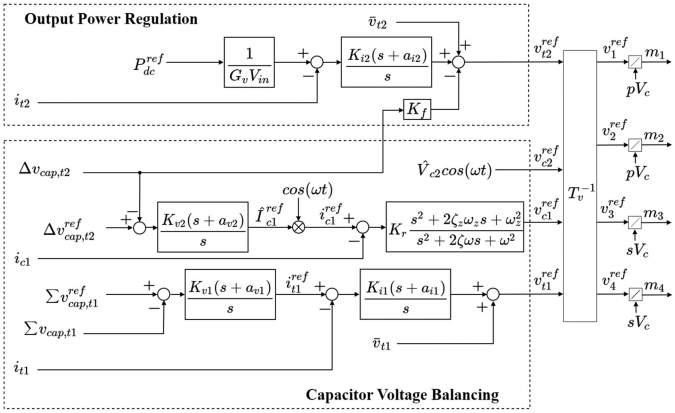

Fig. 5. Proposed dynamic controls for the M2dc-CT.

TABLE I
CONTROL OBJECTIVES FOR M2DC-CT CURRENTS

Current	Frequency Component	Control Goal
i_{t1}	dc	$\Sigma v_{cap,t1}$ regulation
i_{t2}	dc	P_{dc} regulation
i_{c1}	fundametal frequency (ac)	$\Delta v_{cap,t2}$ regulation

component of p and s arms

$$\hat{V}_{c2} \leq \min\{(1-G_v)V_{\text{dci}},\ nG_vV_{\text{dci}}\}. \tag{17}$$

To maximize the ac voltage for both p and s arms across all values of G_v, the transformer turns ratio is chosen as

$$n = (1-G_v)/G_v. \tag{18}$$

Then, $\hat{V}_{c2}$ can be expressed as

$$\hat{V}_{c2} = (1-G_v)V_{\text{dci}}M_{c_2} \tag{19}$$

where $M_{c_2} \in [0,1]$ is the ac modulation index. Recalling (16), the ratio of fundamental frequency to dc current carried by p and s arms [(e.g., arms 1 and 3 in Fig. 3(a)] is

$$\frac{\hat{I}_1}{\frac{I_{\text{dci}}}{2}} = \frac{\hat{I}_3}{\frac{I_{\text{dci}}}{2}\left(\frac{1-G_v}{G_v}\right)} = \frac{2}{M_{c2}}. \tag{20}$$

When maximizing ac arm voltages, i.e., $M_{c_2}=1$, the ac current stresses for the M2dc-CT is 2 p.u. in both p and s arms. This corresponds to the optimal conditions in Fig. 2(c).

IV. CONVERTER CONTROLS

Open-loop control of the M2dc-CT will not maintain balanced SM capacitor voltages during varying dc power transfers. Moreover, closed-loop control of the dc power transfer is needed for grid applications. Fig. 5 proposes a dynamic controller for the two-string M2dc-CT that fulfills these operational requirements. Table I indicates which state variables are associated with specific control goals, as informed by (7)–(10). The benefit of mapping into t and c quantities becomes apparent, as i_{t1}, i_{t2}, i_{c1} are each responsible for a distinct power transfer mechanism. Moreover, dc and fundamental frequency components become decoupled.

The controls in Fig. 5 are apportioned into the following two different blocks: i) output power regulation, and ii) capacitor voltage balancing, where we have the following.

1) The output power regulation scheme regulates the dc component of i_{t2} via proportional-integral control to provide the desired dc power throughput P_{dc}.
2) The capacitor voltage balancing scheme regulates sum capacitor voltage $\Sigma v_{\text{cap},t1}$, where cascaded control loops are used: a) an outer voltage loop regulates the dc component of $\Sigma v_{\text{cap},t1}$ via proportional-integral control to generate i_{t1}^{ref}, and b) an inner-current loop regulates the dc component of i_{t1} via proportional-integral control.
3) The capacitor voltage balancing scheme also regulates difference capacitor voltage $\Delta v_{\text{cap},t2}$, where cascaded control loops are used: a) an outer voltage loop regulates the dc component of $\Delta v_{\text{cap},t2}$ via proportional-integral control to generate $\hat{I}_{c1}^{\text{ref}}$, and b) an inner-current loop regulates the fundamental frequency component of i_{c1} via proportional-resonant control where

$$\begin{bmatrix}\Sigma v_{\text{cap},t1}\\ \Delta v_{\text{cap},t2}\end{bmatrix} = \frac{1}{4}\begin{bmatrix}1 & 1 & 1 & 1\\ 1 & 1 & -1 & -1\end{bmatrix}\begin{bmatrix}\sum_{j=1}^{p} v_{c,j}^{\text{arm1}}\\ \sum_{j=1}^{p} v_{c,j}^{\text{arm2}}\\ \sum_{j=1}^{s} v_{c,j}^{\text{arm3}}\\ \sum_{j=1}^{s} v_{c,j}^{\text{arm4}}\end{bmatrix}. \tag{21}$$

As is common practice with cascaded control loops, the closed-loop response of i_{t1} (and i_{c1}) is set to be significantly faster than the response of $\Sigma v_{\text{cap},t1}$ (and $\Delta v_{\text{cap},t2}$).

The $\Delta v_{\text{cap},t2}$ capacitor voltage balancing loop ensures any dc imbalance between p and s arms is regulated to zero via feedback control of the fundamental frequency component of i_{c1}. This ac current interacts with ac arm voltage v_{c2} to exchange the requisite average ac power between arms, as given by (14) and (15). In contrast, the $\Sigma v_{\text{cap},t1}$ capacitor voltage balancing loop can charge/discharge all capacitor voltages together by appropriate control of the dc component of i_{t1}. $\Sigma v_{\text{cap},t1}^{\text{ref}} = 0.25(p+s)V_c$ and $\Delta v_{\text{cap},t2}^{\text{ref}} = 0.25(p-s)V_c$, where V_c is the nominal SM capacitor voltage. A dynamic phasor model of M2dc derived in [35] identifies an interstate dynamic coupling between i_{t_2} and $\Delta v_{\text{cap},t2}$, and therefore, feed-forward gain K_f is added to decouple i_{t_2} and $\Delta v_{\text{cap},t2}$ dynamics. This is done to improve the dynamic response of M2dc-based topologies [34]. The dynamic controller produces control terms v_{c1}^{ref}, v_{c2}^{ref}, v_{t1}^{ref}, and v_{t2}^{ref}, which are transformed into physical arm voltages based on (4). The nominal dc values of v_{t1} and v_{t2} are expressed as follows:

$$\bar{v}_{t1} = \frac{1}{2}V_{\text{dci}} \quad \bar{v}_{t2} = \frac{1}{2}(1-2G_v)V_{\text{dci}}. \tag{22}$$

TABLE II
SIMULATION PARAMETERS

Converter Parameters	
Input and output voltages, V_{dci}/V_{dci}	400 kV/50 kV
Conversion ratio, G_v	0.125
Input power, P_{dc}	75 MW
Fundamental frequency , ω	$2\pi 150$ rad/s
Primary/secondary arm no. of SMs, p/s	350/50 (half-bridge)
Primary/secondary arm SM capacitor, C_p/C_s	2 mF/14 mF
Primary/secondary arm choke, $L_{a,p}/L_{a,s}$	60 mH/1.2 mH
Nominal SM capacitor voltage, V_c	2 kV
Line impedance, L_s, R_s	40.5 mH, 1.65 Ω
Transformer Parameters	
Transformer power rating, S_{tr}	77.5 MVA
Turns ratio, n	7:1
Primary/secondary winding voltages, V_p/V_s	223 kV/32 kV (rms)
Leakage inductance, L_x	10 mH
Magnetizing current	1%
Controller Parameters	
K_{i1}, K_{i2}, a_{i1}, a_{i2}, K_f	50, 1.5, 10, 20, 0.12
K_{v1}, K_{v2}, a_{v1}, a_{v2}	0.045, 0.006, 15, 30
K_r, ζ, ζ_z, ω_z	10, 0.1, 1.2, 942 rad/s
$\bar{v}_{t1}$, $\bar{v}_{t2}$, $\hat{V}_{c2}$	200 kV, 150 kV, 45 kV
$\Sigma v_{cap,t1}^{ref}$, $\Delta v_{cap,t2}^{ref}$	400 kV, 300 kV

V. SIMULATION RESULTS

Simulations are conducted in PSCAD/EMTDC using a detailed equivalent switching model. Voltage balancing of capacitors within each arm is achieved using the sort and selection method. The two-string M2dc-CT in Fig. 3(a) is designed as an HVdc-MVdc interconnect with 400/50 kV dc ratio ($G_v = 0.125$) and 75 MW rated dc power transfer. The ac frequency is 150 Hz. Simulation parameters are given in Table II. The parameters for the controllers are selected to give settling times of around 100 ms for the dc output current i_{t2} and 150 ms for the capacitor voltages $\Sigma v_{\text{cap},t1}$ and $\Delta v_{\text{cap},t2}$.

The following discussion highlights key converter design considerations for the simulated case study of $G_v = 50/400 = 0.125$. Similar design principles would apply for other dc step ratios. The dc step ratio $G_v = 0.125$ implies selecting $n = 7$ from (18) to minimize the ac current in each arm. The primary and secondary arms in Fig. 3(a) must support dc voltages of 350 and 50 kV, respectively. Considering also the SM capacitor voltage rating is 2 kV and that half-bridge SMs are used to maximize the synthesized ac arm voltages, the number of SMs in primary and secondary arms are chosen to be 350 and 50, respectively. Thus, each of the primary and secondary side windings of the center-tapped transformer are rated for 222.7 kV_{rms} and 31.8 kV_{rms} (assuming a modulation index of 0.9), respectively. The primary windings need to carry 0.094 kA dc and approximately 0.208 kA_{pk} ac at rated power transfer, which corresponds to 0.174 kA_{rms} winding current rating. Similarly, the transformer secondary windings need to carry 0.656 kA dc and approximately 1.458 kA_{pk} ac, which corresponds to 1.222 kA_{rms}. The resulting transformer VA rating is approximately 77.5 MVA. The SM capacitances are picked to yield peak-to-peak capacitor voltage ripples of around 5% for the primary and secondary arms.

Fig. 6 shows steady-state operation of the converter with $P_{\text{dc}} = 75$ MW. i_{t2} has a dc component of 1.5 kA, which is the outcome of P_{dc} control, as $I_{\text{dco}} = i_{t2}$. i_{t1} has a dc component of −562.5 A where $I_{\text{dci}} = i_{t1} + i_{t2}/2$. The 150 Hz component of i_{c1} is 210 A_{pk}, while i_{c2} has a negligibly small 150 Hz component (as expected) due to the large transformer magnetizing impedance.

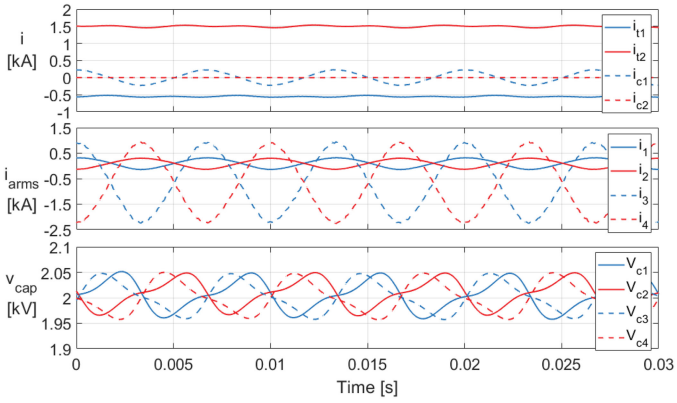

Fig. 6. Steady-state M2dc-CT current and voltage waveforms for $G_v = 0.125$.

TABLE III
FREQUENCY ANALYSIS OF SIMULATED M2DC-CT ARM CURRENTS AND CALCULATED M2DC ARM CURRENTS (AT RATED POWER)

	M2DC-CT [Simulated]		M2DC [calculated for comparison]	
	Primary	Secondary	Primary	Secondary
G_v	p.u.	p.u.	p.u.	p.u.
1/8	2.188	2.286	**15.556**	2.222
2/8	2.211	2.280	**6.667**	2.222
3/8	2.201	2.279	**3.704**	2.222
4/8	2.174	2.272	2.222	2.222
5/8	2.179	2.275	2.222	**3.704**
6/8	2.203	2.267	2.222	**6.667**
7/8	2.211	2.257	2.222	**15.556**

The i_1, i_2 (p arm currents) and i_3, i_4 (s arm currents) waveforms in Fig. 6 verify that the M2dc-CT can realize inherent minimization of ac arm currents similar to the HVdc-AT. This is quantified in the first row (highlighted grey) of Table III, which provides the per-unitized current stresses for the M2dc-CT at $G_v = 1/8 = 0.125$ with $P_{\text{dc}} = 75$ MW. Both primary and secondary ac arm currents in the M2dc-CT are near the 2 p.u. minimal value, as given by Fig. 2(c) [and also by (20) assuming $M_{c2} = 1$]. The idealized 2 p.u. result was obtained by i) neglecting resistive losses, ii) assuming unity modulation index, and iii) neglecting converter internal vars consumption. However, in practice the actual ac currents will be slightly larger as shown in the first row of Table III. For comparison, the first row of Table III also lists the current stresses calculated for a conventional M2dc at $G_v = 1/8$ assuming the same modulation index as in simulation for the M2dc-CT but under lossless conditions. The primary arms see drastically higher current stresses (15.556 p.u. as indicated in bold), as predicted by Fig. 2(a). The M2dc is, therefore, not a viable option for a dc step ratio of 50 kV / 400 kV.

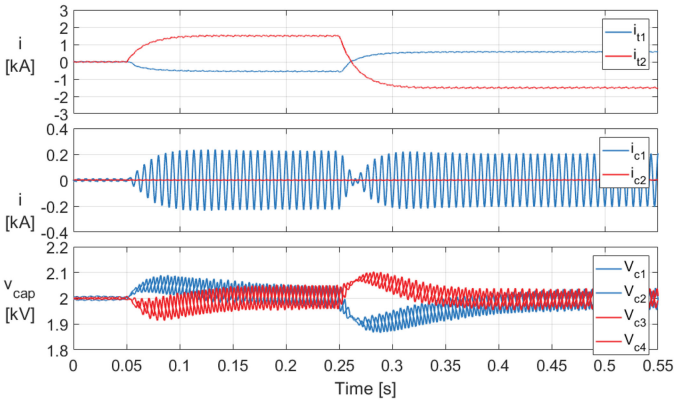

Fig. 7. M2dc-CT waveforms for step-change in $P_{\rm dc}^{\rm ref}$ from 0 MW to +75 MW at $t = 0.05$ s. and from +75 MW to −75 MW at t = 0.25 s.

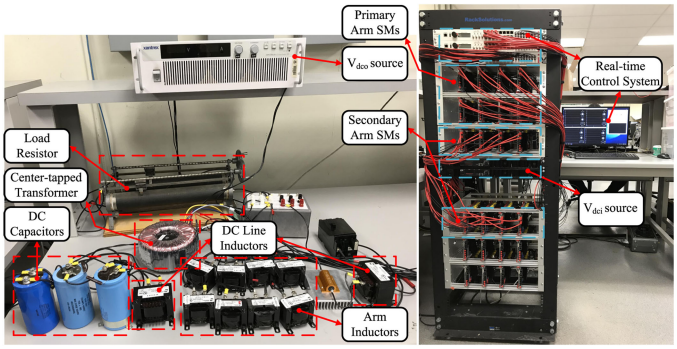

Fig. 8. M2dc-CT experimental setup.

Apart from the simulated case study of $G_v = 50/400 = 1/8$, Table III also provides per-unitized current stresses for the M2dc-CT and M2dc from $G_v = 1/8$ to $G_v = 7/8$. The results confirm that the proposed M2dc-CT is able to minimize arm current stresses at all dc step ratios, while the conventional M2dc suffers from increased current stresses when $G_v \neq 0.5$. This is consistent with the analysis in Fig. 2(a).

Fig. 7 shows two transient responses: $P_{\rm dc}^{\rm ref}$ changed from 0 MW to +75 MW at $t = 0.05$ s and $P_{\rm dc}^{\rm ref}$ changed from +75 MW to −75 MW at $t = 0.25$ s. In each case, capacitor voltage balance is quickly re-established despite the large step-changes in dc power transfer. These results verify the efficacy of the proposed dynamic controller.

VI. Experimental Validation

Experimental results are presented for a scaled-down 250/85 V, 1.25 kW laboratory prototype of the two-string M2dc-CT. The main objectives are to verify i) that ac currents for both primary and secondary arms can be minimized in practice, and ii) the practical efficacy of the proposed dynamic controller. The experimental setup and converter schematic are shown in Figs. 8 and 9, respectively. Half-bridge SMs and real-time controllers from Imperix are used. Experimental parameters are given in Table IV. A transformer with $n = 1.95$ is used that corresponds to $G_v = 0.34$ as per (18). The ac frequency is 150 Hz for consistency with the simulation results.

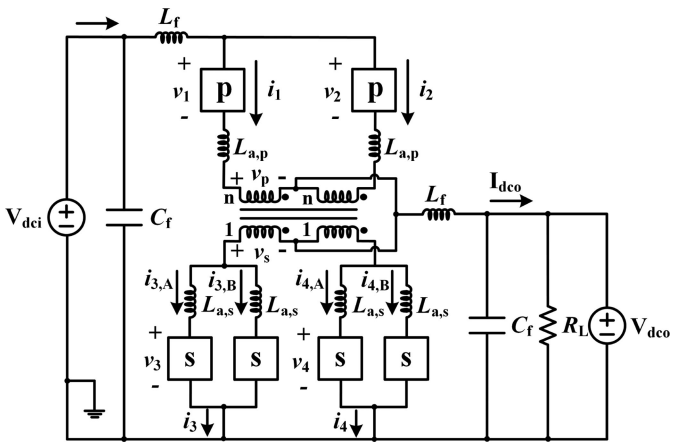

Fig. 9. M2dc-CT experimental schematic.

TABLE IV
Experimental Parameters

Converter Parameters	
Input and output voltages, V_{dci}/V_{dci}	250 V/85 V
Conversion ratio, G_v	0.34
Input power, P_{dc}	1.25 kW
Fundamental frequency , ω	$2\pi 150$ rad/s
Primary/secondary arm no. of SMs, p/s	4/2 (half-bridge)
Primary/secondary arm SM capacitor, C_p/C_s	5 mF/5 mF
Primary/secondary arm choke, $L_{a,p}/L_{a,s}$	2 mH/1 mH
Nominal SM capacitor voltage, V_c	85 V
Line impedance, L_f	2.5 mH
DC bus capacitor, C_f	3 mF
Transformer Parameters	
Transformer power rating, S_{tr}	1.5 kVA
Turns ratio, n	1.95:1
Primary/secondary winding voltages, V_p/V_s	117 V/60 V (rms)
Leakage inductance, L_x	0.085 mH
Magnetizing inductance, L_m	1.516 H
Controller Parameters	
SPWM carrier frequency, f_{sw}	7 kHz
Sample frequency, f_{sample}	7 kHz
K_{i1}, K_{i2}, a_{i1}, a_{i2}, K_f	0.5, 0.5, 20, 25, 0.2
K_{v1}, K_{v2}, a_{v1}, a_{v2}	2.8, 40, 0.8, 25
K_r, ζ, ζ_z, ω_z	15, 0.1, 1.2, 942 rad/s
$\bar{v}_{t1}$, $\bar{v}_{t2}$, $\hat{V}_{c2}$	125 V, 40 V, 76.5 V
$\Sigma v_{cap,t1}^{ref}$, $\Delta v_{cap,t2}^{ref}$	340 V, 0 kV

In Fig. 9, each primary arm consists of four series-cascaded SMs. Each (composite) secondary arm consists of two parallel-connected s arms (A and B), each comprising two series-cascaded SMs. Therefore, all arms have four SMs in total. Operating at $G_v = 250/85$ results in the (composite) secondary arms having approximately twice the dc current and half the dc voltage as the primary arms, and therefore, the s arms are paralleled as shown so that all SMs in the converter have by design approximately the same V, I stress.

A. Steady-State Performance

Fig. 10 shows the steady-state arm voltages v_1, v_3 along with arm currents i_1, $i_{3,A}$ at rated dc power transfer. With $V_{\rm dci} = 250$ V and $V_{\rm dco} = 85$ V, arm 1 must support 165 $V_{\rm dc}$

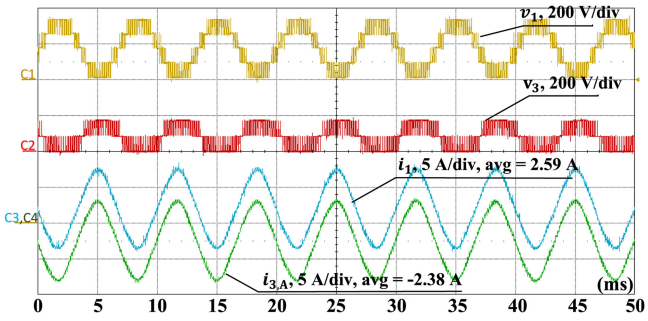

Fig. 10. M2dc-CT steady-state arm voltages v_1, v_3 and arm currents i_1, $i_{3,A}$ at $P_{\text{dc}}^{\text{ref}} = 1.25$ kW; experimental waveforms captured by oscilloscope.

TABLE V
FREQUENCY ANALYSIS OF EXPERIMENTAL M2DC-CT CURRENTS (AT RATED POWER)

M2DC-CT [experimental]	DC	150 Hz
Primary arms	2.59 A	5.72 A_{pk} (2.21 p.u.)
Secondary arms	4.76 A	11.28 A_{pk} (2.37 p.u.)
M2DC [calculated for comparison]	DC	150 Hz
Primary arms	2.5 A	10.78 A_{pk} (4.31 p.u.)
Secondary arms	4.85 A	10.78 A_{pk} (2.22 p.u.)

while arm 2 supports 85 V_{dc}. Therefore, using only half-bridge SMs, the 150 Hz component of v_1 will be approximately twice (165/85 = 1.95 times precisely) that of v_3. This is confirmed in Fig. 10. The center-tapped ac transformer with $n = 1.95$ provides the necessary voltage matching between primary and secondary arms, which enables minimization of the ac arm currents. The dc and 150 Hz components of i_1 and $i_{3,A}$ are by design approximately equal, as confirmed by Fig. 10. The dc and 150 Hz components of i_3, i_4 are by design approximately twice that of i_1, i_2, as confirmed by Fig. 10, due to the paralleling of s arms in Fig. 9.

Table V lists the magnitudes of arms dc and fundamental frequency (150 Hz) currents for the M2dc-CT at $P_{\text{dc}} = 1.25$ kW. Both primary and secondary ac arm currents are near the ideal 2 p.u. minimal value, similar to the simulation case study results in Table III. This confirms the M2dc-CT can in practice achieve ac current minimization for all arms. For comparison, Table V also lists the current stresses calculated for a conventional M2dc assuming the same modulation index as in experiment but under lossless conditions. The 4.31 p.u. ac current carried by the primary arms is much higher (nearly double) relative to the secondary arms.

B. Dynamic Performance

The dynamic response of the M2dc-CT to step-changes in $P_{\text{dc}}^{\text{ref}}$ from 1.25 to 0.25 kW and from 0.625 to 1.25 kW are shown in Figs. 12 and 13, respectively. These results validate the dynamic controller proposed in Fig. 5. The reduction (and increase) in P_{dc} demand in Fig. 12 (and Fig. 13) initially causes a dc voltage imbalance between SM capacitors in the primary and secondary arms, i.e., $\Delta v_{\text{cap},t2}$ deviates from its reference value. The controller re-establishes balanced capacitor voltages

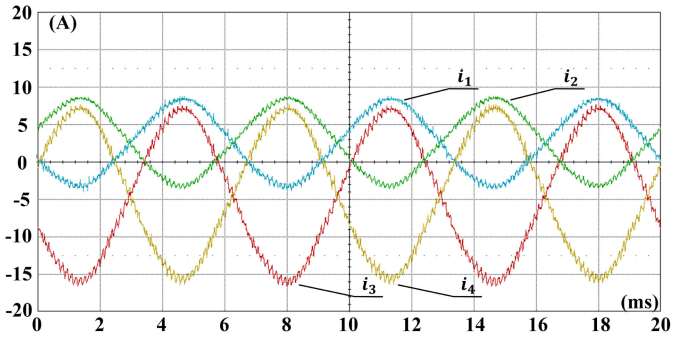

Fig. 11. M2dc-CT steady-state arm currents i_1, i_2, i_3, and i_4 at $P_{\text{dc}}^{\text{ref}} = 1.25$ kW; experimental waveforms captured by oscilloscope.

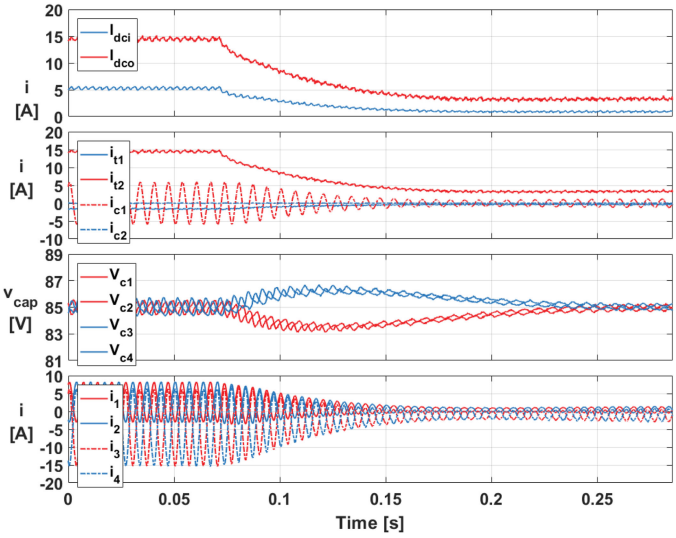

Fig. 12. M2dc-CT dynamics with a step change of $P_{\text{dc}}^{\text{ref}}$ from 1.25 to 0.25 kW at $t = 0.07$ s; experimental waveforms recorded using real-time control software with $f_{\text{sample}} = 7$ kHz.

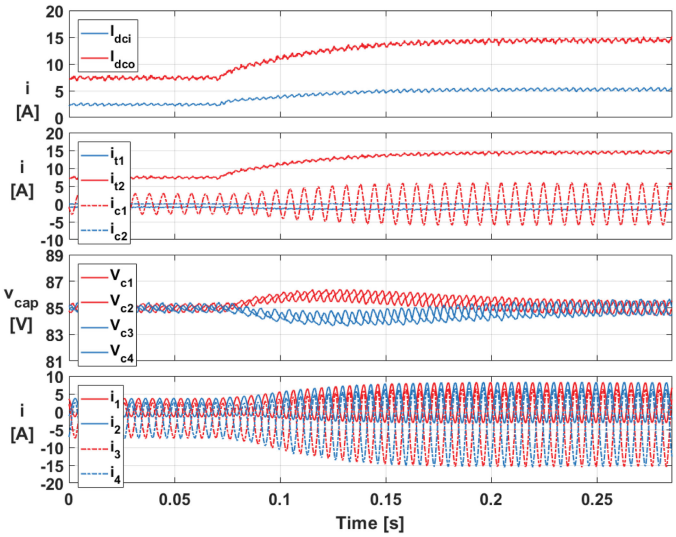

Fig. 13. M2dc-CT dynamics with a step change of $P_{\text{dc}}^{\text{ref}}$ from 0.625 to 1.25 kW at $t = 0.07$ s; experimental waveforms recorded using real-time control software with $f_{\text{sample}} = 7$ kHz.

by requesting the requisite decrease (and increase) in the 150 Hz component of i_{c1}.

VII. Comparison of DC–DC Power Transfer Mechanisms

The M2dc-CT leverages a novel dc–dc power transfer mechanism enabled by an internal center-tapped transformer that is a hybrid of the P3T (for HVdc-AT) and CCL (for M2dc) mechanisms. Consequently, the M2dc-CT is able to merge the best traits of the HVdc-AT and M2dc; namely, inherent minimization of arm ac current stresses and elimination of dc voltage stress between internal transformer windings. This comes, though, at the expense of the transformer windings carrying both dc and ac currents. However, it will be shown in Section VII-B that the absence of interwinding dc voltage stress yields an overall reduction in transformer area product relative to the HVdc-AT, and hence, overall lower magnetics size and weight (and ultimately cost).

This section first compares arm current stresses, semiconductor effort, and magnetics requirements on a per-unitized basis for the M2dc-CT, M2dc, and HVdc-AT. These are all partial power processing dc–dc MMCs. Results are also compared to the conventional two-stage F2F-MMC for reference. The case study analysis considers a converter with $V_{\text{dci}} = 400$ kV, $P_{\text{dc}} = 75$ MW, and $f = 150$ Hz for consistency with the simulations. A wide range of dc step ratios is considered with $G_v \in [0.1, 0.9]$ (in increments of +0.1). Converter losses for all four topologies are then calculated. To conduct a fair comparison, it is assumed half-bridge SMs are employed for each topology and that arms ac voltage utilization is maximized at every operating point. Based on results of the comparative analysis, Section VII-D identifies key applications for the M2dc-CT.

A. Current Stresses and Semiconductor Effort

The semiconductor effort λ is a measure of the power rating of the switches that has to be installed per Watt of real input power [36]–[38]. It is expressed on a per-unit basis as the ratio of the sum of all the semiconductors' apparent power ratings to the dc power throughput. Thus, semiconductor effort depends on the peak current stresses for the arms. Fig. 14 first plots the absolute peak currents of each topology for primary and secondary arms, normalized to the dc input current of each phase leg. For the primary arms, all topologies have the same peak current stress except for the M2dc, which sees very high stresses as G_v decreases below 0.5. This is because the M2dc lacks a transformer for ac voltage matching between arms. For the secondary arms, the M2dc-CT and HVdc-AT achieve the lowest peak current stresses while the current stresses for the M2dc go up as G_v increases above 0.5, reaching a maximum value of over 6 times larger than both the M2dc-CT and HVdc-AT at $G_v = 0.9$. The F2F-MMC has the highest stresses as it is not a partial-power processing topology. All topologies see large secondary arm current stresses at low G_v due to the inherently high dc currents seen by these arms. Based on these results, the semiconductor effort normalized to dc power transfer P_{dc} is lastly plotted in Fig. 14. The M2dc-CT and HVdc-AT have

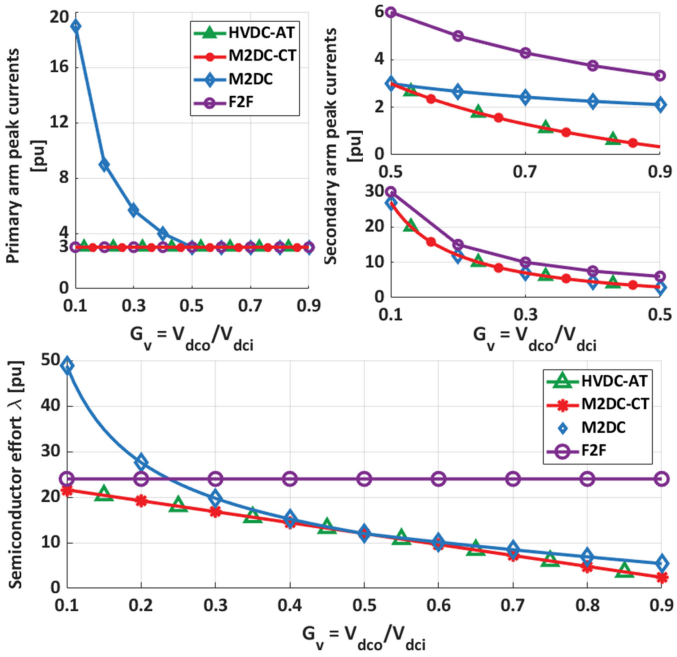

Fig. 14. Arms absolute peak current stresses, at rated power transfer and with maximum arm ac voltage utilization using half-bridge SMs (all currents are normalized to dc input current of each phase leg). Corresponding converter semiconductor efforts normalized to dc power transfer P_{dc}.

the lowest overall semiconductor effort across all dc step ratios. The M2dc has equal semiconductor effort only at $G_v = 0.5$; it has higher values at all other step ratios. The F2F-MMC has constant semiconductor effort owing to its two-stage isolated dc–dc structure with separate MMCs.

B. Magnetics Core Area Product

This section quantifies the impact of core power handling capability S_c and interwinding dc voltage stress $V_{\text{dc,iso}}$ on the size, weight, and cost of the magnetics. The transformer in the HVdc-AT carries ac current while the zig-zag transformer in the M2dc carries dc current. The center-tapped transformer in the M2dc-CT carries both dc and ac currents. The M2dc and M2dc-CT transformers provide core dc magnetic flux cancellation due to windings orientation [16], [18], [21]. S_c is calculated by summing the product of the rms voltage and rms current for each winding [39]. $V_{\text{dc,iso}}$ (see Fig. 2) is determined for asymmetric monopole or bipole configurations.

S_c and $V_{\text{dc,iso}}$ requirements of the magnetics are first plotted in Fig. 15. The F2F-MMC transformer core power is constant while the M2dc transformer core power is the lowest overall. S_c for the M2dc-CT center-tapped transformer is 18.4% higher than the HVdc-AT transformer core power at all dc step ratios. This is because the center-tapped transfomer has a higher overall rms current rating. At very low dc step ratios, the center-tapped transformer in the M2dc-CT has the highest core power. For the interwinding dc voltage stresses, $V_{\text{dc,iso}} = 0.5V_{\text{dci}}$ for the HVdc-AT at all values of G_v while $V_{\text{dc,iso}}$ for the F2F-MMC goes up as G_v decreases. However, $V_{\text{dc,iso}} = 0$ for the M2dc and M2dc-CT.

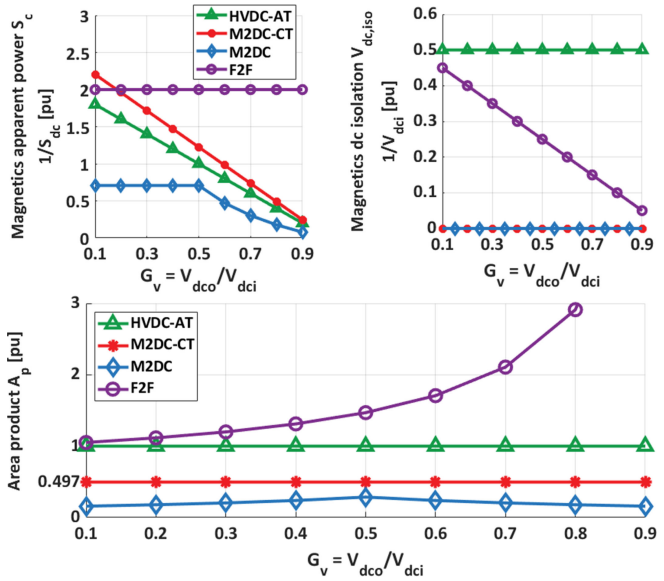

Fig. 15. Converter magnetics requirements: core apparent power rating normalized to dc power transfer P_{dc}; interwinding dc voltage isolation requirements normalized to V_{dci} for asymmetric monopole or full bipole configurations; Corresponding magnetics core area product normalized to F2F-MMC's area product.

The core area product A_p is a figure of merit to compare the costs of the magnetic components and relates to the size of magnetics [26]. It is directly proportional to S_c and inversely proportional to the core window utilization factor K_u, which is a number less than one that models the amount of core window area utilized by copper [39]. K_u depends on insulation requirements including any dc voltage stress that exists between windings. $K_u = 0.4$ is used in [39] to approximate transformer designs without dc voltage isolation requirements, and therefore, this value is used for the M2dc and M2dc-CT. For the HVdc-AT and F2F-MMC, assuming HV cable is used as the insulation mechanism to accommodate interwinding dc isolation requirements [40], K_u is modified to account for the corresponding copper fill reduction as follows:

$$K_u = 0.4 \cdot \frac{\pi R_w^2}{\pi (R_w + d_{ins})^2} \tag{23}$$

where R_w is the cable conductor radius and d_{ins} is the required cable insulation thickness. Data for R_w and d_{ins} considering different HV levels from [41] is used. Exact calculation of the area product A_p requires a detailed magnetics design. The magnetic structure is typically designed based on a tradeoff between size, cost, and efficiency, following the procedure of magnetic structure determination, insulation design, core material selection, and magnetic loss analysis [42], [43]. Given the comparative analysis considers a total of (four different converters)×(nine different dc step ratios)=36 different magnetic structures, generating an optimal design for all cases is outside the scope of this article. Rather, the goal is to provide a relative comparison of A_p for the different topologies that accounts for the impacts of S_c and K_u (the latter of which is influenced by $V_{\text{dc,iso}}$). Thus, in calculating the area product, other transformer parameters such as operating frequency are set to be the same for all topologies.

Fig. 15 shows the calculated A_p for the four topologies, normalized to the area product of the F2F-MMC for reference. The area product for the M2dc is the lowest among all topologies because $V_{\text{dc,iso}} = 0$ and it has the lowest S_c. The M2dc-CT has the next lowest A_p. The HVdc-AT always has larger A_p than the M2dc-CT. There is a 50% reduction in A_p for the M2dc-CT relative to the HVdc-AT. This is in fact a constant outcome regardless of dc step ratio, as the required dc isolation voltage for the M2dc-CT and HVdc-AT does not depend on G_v.

C. Converter Losses

This section calculates the losses of the four dc–dc converter topologies. The conduction and switching losses of the semiconductors as well as winding and core losses of the magnetics are considered as dominant losses in the converters. The semiconductor conduction and switching losses are calculated using a similar method as in [22], [26], and [34]. Since the semiconductor losses calculation is dependent on technology, the Mitsubishi CM1200HC-90R HVIGBT with a rating of 4500 V and 1200 A is used for all topologies (datasheet parameters available in [34]). Insulated-gate bipolar transistors (IGBTs) are paralleled as needed to accommodate arm currents that exceed switch ratings, e.g., at low G_v for the M2dc. The converters operate at $f = 150$ Hz.

In the following, a method to approximate the magnetics losses is proposed that does not require detailed core design[1] (for the reasons stated in Section VII-B) but still accounts for changes in area product due to interwinding dc voltage stresses. The core loss P_{core} and copper loss P_{copper} are the two types of losses in a magnetic structure. Assumptions are made for estimating these loss components as follows.

1) P_{core} and P_{copper} are usually designed to be similar to maximize efficiency [44]–[46], and thus, they are assumed to be the same.
2) Total magnetic losses (P_{core} and P_{copper}) increase with the transferred power [26], and it is estimated to be 0.5% of the magnetic MVA rating [22], [34].

The combined copper and core losses for magnetics in the M2dc and M2dc-CT are, thus, approximated as

$$P_{\text{copper}} + P_{\text{core}} = 0.5\% \cdot S_{\text{tr}}. \tag{24}$$

Loss estimate (24) is suitable for the M2dc and M2dc-CT where there is no dc voltage stress between windings on the core and, hence, no extra insulation requirements. However, it would not account for an increase in the size and weight of the magnetic core that results from increased area product, due to extra insulation requirements needed to accommodate interwinding dc voltage stresses. This core volume increase would cause the core losses to go up for the same power rating [47]. Therefore, to estimate the total magnetics losses for the HVdc-AT and

[1]For information on power converter transformer design, the works in [42], [44], and [45] can be consulted.

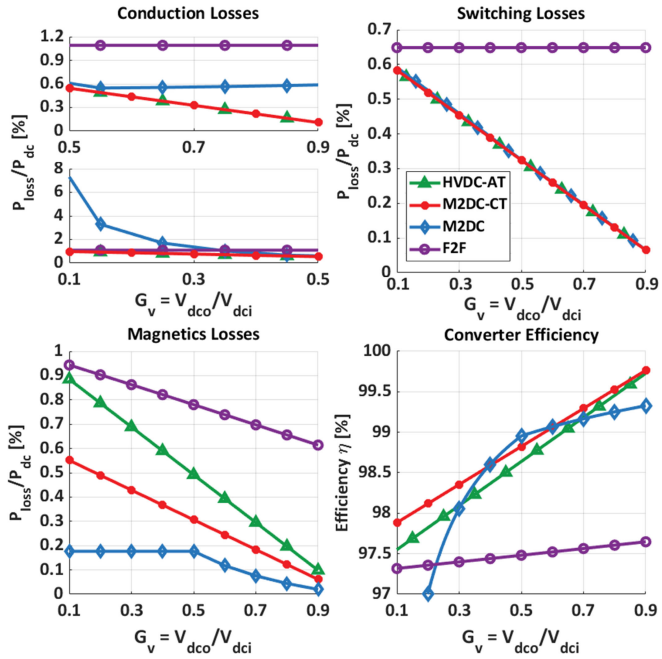

Fig. 16. Losses (normalized to dc power transfer P_{dc}) and efficiency analysis.

F2F-MMC, (24) is modified as follows:

$$P_{\text{copper}} + P_{\text{core}} = 0.5\% \cdot S_{\text{tr}} \cdot \left(\frac{A_p}{A_{p,\text{nom}}}\right)^k \tag{25}$$

where A_p is the actual area product of the magnetic structure and $A_{p,\text{nom}}$ is the area product of the magnetic structure with the same power rating but without extra dc insulation requirement (i.e., with $V_{\text{dc,iso}} = 0$). Coefficient $k = 0.75$ represents the core volume-area product relationship [39].

Fig. 16 plots the computed converter losses as well as the resulting efficiency for the HVdc-AT, M2dc-CT, M2dc, and F2F-MMC. The switching losses for the HVdc-AT, M2dc-CT, and M2dc are nearly identical, however, only the HVdc-AT and M2dc-CT achieve the lowest conduction losses across all dc step ratios. The M2dc experiences increased conduction losses for $G_v \neq 0.5$; specifically, it sees extremely high losses for $G_v \ll 0.5$ and high losses as G_v approaches unity. This is due to the increased arm current stresses at these operating points, as shown in Fig. 14. However, the M2dc enjoys the lowest magnetics losses across all dc step ratios. The magnetics losses for the M2dc-CT falls somewhere between the M2dc and HVdc-AT. The efficiency plot in Fig. 16 reveals the M2dc has the highest efficiency around $G_v = 0.5$, due to relatively low magnetics losses, but at lower and higher dc step ratios the efficiency drops off because of increased conduction losses. Except for dc step ratios ranging from around 0.4 to 0.6, the M2dc-CT has the highest efficiency.

D. Discussion and Implications

The nonisolated M2dc, HVdc-AT, and proposed M2dc-CT were compared in terms of arms peak current stresses, semiconductor effort, magnetics core area product, and converter losses. The isolated F2F-MMC was included in the comparison for reference. The key outcomes are as follows.

1) The M2dc-CT (and the HVdc-AT) has the lowest overall peak current stresses for the arms and has the lowest total semiconductor effort, across all dc step ratios.
2) The core area product for the M2dc-CT is larger than the M2dc but always lower than the HVdc-AT, with the M2dc-CT achieving around a 50% reduction relative to the HVdc-AT across all dc step ratios. This translates to considerable reduction in magnetics size and weight (and consequently lower losses).
3) The M2dc shows superior performance at around $G_v = 0.5 \pm 0.1$ in terms of efficiency and magnetic requirement. However, outside this range of dc step ratios, the M2dc-CT has the highest efficiency due to minimized ac currents and reduced size of magnetic structure. The HVdc-AT also has good efficiency and magnetics requirements for G_v approaching unity, but its losses and magnetics requirements suffer as G_v decreases below 0.5.

From on these observations, potential applications are identified for the M2dc-CT as follows that are categorized based on the required dc step ratio.

1) Lower Values of G_v ($V_{\text{dco}} \ll V_{\text{dci}}$): The benefits of the proposed M2dc-CT are most pronounced at low dc step ratios where the i) M2dc becomes impractical due to very high-current stresses, and ii) the HVdc-AT suffers from large size and weight of the magnetics, becoming comparable to the full rated F2F-MMC transformer. The HVdc-AT and M2dc-CT have similar conduction and switching losses in this region, but the bulky transformer in the HVdc-AT makes its efficiency marginally lower than the M2dc-CT. This factor becomes important for applications where space is limited, for example, when designing dc collector systems for offshore wind farms with pure dc power systems where converter station footprint, weight, efficiency, and cost are critical [7], [48].

Applications that require lower values of G_v, i.e., $G_v \ll 0.4$, where the M2dc-CT is well suited to include the following:

1) HVdc-to-MVdc grids interconnects;
2) connecting offshore wind MVdc collector networks to offshore HVdc stations;
3) HVdc power tapping with MVdc bus output.

2) Higher Values of G_v ($V_{\text{dco}} \approx V_{\text{dci}}$): The M2dc-CT is also an attractive option at high dc step ratios where it has the highest efficiency and the size and weight of its magnetics become somewhat comparable to the M2dc. However, weight and footprint of the converter system are usually not critical for applications where space is not limited, e.g., for HVdc grids interconnection [7]. Thus, the M2dc-CT (and the HVdc-AT) offers an alternative solution to the M2dc with higher efficiency but marginally larger magnetics.

Applications that require higher values of G_v, i.e., $G_v \gg 0.6$, where the M2dc-CT is a competitive option and include the following:

1) interconnecting HVdc (or MVdc) systems of similar voltages;

2) dc line power flow controllers where only incremental series dc voltage injection is needed.

VIII. Conclusion

A new class of partial power processing dc–dc MMC is presented that is able to merge the best traits of the M2dc and HVdc-AT. This new converter, termed the M2dc-CT, exploits a multiwinding center-tapped transformer to minimize ac arm currents for a wide range of dc step ratios while simultaneously avoiding any dc voltage stress between windings. These benefits come at the expense of the transformer carrying both dc and ac currents. However, a comparative analysis reveals that the transformer core area product is always lower than the HVdc-AT due to elimination of interwinding dc voltage stress, yielding an approximate 50% reduction at all dc step ratios. This implies significant savings in magnetics size and weight. Based on a derived mathematical model, a dynamic controller is proposed for the M2dc-CT that regulates dc power transfer while ensuring balanced capacitor voltages. The M2dc-CT operation and dynamic controls are validated through PSCAD/EMTDC simulations and laboratory experiments for a scaled-down 250/85 V, 1.25-kW prototype. Potential applications for the M2dc-CT are identified, which include HVdc-to-MVdc grids interconnects, connection of offshore wind MVdc collector buses to HVdc, HVdc line power tapping, and dc line power flow controllers.

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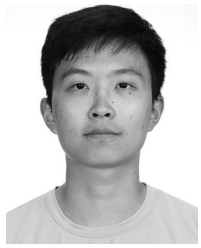

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