Push–Pull Class Φ_2 RF Power Amplifier

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***Abstract*—The Class Φ_2/EF_2 amplifier is an attractive topology for high-voltage and high-frequency power conversion because of the high efficiency, reduced device voltage stress, simplicity of gate driving, and load-independent ZVS operation. Due to many degrees of freedom for tuning, previous studies can only solve the single-ended Φ_2 circuit using numerical methods. This work focuses on improving the design and operating characteristics of a push–pull Φ_2 amplifier with a T network connected between the switch nodes, or a PPT Φ_2 amplifier. The PPT Φ_2 amplifier has less circulating energy and achieves higher cutoff frequency f_T than other Φ_2/EF_2 circuits. We, then, present a series-stacked input configuration to reduce the switch voltage stress and improve the efficiency and power density. A compact 6.78-MHz, 100-V, 300-W prototype converter is demonstrated that uses low-cost Si devices and achieves 96% peak total efficiency and maintains above 94.5% drain efficiency across a wide range of voltage and power. Together with the advances in wide-bandgap semiconductors and magnetic materials, the PPT Φ_2 circuit opens more possibilities for the state-of-the-art performance of solid-state RF amplifiers in high-frequency, high-power applications, including wireless charging for electric vehicles, plasma RF drives, and nuclear magnetic resonance spectroscopy.**

***Index Terms*—Harmonic analysis, power amplifiers, radiofrequency amplifiers, switching converters, soft switching, tuning, zero current switching, zero voltage switching.**

I. Introduction

POWER amplifiers play a critical role in many systems that support our modern infrastructure, ranging from cellphones and radio towers to medical equipment like magnetic resonance imaging and particle accelerator for scientific research purposes. Switched-mode power amplifiers can ideally offer close-to-unity efficiency, which makes them attractive for energy-hungry radio-frequency and microwave applications. By operating the active device as a switch rather than a controlled current source, the overlap between the voltage and current can be mitigated to reduce frequency-dependent switching losses.

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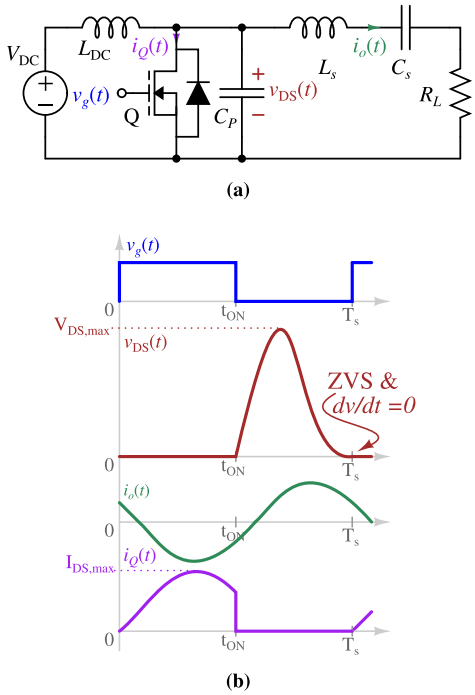

Fig. 1. Class E amplifier with its key waveforms. (a) Schematic. (b) Key waveforms.

The prior art has studied the design of many types of switched-mode power amplifiers. In a Class E amplifier, shown in Fig. 1, the voltage across the active device resonantly rings down to zero before the active device is switched on [1]–[3]. Such zero-voltage switching (ZVS) operation avoids the loss of the energy stored in the parasitic capacitance across the main junction of the active device. Besides ZVS operation in a Class E circuit, the current flowing through the active device is zero when it is switched on, which causes the rate of the voltage change across the parasitic capacitance also to be zero. This is called zero voltage derivative switching (ZVDS) operation.

Despite the high theoretical efficiency, one of the drawbacks of a Class E amplifier is that the peak voltage across the switch equals about 3.6 times the dc input. A Class F amplifier uses multiple-resonator output filters to control the harmonic content of their drain-voltage or drain-current waveforms [4]. Fig. 2 shows a Class F amplifier circuit and its key waveforms. In a voltage-mode Class F amplifier, the impedance across the switch Q is tuned to be open at odd harmonic frequencies except the fundamental and to be short at all of the even harmonic frequencies. With such impedance tuning, the drain voltage in a

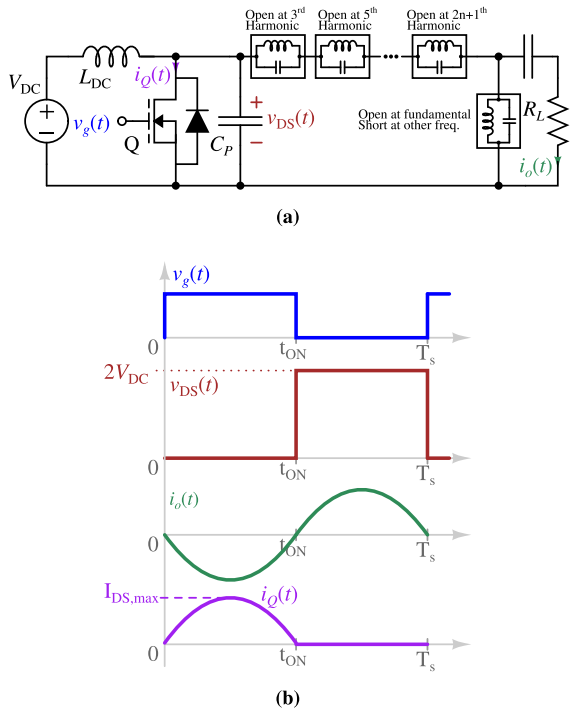

Fig. 2. Class F amplifier with its key waveforms. (a) Schematic. (b) Key waveforms.

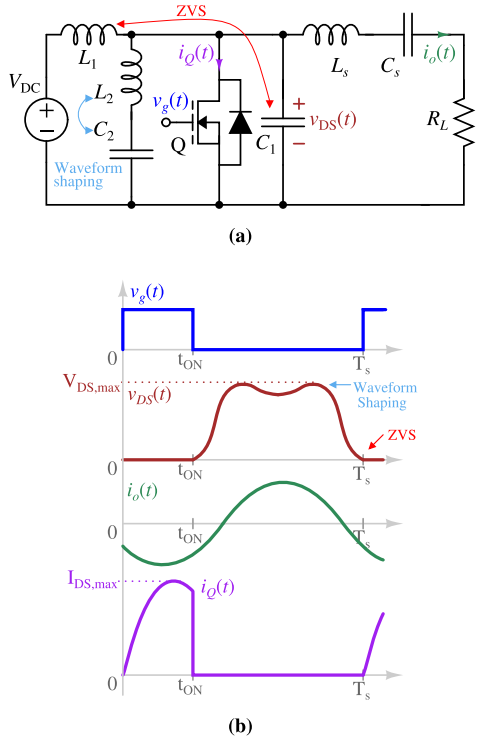

Fig. 3. Class Φ_2 / EF_2 amplifier with its key waveforms. (a) Schematic. (b) Key waveforms.

voltage-mode Class F is a square wave, while the drain current is ideally a half-sine wave. Maximally flat voltage-mode Class F has a peak voltage that is two times the dc input on the switch.

Class F^{-1} is the inverse Class F amplifier and denotes the current-mode Class F operation [5]. The inverse operation of an RF amplifier means that the voltage and current waveforms of the active device are switched. In a Class F^{-1}, the switch current is a square wave, and the voltage is a half-sine wave [6], which requires tuning the impedance across the switch to be short at all the odd harmonic frequencies except the fundamental and to be open at all the even harmonics.

Class F and F^{-1} have more desirable switch waveforms, but the transistor's output capacitance limits the open impedance tuning at high frequencies. Class E has a high peak voltage stress, but incorporates the transistor's output capacitance into the tuning network and achieves ZVS operation. To combine the benefits of Class E and Class F (F^{-1}) operations, Kee *et al.* [7] introduced the Class E/F family of ZVS switching amplifiers. By selectively tuning specific harmonic components in the drain-voltage or drain-current waveforms, a Class EF or E/F amplifier can have a lower peak voltage or current stress than a conventional Class E circuit and still absorb the transistor's output capacitance into the tuning circuit while achieving ZVS. Additionally, this tuning method allows increased tolerance to large transistor output capacitance, improving the high-frequency performance, and extending the frequency range beyond that is achievable with a Class E.

The naming convention of this amplifier family is of the form Class $EF_{n1,n2,n3,...}$ or $E/F_{n1,n2,n3,...}$, where the subscripts indicates the harmonics being tuned. Kee *et al.* [7] explained the generalized method of tuning different harmonics. For instance, Class EF_2 or Φ_2 converter, shown in Fig. 3, is one example of the Class EF family ZVS amplifiers with its second voltage harmonic removed by a resonant short impedance [8]–[10]. The active device in this circuit withstands a peak voltage about 2.2 times the dc input, which makes it attractive for high-voltage and high-power RF amplification. Class Φ inverter, introduced in [11], has fundamentally similar drain waveforms with Class F. The difference is that most Class F amplifiers use a choke input inductor and tune the impedance through the output network [5], while the Class Φ shapes the drain impedance through a quarter-wave transmission line connected at the input. In practice, the quarter-wave transmission line can be approximated by a high-order lumped network to reduce the size, especially at low frequencies. To further reduce the complexity of a high-order lumped network, Rivas *et al.* [8] introduced the Φ_2, which replaces the quarter-wave transmission-line in the Class Φ with a low-order resonant network and mainly focuses on tuning the first three voltage harmonic components while neglecting the others. With proper tuning only on the first, second, and third voltage harmonics, the Φ_2 amplifier can adequately shape a quasi-square wave drain voltage that is similar to the waveform in a Class Φ, F, or D amplifier. This concept is fundamentally similar to Class EF_2 [9], [10], with the primary difference that most work on the Class EF_2 uses a choke input inductor for L_1 in Fig. 3(a), whereas a Φ_2 inverter [8] uses a small-value resonant inductor, which improves the transient response and maximum achievable frequency. A small-value L_1 also enables the Φ_2 to maintain ZVS operation across a wide range of resistive loads. More generally, by using a finite dc-feed inductance L_1, all the

Class E family amplifiers will have a fast transient, and load-independent ZVS operation [12], [13], and these two features are advantageous in many dc–dc applications [14]. The drawback of using a small-value L_1 is that it increases the input current ripple and the filtering capacitance. In contrast, a choke input inductor limits the current ripple but slows the transient response and narrows the ZVS range across power and frequency.

In general, the Φ_2 inverter is an attractive topology for high-voltage and high-frequency power conversion because of the high efficiency, reduced device voltage stress, simplicity of gate driving, and load-independent ZVS operation, and this work focuses on fundamental improvements to this topology that improve both its design and operating characteristics, as described in the following (note that we draw primarily from the tuning method developed for a Φ_2 inverter in [8], so we keep the naming convention of the circuit in Fig. 3(a) as a "Φ_2 amplifier").

Despite significant prior work on modeling the Class EF or E/F family amplifier circuits, there is still no design procedure that gives both simple closed-form design equations and insights of the circuit operation. The fundamental reason is that Class EF or E/F harmonic-tuned amplifier uses a high-order (≥ 4) resonant circuit to simultaneously shape the drain-voltage/drain-current waveform and achieve ZVS operation. As shown in the Φ_2 example of Fig. 3, we rely on separate resonances for different functions: L_1–C_1 for ZVS, and L_2–C_2 for waveform shaping to reduce peak voltage. It is challenging to intuitively solve a fourth-order or higher differential equation that models the circuit's operation.

Previous work [8]–[10] has introduced different tuning methods to select the component values of the multiresonant network in a Φ_2 amplifier. With an assumption of a choke input inductor, [9] derives a numerical algorithm that can calculate circuit parameters in a Class Φ_2 converter. The table provided in [9] is a convenient solution to designing the converter operating at a fixed point. This numerical model, however, provides little insight into circuit operation. Besides, a Φ_2 converter designed following the guidelines in [9] cannot maintain ZVS operation across a wide load range, which causes the efficiency to drop when the load changes. Rather than providing a single set of design equations, Aldhaher *et al.* [10] extended this numerical study and derives multiple solutions to optimize the different performance of a Class Φ_2 circuit, such as maximizing the power-output capability or the operating frequency with ZVS, which provides more design freedom for the readers.

To provide a more intuitive design guideline, Rivas *et al.* [8] described a tuning procedure by looking at the impedance bode plot across the active device. A set of simple equations first provide initial values for the resonant components L_1, L_2, C_2, and C_1. These values are then adjusted to make this multiresonant impedance meet specific empirical rules. For a switched-mode power amplifier, the impedance $Z_{\rm DS}(\omega)$ across the drain and source determines the MOSFET's steady-state time-domain waveform $v_{\rm DS}(t)$ and $i_{\rm DS}(t)$ [4], [6], [7]. The design procedure in [8] gives intuitive and fast response feedback but relies on repetitive tuning and accurate SPICE modeling of the active device's parasitics and passive components during prototyping.

We see first, then, that no scalable, flexible analytical technique exists to design the Class Φ_2, a significant impediment to adoption that we aim to solve in this work. Furthermore, is there a solution that combines the advantages of different types of Φ_2 and improves the performance than achievable with existing design procedures? If such a circuit exists, this "mixed" Φ_2 amplifier should preserve the following features:

1) easy to implement, where the gate-driving signal is ground or dc-level referenced;
2) reduced voltage stress, with the peak switch voltage near two times of $V_{\rm dc}$ or even lower;
3) resistive-load independent ZVS operation;
4) small input current ripple to reduce the filtering requirement.

Here, we show that a **P**ush–**P**ull Φ_2 amplifier structure with a ***T***-network connected between the switch nodes, which we call a **PPT** Φ_2 amplifier, can preserve all the abovementioned features while reducing the circulating energy and improving the achievable drain efficiencies compared to a single-phase Φ_2. Furthermore, we find an analytical design process for the components in a PPT Φ_2 amplifier by exploiting the circuit's symmetry and periodicity and separating the key waveforms into odd and even modes. Later, we propose a series-stacked structure of the PPT Φ_2 amplifier to further reduce the peak switch voltage to $1.1V_{\rm dc}$ instead of $2.2V_{\rm dc}$ and improve the performance.

This article is organized as follows. In Section II, we introduce the PPT Φ_2 amplifier circuit and its operation and design analysis. Section III presents the series-stacked PPT Φ_2 configuration and discusses how this reduces the switch voltage stress and can improve the efficiency compared with a nonstacked case. Section IV compares the PPT Φ_2 amplifier with other ZVS resonant amplifier topologies and discusses the pros and cons of different circuits. Section V demonstrates a design example using the developed analysis and presents the experimental results of the prototype. Finally, Section VI concludes this article.

II. Push–Pull Φ_2 Amplifier With T Network

Fig. 4(a) shows a generalized push–pull Class EF or E/F harmonic-tuned amplifier with a T network connected between the switch nodes. Kee *et al.* [7] first introduced this structure. Using the T-network can separate the effects of the odd and even harmonics tuning in a push–pull Class E/F amplifier. The following is a brief review of how this tuning works.

A push–pull amplifier typically connects the dc input of two identical amplifiers in parallel and the ac load differentially between the switch nodes. By operating the two amplifiers 180° shifted, the dc input current ripples are significantly reduced and shifted to two times the switching frequency [7], [14]–[16]. Fig. 4 shows that a T network consisting of symmetric differential-mode impedance $Z_D/2$ and common-mode conductance Y_C can create different impedance for a push–pull amplifier at odd and even harmonic frequencies [7]. In a push–pull amplifier, the drain-voltage waveforms are shifted by half a switching cycle $0.5T_S$ apart, which can be expressed as

$$v_{\rm DS2}(t) = v_{\rm DS1}\left(\omega_S(t-0.5T_S)\right),\ \omega_S = 2\pi f_S \qquad (1)$$

where f_S is the switching frequency and T_S is the period. If we decompose the voltage waveforms into different harmonic

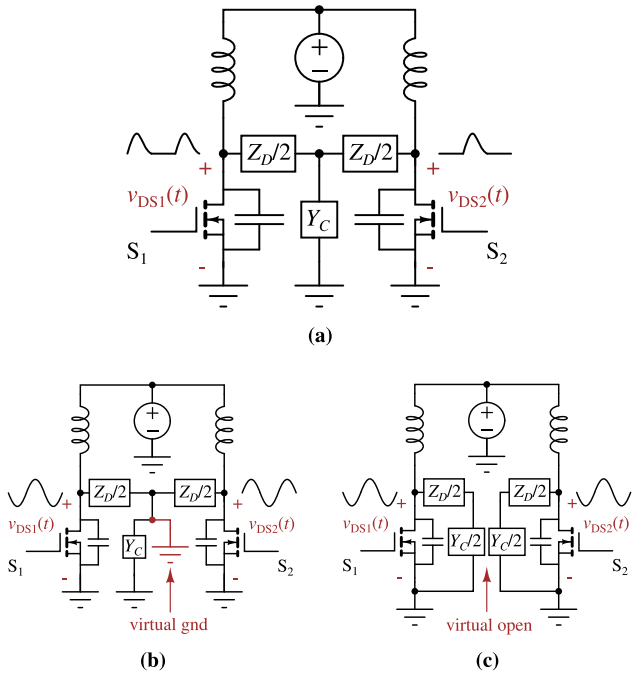

Fig. 4. Push–pull Class EF or E/F harmonic-tuned amplifier with a T network. (a) Actual circuit. (b) Odd-mode equivalent circuit with virtual ground. (c) Even-mode equivalent circuit with virtual open.

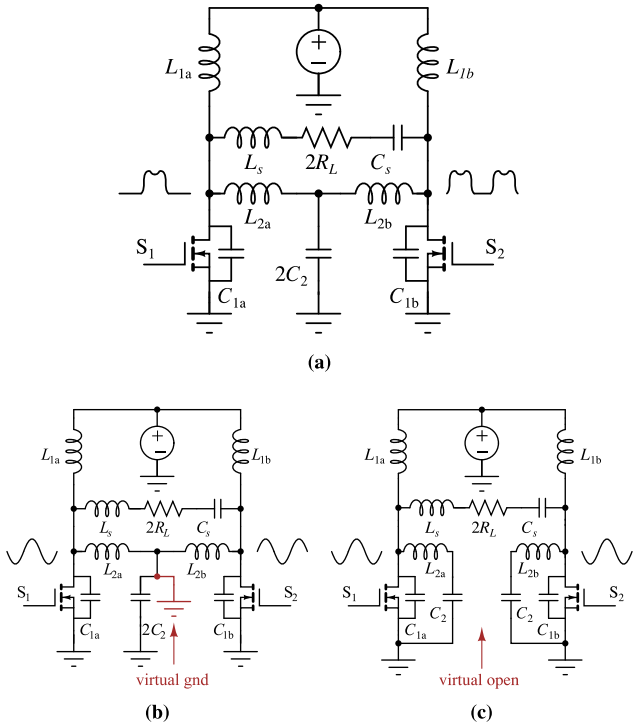

Fig. 5. **P**ush–**P**ull Φ_2 amplifier with **T** network, i.e., PPT Φ_2 amplifier. L_s and C_s resonate at f_S. (a) Actual circuit. (b) Odd-mode equivalent circuit with virtual ground. (c) Even-mode equivalent circuit with virtual open.

components, then

$$v_{\mathrm{DS1}}(t) = V_{\mathrm{dc}} + \sum_{n=1}^{\infty} V_{\mathrm{DS},n}\cos(n\omega_S t - \phi_n) \tag{2}$$

$$v_{\mathrm{DS2}}(t) = V_{\mathrm{dc}} + \sum_{n=1}^{\infty} V_{\mathrm{DS},n}\cos(n\omega_S t - n\pi - \phi_n). \tag{3}$$

This time shift will cause different phase shifts between the harmonic components of $v_{\mathrm{DS1}}(t)$ and $v_{\mathrm{DS2}}(t)$. For the odd harmonics at frequencies of $(2k+1)f_S$, the phase shift is $(2k+1)\pi$ degrees, $k = 0, 1, 2...$, respectively. Due to symmetry, the midpoint between the two drain nodes is clamped to zero potential and a virtual ground for odd harmonics. The effective impedance seen by each MOSFET is only $Z_D/2$ at frequencies of $(2k+1)f_S,\ k = 0, 1, 2\ldots$, as shown in Fig. 4(b).

Conversely, for the even harmonics at each frequency of $2kf_S$, the phase shift between the two drain nodes is $2k\pi$ degrees, $k = 1, 2...$, respectively. Consequently, the even-mode harmonic voltages are always in phase, and the midpoint has the same potential as each drain node. The midpoint becomes a virtual open circuit for even harmonics. Effectively, the common-mode conductance Y_C can be divided into two halves and connected to each side separately, as shown in Fig. 4(c). At even harmonic frequencies of $2f_S,\ k = 1, 2\ldots$, the effective impedance seen by each MOSFET is $Z_D/2$ in series with $Y_C/2$. Therefore, the same T network creates different impedance across the switches' drain nodes at odd and even harmonic frequencies.

Combining the abovementioned idea and the detail tuning procedure for a single-ended Φ_2 inverter [8], Glaser and Rivas [15] first introduced the key concepts of a push–pull Φ_2 amplifier

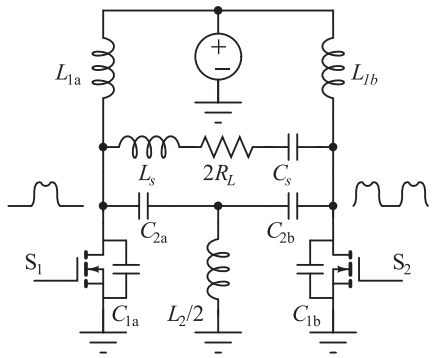

Fig. 6. Alternative PPT Φ_2 amplifier that is suboptimal.

that also utilizes a T network. In this early work, Glaser and Rivas documented two possible implementations of a push–pull Φ_2 [see Figs. 5(a) and 6] and the advantage of using a T network independently to tune the impedance at f_S, $2f_S$, and $3f_S$, but neither a systematic design procedure nor the strengths of each implementations are discussed in [15].

Fig. 5(a) shows the implementation that is the focus of this study. The loading circuit is a series L-R-C circuit connected between the switch nodes. The T-network for tuning consists of two inductors $L_{2a,2b}$[1] and a combined capacitor $2C_2$.[2]

[1]Ideally, the symmetric components X_{na} and X_{nb} in the two phases have the same values of X_n. This holds throughout the article.

[2]Without $2C_2$, the circuit becomes similar to the current-mode Class D [17] or Class E/F$_{\mathrm{odd}}$ [7].

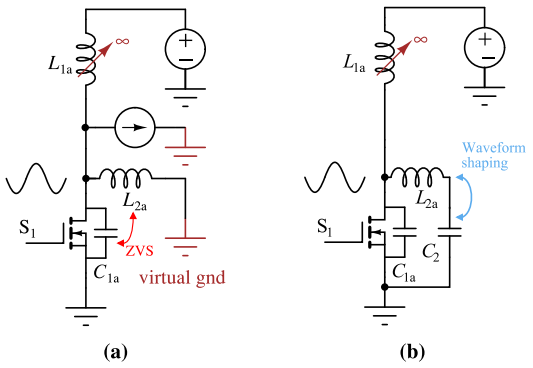

Fig. 7. Equivalent single-ended circuit of a PPT Φ_2 amplifier, (a) for odd harmonic frequencies and (b) for even harmonic frequencies.

Fig. 6 shows the alternative implementation that uses the resonant dual for the T network. Inspired by the work from [6]–[8], [15], the rest of this article will show that the implementation of Fig. 5(a) is fundamentally better than the implementation of Fig. 6 and any other single-phase Φ_2 amplifiers in terms of power and frequency limits, and we move now to the analysis of this circuit.

For convenience, we call the push–pull Φ_2 amplifier with a T-network a "PPT Φ_2 amplifier," referring only to the implementation in Fig. 5(a). Because of symmetry and the interleaved operation, the midpoint between L_{2a} and L_{2a} is a virtual ground for the odd harmonics, as shown in Fig. 5(b), and a virtual open for the even harmonics, as shown in Fig. 5(c).

This midpoint node, which is either a virtual ground or open, creates different effective impedances across the switch depending on the harmonic frequencies. To understand these impedances, we review the single-ended equivalent circuit in Fig. 7, which shows the effective impedance of the T network created by the virtual ground and the virtual open. Assuming the quality factor of the loading circuit is high enough, the load current is an ideal sine wave at the fundamental frequency. At odd harmonic frequencies, e.g., f_S and $3f_S$, with the load modeled as a current source, the impedance seen by each drain node is two parallel inductors $X_{L_2}||X_{L_1}$. At even harmonic frequencies, e.g., $2f_S$, the impedance across a switch is $(X_{L_2}+X_{C_2})||X_{L_1}$. The input inductor L_1 is in parallel connection under both cases, so L_1 can be made arbitrarily large and ignored. Effectively then, the impedance across the switch created by the same T network is a single inductor L_2 at odd harmonics, and an inductor-capacitor series resonant circuit L_2–C_2 at even harmonics.

Such frequency-dependent impedance configuration enables us to shape a quasi-square wave with ZVS for both switches by only tuning the T network in the PPT Φ_2 amplifier. To achieve ZVS of a power MOSFET, the inductive impedance at the fundamental frequency, created by L_2, can generate a phase-lagging current to discharge the shunt capacitance C_1 to zero volts before the MOSFET is turned on [18], [19], where C_1 includes the output capacitance C_{oss} of the power MOSFET. To shape a quasi-square voltage waveform, the even harmonic components (especially the second harmonic) need to be eliminated. A series resonance at $2f_S$ formed by L_2–C_2 can remove the second harmonic voltage component. Therefore, in a critical departure from and an improvement to the single-phase Φ_2 configurations [8]–[10], [13], [14], the two functions (ZVS operation and waveform shaping) can be achieved solely by the resonant components L_2 and C_2 configured in a T network. All of the previously-studied single-phase Φ_2 circuits require at least one extra resonant inductor to achieve ZVS, in addition to the resonant short impedance at $2f_S$ formed by L_2–C_2 for waveform shaping.

With the same analysis, we can justify that the possible implementation in Fig. 6 is suboptimal for a push–pull Φ_2 amplifier. This alternative T network cannot simultaneously achieve ZVS and waveform shaping for the two switches by itself. In fact, at odd harmonic frequencies, this alternative T network in Fig. 6 adds a capacitive impedance $C_{2a,2b}$ in parallel to the drain nodes, which limits the maximum frequency, increases the circulating energy, and degrades the efficiency [7]. This alternative T network can still short the second voltage harmonic if L_2 and C_2 resonate at $2f_S$. However, to achieve ZVS, either the input feed $L_{1a,1b}$ must be small value (more inductive) or the loading tank L_s-$2R_L$-C_s must be tuned to be inductive, both of which increase the circulating energy.

Generally, moving from a single-ended amplifier to this push–pull configuration brings multiple benefits, including reduced input ripple, a potential increase of power density, and in some cases, increased switch performance [5]–[7], [15], [16], [20]. An apparent drawback is the increased number of components, which can increase the cost and complexity of practical implementation. For applications with a ground-referenced load, a push–pull amplifier would require a transformer or balun to convert the differential load to a single-ended one. Beyond these general design tradeoffs between single ended and push–pull, going from a single-phase Φ_2 to the PPT Φ_2 amplifier in Fig. 5(a) will bring some fundamental benefits that are discussed in the following sections in detail:

1) a simpler tuning procedure with analytical solutions;
2) reduced circulating energy, which can increase the frequency, power, or efficiency performance limit under the same constraints;
3) simultaneously low EMI and load-independent ZVS operation.

A. Circuit Analysis and Analytical Solution

The PPT Φ_2 amplifier in Fig. 5(a) enables us to solve for the analytical solutions for the component values in a much-simplified way. In the early work of [7], with Fourier analysis, Kee presents the generalized mathematical formulas of the voltage and current waveforms for any specifically-tuned push–pull Class E/F inverter. However, no closed-form design equation is provided for determining the component values. Because of many degrees of freedom for tuning a single-ended Φ_2 circuit, Kaczmarczyk [9] Aldhaher *et al.* [10] showed that the analytic solutions for the components can only be solved using numerical methods with a certain optimization goal. An important benefit of the PPT Φ_2 amplifier is that we can reduce the degrees of freedom for tuning to only two components' values: C_1, and L_2. This provides the opportunity to solve for the two values straightforwardly.

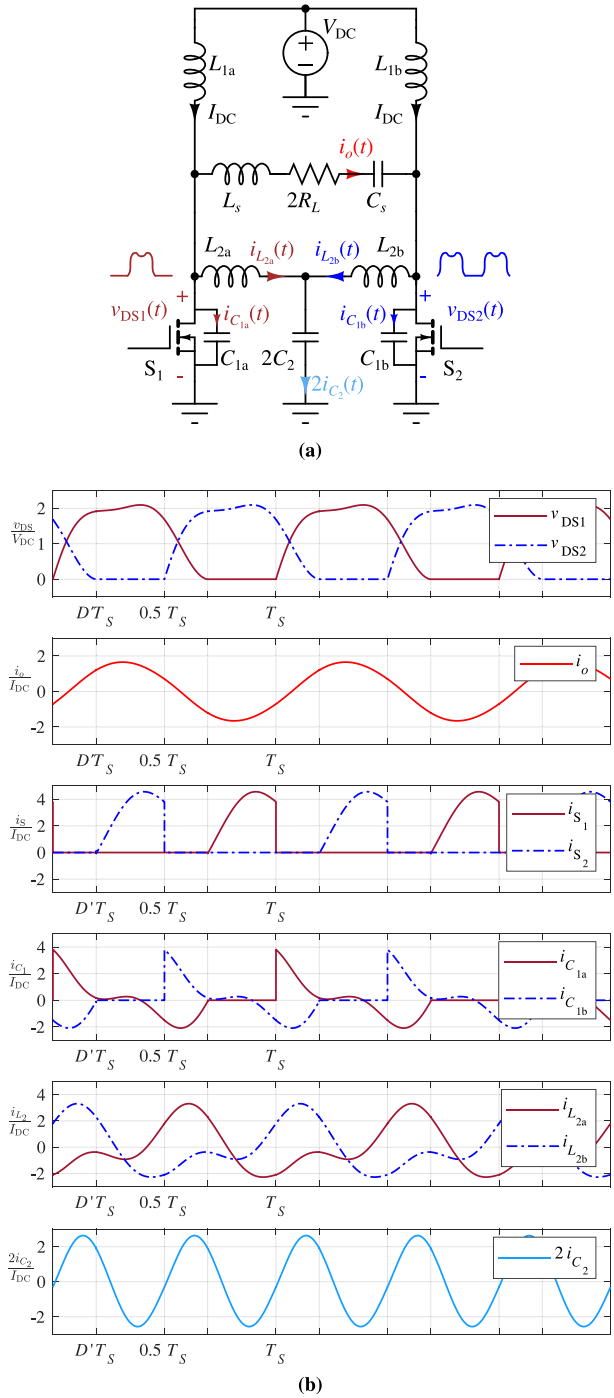

Fig. 8. PPT Φ_2 amplifier with its key waveforms. (a) Schematic with waveform variables labeled. (b) Key waveforms.

To simplify the analysis and provide a different perspective, we utilize the symmetry and periodicity of the circuit and make proper engineering approximations when solving for the values of the resonant components in the PPT Φ_2 converter. Fig. 8 shows the detailed circuit and key voltage and current waveforms. The waveforms shown here are normalized to $V_{\rm dc}$ and $I_{\rm dc}$. Similar to a single-phase Φ_2 circuit, the voltage at each drain node $v_{\rm DS1}(t)$ and $v_{\rm DS2}(t)$ is a quasi-square wave. As discussed previously, we make the input inductors $L_{1a,b}$ dc chokes, so the current flowing through $L_{1a,b}$ are constant dc current. In the loading circuit, L_s and C_s resonate at f_S, and the quality factor of this series resonance is high enough that the load current $i_o(t)$ is an ideal sine wave at f_S. The output voltage of the PPT amplifier is the total voltage across the L-R-C loading circuit.

For the convenience of comparison between single-phase and push–pull configurations, R_L is the required load resistance for a certain power of $P_{\rm dc}$ and input voltage of $V_{\rm dc}$ in a single-phase Φ_2 converter, so $2R_L$ is the total load resistance required for the power of $2P_{\rm dc}$ and voltage of $V_{\rm dc}$ in the push–pull converter. In the T network, the total common-mode capacitance is $2C_2$ and the total current is $2i_{C_2}(t)$. Similar to the voltage, the current flowing through different components in two phases are also shifted by half a switching cycle $0.5T_S$ due to the interleaved operation, as shown in Fig. 8(b)

$$i_{\rm S_2}(t) = i_{\rm S_1}\left(\omega_S(t-0.5T_S)\right) \tag{4}$$

$$i_{C_{\rm 1b}}(t) = i_{C_{\rm 1a}}\left(\omega_S(t-0.5T_S)\right) \tag{5}$$

$$i_{L_{\rm 2b}}(t) = i_{L_{\rm 2a}}\left(\omega_S(t-0.5T_S)\right). \tag{6}$$

The current flowing through the common-mode capacitor has a frequency of $2f_S$.

Due to the frequency-dependent impedance configuration created by the T network, the current in the inductors $L_{\rm 2a}$ and $L_{\rm 2b}$ have both significant odd and even harmonic components. Fig. 9 highlights only the odd-mode waveform and related components of the PPT Φ_2 converter. We define the sum of the odd harmonic frequency components $(f_S, 3f_S, 5f_S\ldots)$ of $i_{L_{\rm 2a}}(t)$ as odd-mode current $i_{\rm odd}(t)$, and the sum of the even harmonic frequency components $(2f_S, 4f_S, 6f_S\ldots)$ as even-mode current $i_{\rm even}(t)$, i.e.,

$$i_{L_{\rm 2a}}(t) = i_{\rm odd}(t) + i_{\rm even}(t). \tag{7}$$

With (6), we have

$$i_{L_{\rm 2b}}(t) = -i_{\rm odd}(t) + i_{\rm even}(t) \tag{8}$$

$$2i_{C_2}(t) = 2i_{\rm even}(t). \tag{9}$$

To shape the quasi-square voltage waveform, L_2 and C_2 resonate and create a short impedance at $2f_S$

$$C_2 = \frac{1}{4\omega_S^2 L_2}. \tag{10}$$

The current flowing through C_2 is dominated by an ideal sine wave at $2f_S$

$$i_{\rm even}(t) = I_2 \sin(2\omega_S t - \phi_2). \tag{11}$$

The output voltage of the PPT amplifier is

$$v_o(t) = v_{\rm DS1}(t) - v_{\rm DS2}(t) \tag{12}$$

a symmetric square wave with resonant rising and falling transitions. The output current $i_o(t)$ is an ideal sine wave in phase with the fundamental component of $v_o(t)$. With an effective square wave driving the inductance $L_{\rm 2a} + L_{\rm 2b}$, a triangular wave $i_{\rm odd}$ is generated, which contains both fundamental f_S and third harmonic $3f_S$ components. For simplicity, we approximate $i_{\rm odd}$ as an ideal sine wave at f_S, with 90° lagging behind i_o because

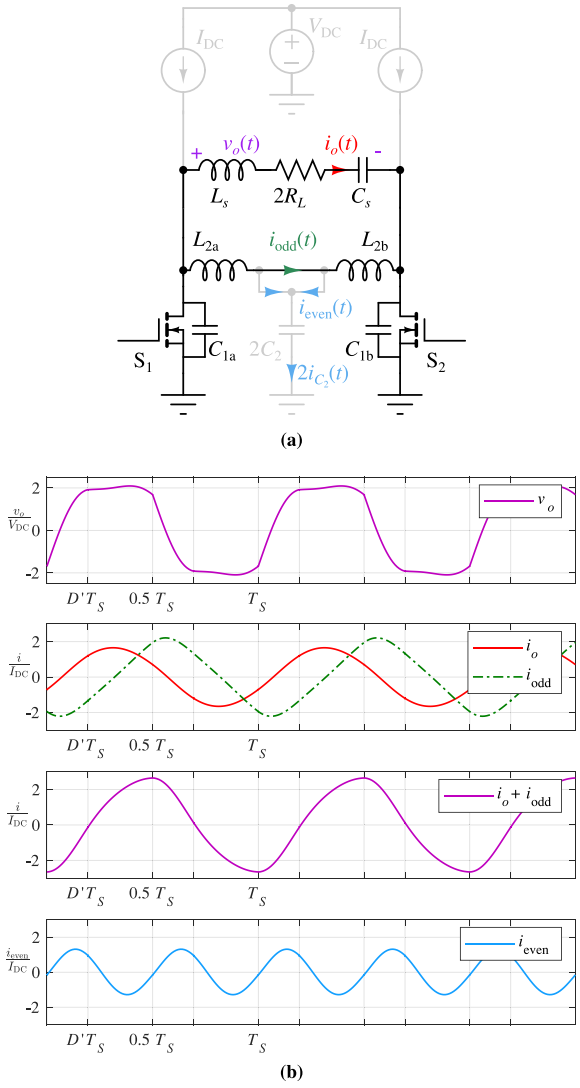

Fig. 9. PPT Φ_2 amplifier with odd-mode components highlighted. (a) Schematic. (b) Odd-mode waveforms.

of the inductive impedance. We can express i_o and i_{odd} as

$$i_o(t) = I_o \sin(\omega_S t - \phi_1) \tag{13}$$

$$i_{\text{odd}}(t) \approx I_{L_2,1} \sin\left(\omega_S t - \phi_1 - \frac{\pi}{2}\right) \tag{14}$$

where I_o and $I_{L_2,1}$ are the amplitudes of the current, and ϕ_1 is the phase of the load current, which is also the phase of the fundamental component of the output voltage. Defining the total differential-mode current i_{diff} to be the sum of i_o and i_{odd}, we find

$$i_{\text{diff}}(t) = i_o(t) + i_{\text{odd}}(t) \approx I_{\text{pk}} \sin(\omega_S t - \phi_1 - \alpha) \tag{15}$$

where

$$I_{\text{pk}} = \sqrt{I_o^2 + I_{L_2,1}^2} \tag{16}$$

$$\cos\alpha = \frac{I_o}{I_{\text{pk}}},\ \sin\alpha = \frac{I_{L_2,1}}{I_{\text{pk}}}. \tag{17}$$

From Fig. 9, we can make some approximations about $v_o(t)$. The peak voltage is constant. The resonant transitions result from the total differential-mode current $i_{\text{diff}}(t)$ driving the capacitor C_{1a} and C_{1b} when both switches are OFF. At the time when $v_o(t)$ reaches positive or negative peak voltage, the derivative of $v_o(t)$ is zero,[3] which means the differential current $i_{\text{diff}}(t)$ is zero.

The gating signal has a duty cycle of D and $D' = 0.5 - D$. From (15), we have

$$i_{\text{diff}}(D'T_S) \approx I_{\text{pk}} \sin(\omega_S D' T_S - \phi_1 - \alpha) = 0. \tag{18}$$

Denoting the zero of the $i_{\text{diff}}(t)$ as φ, we get

$$\varphi = 2D'\pi = \phi_1 + \alpha. \tag{19}$$

The output voltage can be expressed as

$$v_o(t) \approx \begin{cases} \frac{2}{C_1}\int_0^t -i_{\text{diff}}(\tau)\,\mathrm{d}\tau - V_{\text{pk}}, & t \in [0, \frac{\varphi}{\omega_S}) \\ V_{\text{pk}}, & t \in [\frac{\varphi}{\omega_S}, \frac{T_S}{2}) \\ \frac{2}{C_1}\int_{\frac{T_S}{2}}^t -i_{\text{diff}}(\tau)\,\mathrm{d}\tau + V_{\text{pk}}, & t \in [\frac{T_S}{2}, \frac{T_S}{2} + \frac{\varphi}{\omega_S}) \\ -V_{\text{pk}}, & t \in [\frac{T_S}{2} + \frac{\varphi}{\omega_S}, T_S]. \end{cases} \tag{20}$$

C_1 is the capacitance value of C_{1a} and C_{1b}. This approximated voltage is the same as the switch-node voltage in a Class DE inverter [21].

From 0 to $D'T_S$, $v_o(t)$ swings from $-V_{\text{pk}}$ to V_{pk}

$$2V_{\text{pk}} = \frac{2}{C_1}\int_0^{D'T_S} -i_{\text{diff}}(\tau)\,\mathrm{d}\tau. \tag{21}$$

Therefore, we have

$$V_{\text{pk}} = \frac{I_{\text{pk}}}{\omega_S C_1}(1 - \cos\varphi). \tag{22}$$

Substituting (22) into (20), we have

$$v_o(t) \approx \begin{cases} V_{\text{pk}}\frac{2\cos(\omega_S t - \varphi) - 1 - \cos\varphi}{1 - \cos\varphi}, & t \in [0, \frac{\varphi}{\omega_S}) \\ V_{\text{pk}}, & t \in [\frac{\varphi}{\omega_S}, \frac{T_S}{2}) \\ -V_{\text{pk}}\frac{-2\cos(\omega_S t - \varphi) - 1 - \cos\varphi}{1 - \cos\varphi}, & t \in [\frac{T_S}{2}, \frac{T_S}{2} + \frac{\varphi}{\omega_S}) \\ -V_{\text{pk}}, & t \in [\frac{T_S}{2} + \frac{\varphi}{\omega_S}, T_S]. \end{cases} \tag{23}$$

We can calculate the phasor of v_o's fundamental component

$$\begin{aligned} \mathbf{V}_{o,1} &= \frac{\omega_S}{\pi}\int_0^{T_S} v_o(t) e^{-j\omega_S t}\,\mathrm{d}t \\ &\approx \frac{2V_{\text{pk}}}{\pi}\frac{\varphi\cos\varphi - \sin\varphi - j\varphi\sin\varphi}{1 - \cos\varphi}. \end{aligned} \tag{24}$$

The peak voltage on the switch v_{pk} is approximately $2V_{\text{dc}}$ in a Φ_2 circuit [8], [9], so the amplitude of v_o's fundamental component is

$$V_{o,1} \approx \frac{4V_{\text{dc}}\sqrt{(\varphi\cos\varphi - \sin\varphi)^2 + (\varphi\sin\varphi)^2}}{\pi(1 - \cos\varphi)}. \tag{25}$$

[3]For details on this step, see Appendix A.

Similarly, the phasors of load current i_o's and odd-mode current i_{odd}'s fundamental components are

$$\mathbf{I}_o = \frac{\omega_S}{\pi}\int_0^{T_S} i_o(t)e^{-j\omega_S t}\,\mathrm{d}t = I_o e^{-j(\phi_1+\frac{\pi}{2})} \tag{26}$$

$$\mathbf{I}_{\text{odd}} = \frac{\omega_S}{\pi}\int_0^{T_S} i_{\text{odd}}(t)e^{-j\omega_S t}\,\mathrm{d}t \approx I_{L_2,1}e^{-j(\phi_1+\pi)}. \tag{27}$$

By Ohm's Law, between the switch nodes in Fig. 9, we have

$$\mathbf{V}_{o,1} = \mathbf{I}_o * 2R_L = \mathbf{I}_{\text{odd}} * j2\omega_S L_2. \tag{28}$$

From (28), we can get

$$I_o = \frac{V_{o,1}}{2R_L} \tag{29}$$

$$I_{L_2,1} = \frac{V_{o,1}}{2\omega_S L_2} \tag{30}$$

$$\phi_1 = \tan^{-1}\frac{\sin\varphi - \varphi\cos\varphi}{\varphi\sin\varphi}. \tag{31}$$

For a given input voltage V_{dc}, total power $2P_{\text{dc}} = 2V_{\text{dc}}I_{\text{dc}}$, and duty cycle D, and ignoring the losses in the circuit, we can calculate the required load resistance R_L

$$R_L = \frac{V_{o,1}^2}{8P_{\text{dc}}}. \tag{32}$$

With (29) and (30), we can get the values of resonant inductor $L_{2\text{a}}$ and $L_{2\text{b}}$

$$L_2 = \frac{R_L}{\omega_S\tan\alpha}. \tag{33}$$

With (17) and (22), we can calculate the values of $C_{1\text{a}}$ and $C_{1\text{b}}$

$$C_1 = \frac{1-\cos\varphi}{\omega_S R_L\cos\alpha}\times\frac{V_{o,1}}{4V_{\text{dc}}}. \tag{34}$$

The Φ_2 converter circuit is most efficient with minimum peak voltage stress around $2V_{\text{dc}}$ when the duty cycle D is around 0.3–0.35 [8]–[10]. When D is outside of this range, the peak voltage increases significantly. For $D = 0.35$, the key the closed-form design equations are

$$V_{o,1} = 2.43V_{\text{dc}} \tag{35}$$

$$R_L = 0.74\frac{V_{\text{dc}}^2}{P_{\text{dc}}} \tag{36}$$

$$\alpha = 0.13\times 2\pi = 0.8168\ \text{rad} \tag{37}$$

$$L_2 = 0.94\frac{R_L}{\omega_S} \tag{38}$$

$$C_2 = \frac{1}{4\omega_S^2 L_2} \tag{39}$$

$$C_1 = \frac{0.61}{\omega_S R_L}. \tag{40}$$

Note that approximations are made during derivations, i.e., the component values calculated using (36)–(40) do not guarantee a direct ZVDS operation, but generally ensure ZVS operation of the switches S_1 and S_2. We can modify the values of C_1 slightly to achieve ZVDS operation.

From the analysis abovementioned, we know that a larger L_2 will result in a smaller inductive current i_{odd}, which makes achieving ZVS more difficult. In contrast, increasing L_2 reduces the circulating energy and conduction losses. Similarly, smaller C_1 values tend towards ZVS operation at the expense of larger voltage ringing on the switch during the OFF-time.

B. Lower Circulating Energy Than Single-Phase Converters

In a practical implementation, the normalized reactive energies stored in the passive components, i.e., loaded quality factor, play a critical role in determining the efficiency and power density. Going from a single-phase design to the PPT Φ_2 in Fig. 5(a) not only enables solving the component values analytically but also minimizes the total circulating energy in the passive components and improves efficiency.

The loaded quality factor Q_{L,X_n} of each passive component is the peak stored energy normalized to the energy delivered to the load per radian of the cycle. Each passive has its own power loss quality factor Q_{X_n}, which is the peak stored energy normalized to the energy dissipated in this component per radian of the cycle. The loss in each resonant component will be $P_o Q_{L,X_n}/Q_{X_n}$, where P_o is the output power. High loading quality factors Q_{L,X_n}s will cause high power losses or a large volume of the passive components. In any resonant amplifier design, to maximize the energy efficiency, both the switch losses and the passive losses have to be minimized.

Because of the many degrees-of-freedom in tuning a single-phase Φ_2, previous studies using numerical methods [9], [10] set maximizing the switch performance as the primary goal without strictly constraining the circulating energies in the passive components. The numerical algorithms search for a set of ZVS and ZVDS operating points that have the lowest voltage and current stress in the switch, while the loading quality factors Q_{L,X_n}s of the passives are only loosely constrained. The efficiencies of these optimizations could be improved by including the total stored reactive energy in the cost function for the optimization.

A more direct reason why the PPT Φ_2 has lower circulating energy is that the shunt tuning for second harmonic always adds extra capacitance at the fundamental across the switch in a single-phase Φ_2 amplifier. In principle, we can generalize a single-phase Φ_2 amplifier into two categories, depending on whether the load resistance is connected in series or parallel with the inductive reactance. Fig. 10 shows the schematics of the two different types. L_s and C_s resonate at f_S for both cases, so their total effective impedance is zero at f_S. Series types [9], [10] use a choke input inductor L_{dc}, which greatly limits the conductive EMI generated on the dc bus of the system. To achieve ZVS and ZVDS operation on the switch, an inductive impedance L_x is inserted in series with the resistive load. The drawback of using a series-connected inductive impedance is that it limits the load range where ZVS operation can be maintained [13]. The parallel-type Φ_2 [8], [13], [14], uses a small-value input inductor L_1 to

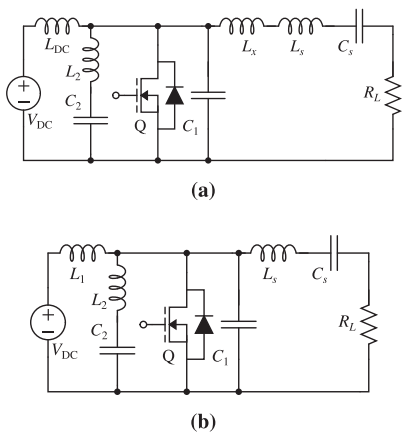

Fig. 10. Different circuit configurations of single-phase Φ_2 amplifiers. L_s and C_s resonate at f_S. (a) Series type [9], [10], $L_{\rm dc}$ is choke inductor, L_x is a small-value inductor. (b) Parallel type [8], [13], [14], L_1 is a small-value inductor.

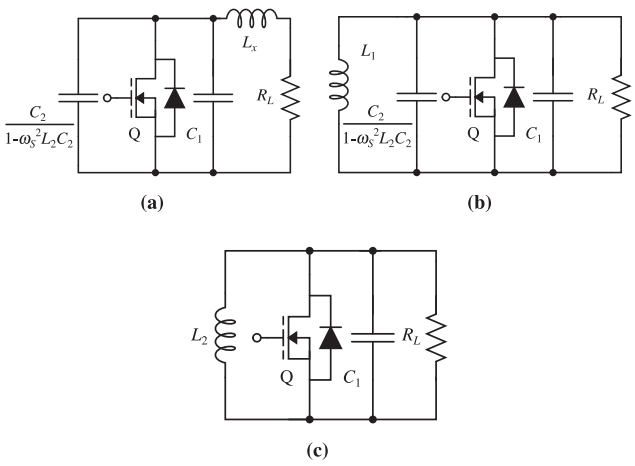

Fig. 11. Equivalent circuit at fundamental frequency of different Φ_2 configurations. (a) Series type, Fig. 10(a). (b) Parallel type, Fig. 10(b). (c) PPT structure, Fig. 5(a).

achieve the inductive impedance at the fundamental frequency and ensure ZVS operation as the load changes. Hence, a parallel type has a faster transient response than the series type and can achieve ZVS operation from a nominal resistive load to an open circuit [13], but has worse input EMI characteristics.

Fig. 11 shows the equivalent circuits at the fundamental frequency of the two single-phase types and PPT Φ_2 converter. In both types of single-phase Φ_2, the impedance of L_2–C_2 at the fundamental frequency is $j\omega_s L_2 - j\frac{1}{\omega_s C_2}$, and it is capacitive. In fact, this extra capacitive impedance also exists for the Class E/F$_3$ [9] or any other single-ended Class EF$_{\rm n}$ or E/F$_{\rm n}$ amplifier [7], as L_2 and C_2 are generally tuned at a harmonic frequency higher than the fundamental. Because of the differential ground at odd harmonics, the PPT Φ_2 does not bear this extra capacitive impedance from the shunt tuning and thereby reduces the circulating energy.

To achieve ZVS operation, a certain amount of inductive circulating energy is required to resonate with the capacitive impedance across the switch at the fundamental. Without changing any components or operating conditions, going from a single ended to a PPT Φ_2 will eliminate the extra effective capacitance across the switch, which gives us many possible directions to retune the amplifier.

First, if the total switch die area is kept constant, we can reduce the required inductive circulating energy because there is less capacitive impedance that needs to be resonantly charged/discharged. The reduced inductive energy can lower the losses and shrink the requisite size of the inductors, which improves the efficiency and power density.

If instead, the conduction loss in the switch is the bottleneck in the single-phase Φ_2 case, we can now use switches with a larger total die area because of the removal of the extra capacitive impedance. A larger die will reduce the ON-resistance of the switches and, therefore, conduction losses, which may increase the efficiency in this case.

Another way of benefiting from the removed capacitive impedance is to tune the converter to work at a higher frequency. With the same waveform tuning, the impedance of each component should be constant independent of the frequency [7]. We can use this principle to estimate the new maximum operating frequency of a PPT Φ_2 circuit.

With L_2 and C_2 resonant at $2f_S$, $1-\omega_S^2 L_2 C_2 = 0.75$. Therefore, the additional effective capacitance from the second harmonic shunt is $1.33C_2$ in a single-phase Φ_2. To keep the capacitive impedance across the switch constant at different frequencies, we have

$$\frac{1}{2\pi f_{\rm T,s}(1.33C_2 + C_1)} = \frac{1}{2\pi f_{\rm T,p} C_1} \tag{41}$$

where $f_{\rm T,s}$ is the maximum operating frequency of the single-phase Φ_2, and $f_{\rm T,p}$ is the maximum operating frequency of the PPT Φ_2. Rearranging, we get

$$f_{\rm T,p} = \frac{1.33C_2 + C_1}{C_1} f_{\rm T,s}. \tag{42}$$

According to [10], the maximum frequency point occurs at $C_1 = 1.57C_2$ (for a given output load and switch capacitance), and substituting this into (42), we see that the PPT Φ_2 extends the maximum operating frequency of the single-phase Φ_2 by 1.85 times.

C. Simultaneously Low EMI and Resistive Load Independent ZVS Operation

Going from a single-phase Φ_2 to the PPT structure not only simplifies the tuning and minimizes the circulating energy, but also enables load-independent ZVS operation. The T-network makes the inductive current $i_{\rm odd}$ in parallel with the load current. With the same input/output voltage, $i_{\rm odd}$ remains constant even when the resistive load R_s varies. This constant parallel inductive current $i_{\rm odd}$ enables the PPT Φ_2 converter to maintain ZVS operation from a nominal resistive load to an open circuit. With careful design, the PPT Φ_2 converter can maintain high efficiency from no load to a given maximum output power. Aldhaher *et al.* [10], Roslaniec *et al.* [13], and Gu *et al.* [14] discussed the conditions of achieving resistive load-independent

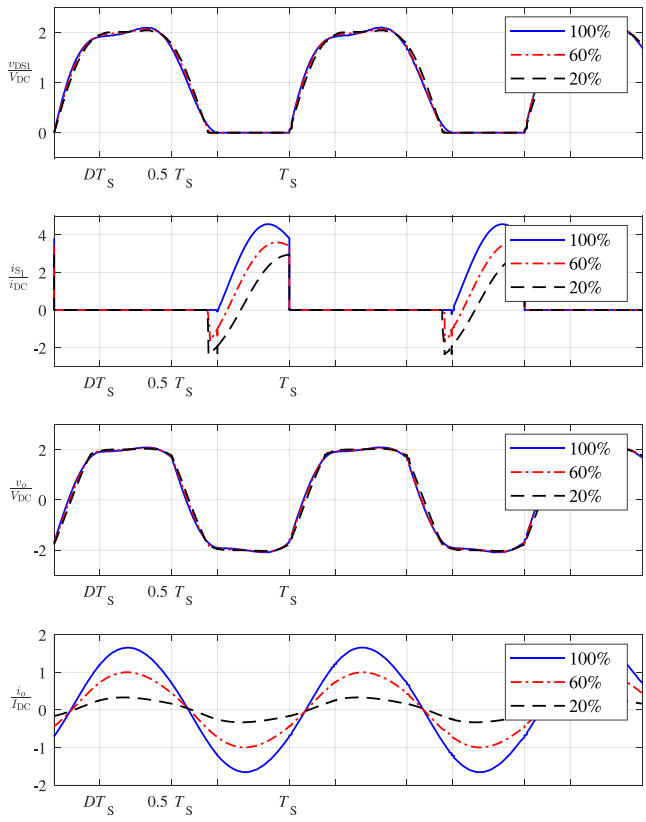

Fig. 12. Simulation waveform of the PPT Φ_2 amplifier under variable resistive load. The output current changes from 20% to 100%.

operation of single-ended Class EF and E/F circuits in more detail.

One drawback brought by the load-independent ZVS design in single-ended Class EF and E/F circuits is the large input ripple, which may increase the conductive EMI on the system's dc bus. The PPT Φ_2 can achieve very low EMI and load-independent ZVS simultaneously because the input still uses choke inductors, and the ripples are canceled [7].

Fig. 12 shows the simulated waveform of the PPT Φ_2 amplifier in LTSPICE. By varying the load resistance, we set the output power to be 100%, 60%, and 20% of the nominal value. Under different power, we can see the drain-to-source voltage $v_{\mathrm{DS1}}(t)$ still maintains ZVS but lose ZVDS operation at light load. As the power decreases, the switch current waveform $i_{\mathrm{S}_1}(t)$ shifts downwards. The loss of ZVDS operation at light load is because the switch current is a negative value instead of zero at the moment of the turn ON. The output voltage $v_o(t)$ is almost constant, while the output current $i_o(t)$ varies from nominal load to 20% of the load.

III. Series-Stacked PPT Φ_2 Amplifier

By actively shaping the voltage waveform through creating a short impedance at $2f_S$, we can reduce the switch voltage stress in a Class Φ_2 amplifier to around $2.1V_{\mathrm{dc}}$, which is much smaller than the $3.6V_{\mathrm{dc}}$ case in a Class E inverter. One way to further

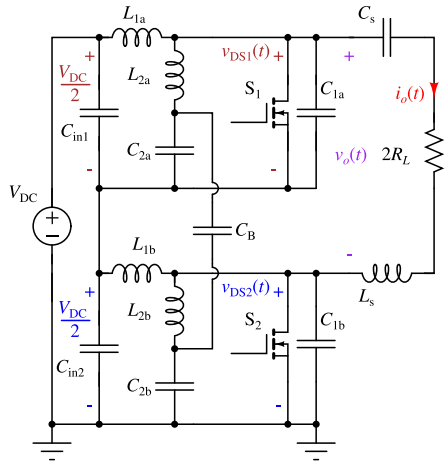

Fig. 13. Input series-stacked PPT Φ_2 amplifier.

reduce this voltage stress is to use a stacked structure, as shown in Fig. 13.

A series-stacked or multilevel structure has been widely applied in switched-capacitor converters and allows the usage of low-voltage-rated semiconductor devices with better performance metrics [22]–[27]. Early work in [28] also showed examples of high-voltage RF amplifiers using a stacked structure for satellite and phased-array applications. In Fig. 13, we construct the equivalent PPT structure using two stacked single-phase Φ_2 amplifiers. C_{in1} and C_{in2} are connected in series, and each capacitor has a dc voltage of $0.5V_{\mathrm{dc}}$. The two phases still operate with interleaving. The dc voltage on C_{in1} and C_{in2} self-balance at $0.5V_{\mathrm{dc}}$ as long as C_{in1} and C_{in2} are large value and have small ac impedance. To achieve the same T-network as the nonstacked case at ac, we insert a dc block capacitor C_{B} between the two shunt tuning legs. C_{B} withstands a dc voltage of $0.5V_{\mathrm{dc}}$ and is effectively a short impedance at high frequency. As C_{in2} is also a short impedance at high frequency, $C_{2\mathrm{a}}$ and $C_{2\mathrm{b}}$ are effectively in parallel at ac. The design analysis presented in Section II also applies to this series-stacked PPT Φ_2 converter, here, provided that the effective input voltage is $0.5V_{\mathrm{dc}}$.

The input series-stacked PPT Φ_2 amplifier in Fig. 13 brings multiple advantages in applications requiring high-voltage and high-frequency RF amplification. First, the peak voltage stress on S_1 and S_2 is reduced to $1.05V_{\mathrm{dc}}$, much smaller than the $2.1V_{\mathrm{dc}}$ in a nonstacked Φ_2 and $3.6V_{\mathrm{dc}}$ in a Class E. With current commercially-available devices, the series-stacked push–pull structure extends the application range of a Φ_2 circuit. Lower voltage stress allows the use of devices with better performance metrics and could reduce the devices' conduction losses. The unit area ON-resistance $R_{\mathrm{on},sp}$ of a high-voltage Si power MOSFET scales roughly with the power of 2.5 of the breakdown voltage V_{BV} [29]

$$R_{\mathrm{on},sp} \propto V_{\mathrm{BV}}^{2.5}. \tag{43}$$

With the power constant and the voltage scaled by half, the conduction losses scales by

$$I^2 R_{\mathrm{on}}|_{2V_{\mathrm{dc}}} \rightarrow 0.7 I^2 R_{\mathrm{on}}|_{V_{\mathrm{dc}}}. \tag{44}$$

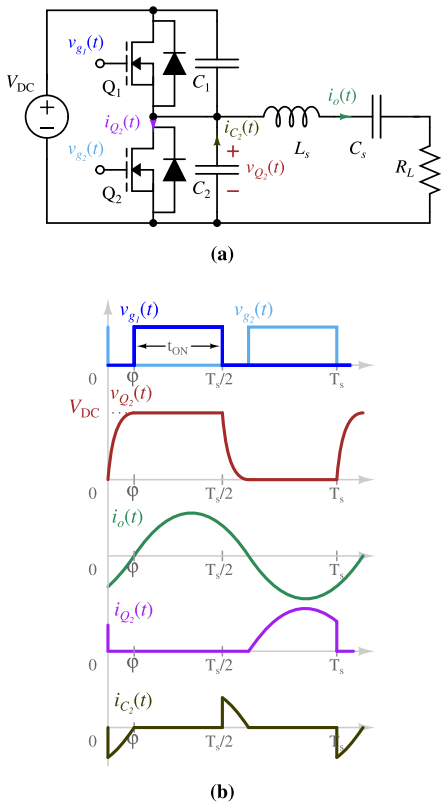

Fig. 14. Class D amplifier with ZVS and ZVDS operation. (a) Schematic. (b) Key waveforms.

With the same device area but half of the voltage stress, conduction losses can be reduced by 30%. Here, we assume the specific output capacitance $C_{\text{oss},sp}$ is independent of V_{BV}, and are providing a first-order estimation of the transistor's loss reduction by using a stacked architecture. Glaser *et al.* [30] systematically analyzed the benefits of a stacked architecture for high-frequency amplifiers when also considering the $C_{\text{oss},sp}$ dependence on V_{BV}.

Second, compared with a half-bridge-based Class D amplifier, the series-stacked PPT Φ_2 converter has the same peak voltage stress. Although this series-stacked PPT Φ_2 converter also uses two switches, the top switch S_1 only needs to be driven by a dc level-shifted gating signal. Fig. 14 shows the circuit and typical waveform of a Class D amplifier with ZVS and ZVDS operation. The top switch Q_1 in the Class D amplifier needs to be driven by a floating signal, which can be challenging to implement under high-voltage, high-frequency conditions. This common-mode requirement often limits the maximum achievable frequency and/or power for Class D amplifiers. Only requiring a dc level-shifted gating signal makes the series-stacked PPT Φ_2 amplifier a more viable design choice for high-voltage, high-frequency RF amplification.

Finally, the series-stacked PPT Φ_2 amplifier has a higher gain from the dc input to the ac output than a Class D amplifier. The series-stacked PPT Φ_2 amplifier has a dc–ac gain of $0.5 \times 2.43 = 1.215$, while a Class D circuit has a maximum dc–ac gain of $2/\pi = 0.64$.

In the nonstacked PPT Φ_2 amplifier of Fig. 5, both because of the interleaving operation and the fact that $L_{1\text{a}}$ and $L_{1\text{b}}$ are choke inductors, the total input current ripple is extremely small. For the series-stacked circuit of Fig. 13, the input current ripple could be nontrivial and depends on the inductance of $L_{1\text{a}}$ and $L_{1\text{b}}$ and the ratio of $C_{\text{in2}}/C_{\text{in1}}$.

When selecting the input inductance in the series-stacked PPT Φ_2 amplifier, if we normalize

$$L_1 = kL_2 \tag{45}$$

where L_1 is the inductance of $L_{1\text{a}}$ and $L_{1\text{b}}$, L_2 is the inductance of $L_{2\text{a}}$ and $L_{2\text{b}}$, and define

$$n = \frac{C_{\text{in2}}}{C_{\text{in1}}} \tag{46}$$

then the input current ripple Δi_{dc} is minimized when[4]

$$n_{\text{opt}} = 2k - \frac{k-2}{k+2}. \tag{47}$$

IV. Comparison of ZVS Resonant Inverters

The selection of amplifier topology can depend on many aspects: design complexity, cost, efficiency, and power density, among others. For many applications, including wireless power transfer and plasma generation, the efficiency performance of the amplifier is a critical metric. The total power losses in a ZVS amplifier consist of the conduction losses in all the components, including inductors, capacitors, and switching devices, and frequency-dependent losses that include the gate driving and turn-OFF losses of the switching devices. Resonant gating techniques can reduce the driving losses [31]–[33]. Under certain voltage and frequency conditions, the resonant charging/discharging process of the switching device's junction capacitor C_{oss} could generate significant power losses [34]–[36].

The transistor utilization factor c_{pmr} of a switching amplifier is the ratio of the output power to the total product of switch's peak voltage stress V_{pk} and rms current $I_{\text{S,rms}}$ [9]

$$c_{\text{pmr}} = \frac{\eta_{\text{D}} V_{\text{dc}} I_{\text{dc,total}}}{N V_{\text{pk}} I_{\text{S,rms}}} \tag{48}$$

where η_{D} is the drain efficiency of the amplifier and N is the number of switches. If switch conduction loss is the dominant loss mechanism, c_{pmr} provides a metric for an amplifier topology's normalized output power capability over the device stress. Assuming the conduction loss in the switches dominates the total power losses and the output power is P_o, the drain efficiency of the amplifier can be calculated as

$$\begin{aligned}\eta_{\text{D}} &= \frac{P_o}{P_o + N I_{\text{S,rms}}^2 R_{\text{on}}(V_{\text{pk}})} \\ &= \frac{1}{1 + \frac{P_o R_{\text{on}}(V_{\text{pk}})}{c_{\text{pmr}}^2 V_{\text{pk}}^2 N}} \\ &\approx 1 - \frac{P_o R_{\text{on}}(V_{\text{pk}})}{c_{\text{pmr}}^2 V_{\text{pk}}^2 N}\end{aligned} \tag{49}$$

[4]For detailed minimization analysis, see Appendix B.

TABLE I
DEVICE STRESS COMPARISON OF ZVS SWITCH-MODE AMPLIFIERS

	v_{pk}	N	$i_{\mathrm{S},rms}$	c_{pmr}
E	3.6	1	1.54	0.18
Φ_2 (EF_2)	2.1	1	1.9	0.25
E/F	3.14	2	0.75	0.21
Push-pull Φ_2	2.1	2	0.95	0.25
Series-stacked PPT Φ_2	1.05	2	1.9	0.25
DE (Duty=0.33)	1	2	1.9	0.26
D (Duty=0.5)	1	2	1.57	0.32

where $R_{\mathrm{on}}(V_{\mathrm{pk}})$ refers to the ON-resistance of the switching device as a function of peak voltage stress V_{pk}.

From (49), we know that to generate the same output power, the circuit with higher c_{pmr} has fewer conduction losses in the switching devices if using the same device technology and area. In other words, the circuit with a higher c_{pmr} can deliver more output power than others if the conduction losses are kept identical, resulting in higher efficiency.

Table I lists the normalized voltage and current stress and c_{pmr} of different ZVS amplifier topologies. v_{pk} is the normalized peak voltage stress to the input voltage V_{dc}, while $i_{\mathrm{S,rms}}$ is the normalized rms current in a single switch to the total input current. c_{pmr} values are calculated assuming 100% drain efficiency η_D. Class E has the lowest normalized output power capability but has the simplest circuit configuration. A single ground-referenced switch makes the Class E easier to drive and suitable for very-high-frequency, low-to-medium voltage (10–150 V) applications, as high-voltage MOSFETs suitable for high-frequency operation are rated mostly up to 650 V. Similarly, the Φ_2 amplifier, either single phase or push–pull, only has a ground-referenced switch(es), but higher output power capability and lower peak voltage stress than the Class E, which makes the Φ_2 a favorable choice for high-frequency, medium-voltage applications (up to 250 V). The 2.1 times normalized voltage stress still limits the usage of Φ_2 in high-voltage applications (>350 V). With lower switch voltage stress, the proposed series-stacked PPT Φ_2 converter extends the application voltage range.

Ideally, with a duty cycle of $D = 0.5$, the Class D has the highest output power capability among the topologies. At high frequencies (>5 MHz), the required dead time, which is the resonant charging/discharging time of the switches' junction capacitance C_{oss}, can become a significant portion of the switching cycle, as shown in Fig. 14(b). With this effective duty cycle D decreasing, the output power capability becomes smaller in a Class D amplifier. Listed in Table I, when the duty cycle $D = 0.33$, the output power capability of a Class D amplifier is almost the same as the series-stacked PPT Φ_2 amplifier in Fig. 13. For low-to-medium frequency applications, Class D can be the most efficient and power-dense solution among all the resonant topologies but suffers from limitations surrounding the isolated, high-dV/dt gate drive for the high-side device. For high-frequency, high-voltage applications, e.g., plasma RF driver, the series-stacked PPT Φ_2 converter combines many of the advantages of all the topologies, including the lowest device voltage stress, simplicity of gate driving, and large dc–ac gain.

TABLE II
KEY SPECIFICATIONS OF THE PROTOTYPE CONVERTER

Specifications	Values
Input voltage V_{DC}	100 V
Frequency f_S	6.78 MHz
Output power P_o	320 W

TABLE III
BILL OF MATERIALS OF THE PROTOTYPE CONVERTER

Device Symbols	Component Description	
S_1, S_2	Infineon BSC160N15NS5 150V Si	
Gate driver	Texas Instruments LM5114	
C_{in1}	0.1μF C0G ceramic	
C_{in2}	1μF C0G ceramic	
C_{B}	0.2μF C0G ceramic	
	Calculated	**Implementation**
$2R_L$	23.2Ω	25Ω, arrays of RP60975R0100JNBK
L_{1a}, L_{1b}	1.53μH	1.46μH, Fair-rite 67 EEQ20/9, 18AWG 4 turns, 0.15mm gap
L_{2a}, L_{2b}	305nH	297nH, Fair-rite 67 EEQ20/9, 12AWG 2 turns, 0.4mm gap
L_s	1μH Q_s=1.85	1.1μH, Fair-rite 67 EEQ20/13, 14AWG 5 turns, 1.2mm gap
C_s	550pF	C0G ceramic, 200V
C_{2a}, C_{2b}	451pF	C0G ceramic, 500V
C_{1a}, C_{1b}	1.16nF	S_1 C_{oss} + 630pF, C0G ceramic, 500V

V. EXPERIMENTAL VERIFICATION

This section demonstrates a design example of the proposed series-stacked PPT Φ_2 amplifier in Fig. 13. A prototype converter is built and experimentally tested here. Table II lists the key design specifications. Following the analysis in Section III with a series-stacked input, the effective input voltage is $0.5V_{\mathrm{dc}}$ (50 V). For the push–pull circuit, the total input power is $2P_{\mathrm{dc}}$. Assuming ideally a 100% dc–ac efficiency, P_{dc} is 160 W. With (36), we can calculate the required load resistance per phase

$$R_L = 0.74 \times \frac{50^2}{160}\ \Omega = 11.6\ \Omega. \tag{50}$$

Most available high-power RF resistors have values of 50 Ω or 100 Ω, so for convenience, we use a total load resistance of 25 Ω instead of 23.2 Ω, as 25 Ω can be implemented by paralleling multiple RF resistors. In this example, we select an input inductor L_1 as 5 times L_2, so C_{in2} should be roughly 9.6 times of C_{in1} using (47). The rest of the components can be calculated using (38)–(40). By selecting a quality factor Q_s of 1.85 in the loading circuit, we can calculate the values of L_s and C_s. Table III lists the calculated values of all the components using equations (36)–(40) and the detailed implementations in the actual prototype.

Fig. 15 shows the photograph of the prototype converter, with Fig. 16 showing a thermal image of the prototype under steady-state operation at full power. The thermal camera used here is FLIR A655sc. The maximum temperature on the MOSFET case is 41.7 °C in thermal steady state, and the average case temperature of the MOSFET is 38 °C.

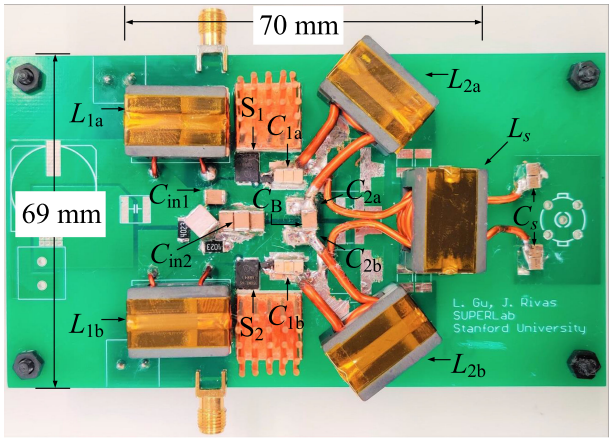

Fig. 15. Prototype series-stacked PPT Φ_2 amplifier.

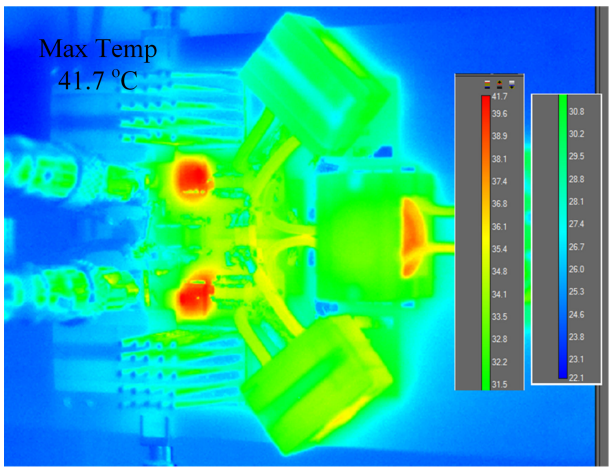

Fig. 16. Thermal photograph of prototype when operating at full power.

Fig. 17 shows the oscilloscope waveform of the drain voltage across the two MOSFETs when we keep the load resistance constant and vary the input voltage. Across the input voltage range 0–100 V, the dc voltage on C_{in1} and C_{in2} is stable at 0.5 V_{dc}, as discussed previously. To help the start-up transient, a surface-mount R2010 resistor is added in parallel to both C_{in1} and C_{in2}. Both resistors are 400 kΩ, so the dc voltage divider ratio is 0.5. At low input voltage (<60 V), S_1 and S_2 only achieve partial ZVS due to the nonlinearity of C_{oss}, where the effective C_{oss} increases with lower applied voltage V_{DS}. At higher voltage ($\geq$ 60 V), S_1 and S_2 achieve full ZVS. Similarly because of this nonlinearity, C_{oss} can become an order of magnitude larger as the bias voltage reaches zero than that biased under high voltage, so S_1 and S_2 can achieve close-to ZVDS operation, as shown in Fig. 17(c) and (d).

Fig. 18 shows the measured efficiency versus dc input voltage of the prototype. The drain efficiency curve is flat and above 96% across the entire input voltage range. With external 630 pF ceramic capacitors parallel to the MOSFET, the nonlinearity of the junction capacitance C_{oss} is mitigated, flattening the drain efficiency curve. This flat efficiency curve benefits applications using amplitude modulation like envelope tracking power amplifiers. Even including the gate driving losses of the Si MOSFETs,

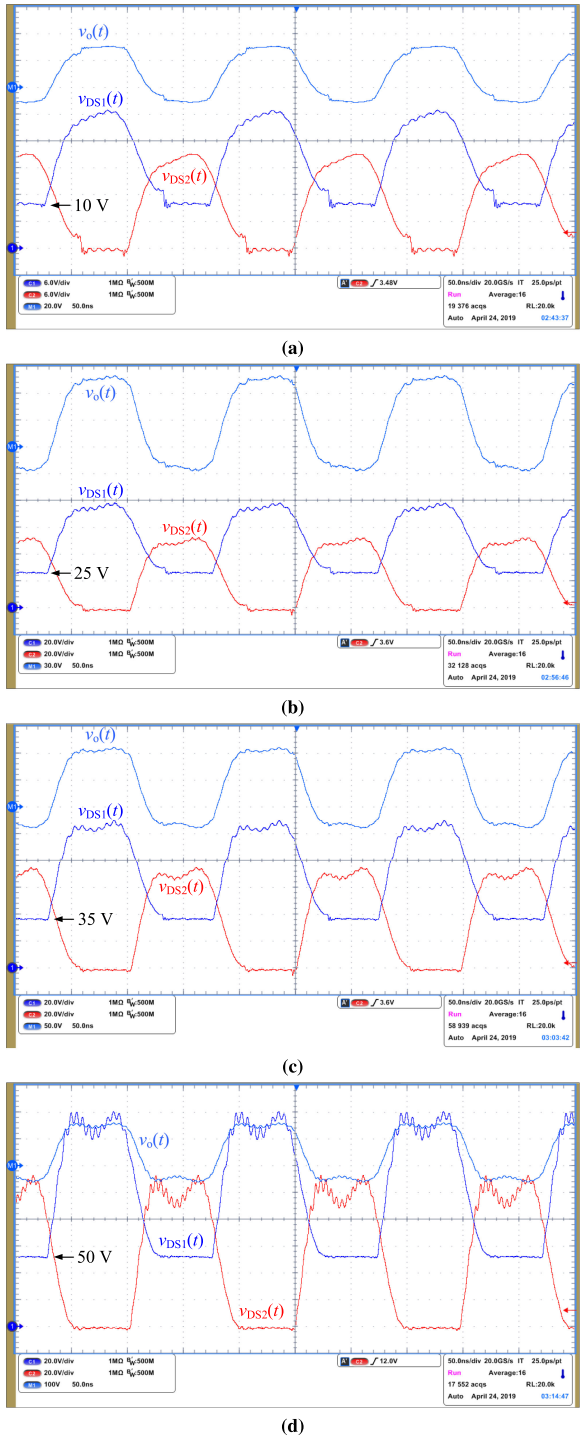

Fig. 17. Series-stacked PPT Φ_2 prototype converter drain-to-source voltage waveform. (a) 20 V_{dc}. (b) 50 V_{dc}. (c) 70 V_{dc}. (d) 100 V_{dc}.

the total efficiency remains above 90% from 30 V_{dc} to 100 V_{dc}, which corresponds to an output power from 25 to 312 W. The peak efficiency of the prototype is 95.7% at 100 V input and 312 W output.

To verify the load-independent operation, we also test the prototype under variable output power. Keeping the input voltage constant at 100 V and varying the load resistance, we test

TABLE IV
PERFORMANCE COMPARISON OF RECENTLY PUBLISHED AND COMMERCIAL WORK ON HF AMPLIFIERS

	This work	[37]	[38]	[10]	[39]	[40]	[41]
Device	150 V Si MOSFET	650 V GaN FET	1.2 kV SiC JFET	100 V Si MOFSET	1.2 kV SiC MOSFET	1.2 kV SiC MOSFET	500 V Si MOSFET
Efficiency	96%	88%	91%	91%	94%	93%	85%
Output Power [W]	312	300	640	23	100	2200	1100
Input Voltage [V]	100	100	200	30	50	440	125
Frequency [MHz]	6.78	6.78	13.56	6.78	6	6.78	7
Topology Class	Series-stacked PPT Φ_2	Push-pull EF_2	E	EF_2	E	Φ_2	$E/F_{2,odd}$

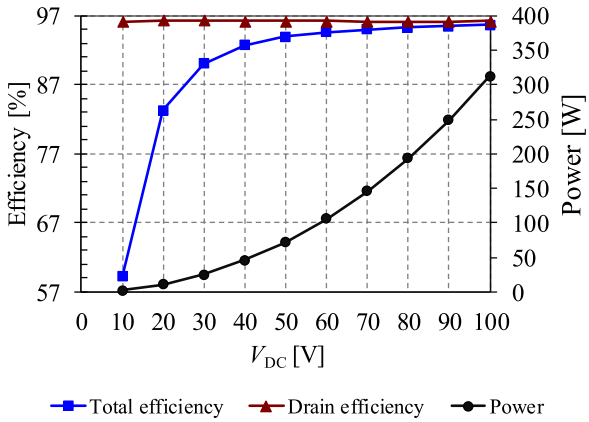

Fig. 18. Prototype's measured efficiency versus input voltage V_{dc}

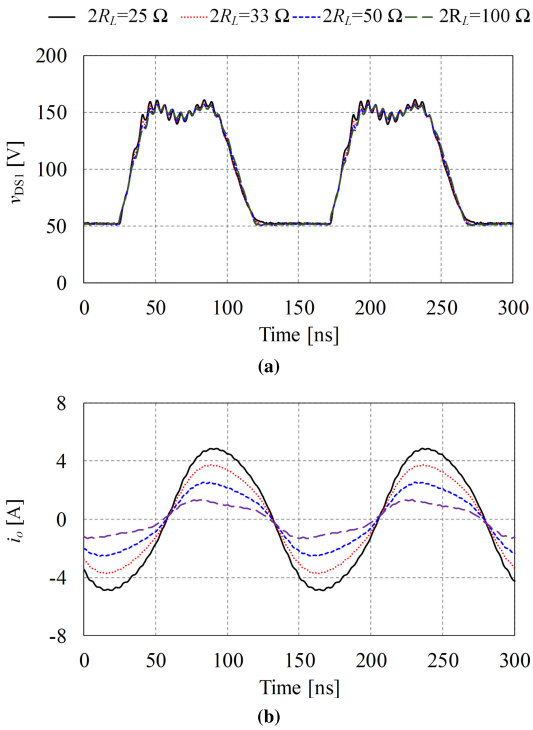

Fig. 19. Measured prototype converter's drain voltage and output current waveforms under variable resistive load. (a) $v_{DS1}(t)$. (b) $i_o(t)$.

the prototype at 25%, 50%, 75%, and 100% power. Fig. 19 shows the oscilloscope waveforms of the drain voltage and output current. The switch voltage $v_{DS1}(t)$ is almost the same

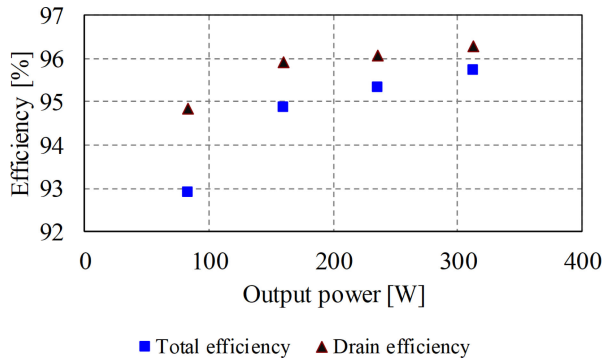

Fig. 20. Prototype converter's efficiency versus output power P_o, V_{dc}=100 V.

and shows ZVS operation, while the load current $i_o(t)$ varies by four times. The measured waveforms Fig. 19 match well with the simulated waveforms of Fig. 12. Fig. 20 shows the efficiency of the prototype under different output powers. Across 25%–100% power range, the drain efficiency remains above 94.5%, and the total efficiency remains above 93%.

The output power is measured using Pearson 2878 current probe, which has a 30 Hz–70 MHz 3 dB bandwidth and a +1/−0% accuracy. An array of RF resistors is used as the variable load, and we use a liquid cooling system to keep the temperature of these loads constant during testing.

To show that the proposed series-stacked PPT Φ_2 converter combines the best advantages of Class EF and E/F circuits, we compare the prototype converter's performance of this work with some recent academic and commercial work on HF Class EF or E/F amplifiers in Table IV. With 1.05 times normalized voltage stress, we are able to use a low-cost 150 V Si MOSFET for an input voltage of 100 V. Generally, in other types of Class EF or E/F family harmonic-tuned amplifiers, semiconductor devices with much higher voltage ratings than the dc input are required. At high frequencies, wide-bandgap (WBG) power semiconductors, e.g., GaN and SiC, are preferred choices due to the low gate driving power. The T network reduces the circulating energy, which makes it easier to design an amplifier with high efficiency using the proposed PPT Φ_2 circuit. Among the listed works, the prototype series-stacked PPT amplifier achieves the highest peak efficiency, even with low-cost Si devices.

VI. CONCLUSION

Class EF and E/F switching amplifiers share the advantages of Class E and F circuits, including simplicity of gate driving and improved switch waveforms, and have a higher output

power capability than a conventional Class E circuit. Among this family of circuits, the push–pull Φ_2/EF$_2$ amplifier with a T network combines these benefits together, achieving low peak switch voltages, low circulating energy, low input current ripple, and load-independent ZVS operation, which are particularly attractive for high-voltage and high-frequency RF applications. Utilizing the circuit's symmetry and periodicity, we find an analytical design process for the components by separating the key waveforms into odd and even modes. This analysis provides more intuition about harmonic-tuned amplifiers than previous analyses solely based on numerical methods. A 6.78-MHz 300-W series-stacked PPT Φ_2 prototype converter is built using low-cost Si devices and tested, and this prototype achieves 96% peak total efficiency with high efficiency across a wide range of voltage and power. Together with the advances in WBG power semiconductors and magnetic materials, the PPT Φ_2 circuit opens more possibilities for the state-of-the-art performance of solid-state RF amplifiers in high-frequency, high-power applications, including wireless charging for electric vehicles, plasma RF drives, and nuclear magnetic resonance spectroscopy.

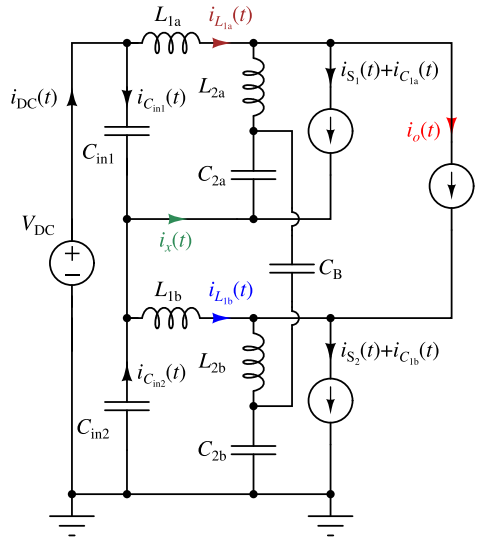

Fig. 21. Simplified series-stacked PPT Φ_2 schematic with current variables labeled.

Appendix A

This appendix shows the process of approximating the derivative of output voltage $v_o(t)$ as zero at the time when it reaches positive or negative peak voltage.

Differentiating both sides of (12), we have

$$\frac{\mathrm{d}v_o(t)}{\mathrm{d}t} = \frac{\mathrm{d}v_{\mathrm{DS1}}(t)}{\mathrm{d}t} - \frac{\mathrm{d}v_{\mathrm{DS2}}(t)}{\mathrm{d}t}. \tag{51}$$

At $t = D'T_S$, we have

$$\left.\frac{\mathrm{d}v_o(t)}{\mathrm{d}t}\right|_{t=D'T_S} = \left.\frac{\mathrm{d}v_{\mathrm{DS1}}(t)}{\mathrm{d}t}\right|_{t=D'T_S} - \left.\frac{\mathrm{d}v_{\mathrm{DS2}}(t)}{\mathrm{d}t}\right|_{t=D'T_S}. \tag{52}$$

Shown in Fig. 8, at $t = D'T_S$, S_2 turns ON with ZVS and ZVDS to minimize switching loss, then we have

$$v_{\mathrm{DS2}}(D'T_S) = 0 \tag{53}$$

$$\begin{aligned}\frac{\mathrm{d}v_{\mathrm{DS2}}(D'T_S)}{\mathrm{d}t} &= \frac{1}{C_1}\left(I_{\mathrm{dc}} + i_o(D'T_S) - i_{L_{2b}}(D'T_S)\right)\\ &= \frac{1}{C_1}\left(I_{\mathrm{dc}} + i_o(D'T_S) + i_{\mathrm{odd}}(D'T_S)\right.\\ &\quad \left. -i_{\mathrm{even}}(D'T_S)\right)\\ &= 0.\end{aligned} \tag{54}$$

Between 0 and $(0.5 + D')T_S$, the voltage on S_1 is

$$\begin{aligned}v_{\mathrm{DS1}}(t) = \frac{1}{C_1}\int_0^t I_{\mathrm{dc}} - i_o(\tau) - i_{L_{2a}}(\tau)\,\mathrm{d}\tau,\\ t \in [0, (0.5 + D')T_S].\end{aligned} \tag{55}$$

To minimize the peak voltage stress on S_1, the ringing on $v_{\mathrm{DS1}}(t)$ should be limited when $t \in [D'T_S, 0.5T_S]$. In other words, the voltage derivative should be small, approximately zero. Hence, we have

$$\begin{aligned}\frac{\mathrm{d}v_{\mathrm{DS1}}(t)}{\mathrm{d}t} &= \frac{1}{C_1}\left(I_{\mathrm{dc}} - i_o(t) - i_{L_{2a}}(t)\right)\\ &= \frac{1}{C_1}\left(I_{\mathrm{dc}} - i_o(t) - i_{\mathrm{odd}}(t) - i_{\mathrm{even}}(t)\right)\\ &\approx 0,\ t \in [D'T_S, 0.5T_S].\end{aligned} \tag{56}$$

A special case is at $t = D'T_S$, the voltage derivative on S_1 is exactly zero

$$\begin{aligned}\left.\frac{\mathrm{d}v_{\mathrm{DS1}}(t)}{\mathrm{d}t}\right|_{t=D'T_S} &= \frac{1}{C_1}\left(I_{\mathrm{dc}} - i_o(D'T_S) - i_{L_{2a}}(D'T_S)\right)\\ &= \frac{1}{C_1}\left(I_{\mathrm{dc}} - i_o(D'T_S) - i_{\mathrm{odd}}(D'T_S)\right.\\ &\quad \left. -i_{\mathrm{even}}(D'T_S)\right)\\ &= 0.\end{aligned} \tag{57}$$

Substituting (54) and (57) into (52), we have

$$\left.\frac{\mathrm{d}v_o(t)}{\mathrm{d}t}\right|_{t=D'T_S} = 0. \tag{58}$$

Together with (15), (54), and (57), we can get

$$I_{\mathrm{dc}} - i_{\mathrm{even}}(D'T_S) = 0 \tag{59}$$

$$i_o(D'T_S) + i_{\mathrm{odd}}(D'T_S) = i_{\mathrm{diff}}(D'T_S) = 0. \tag{60}$$

Equation (60) corresponds to (18).

Therefore, we can approximate that at the time when $v_o(t)$ reaches positive or negative peak voltage, i.e., $t = D'T_S$ or $(0.5 + D')T_S$, the derivative of $v_o(t)$ is zero.

Appendix B

This appendix solves the optimum ratio of stacked capacitors $C_{\mathrm{in2}}/C_{\mathrm{in1}}$ that can minimize the input current ripple Δi_{dc} in the series-stacked PPT Φ_2 amplifier.

Fig. 21 shows a simplified schematic of series-stacked PPT Φ_2 amplifier with all the current variables labeled. From this

figure, we can calculate the input current $i_{\rm dc}(t)$ as

$$i_{\rm dc}(t) = i_{L_{1a}}(t) + i_{C_{\rm in1}}(t). \tag{61}$$

At the midpoint node between $C_{\rm in1}$ and $C_{\rm in2}$, the current flowing through each capacitor depends the capacitance ratio, $n = C_{\rm in2}/C_{\rm in1}$

$$i_{C_{\rm in1}}(t) = \frac{1}{n+1}\left(i_x(t) + i_{L_{1b}}(t)\right). \tag{62}$$

We can further calculate

$$\begin{aligned} i_x(t) &= -i_{C_{2a}}(t) - \left(i_{S_1}(t) + i_{C_{1a}}(t)\right) \\ &= i_{\rm odd}(t) + i_o(t) - i_{L_{1a}}(t). \end{aligned} \tag{63}$$

As $L_1 = kL_2$, we have

$$i_{L_{1a}}(t) = I_{\rm dc} - \frac{i_{\rm odd(t)}}{k} \tag{64}$$

$$i_{L_{1b}}(t) = I_{\rm dc} + \frac{i_{\rm odd(t)}}{k}. \tag{65}$$

Substituting (62)–(65) into (61), we get

$$i_{\rm dc}(t) = I_{\rm dc} + \frac{k+1-n}{k(n+1)} i_{\rm odd}(t) + \frac{1}{n+1} i_o(t). \tag{66}$$

Hence, the input current ripple $\Delta i_{\rm dc}$ is

$$\Delta i_{\rm dc}(t) = \frac{k+1-n}{k(n+1)} i_{\rm odd}(t) + \frac{1}{n+1} i_o(t). \tag{67}$$

As $i_{\rm odd}(t)$ and $i_o(t)$ have similar amplitude I_o but 90° phase shift, the total input current ripple's amplitude is

$$\begin{aligned} \frac{\Delta i_{\rm dc}}{I_o} &= \sqrt{\left(\frac{k+1-n}{k(n+1)}\right)^2 + \left(\frac{1}{n+1}\right)^2}. \\ &= \sqrt{f(n)}. \end{aligned} \tag{68}$$

Solve the derivative of $f(n)$ over n, we have

$$\frac{{\rm d}f(n)}{{\rm d}n} = \frac{(k+2)n - 2\,k^2 - 3k - 2}{k^2(n+1)^4}. \tag{69}$$

With (69), we can calculate the optimum ratio value $n_{\rm opt}$ that minimize $\Delta i_{\rm dc}$ in (47).

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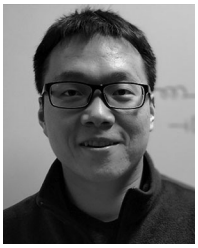

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