Electrothermal Cosimulation for Predicting the Power Loss and Temperature of SiC MOSFET Dies Assembled in a Power Module

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***Abstract*—The electrothermal cosimulation proposed in this paper accurately reproduces the power loss and the temperature of the silicon carbide (SiC) metal–oxide–semiconductor field-effect transistor (MOSFET) dies assembled in a power module comprising a buck converter. The current–voltage characteristic of the body diode embedded in a SiC MOSFET is not like that of an ideal diode because this characteristic depends on the negative gate–source voltage of the transistor. Our device model was, therefore, created to reflect this unique feature and the temperature dependence of the drain current for predicting the power loss of the MOSFET. The simulation uses a look-up table to reduce the computation time. This yields accurate results for the power loss in a buck converter operating at switching frequencies (f_{sw}) ranging from 50 to 350 kHz. The f_{sw}-dependent steady-state temperature of the SiC MOSFET was reproduced well; it ranged from 60 °C to 140 °C. The maximum deviation between the measured and the simulated results was less than 3.0 W and 8 °C, respectively, for the power loss and the temperature of the dies.**

***Index Terms*—Body diode (BD), device modeling, electrothermal cosimulation, metal–oxide–semiconductor field-effect transistor (MOSFET), silicon carbide (SiC).**

I. Introduction

SILICON carbide (SiC) metal–oxide–semiconductor field-effect transistors (MOSFETs) have been attracting considerable attention recently as promising devices in power electronics. Their ON-resistance values are lower than those of Si power devices. SiC MOSFETs have higher breakdown voltages and switching speeds than Si power devices, and they can operate at high temperatures [1], [2]. These properties of SiC MOSFETs make them suitable for use as switching devices in power converters, especially under high-voltage, high-current, and high-temperature conditions.

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However, thermal management is always important for the safety, reliability, and performance of SiC MOSFETs. SiC MOSFETs have high-voltage and high-current tolerance. This means that SiC MOSFETs are often exposed to severe heat stresses, which are partly caused by power loss during their own switching operations. In power modules (PMs) with SiC MOSFET dies, the modules are miniaturized to achieve a device with high-speed switching performance. In these PMs, the heat stress is much worse because the path for heat dissipation is narrow. Experimental approaches to thermal management, however, require multiple rounds of time-consuming prototyping and testing. Therefore, a front-end loading design is required for reliable thermal management. Therefore, electrothermal cosimulation has been intensely researched [3]–[10].

The transient behavior of switching devices in a power converter partly determines its power loss. Hence, device modeling is very important in high-quality electrothermal cosimulation. Several device models of SiC MOSFETs have recently been developed to simulate the switching behavior of the SiC MOSFETs [11]–[17], and some of these models can successfully reproduce the transient characteristics and power losses of SiC MOSFETs. However, these models do not consider the peculiar current–voltage (I–V) characteristic in which the body diode (BD) of a SiC MOSFET depends on the negative gate–source voltage (V_{gs}) of the transistor [18]. In power converters, current flows through the BD at the dead time period if it is used as a freewheeling diode. Hence, the BD generates a power loss, which depends on the forward voltage (V_F) of the BD. In the operation, a negative V_{gs} is commonly applied to the transistor, mainly to avoid a false turn-ON [19]. In this situation, the V_F is significantly affected by the negative V_{gs}; therefore, the V_{gs}-dependent BD model is important for predicting power losses.

There is still room for improvement in the verification of electrothermal cosimulation. Some research papers provide only simulated temperatures without making any comparison with the experimental data; therefore, the validity of these results is not clear [6]–[10]. Other researchers have claimed that the measured and simulated temperatures are in good agreement [3], [4]; however, their predictable temperature range is much lower (up to 60 °C) than the possible junction temperature of semiconductor dies in practical power converters. Practical electrothermal cosimulation must be validated by comparing

the predicted results with the experimental values for the temperature range expected in practical power converters.

In this paper, we describe an accurate electrothermal cosimulation and prove its validity by comparing the simulation results with the experimental values. In Section II, we explain the fundamentals of the electrothermal cosimulation scheme proposed in this paper. This section explains how we improved the model of the SiC MOSFET device that we reported previously [20]. The modified model incorporates a temperature-dependent drain current ($I_{\rm d}$) modeled as a function of the drain–source voltage ($V_{\rm ds}$). The BD was upgraded to reflect the $V_{\rm gs}$-dependent *I–V* characteristics. We then describe how we set up and performed the experiments in Section III. In the experiments, a PM was used with two SiC MOSFETs to validate the simulation results. The PM with a heat sink was used as the half-bridge in the buck converter. The buck converter operates at a switching frequency ($f_{\rm sw}$) ranging from 50 to 350 kHz. The validation of the simulation is discussed in Section IV. We describe how precisely our simulation predicts the power losses and temperatures of the SiC dies ($T_{\rm die}$). The maximum predicted $T_{\rm die}$ is 140 °C. The maximum deviation between the measured and simulated power loss and the $T_{\rm die}$ results was less than 3.0 W and 8 °C, respectively. In Section V, we conclude this paper and summarize the findings of this research.

II. Electrothermal Cosimulation

In the conventional electrothermal cosimulation, the electrical and thermal simulations are connected. Starting with the ambient temperature, the electrical simulation calculates the power loss of the semiconductor dies in the first time step; this power loss is used by the thermal simulation to calculate the temperature of the dies. This temperature is then used by the electrical simulation in the second time step, and so on. In general, however, this very simple cosimulation scheme inevitably requires a large calculation time because for a power converter, the electrical simulation ranges from a few nanoseconds to a few microseconds, whereas the thermal simulation takes up to 10^3 s. Therefore, several methods have been proposed to solve this problem [3]–[10]. Among these methods, we have adopted the look-up table (LUT) method [5] as the basic simulation scheme because it reduces the computation time.

The accuracy of our LUT-based electrothermal cosimulation depends substantially on the LUT quality, which, in turn, depends on the simulated estimates of $P_{\rm die}$ and $T_{\rm die}$ ($P_{\rm die}$ denotes the power loss averaged over one switching cycle). The accuracy of the estimated $P_{\rm die}$ is positively correlated with how well the model of a transistor die reproduces its actual behavior. Here, the transistor die used for the experiments was a SiC MOSFET. The structure of our device model is explained in Section II-A. The thermal network model gives a highly accurate estimate of $T_{\rm die}$. The details of this model are described in Section II-B. Finally, in Section II-C, we describe the fundamental process to predict $P_{\rm die}$ and $T_{\rm die}$ by using LUT-based electrothermal cosimulation.

A. Device Model

The basic device model of the SiC MOSFET die used here is the one that we reported in [20]; however, we had some issues on the BD and on the $I_{\rm d}$–$V_{\rm ds}$ relation. In [20], the model did not fully consider the characteristic of the BD. Nevertheless, the power loss in the BD is not negligible in practical power converters because the load current flows thorough the BD of a SiC MOSFET during the OFF state of the transistor. As mentioned in Section I, however, the BD has negative $V_{\rm gs}$-dependent *I–V* characteristics, whereas a negative $V_{\rm gs}$ is commonly applied to a SiC MOSFET during its OFF state; this is done mainly to avoid a false turn-ON. Therefore, an accurate $V_{\rm gs}$-dependent model of the BD is necessary for simulating $P_{\rm die}$.

TABLE I
SYMBOLS USED IN THE BD MODEL EQUATION

Symbol	Meaning
$I_{\rm F}^{\rm BD}$	Forward current of the BD, which is equal to $I_{\rm d}$ flowing from the source to the drain of the transistor
$I_{\rm sat}$	Saturation current
$V_{\rm FD}$	Threshold parameter for $I_{\rm F}^{\rm BD}$
α	Base of the exponential function
β, γ	Scaling factors for $V_{\rm gs}$ dependency of $I_{\rm F}^{\rm BD}$
n	Emission coefficient
k	Boltzmann's constant

The BD model proposed here is

$$I_{\rm F}^{\rm BD}\left(V_{\rm ds},\ V_{\rm gs}\right) = I_{\rm sat}\left\{\alpha^{\left(\frac{q(-V_{\rm ds}+V_{\rm FD})+\beta\tanh\left(\gamma V_{\rm gs}\right)}{nkT}\right)}-1\right\}. \tag{1}$$

The symbols in (1) are summarized in Table I.

The parameters $V_{\rm FD}$, α, β, and γ are empirical. To reproduce the temperature dependence of the *I–V* characteristics, the parameters $I_{\rm sat}$, n, $V_{\rm FD}$, β, and γ are assumed to change linearly with temperature

$$I_{\rm sat} = \boldsymbol{I_{sat0}}\left(1+\boldsymbol{K_{Isat}}\Delta T\right) \tag{2}$$

$$n = \boldsymbol{n_0}\left(1+\boldsymbol{K_n}\Delta T\right) \tag{3}$$

$$V_{\rm FD} = \boldsymbol{V_{FD0}}\left(1+\boldsymbol{K_{VFD}}\Delta T\right) \tag{4}$$

$$\beta = \boldsymbol{\beta_0}\left(1+\boldsymbol{K_\beta}\Delta T\right) \tag{5}$$

$$\gamma = \boldsymbol{\gamma_0}\left(1+\boldsymbol{K_\gamma}\Delta T\right) \tag{6}$$

$$\Delta T \equiv T_{\rm die} - T_a. \tag{7}$$

Here, the additional subscript 0 is for the ambient temperature; $\boldsymbol{K_{Isat}}$, $\boldsymbol{K_n}$, $\boldsymbol{K_{VFD}}$, $\boldsymbol{K_\beta}$, and $\boldsymbol{K_\gamma}$ are the coefficients for the temperature dependence. T_a is the ambient temperature.

In order to model the BD, we used a commercially available parameter extraction tool (IC-CAP; Keysight Technologies). The measured *I–V* data were fed into IC-CAP, and the simulated data were fitted to the measured data for parameter extraction. The fitting was performed with the nonlinear least-squares-fit algorithm in IC-CAP until the root-mean-squared (rms) error was less than 10%.

Fig. 1 shows the experimental and modeled $I_{\rm d}$–$V_{\rm ds}$ curves of the BD for $T_{\rm die}$ = 25 °C and 150 °C. $V_{\rm gs}$ was varied from −5 to 0 V in steps of 1.0 V. The extracted model parameters are shown in Table II. As clearly shown in this figure, the model reproduces well the negative $V_{\rm gs}$-dependent *I–V* characteristics, especially for high current and large negative $V_{\rm gs}$.

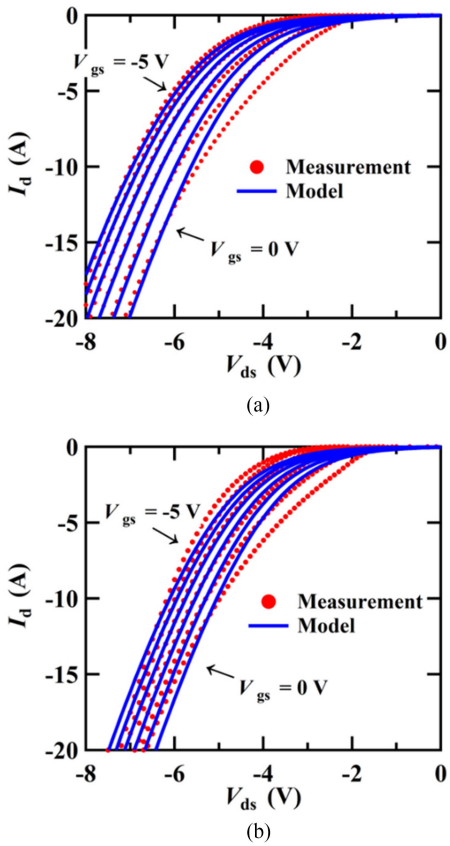


Fig. 1. Experimental and simulated $I_{\rm d}$–$V_{\rm ds}$ curves for the BD. The dots and solid lines denote the experimental and simulated $I_{\rm d}$–$V_{\rm ds}$ curves, respectively. $V_{\rm gs}$ was varied from −5 to 0 V in steps of 1.0 V. (a) $T_{\rm die} = 25$ °C. (b) $T_{\rm die} = 150$ °C.

TABLE II
EXTRACTED PARAMETERS OF THE BD MODEL

Symbol	Value
$V_{\rm FD0}$	0.458 V
$I_{\rm sat0}$	9.76×10^{-5} A
n_0	0.382
α_0	2.11
β_0	1.48 eV
γ_0	0.216 V^{-1}
$K_{\rm Isat}$	1.00×10^{-6} K^{-1}
$K_{\rm n}$	1.00×10^{-6} K^{-1}
$K_{\rm VFD}$	-5.48×10^{-3} K^{-1}
K_β	-5.48×10^{-3} K^{-1}
K_γ	7.23×10^{-3} K^{-1}

The current equation of the transistor was modified to improve the temperature dependence of its $I_{\rm d}$–$V_{\rm ds}$ relation. We introduced temperature-dependent parameters into the original $I_{\rm d}$–$V_{\rm ds}$ equations reported in [20]. The parameters A and D in [20] are also used here, but these parameters were fixed and independent of the temperature in the original version of the model. These original stationary parameters are replaced by temperature-dependent parameters as follows:

$$A_T = A(1 + \boldsymbol{K_{A1}}(1 + \tanh(\boldsymbol{K_{A2}} + \boldsymbol{K_{A3}} V_{\rm ds}))\Delta T) \quad (8)$$

$$D_T = D(1 + \boldsymbol{K_{D1}} \tanh(\boldsymbol{K_{D2}} \Delta T)) \quad (9)$$

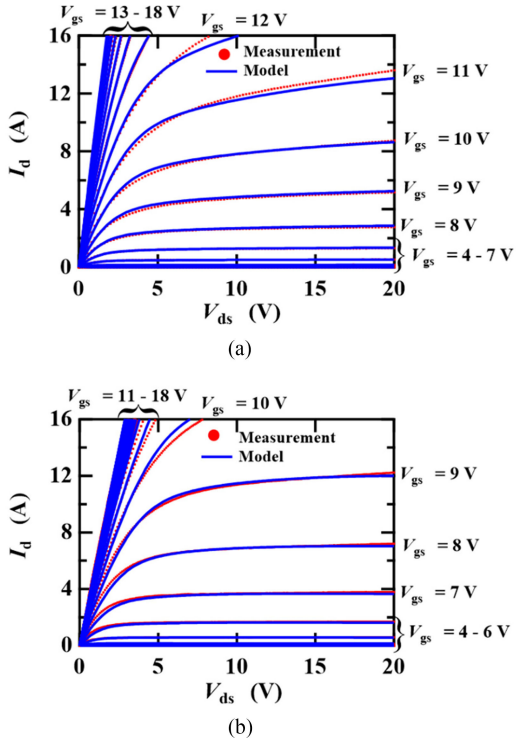


Fig. 2. Experimental and modeled results of $I_{\rm d}$–$V_{\rm ds}$ characteristics. The dots and lines denote the experimental and modeled $I_{\rm d}$–$V_{\rm ds}$ curves, respectively, of the SiC die for $V_{\rm gs} = 4$–18 V in steps of 1.0 V. (a) $T_{\rm die} = 25$ °C. (b) $T_{\rm die} = 150$ °C.

TABLE III
EXTRACTED PARAMETERS OF THE TEMPERATURE DEPENDENCE OF $I_{\rm d}$–$V_{\rm ds}$ CHARACTERISTIC

Symbol	Value
$K_{\rm A1}$	5.50 K^{-1}
$K_{\rm A2}$	0.317
$K_{\rm A3}$	-1.48×10^{-2} V^{-1}
$K_{\rm D1}$	−31.8
$K_{\rm D2}$	1.00×10^{-2} K^{-1}

where $\boldsymbol{K_{A1}}$, $\boldsymbol{K_{A2}}$, $\boldsymbol{K_{A3}}$, $\boldsymbol{K_{D1}}$, and $\boldsymbol{K_{D2}}$ are the coefficients for temperature dependence. For modeling the temperature dependence of the $I_{\rm d}$–$V_{\rm ds}$ characteristic, we used IC-CAP in the same way as when modeling the BD. Fig. 2 shows the experimental and modeled $I_{\rm d}$–$V_{\rm ds}$ characteristics at $T_{\rm die} = 25$ °C and 150 °C with the $V_{\rm gs}$ values varying from 4 to 18 V in steps of 1.0 V. The extracted model parameters are shown in Table III. The modified transistor model follows well the temperature dependence of the $I_{\rm d}$–$V_{\rm ds}$ characteristics of the SiC MOSFET.

B. Thermal Network Model

The PM was used with a heat sink in the validation experiments. The details are given in Section III. We created the thermal network model based on the cross-sectional diagram shown in Fig. 3. The PM was assumed to have five thermal impedances—$Z_{\rm th(1,1)}$, $Z_{\rm th(2,2)}$, $Z_{\rm th(1,2)}$, $Z_{\rm th(2,1)}$, and $Z_{\rm th\_hs}$ (see Fig. 3). $Z_{\rm th(1,1)}$ and $Z_{\rm th(2,2)}$ denote the thermal impedances of the self-heating flow paths for each die. Here, self-heating means that the temperature rise is caused by the die's own

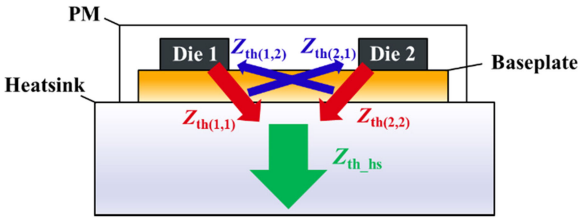


Fig. 3. Schematic cross section of the PM, including dies with a heat sink. The arrows express the heating flow paths. $Z_{\mathrm{th}(1,1)}$ and $Z_{\mathrm{th}(2,2)}$ are the thermal impedances of the self-heating for each die. $Z_{\mathrm{th}(1,2)}$ and $Z_{\mathrm{th}(2,1)}$ are the thermal impedances of cross heating between the dies. $Z_{\mathrm{th\cdot hs}}$ is the thermal impedance of the heat sink.

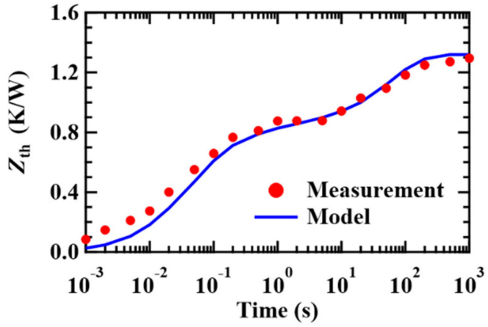
TABLE IV
PROPERTIES OF THE MATERIALS USED IN THE FE MODEL

	Thermal conductivity ($\mathrm{W\,m^{-1}\,K^{-1}}$)	Specific heat ($\mathrm{J\,K^{-1}\,kg^{-1}}$)	Density ($\mathrm{g\,cm^{-3}}$)
SiC	370	690	3.21
Solder	64	220	7.40
Al	237	880	2.69
Cu	402	385	8.96
SiN	58	600	3.50
Thermal grease	4.5	2200	2.50

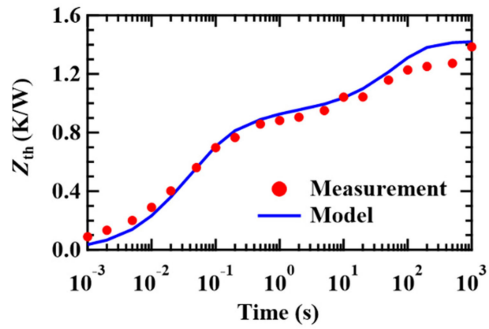
power loss. $Z_{\mathrm{th}(1,2)}$ and $Z_{\mathrm{th}(2,1)}$ denote the thermal impedances of the cross-heating flow paths between the dies. Here, cross heating means that the temperature rise in one die is caused by the power loss in the other die. This cross heating was not negligible because the dies were closely arranged in the PM. $Z_{\mathrm{th\_hs}}$ denotes the thermal impedance of the heat sink. We modeled these thermal impedances using the scheme reported in [6]. A finite-element (FE) simulator (Femtet; Murata Software) was used for the transient thermal analysis of the FE model of the PM. Table IV shows the properties of the materials that were used in the FE simulation of the PM.

In order to improve the accuracy of the FE simulation, we calibrated the heat transfer coefficient of the heat sink using experimentally measured thermal impedances of the PM. Calibration was performed by adjusting the heat transfer coefficient until the rms error between the measured and the simulated thermal impedances was less than 10%.

Fig. 4 shows the measured and simulated thermal impedances of the high-side (HS) and low-side (LS) dies in the PM. The calibrated heat transfer coefficient of the heat sink was 800 $\mathrm{W{\cdot}m^{-2}{\cdot}K^{-1}}$. As clearly shown in this figure, the FE simulation accurately reproduces the measurement results. Then, using the FE simulation model, we obtained $Z_{\mathrm{th}(1,1)}$, $Z_{\mathrm{th}(2,2)}$, $Z_{\mathrm{th}(1,2)}$, $Z_{\mathrm{th}(2,1)}$, and $Z_{\mathrm{th\_hs}}$. The process to extract $Z_{\mathrm{th}(1,1)}$, $Z_{\mathrm{th}(2,2)}$, $Z_{\mathrm{th}(1,2)}$, $Z_{\mathrm{th}(2,1)}$, and $Z_{\mathrm{th\cdot hs}}$ from these FE simulation results is as follows. $Z_{\mathrm{th}(1,1)}$ was obtained by simulating the transient temperature difference ($\Delta T_{\mathrm{trans}}$) between die 1 and the bottom of the baseplate, shown in Fig. 3, for the 1-W power loss of die 1. $Z_{\mathrm{th}(2,1)}$ was obtained similarly with only one difference that $\Delta T_{\mathrm{trans}}$ came from die 2. The process was the same for $Z_{\mathrm{th}(1,2)}$ and $Z_{\mathrm{th}(2,2)}$, but the power loss was generated by die 2. We obtained $Z_{\mathrm{th\_hs}}$ by simulating $\Delta T_{\mathrm{trans}}$ between the top and bottom of the heat sink for 1-W loss of die 1 or die 2. Every thermal impedance was modeled using four-level



(a)



(b)

Fig. 4. Measured and simulated thermal impedances of the HS and LS dies in the PM. The dots and lines denote the experimental and simulated Z_{th}, respectively. (a) HS SiC MOSFET die. (b) LS SiC MOSFET die. The simulated data were obtained from the transient thermal simulation. The calibrated heat transfer coefficient of the heat sink was 800 $\mathrm{W{\cdot}m^{-2}{\cdot}K^{-1}}$.

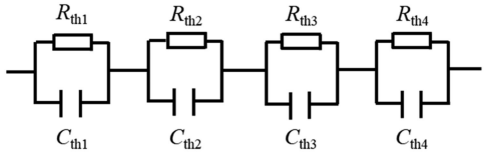


Fig. 5. Four-level Foster thermal network. This model comprises four pairs of a thermal resistance and capacitance. $R_{\mathrm{th}i}$ and $C_{\mathrm{th}i}$ denote a thermal resistance and capacitance, respectively ($i = 1$–4).

Foster thermal networks, as shown in Fig. 5 [7]. Fig. 6 shows the modeled results for each thermal impedance using four-level Foster thermal networks.

C. Electrothermal Cosimulation Based on the LUT Method

LUT was calculated by using the electrical simulation based on the device model described above for several specific temperatures. Electrothermal cosimulation was performed using the following equations:

$$\begin{bmatrix} T_{\mathrm{die}(1)}(t) \\ T_{\mathrm{die}(2)}(t) \end{bmatrix} = \begin{bmatrix} Z_{\mathrm{th}(1,1)} & Z_{\mathrm{th}(1,2)} \\ Z_{\mathrm{th}(2,1)} & Z_{\mathrm{th}(2,2)} \end{bmatrix} \begin{bmatrix} P_{\mathrm{die}(1)}(t) \\ P_{\mathrm{die}(2)}(t) \end{bmatrix} + Z_{\mathrm{th\_hs}} \begin{bmatrix} P_{\mathrm{die}(1)}(t) + P_{\mathrm{die}(2)}(t) \\ P_{\mathrm{die}(1)}(t) + P_{\mathrm{die}(2)}(t) \end{bmatrix} + \begin{bmatrix} T_a \\ T_a \end{bmatrix} \tag{10}$$

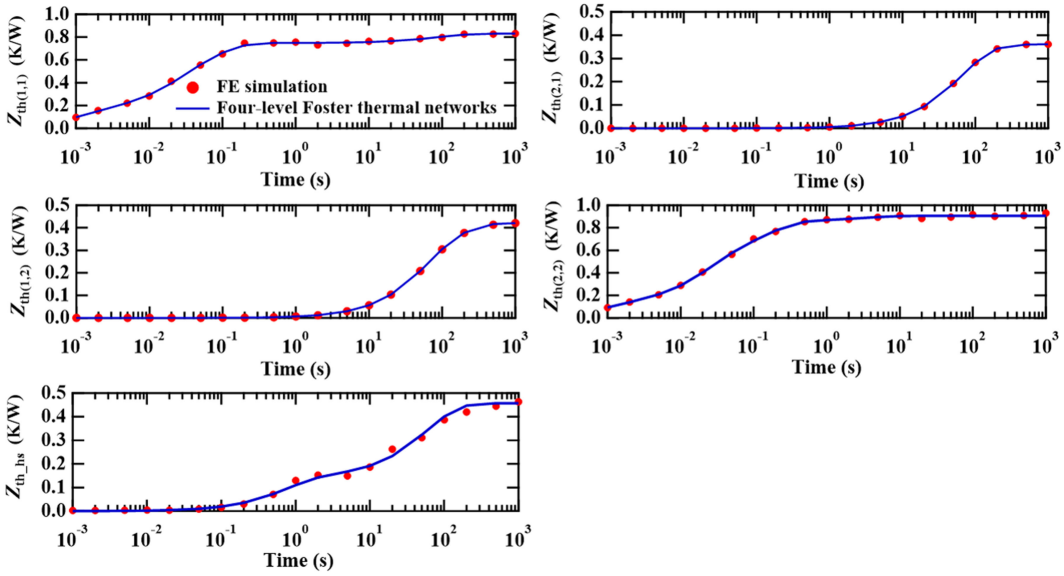


Fig. 6. Modeled results for each thermal impedance using four-level Foster thermal networks. The dots are the FE simulation results, and the lines are the modeled results using four-level Foster thermal networks.

$$\begin{bmatrix} P_{\mathrm{die}(1)}(t) \\ P_{\mathrm{die}(2)}(t) \end{bmatrix} = \begin{bmatrix} f_{\mathrm{LUT}(1)}\left(\begin{bmatrix} T_{\mathrm{die}(1)}(t) \\ T_{\mathrm{die}(2)}(t) \end{bmatrix}\right) \\ f_{\mathrm{LUT}(2)}\left(\begin{bmatrix} T_{\mathrm{die}(1)}(t) \\ T_{\mathrm{die}(2)}(t) \end{bmatrix}\right) \end{bmatrix} \tag{11}$$

where the subscripts 1 and 2 denote the die, and f_{LUT} denotes the function used to calculate P_{die}; f_{LUT} is constructed by a linear interpolation of the specific calculated data points in the LUT.

The electrothermal cosimulation was started at $T_{\mathrm{die}(1)} = T_a$ and $T_{\mathrm{die}(2)} = T_a$. First, the electrical simulation was performed for T_a, and the I_{d} and V_{ds} waveforms obtained were used to calculate the first values of $P_{\mathrm{die}(1)}$ and $P_{\mathrm{die}(2)}$. These were substituted into (10) to obtain $T_{\mathrm{die}(1)}$ and $T_{\mathrm{die}(2)}$. These $T_{\mathrm{die}(1)}$ and $T_{\mathrm{die}(2)}$ values are used as the next input in (11) to calculate $P_{\mathrm{die}(1)}$ and $P_{\mathrm{die}(2)}$ for the next time step. This simulation loop was repeated until all T_{die} and P_{die} values reached a steady state.

III. Experiments

A. Experimental Setup

We performed experiments with a test PM using a heat sink, as shown in Fig. 7. The PM was a half-bridge converter with two SiC MOSFETs (S2301, ROHM; rated voltage = 1200 V; rated current = 40 A) [21]. One MOSFET operated as the HS switch, and the other operated as the LS switch. These MOSFET dies were bonded onto the baseplate using the conventional solder reflow and wire bonding technique. The baseplate consisted of a 0.635-mm SiN ceramic tile with 0.4-mm thick plates of Cu on both sides. The upper Cu plate, which can be seen in Fig. 7, was patterned to form the half-bridge circuit. The SiC dies were attached onto the plate using eutectic Sn–Ag–Cu solder joints having a thickness of 100 μm. Al wires (having a diameter of 400 μm) were used to electrically connect the dies to the upper

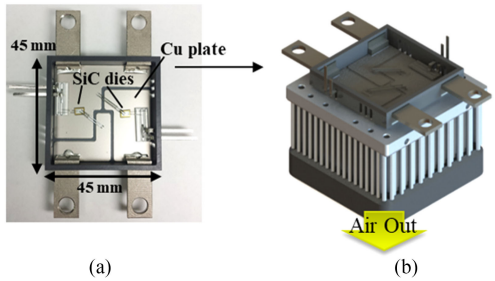


Fig. 7. (a) Inner structure of the PM. (b) PM with forced air-cooled heat sink to dissipate the heat generated in the PM.

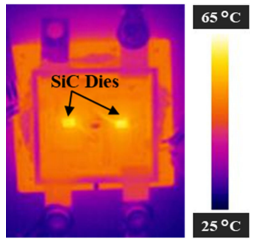


Fig. 8. Thermal image example of the PM captured by the thermography.

Cu plate. In order to cool down the PM during our experiments, a forced air-cooled heat sink (FH6030MU; Alpha) [22] was attached to the back of the PM using thermal grease (G751; Shin-Etsu MicroSi) [23]. Thermography (U5855A; Keysight Technologies) was used to measure T_{die}, and the PM was covered with carbon black to homogenize the emission coefficients of the materials. For this reason, the PM was not filled with the dielectric silicone gel. A thermal image example of the PM captured by the thermography is shown in Fig. 8; T_{die} can be extracted by using this image.

The PM was operated as the half-bridge in the buck converter, as shown in Fig. 9. The circuit specifications are shown in

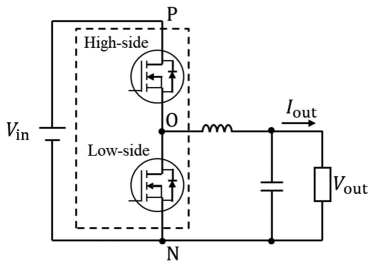


Fig. 9. Circuit diagram of the buck converter implemented with the PM.

TABLE V
CIRCUIT SPECIFICATIONS

Symbol	Meaning	Set value
V_{in}	Input voltage	100 V
V_{out}	Output voltage	50 V
I_{out}	Output current	15 A
f_{sw}	Switching frequency	50–350 kHz with 50 kHz step
Gate drive condition		On: 18 V, off: −5 V
Dead time		0.5 μs

Table V. Note that we set a relatively low value for V_{in} as compared with the rated voltage of the dies. This was done because the PM was not filled with the dielectric silicone gel, and the electrical insulation distance between the source and drain electrode of the dies was not enough to withstand more than 100 V. Although we performed the testing at a low voltage for V_{in}, these conditions are more than sufficient for validating the improvements made to our device model, as presented in this paper. These improvements include the BD and temperature dependence of the I_d–V_{ds} characteristics. The main reason for their inclusion is accurately reproducing the V_F of the BD and ON-state resistance of the device channels at high T_{die}. Neither of these characteristics are dependent on the value of V_{in}. If we test at a higher voltage for V_{in}, P_{die} and T_{die} will increase due to the higher switching power losses incurred. In order to predict them, the reproducibility of switching behavior of the dies is required; we already validated it under several voltage levels of V_{in} up to and including 800 V, as previously reported in [20].

An oscilloscope (DL7480; Yokogawa Test Measurement) with two differential probes 701921 and 700924 (Yokogawa Test Measurement) were used to measure the V_{gs} and V_{ds} waveforms, respectively. A current probe (CWT3 Ultra-mini; PEM) was used to measure the I_d waveform of each SiC die. P_{die} was calculated from these measured waveforms.

IV. VALIDATION OF THE SIMULATION

The circuit simulated by the device model provides the LUT for the HS and LS SiC MOSFET dies at the following temperature combinations (T_{high}, T_{low}): (25 °C, 25 °C), (25 °C, 87.5 °C), (25 °C, 150 °C), (87.5 °C, 25 °C), (87.5 °C, 87.5 °C), (87.5 °C, 150 °C), (150 °C, 25 °C), (150 °C, 87.5 °C), and (150 °C, 150 °C). T_{high} and T_{low} denote T_{die} of the HS and LS SiC MOSFET dies, respectively. The electrothermal cosimulation was conducted as described in Section III-C.

We compared the steady-state simulated P_{die} and T_{die} with the measured values after the experimental system had run for 10^3 s.

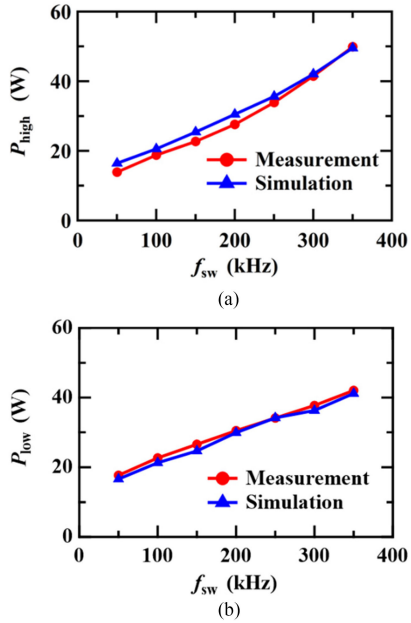


Fig. 10. Measured and simulated power loss of the HS and LS dies. The dots and lines denote the experimental power losses. The triangles and lines denote the simulated power losses. (a) HS SiC MOSFET die. (b) LS SiC MOSFET die.

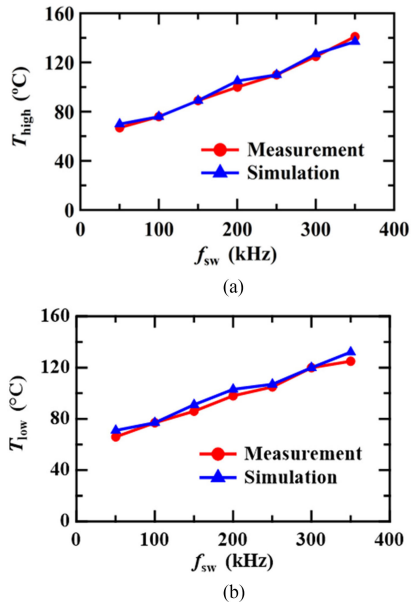


Fig. 11. Measured and simulated die temperatures for several f_{sw} conditions. The dots and lines denote the experimental T_{die}. The triangles and lines denote the simulated T_{die}. (a) HS SiC MOSFET die. (b) LS SiC MOSFET die.

We have used the steady-state values of P_{die} and T_{die}, unless otherwise stated. Fig. 10 shows the simulated and measured P_{high} and P_{low} as a function of f_{sw}. Here, P_{high} and P_{low} denote P_{die} for the HS and LS SiC MOSFET dies, respectively. The experimental and simulated values for P_{high} and P_{low} coincide well; the maximum error was within 3.0 W.

Fig. 11 shows the experimental and simulated T_{high} and T_{low} as a function of f_{sw}. As clearly seen, the simulated data successfully reproduce the experimental data for a wide temperature

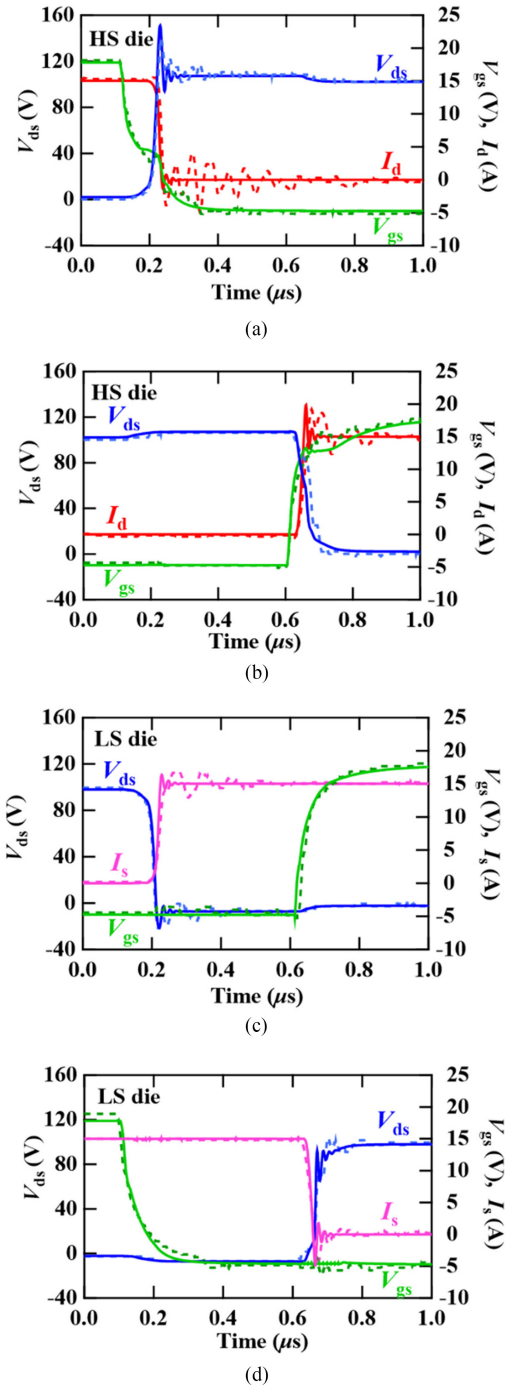


Fig. 12. Switching transient experimental and simulated waveforms of $V_{\rm gs}$, $V_{\rm ds}$, $I_{\rm d}$, and I_s at $f_{\rm sw} = 200$ kHz. Dashed and solid lines are experimental and simulated waveforms, respectively. (a) Turn-OFF waveforms of the HS SiC MOSFET die. (b) Turn-ON waveforms of the HS SiC MOSFET die. (c) Turn-ON waveforms of the LS SiC MOSFET die. (d) Turn-OFF waveforms of the LS SiC MOSFET die.

range from 60 °C to 140 °C. In addition, the maximum deviation between the two datasets is less than 8 °C.

Here, we show how accurately our device model predicted $P_{\rm die}$ and $T_{\rm die}$ in the buck converter. Fig. 12 shows that the switching transient experimental and simulated waveforms of the HS and LS SiC MOSFET dies at $f_{\rm sw} = 200$ kHz. In Fig. 12, $I_{\rm s}$ denotes the source current of the LS SiC MOSFET die.

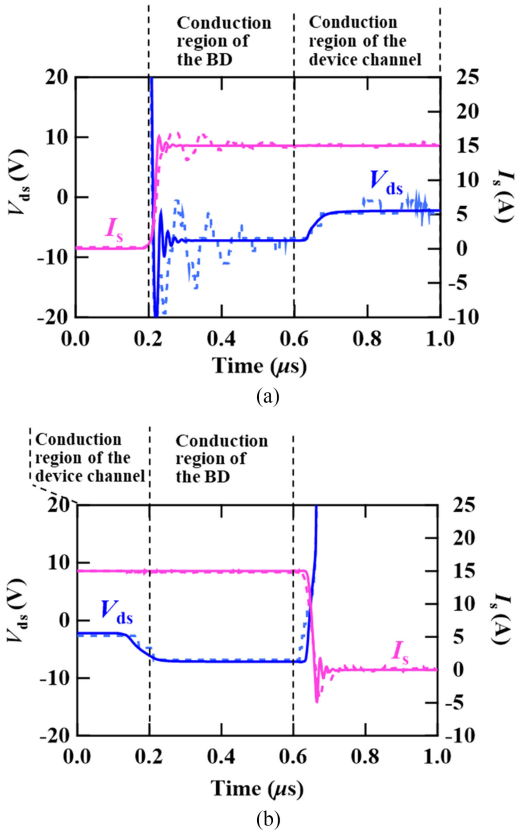


Fig. 13. $V_{\rm ds}$ and I_s waveforms of the LS SiC MOSFET die. The range of the $V_{\rm ds}$ waveforms was expanded from -20 to 20 V. Dashed and solid lines are experimental and simulated waveforms, respectively. (a) Turn-ON waveform. (b) Turn-OFF waveform.

Under the $f_{\rm sw}$ condition, $T_{\rm high}$ and $T_{\rm low}$ were 100 °C and 98 °C, respectively (see Fig. 11). Fig. 12 indicates that our device model reproduced the experimental switching behaviors well for high $T_{\rm die}$ conditions. We confirmed that our device model also accurately predicted experimental switching waveforms at all other $f_{\rm sw}$ and $T_{\rm die}$ conditions. These results clearly show that our model, which included temperature dependence of $I_{\rm d}$–$V_{\rm ds}$ characteristic, realized the accurate prediction of $P_{\rm die}$ and $T_{\rm die}$ for a wide range of $T_{\rm die}$ conditions.

Fig. 13 shows the $V_{\rm ds}$ and $I_{\rm s}$ waveforms of the LS SiC MOSFET die in Fig. 12(c) and (d). In Fig. 13, we set the range of the $V_{\rm ds}$ waveforms from -20 to 20 V. Fig. 13 indicates the BD behaviors of the LS SiC MOSFET die in the buck converter. During the period from 0.2 to 0.6 μs (conduction region of the BD), the measured and simulated values of the $V_{\rm ds}$ were relatively low because the BD operated as the freewheeling diode at the negative $V_{\rm gs}$ condition ($V_{\rm gs} = -5$ V). As clearly shown in Fig. 13, the simulated results could accurately reproduce the BD's behavior. If the $V_{\rm gs}$ dependence of the BD was not considered in our device model, the simulated values of the $V_{\rm ds}$ in the period would be relatively high as compared with the measured counterpart. This leads to underestimating $P_{\rm die}$, which has an undesirable influence on the accuracy of the $T_{\rm die}$ prediction in the electrothermal cosimulation. Hence, modeling the $V_{\rm gs}$ dependence of the BD is important for predicting $P_{\rm die}$ and $T_{\rm die}$ if the BD is used as the freewheeling diode. If antiparallel

Schottky diodes are connected with SiC MOSFETs, current would flow mainly through the antiparallel Schottky diodes. Therefore, the BD model is not necessarily needed in the case.

The excellent agreement between the values of the measured and the simulated $P_{\rm die}$, $T_{\rm die}$, and switching transient waveforms validates our electrothermal cosimulation method and also our device and thermal network models.

V. Conclusion

In this paper, we reported electrothermal cosimulation that reproduces well $P_{\rm die}$ and $T_{\rm die}$ of the two SiC MOSFET dies assembled in a PM. The device model used for the simulation was an improved version of the one that was described in our previous work [20]. This new version includes the negative $V_{\rm gs}$-dependent I–V characteristic of the BD embedded in the transistor and the temperature dependence of the $I_{\rm d}$–$V_{\rm ds}$ characteristic of the transistor. The device model could accurately reproduce $P_{\rm die}$ and transient switching waveforms at the conditions the BD was used as a free-wheeling diode and $T_{\rm die}$ was high. In order to model the thermal network accurately, we calibrated the heat transfer coefficient of the heat sink on the basis of the measured thermal impedances of the PM. Using the device model and the thermal network model, an LUT was prepared for the electrothermal cosimulation, which successfully calculated $P_{\rm die}$ and $T_{\rm die}$. The simulated and the measured temperatures agreed in the range from 60 °C to 140 °C, which reflects the $T_{\rm die}$ range commonly observed in practical power converters. The maximum deviation between the measured and the simulated $P_{\rm die}$ and $T_{\rm die}$ was less than 3.0 W and 8 °C, respectively. These results validate the usefulness of the electrothermal cosimulation including our device model and thermal network model for the front-end loading design for the thermal management of power converters.

References

[1] B. J. Baliga, *Silicon Carbide Power Device*. Singapore: World Scientific Publishing Co. Pvt. Ltd., 2005.

[2] T. Kimoto, Material science and device physics in SiC technology for high-voltage power devices, *Jpn. J. Appl. Phys.*, vol. 54, no. 4, Mar. 2015, Art. no. 040103.

[3] C. Batard, N. Ginot, and J. Antonios, "Lumpted dynamic electrothermal model of IGBT module of inverters," *IEEE Trans. Comp., Packag., Manuf. Technol.*, vol. 5, no. 3, pp. 355–364, Mar. 2015.

[4] V. Sodan, S. Stoffels, H. Oprins, M. Baelmans, S. Decoutere, and I. D. Wolf, "Distributed electro-thermal model based on fast and scalable algorithm for GaN power devices and circuit simulations," in *Proc. Int. Symp. Power Semicond. Devices ICs*, May 2017, pp. 179–182.

[5] T. Kojima *et al.*, "Novel electro-thermal coupling simulation technique for dynamic analysis of HV inverter," in *Proc. 37th Power Electron. Spec. Conf.*, Jun. 2006, pp. 2048–2052.

[6] J. Li, A. Castelazzi, M. A. Eleffendi, E. Gurpinar, C. M. Johnson, and L. Mills, "A physical RC network model for electro-thermal analysis of a multichip SiC power module," *IEEE Trans. Power Electron.*, vol. 33, no. 3, pp. 2494–2508, Mar. 2018.

[7] A. Raciti, D. Cristaldi, G. Greco, G. Vinci, and G. Bazzano, "Electro-thermal PSpice modeling and simulation of power modules," *IEEE Trans. Ind. Electron.*, vol. 62, no. 10, pp. 6260–6271, Oct. 2015.

[8] C. Sintamarean, F. Blaabjerg, and H. Wang, "A novel electro-thermal model for wide bandgap semiconductor based devices," in *Proc. 15th Eur. Conf. Power Electron. Appl.*, Oct. 2013.

[9] L. Ceccarelli, A. S. Bahman, F. Iannuzzo, and F. Blaabjerg, "A fast electro-thermal co-simulation modeling approach for SiC power MOSFETs," in *Proc. IEEE Appl. Power Electron. Conf. Expo.*, Mar. 2017, pp. 966–973.

[10] D. Lena, M. Grosso, A. Bocca, A. Macii, and S. Rinaudo, "A compact IGBT electro-thermal model in Verilog-A for fast system-level simulation," in *Proc. Conf. IEEE Ind. Electron. Soc.*, Oct. 2016, pp. 3793–3798.

[11] R. Fu, A. Grekov, J. Hudgins, A. Mantooth, and E. Santi, "Power SiC DMOSFET model accounting for nonuniform current distribution in JFET region," *IEEE Trans. Ind. Appl.*, vol. 48, no. 1, pp. 181–190, Nov. 2012.

[12] R. Kraus and A. Castelazzi, "A physics-based compact model of SiC power MOSFETs," *IEEE Trans. Power Electron.*, vol. 31, no. 8, pp. 5863–5870, Aug. 2016.

[13] T. MuNutt, A. Hefner, A. Mantooth, D. Berning, and S. H. Ryu, "Silicon carbide MOSFET model and parameter extraction sequence," *IEEE Trans. Power Electron.*, vol. 22, no. 2, pp. 353–363, Mar. 2007.

[14] M. Mudholkar, S. Ahmed, M. N. Ericson, S. Frank, C. Britton, and A. Mantooth, "Datasheet driven silicon carbide power MOSFET model," *IEEE Trans. Power Electron.*, vol. 29, no. 5, pp. 2220–2227, May 2014.

[15] Y. Nakamura, M. Shintani, K. Oishi, T. Sato, and T. Hikihara, "A simulation model for SiC power MOSFET based on surface potential," in *Proc. IEEE Int. Conf. Simul. Semicond. Processes Devices*, Sep. 2016, pp. 121–124.

[16] A. P. Arribas, F. Shang, M. Krishnamurthy, and K. Shenai, "Simple and accurate circuit simulation model for SiC power MOSFET," *IEEE Trans. Electron Devices*, vol. 62, no. 2, pp. 449–457, Feb. 2015.

[17] Z. Chen, D. Boroyevich, R. Burgos, and F. Wang, "Characterization and modeling of 1.2 kV, 20 A SiC MOSFETs," in *Proc. IEEE Energy Convers. Congr. Expo.*, Sep. 2009, pp. 1480–1487.

[18] X. Hou, D. Boroyevich, and R. Burgos, "Characterization on latest-generation SiC MOSFET's body diode," in *Proc. IEEE Workshop Wide Bandgap Power Devices Appl.*, Nov. 2016, pp. 247–252.

[19] ROHM Co. Ltd., "SiC power devices and modules application note," ROHM Co. Ltd., Kyoto, Japan, Jun. 2013.

[20] H. Sakairi, T. Yanagi, H. Otake, N. Kuroda, H. Tanigawa, and K. Nakahara, "Measurement methodology for accurate modeling of SiC MOSFET switching behavior over wide voltage and current ranges," *IEEE Trans. Power Electron.*, vol. 33, no. 9, pp. 7314–7325, Sep. 2018.

[21] ROHM Co., Ltd., *S2301 N-channel SiC power MOSFET bare die datasheet*, ROHM Co., Ltd., Kyoto, Japan, Apr. 2017.

[22] Alpha Co. Ltd., "Active heat sink FH60," Oct. 2013.

[23] Shin-Etsu Micro Si Inc., "Technical data sheet for G751," Jan. 2015.

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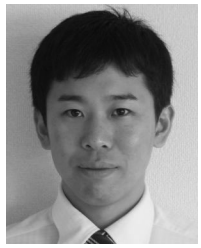

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