An Overview of Assessment Methods for Synchronization Stability of Grid-Connected Converters Under Severe Symmetrical Grid Faults

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Abstract—Grid-connected converters exposed to weak grid conditions and severe fault events are at risk of losing synchronism with the external grid and neighboring converters. This predicament has led to a growing interest in analyzing the synchronization mechanism and developing models and tools for predicting the transient stability of grid-connected converters. This paper presents a thorough review of the developed methods that describe the phenomena of synchronization instability of grid-connected converters under severe symmetrical grid faults. These methods are compared where the advantages and disadvantages of each method are carefully mapped. The analytical derivations and a detailed simulation model are verified through experimental tests of three case studies. Steady-state and quasi-static analysis can determine whether a given fault condition results in a stable or unstable operating point. However, without considering the dynamics of the synchronization unit, transient stability cannot be guaranteed. By comparing the synchronization unit to a synchronous machine, the damping of the phase-locked loop is identified. For accurate stability assessment, either nonlinear phase portraits or time-domain simulations must be performed. Until this point, no direct stability assessment method is available which consider the damping effect of the synchronization unit. Therefore, additional work is needed on this field in future research.

Index Terms—Fault ride through, grid connection, severe grid fault, synchronization stability, voltage-source converter (VSC).

I. Introduction

WITH globally increasing electricity demand and a desire to bring down CO_2 emissions, a transition from fossil fuels to sustainable energy is needed [1]. This objective has highly increased the installed capacity of grid-connected renewables such as wind and photovoltaics (PV) in modern power systems. The continuous advancements in renewable energy sources (RES) will cause a high share of distributed power generation to centralized power generation in the coming decades [2].

Today, the main production of electrical energy comes from centralized power plants, which due to their large rotational inertia, provide the power system with high transient stability and robust performance [3]. Eventually, the rotational inertia, which provides the immediate response to a grid frequency disturbance, will be lost in a power electronic based power system as power electronic converters do not inherently provide inertia [3], [4]. Having a high penetration level of distributed generation (DG) greatly affect how the network is being supported during disturbances and fault situations. Unlike synchronous machines, the transient behavior of a converter is almost entirely determined by the control structure employed [5]. Previously, it was desirable for small power generation units such as wind turbines (WTs) and PV systems to disconnect from the utility grid during abnormal situations. This was acceptable since the small power generation deficit was nearly unmeasurable. With a significant increase of renewables, loss of generation will have an immense impact on the network such as frequency instabilities that eventually can lead to disruption of power and even black out [5]. The aforementioned conditions have enforced transmission system operators (TSOs) and distribution system operators (DSOs) to require certain behavior of DGs during disturbances and faults. To assure a high security of supply, low-voltage ride-through (LVRT) capability is required by DGs.

For interconnection of RES like PV and WTs with the grid, the voltage-source converter (VSC) is a commonly used topology [6]. In order to attenuate high-frequency switching harmonics emitted by the converter, line filtering is needed and a third-order LCL filter is usually employed due to its high attenuation capability and its compactness compared to a single bulky output reactor [7]–[9]. Currently, the majority of grid-tied converters used in PV applications and wind power systems can be classified as grid-feeding/following current-controlled converters that aim to inject maximum power in the form of sinusoidal currents to the grid [5], [10]. Therefore, with grid-feeding converters dominating today's control of grid-connected RES and considering that they should support the network according to grid code requirements, it is important to evaluate the performance of such systems with respect to LVRT capability and ancillary support functionalities.

Extensive research has studied the control of WTs and PV power plants during grid fault conditions including LVRT capability [11]–[19]. Although several grid codes demand LVRT capability down to a complete absence of the grid voltage, the most research only considers voltage sags to a minimum of 10%–50%. This greatly changes the picture of how the transition control during nearly zero-voltage situations should be accomplished.

Most grid-supporting converters, which are voltage-controlled rather than current-controlled, are switched to a grid-feeding structure during the fault in order to safely limit the converter current [20]. Therefore, the analysis of grid feeding, i.e., a current-controlled converter, during a severe grid fault is applicable for almost any control structure employed. However, during power system faults, a grid-feeding strategy might be unable to achieve a successful synchronization with the grid; moreover, instabilities of the current controller at nearly zero voltage situations are reported in [21], [22] which originates from the phase-locked loop (PLL) being incapable to remain synchronized with the grid. This is referred to as loss of synchronization (LOS). In [23], multiple PLL strategies tested under different voltage sag profiles are reviewed. Here, a three-phase symmetrical fault is considered but the voltage sag introduced cannot be classified as severe, which in the case of a solid fault could cause instability of the PLL. For a grid-feeding converter to be able to ride through a nearly zero voltage situation, one must be able to model the PLL instability and determine whether any action or modifications must be done to enhance the PLL structure or the tuning method during a fault. Numerous studies have discussed PLL instability in weak grid conditions but little research has been conducted to fully understand the underlying mechanism characterizing LOS of the PLL during severe grid faults. Nevertheless, some work have addressed PLL instability during low-voltage situations using different approaches of modeling and analysis methods [21], [24]–[30]. Alongside modeling, several studies propose controller mitigation techniques to avoid LOS during low- and zero-voltage grid events including freezing/blocking the PLL [31], [32], zero or limited current injection [33], voltage-dependent active current injection [24], current injection based on X/R characteristics of the network impedance [27], and active current injection based on the PLL frequency error [21], [30].

In [21], [24], the current injection limit resulting in LOS is derived for steady-state network conditions. Including the PLL dynamics, a quasi-static large-signal model is developed in [25]–[27] which identifies a destabilizing positive feedback term to the PLL model as a result of the coupling between the injected current and grid voltage. Another assessment tool is developed in [28]–[30] where the Equal Area Criterion (EAC) normally used for rotor-angle transient stability assessment of synchronous machines is utilized to analyze the LOS mechanism. Last, transient stability is analyzed in [28] where nonlinear methods are used to assess the stability of the inherent nonlinear system.

The demonstrations from above studies all aim to analyze the synchronization stability of grid-connected converters but with a very different cause of action which complicates the

TABLE I
MAIN PARAMETERS OF THE SYSTEM IN Fig. 1

Symbol	Description	Value
S_b	Rated power	7.35 kVA
V_b	Nominal grid voltage (l-l, rms)	400 V
V_{dc}	dc-link voltage	650 V
f_0	Rated frequency	50 Hz
f_{sw}	Switching frequency	10 kHz
f_s	Sampling frequency	10 kHz
L_{cf}	Converter-side inductor	0.07 pu
L_{gf}	Grid-side inductor	0.04 pu
C_f	Filter capacitor	0.07 pu

understanding of LOS and how to prevent it. Therefore, this paper aims to give an overview of the available methods for LOS assessment of grid-feeding grid-connected converters during severe symmetrical faults. This is done by answering the following questions which lack insight from the prior art.

1) *When is the PLL no longer able to maintain synchronized with the grid?*
2) *Which factors influence LOS and what actions can be taken to improve the synchronization stability of a conventional grid-feeding converter?*

By answering such questions, a future power system dominated by paralleled converters might be easier to design, understand, and operate during severe grid events.

The remainder of the paper is structured as follows: Section II presents the considered case study including relevant parameters and control structure. Grid requirements are shortly reviewed in Section III. In Section IV, an overview of different LOS analysis methods are presented. A comparison between the reviewed stability assessment methods is given, which is based on three case studies including a severe low-voltage fault. The different stability prediction methods are compared in Section V through three case studies aiming to reveal the performance including a mapping of advantages/disadvantages of the reviewed methods. Simulation and experimental results are provided of the different methods all benchmarked to a conventional grid-feeding control structure. A discussion on the remaining challenges and future trends in the field of synchronization stability of grid-connected converters is given in Section VI. Finally, conclusions are drawn in Section VII.

II. SYSTEM OVERVIEW

This paper considers a typical structure of a distributed generator system: a Type 4 WT configuration consisting of a synchronous machine using a full-scale power electronic converter interfaced with the grid through an output LCL filter. Parameters used for simulation and experimental verification of the system are shown in Table I.

As the generator-side converter and line-side converter (LSC) are tightly regulated with independent control objectives separated by a dc link, these can be considered as decoupled. Therefore, only the LSC with a constant dc-link voltage will be considered for the analysis and comparisons performed throughout this paper. Even though, the aim of this paper is on
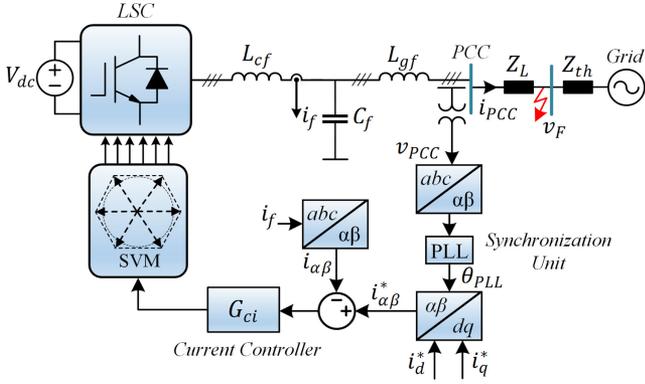
Fig. 1. Structure of LSC control including PLL and inner current controller together with the location of the considered severe symmetrical fault.
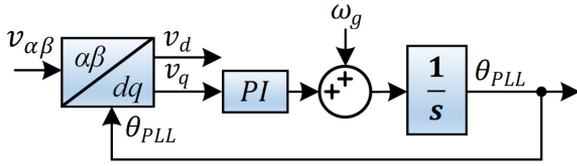

Fig. 2. Structure of SRF-PLL used to estimate the phase angle of the PCC voltage.

Fig. 3. Requirement from BDEW for low-voltage ride-through capability during a fault event. V is the lowest value of the three line-to-line voltages and V_b is the nominal voltage.

Fig. 4. Voltage support by injection of reactive current in either overexcited or underexcited operation [39]. The reactive power injection should be activated within 20 ms.

the synchronization stability of the converter system and not the interactions between the dc and ac side, a brief argument of why the dc side can be considered constant is given. Due to the current being limited and the grid voltage being low during a severe symmetrical fault, surplus energy will be accumulated at the dc side which quickly can cause destructive over-voltages on the dc-link capacitor. Generally, a chopper circuit is implemented in the dc side in order to consume the accumulated power during any dc-side over-voltages which justify the assumption of a nearly constant dc-link voltage.

The grid-feeding converter control structure is shown in Fig. 1 where a synchronous reference frame PLL (SRF-PLL) is used to estimate the instantaneous terminal voltage phase-angle for grid synchronization. In order to track the reference current, selecting between different current controller structures, a proportional-resonant controller implemented in the stationary $\alpha\beta$-reference frame is used as presented in [10].

Since the SRF-PLL is an often used method for grid synchronization among researchers and industry, the stability analysis regarding LOS throughout this paper is developed for a grid-connected converter using a SRF-PLL structure. The SRF-PLL structure used throughout this paper is visualized in Fig. 2.

III. GRID REQUIREMENTS

Due to the increasing installation of DGs, TSOs and DSOs have issued requirements for power-converter-based RESs [34]–[36]. During the last decade, requirements for advanced grid support have emerged in several European countries which implies that the control strategy of WT converters should provide ancillary services to enhance the stability of the grid [37]. According to grid codes, such systems should tolerate deep voltage sags and provide voltage support by injecting reactive
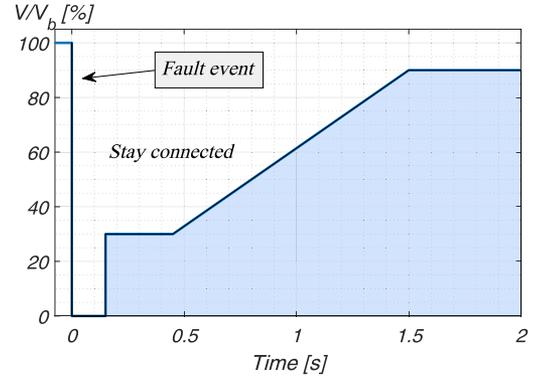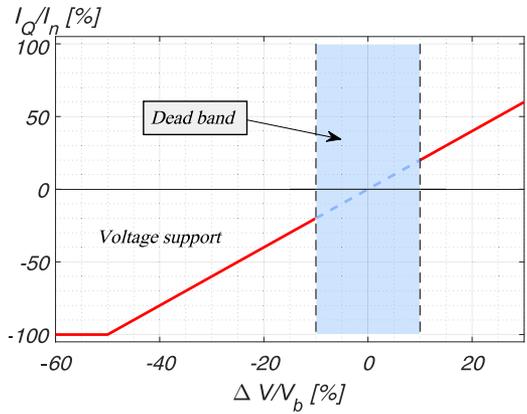
current into the grid to avoid a potential network collapse. The requirements deliberated in this paper is the German grid code for generating plants connected to the medium-voltage network issued by the German association of energy and water industries (BDEW), in 2008 [38]. DGs can be subjected to low-voltage situations that occur as a result of different types of grid abnormalities. Such situations can trip the converters interfacing RES with the point of common coupling (PCC), which causes an unintended disconnection of the power generation posing a threat to the security of supply, frequency stability, and the possibility for network collapse. Due to this, distributed energy resources are required to ride-through low-voltage conditions and support the grid [38], [40]–[43]. The required ride-through behavior during low-voltage conditions is presented in Fig. 3, where DGs are required to stay ground-connected for up to 150 ms. In case of faults, the generating unit must provide reactive current in order to support the network voltage where the reactive power injection must be activated as dictated in Fig. 4. When the deviation from the nominal voltage is more than 10%, the converter should provide 2% reactive current per percent of the voltage deviation. During voltage support, the reactive current has higher priority than that of the active current; hence, in

the case of a voltage drop below half of the nominal voltage, the converter should allocate the full rated current to reactive power injection.

IV. ANALYSIS OF LOSS OF SYNCHRONIZATION

As mentioned, DGs operating at a weak-grid connection is susceptible to grid-synchronization issues using PLLs. The strength of the connection between PCC and the grid is defined by the short-circuit ratio (SCR) at the connection point. A low SCR occurs as a result of high equivalent network impedances which is well known to cause PLL instability, i.e., LOS [22]. Nevertheless, grid-connected converters connected to a strong grid might still lose synchronism with the grid when exposed to severe symmetrical faults. This phenomenon happens since during low-voltage conditions, the local voltage of the converter (v_{PCC}) is significantly influenced by the injected converter currents, i.e., during faults, an increased relative sensitivity of the PCC voltage is observed compared to normal operating conditions for a given current injection. Accordingly, a severe fault condition may be interpreted as a momentary weak grid condition seen from the PLL synchronization point of view, since this relatively larger voltage sensitivity during the fault is indistinguishable from the situation of an increased equivalent impedance (lower SCR) at nominal voltage conditions. Consequently, even for a strong network, synchronization instability between the WT and grid may be developed by cause of a weaker coupling between the equivalent grid voltage and the PCC voltage during severe grid faults. As it is pointed out for LOS during weak grid conditions [22], the synchronization instability origins from the fact that PCC voltage which is to be synchronized to, is tightly coupled with the operation mode, network parameters, and injected current of the converter. In this section, different ways of analyzing LOS developed with the purpose to assess the synchronization stability of a grid-connected converter are reviewed. These all aim to develop a simplified model of the converter, control system, and grid network which attempts to describe why LOS occurs and how the PLL is affected by the converter mode of operation together with grid impedances and disturbances.

Among others, it will be shown that the analysis to be performed in Sections IV-A and IV-B are independent of the synchronization unit employed given that the stability assessment method concludes the system to be unstable. It should be noted that in a realistic implemented case, a sequence extraction algorithm is included in front of the synchronization unit in order to extract the positive sequence component of the grid voltage to account for asymmetrical conditions. This is normally accomplished using either a second-order gneralized integrator PLL [44], a Decoupled Double Synchronous Reference Frame PLL [45], or an SRF-PLL with a complex coefficient notch and band-pass filter [46]. Common to all of these is that a low-pass filtering effect is introduced in addition to the dynamics of the PLL. Any filtering techniques used in front of the PLL is beyond the scope of this work, but it can be mentioned that the inclusion of a sequence extractor tend to have a destabilizing effect on stability issues related to LOS. Therefore, if a considered
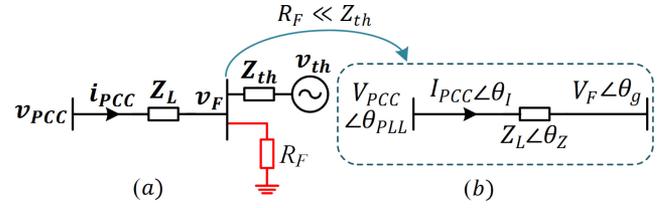

Fig. 5. (a) Power transfer between wind turbine connection point and fault point represented as a single line diagram. (b) When a nearly solid three-phase fault occurs, the digram can be simplified as indicated by the blue arrow. Bold face symbols denote vector notation.

system is concluded stable using any of the methods discussed throughout this paper, a closer inspection should be made on the stability assessment when the low-pass filtering effect caused by any prefiltering procedure is included. Additionally, symmetrical faults are exclusively studied in this paper since even the most severe asymmetrical fault (a solid double-line-to-ground fault) will only cause the positive sequence voltage to drop to 0.33 pu which is way above the range where LOS occurs considering ordinary values of the network impedances.

A. Steady-State Network Analysis

The circuit diagram of a DG connected to a Thevenin equivalent grid at a fault instant is depicted in Fig. 5(a). Assuming a nearly solid fault where $R_F << Z_{\mathrm{th}}$, the circuit can be represented as shown in Fig. 5(b).

Deriving the often used power flow equations for a single-line diagram and dividing with the sending end voltage, expressions for the active and reactive current components can be established as

$$I_a = \frac{V_{\mathrm{PCC}}R_L}{Z_L^2} + \frac{V_F X_L \sin(\delta)}{Z_L^2} - \frac{V_F R_L \cos(\delta)}{Z_L^2} \quad (1)$$

$$-I_r = \frac{V_{\mathrm{PCC}}X_L}{Z_L^2} - \frac{V_F X_L \cos(\delta)}{Z_L^2} - \frac{V_F R_L \sin(\delta)}{Z_L^2} \quad (2)$$

where $Z_L = \sqrt{R_L^2 + X_L^2}$ and $\delta = \theta_{\mathrm{PLL}} - \theta_g$ is the angle between v_{PCC} and v_F. It should be noted that to achieve positive reactive power the current vector must lag the voltage vector. Therefore, the reactive current (I_r) in (2) is negative. For solid symmetrical faults, the active and reactive power are dictated by the line impedance in the form of losses as

$$I_a = \frac{V_{\mathrm{PCC}}R_L}{Z_L^2} \quad (3)$$

$$I_r = -\frac{V_{\mathrm{PCC}}X_L}{Z_L^2} \quad (4)$$

$$\Rightarrow \frac{I_a}{I_r} = -\frac{R_L}{X_L} \quad (5)$$

which implies that during such situations, neither pure active or pure reactive power can be transferred as required by the grid code. From this, it can be concluded that if the voltage at the fault locations drops below a certain critical value dependent on network parameters, pure reactive current injection cannot be
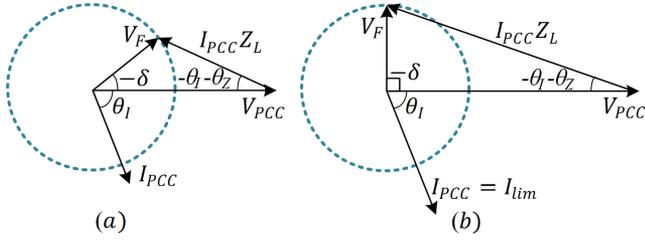
Fig. 6. Phasor diagram of current injection where the dotted blue circles represent a fault voltage with constant magnitude and arbitrary angle. (a) Stable case, (b) Limit case where the angle between sending end and receiving end voltage is 90° [21].

realized since the converter attempts to operate at an unstable equilibrium point. To derive the steady-state limits for the current transfer, it is assumed that the voltage magnitude at the fault location is not affected by the current injected by the WT. As described in [47], power system faults are mainly resistive and as analyzed in [48], reactive current injection has negligible effect on the voltage magnitude at the fault location. Using this, the blue-dotted lines shown in Fig. 6 can be used to obtain the stability limit of the depicted two-bus system.

As it can be seen in Fig. 6(a), an arbitrary current vector is injected to the grid that causes a voltage drop across the line impedance, Z_L, which forms the vector diagram shown. If the magnitude of the injected current is increased, the angle between the voltage at the PCC and the voltage at the fault location is increased as well. To that end, if the current is increased further from the case shown in Fig. 6(b), the resultant voltage vector v_F cannot be located at the circle with constant magnitude. This means that a nonexisting operating point is attempted which will lead to LOS of the PLL since the voltage at the PCC has to change to satisfy the laws of physics which implies that said current is no longer the same due to the change in terminal voltage. The limit case shown in Fig. 6(b) can mathematically be formulated as when the vertical component of the voltage drop across the line impedance equals the fault voltage magnitude which can be expressed as

$$V_F = Z_L I_{\lim} \sin(-\theta_I - \theta_Z). \tag{6}$$

More generally, the current magnitude limit for a given θ_I can be expressed as

$$I_{\lim} = \frac{V_F}{Z_L |\sin(\theta_I + \theta_Z)|} \quad \forall \ \theta_I, \theta_Z \in \Re. \tag{7}$$

During purely overexcited operation where $\theta_I = -90°$, this reduces to

$$I_{\lim} = \frac{V_F}{Z_L \cos(\theta_Z)} = \frac{V_F}{R_L}. \tag{8}$$

It can be seen from (7) that when the current vector is aligned with the negative of the impedance angle, the injected current has no limit, and theoretically an infinite amount of current can be injected. It should be noted that this analysis is derived on the assumption of steady-state conditions, thus during disturbances and fault conditions, the instability may occur for current limits more strict than that predicted here.

B. Quasi-Static Large-Signal Analysis

Compared to the just described steady-state approach, this method, as developed in [25], [27], [49], has the advantage of including the effect that the PLL has on the injected current, which is coupled to the PCC voltage. The inner current loop can be assumed to behave as a controlled current source provided the bandwidth, in general, is much higher than that of the PLL. Considering the circuit diagram in Fig. 5(a), the PCC voltage can be expressed using the superposition principle of linear circuits as

$$\boldsymbol{v}_{\text{PCC}} = K_g(\omega_g) V_{\text{th}} e^{j(\theta_g + \phi_g)} + K_c(\omega_{\text{PLL}}) I_{\text{PCC}} e^{j(\theta_c + \phi_c)} \tag{9}$$

where

$$K_g(\omega_g) = \left| \frac{R_F}{R_F + \boldsymbol{Z}_{\text{th}}(\omega_g)} \right| \tag{10}$$

$$K_c(\omega_{\text{PLL}}) = \left| \boldsymbol{Z_L}(\omega_{\text{PLL}}) + \frac{R_F \boldsymbol{Z_{th}}(\omega_{\text{PLL}})}{R_F + \boldsymbol{Z_{th}}(\omega_{\text{PLL}})} \right| \tag{11}$$

$$\phi_g(\omega_g) = \angle \left(\frac{R_F}{R_F + \boldsymbol{Z}_{\text{th}}(\omega_g)} \right) \tag{12}$$

$$\phi_c(\omega_{\text{PLL}}) = \angle \left(\boldsymbol{Z_L}(\omega_{\text{PLL}}) + \frac{R_F \boldsymbol{Z}_{\text{th}}(\omega_{\text{PLL}})}{R_F + \boldsymbol{Z}_{\text{th}}(\omega_{\text{PLL}})} \right). \tag{13}$$

Here, θ_g is the angle of the grid voltage and $\theta_c = \theta_{\text{PLL}} + \theta_I$ is the angle of the injected current vector. Expressing the PCC voltage in the rotating frame of the PLL (subtracting θ_{PLL} from both terms in (9)) and evaluating the imaginary part, one obtains that the q-axis component of $\boldsymbol{v}_{\text{PCC}}$ is

$$v_{\text{PCC},q} = \underbrace{K_g(\omega_g) V_{\text{th}} \sin(\theta_g + \phi_g - \theta_{\text{PLL}})}_{\text{Grid-synchronization term, } v_{q-}}$$
$$+ \underbrace{K_c(\omega_{\text{PLL}}) I_{\text{PCC}} \sin(\theta_I + \phi_c)}_{\text{Self-synchronization term, } v_{q+}} \tag{14}$$

where $\theta_I = \tan^{-1}(i_q^{\text{ref}}/i_d^{\text{ref}})$ is the angle of the injected current reference relative to the PLL phase angle. The second term in (14) represents a dc signal behaving as a positive feedback term in the PLL model, denoted as the self-synchronization term. The first term, denoted as the grid-synchronization term, represents a signal depending on the grid impedance, voltage level, and the synchronization error between the grid voltage angle and the angle of the PLL. The grid-synchronization term is regulated by the PLL such to cancel the positive-feedback disturbance introduced by the self-synchronization loop and thereby, controlling the q-axis component of the PCC voltage to zero. These terms define the quasi-static PLL model, which is visualized as a block diagram in Fig. 7. From this, it is expected that LOS will definitely occur when $v_{q+} > v_{q-}$ which happens when

$$K_c(\omega_{\text{PLL}}) I_{\text{PCC}} |\sin(\theta_I + \phi_c(\omega_{\text{PLL}}))| > V_{\text{th}} K_g(\omega_g) \tag{15}$$

since the PLL cannot regulate the system to an angle which causes the grid-synchronization loop in Fig. 7 to exceed $V_{\text{th}} K_g(\omega_g)$ due to the nonlinear trigonometric phase detector
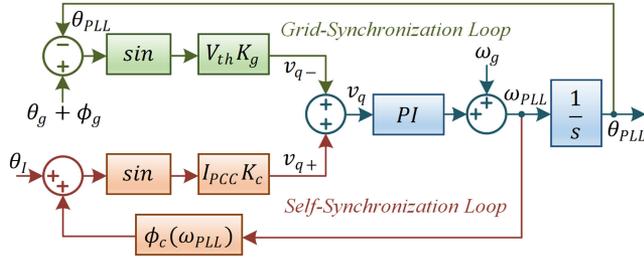
Fig. 7. Quasi-static large-signal model of converter, grid network, and SRF-PLL [25]. The grid-synchronization loop (green part) represents the usually seen synchronization model of an SRF-PLL, whereas the self-synchronization loop (red part) represents the interaction between the converter operation and the voltage at the PCC. The parameters shown in the figure are calculated using (10)–(13).
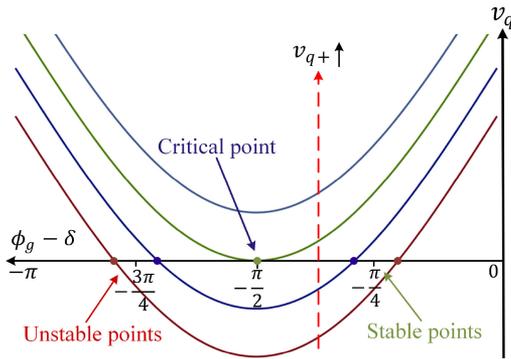

Fig. 8. Operating points for $v_q = 0$ for increasing self-synchronization term during injection of capacitive reactive current [27]. δ is the angle difference between the PCC voltage and grid voltage.

of the PLL. This gives the constraint of the injected current as

$$I_{\text{PCC}} < \frac{V_{\text{th}}K_g(\omega_g)}{K_c(\omega_{\text{PLL}})|\sin(\theta_I + \phi_c(\omega_{\text{PLL}}))|} \qquad (16)$$

which when considering a solid fault ($R_F \approx 0$, $V_{\text{th}}K_g(\omega_g) \approx V_F$, and $\theta_I = -90°$), gives the same result as for the steady-state injection limits presented previously. In Section IV-A, it was seen that when the angle between the fault voltage and PCC voltage exceeded 90°, the system would become unstable. This is supported in Fig. 7, where it can be seen that when the angle exceeds 90°, the contribution from the grid-synchronization loop will start to decrease. As also seen from Fig. 7 during reactive current injection and assuming the constraint in (16) to be violated, the frequency of the PLL will keep decreasing due to the integrator and the presence of a sustained negative v_q component. Hence, if LOS occurs during capacitive reactive current injection, the estimated PLL frequency should decrease toward $-\infty$. For the PLL to be stable, a feasible operating point has to exist (i.e., a value for θ_{PLL} that solves $v_q = 0$), which means that the grid-synchronization term and the self-synchronization term in (14) should be canceled out. As it can be seen in Fig. 8, when the self-synchronization term (dc-bias) is increased to a point where the negative peak of the sinusoidal is not able to intersect with the horizontal axis, instability can be expected to occur. Furthermore, when the PLL can be regulated to obtain $v_q = 0$, one must assure that $\pi/2 > \phi_g - \delta > -\pi/2$ which is shown as

the critical point in Fig. 8 when the converter is controlled to inject capacitive reactive current, i.e., operated in overexcited mode. These operating points, where $\pi/2 > \phi_g - \delta > -\pi/2$ is violated, are unstable since poles with a positive real part exist in the small-signal model, leading to small-signal instability [27].

Along these lines, using the large-signal quasi-static model shown in Fig. 7, the stability of the PLL can be predicted provided that the current can be considered equal to its reference value. However, when deriving transfer limits of the quasi-static model, an identical result as obtained for the steady-state case is achieved. This is due to the fact that the transient response of the PLL is not considered in the derived constraints. This means that even though a stable equilibrium point exists during the fault, the PLL may not be able to remain stable and arrive at that equilibrium point. Therefore, the dynamics of the PLL should be included in the model in order to improve the stability prediction capability.

C. PLL Analogous to Synchronous Machines

From the quasi-static and steady-state analysis, some aspects of the underlying mechanism of what causes LOS is revealed. This include physical circuit parameters such as high injection of current, low grid voltage, and high grid impedance. Even though the quasi-static large-signal model includes the controller parameters of the PLL, no insight how these affect LOS is resolved since its solution require numerical methods. Hence, the following method, as developed in [28]–[30], is included. Here, it is described that the PLL synchronization mechanism is analogous to that of a synchronous machine which enables a definition of PLL damping. A disadvantage of this approach is that for a line impedance consisting of both a resistive and an inductive part, the mathematical derivation becomes extremely complicated which makes it difficult to declare any applicable insight. To circumvent this, the analysis is performed for a purely resistive and purely inductive network separately.

To simplify the mathematical analysis, the circuit diagram shown in Fig. 5(b) is used. Since the focus is on nearly zero-voltage conditions, it is assumed that $R_f \approx 0$, which implies that $K_g V_{\text{th}}$ can simply be replaced by the voltage at the fault location, V_F [30]. Doing this, (14) can be simplified to

$$v_q = V_F \sin(-\delta) + Z_L(\omega_{\text{PLL}})I_{\text{PCC}} \sin(\theta_I + \phi_c). \qquad (17)$$

From the block diagram shown in Fig. 7, the PLL phase angle is

$$\theta_{\text{PLL}} = \int v_q \left(K_p + \int K_i dt \right) + \omega_g \, dt. \qquad (18)$$

Using that $\int \omega_g \, dt = \theta_g$ and by differentiating the expression twice, one obtains that

$$\ddot{\delta} = K_p \left(-\dot{\delta} V_F \cos(\delta) + \frac{d(Z_L I_{\text{PCC}} \sin(\theta_I + \phi_c))}{dt} \right)$$
$$+ K_i \left(Z_L I_{\text{PCC}} \sin(\theta_I + \phi_c) - V_F \sin(\delta) \right) \qquad (19)$$

where both Z_L and ϕ_c are dependent on ω_{PLL}. In case of a resistive line impedance, this is reduced to

$$\ddot{\delta}_R = -\dot{\delta}K_p V_F \cos(\delta) + K_i \left(R_L I_{\text{PCC}} \sin(\theta_I) - V_F \sin(\delta) \right) \tag{20}$$

whereas for an inductive line it can be expressed as

$$\ddot{\delta}_L = \frac{K_i(L_L(\omega_0 + \dot{\delta})I_{\text{PCC}} \cos(\theta_I) - V_F \sin(\delta))}{1 - K_p L_L I_{\text{PCC}} \cos(\theta_I)}$$
$$- \frac{K_p \dot{\delta} V_F \cos(\delta)}{1 - K_p L_L I_{\text{PCC}} \cos(\theta_I)}. \tag{21}$$

During a fault situation where the converter is required to inject full reactive current ($\theta_I = -90°$), this reduces to

$$\ddot{\delta}_L = -\dot{\delta}K_p V_F \cos(\delta) - K_i V_F \sin(\delta). \tag{22}$$

For a second-order system on the form

$$0 = \ddot{\delta} + D(\delta)\dot{\delta} + F(\delta) \tag{23}$$

the function $D(\delta)$ represents a nonconservative force, which is accountable for any damping acting on the system. To exemplify this and provide knowledge of which parameters influence this damping term, (21) can be expressed as

$$0 = \ddot{\delta} + \dot{\delta}C_1 \left(C_3 V_F \cos(\delta) - C_2 \right) - C_1(\omega_0 C_2 - V_F \sin(\delta)) \tag{24}$$

where

$$C_1 = \frac{K_i}{1 - K_p C_2}, \quad C_2 = L_L I_{\text{PCC}} \cos(\theta_I), \quad C_3 = \frac{K_p}{K_i}.$$

Rearranging (24) to put it on the more familiar swing equation form governing the rotor dynamics of a synchronous machine gives

$$\underbrace{\frac{1}{C_1}}_{M_v} \ddot{\delta} = \underbrace{\omega_0 C_2 - V_F \sin(\delta)}_{P_m - P_e} - \dot{\delta}\underbrace{(C_3 V_F \cos(\delta) - C_2)}_{\text{Damping coefficient}} \tag{25}$$

where M_v is the virtual angular momentum of the system, P_m represents the equivalent mechanical power, and P_e represents the equivalent electrical power. The more used inertia constant (H) can be directly expressed in terms of the angular momentum, M_v, rated power, and synchronous speed. Ignoring the damping coefficient, it can be seen that when $P_m > P_e$, the estimated PLL frequency will keep increasing, whereas when $P_m < P_e$, the estimated PLL frequency will keep decreasing which is the same closure as revealed for the quasi-static large-signal analysis. This implies that LOS occurs due to the imbalance in active power between the grid-connected converter and external grid.

The derivation presented in (25) is depicted in Fig. 9, which has the identical form as if performed for a synchronous machine [29]. As it can be seen, to improve the stability by increasing the damping coefficient, C_3 should be increased and C_2 should be decreased. As anticipated, the damping is decreased when the injected current is high or when the fault voltage is low. As it can be seen from the expression of C_3, a high ratio of K_p/K_i can be used to improve the stability. Furthermore, with respect to C_2 for an inductive grid, the damping is maximized when the injected current is purely reactive, which is a positive disclosure

Fig. 9. Block diagram of synchronization model based on the second-order nonlinear equation in (25) derived for an inductive grid [29]. This has an identical structure as that of a synchronous machine where the damping coefficient in (25) is depicted in the green dashed area.

for fault ride-through performance in high-voltage inductive grids. It is important to notice that for an inductive grid during reactive current injection, $C_2 = 0$ and by using strictly positive PLL controller parameters, the damping coefficient will always remain positive no matter the severity of the voltage sag. This is in direct agreement with the steady-state analysis in (8) where the current transfer limit approaches infinity for a low-resistive grid. Moreover, it is in agreement with the quasi-static large-signal model described in (14) where the self-synchronization term v_{q+} approaches zero for inductive grids during fault events. Thus, it can be anticipated that LOS during nearly zero-voltage ride through for inductive grids should not be a problem when complying with grid code requirements. On the other hand, it suggests that the stability of the PLL during a low-voltage fault event depends solely on the line resistance.

Using the second-order nonlinear differential equation for the PLL model, the damping coefficient of the system has been identified and actions to take to improve the stability is proposed. Nevertheless, it is still desired to solve the actual system in order to assess whether LOS will occur or not. To analyze this, two methods will be embodied: EAC used for rotor-angle stability of synchronous machines and phase portraits which is a graphical tool used to solve nonlinear first- and second-order differential equations.

a) Equal Area Criterion (EAC): The EAC is a direct method for assessing the transient stability of a one-machine connected to an infinite bus or a two-machine system without having to solve the nonlinear swing equation. The EAC assumes conservation of energy based on the kinetic and potential energy when evaluating the transient stability of the system. Therefore, this method is only valid under the assumption that the nonconservative damping force is zero. To that end, the assessment based on this method will be more conservative than needed, and could predict a stable system to be unstable. Ignoring the damping coefficient in (25), the following second-order nonlinear differential equation is obtained:

$$\frac{1}{C_1}\ddot{\delta} = X_L I_{\text{PCC}} \cos(\theta_I) - V_F \sin(\delta) \tag{26}$$

which cannot be directly solved analytically due to its nonlinear nature. Multiplying both sides by $d\delta/dt$ gives
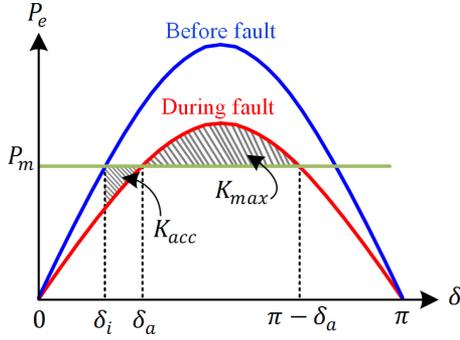
Fig. 10.　P_e and P_m versus δ from (25) is shown for the prefault condition and during the fault. The accelerating area ($K_{\rm acc}$) and maximum decelerating area ($K_{\rm max}$) used to assess the transient synchronization stability are visualized.

$$\frac{1}{C_1}\underbrace{\frac{d\delta}{dt}\frac{d^2\delta}{dt^2}}_{\omega^3} = \underbrace{\frac{d\delta}{dt}}_{\omega}\left(X_L I_{\rm PCC}\cos(\theta_I) - V_F\sin(\delta)\right) \quad (27)$$

which is u

$$\frac{1}{C_1}\omega^2 = X_L I_{\rm PCC}\cos(\theta_I) - V_F\sin(\delta). \quad (28)$$

Performing integration on both sides with respect to δ gives

$$\int\frac{1}{C_1}\omega^2\,d\delta = \int X_L I_{\rm PCC}\cos(\theta_I) - V_F\sin(\delta)\,d\delta. \quad (29)$$

Realizing that the left-hand side equals $\int \omega/C_1\,d\omega$ and introducing integration limits gives

$$\underbrace{\left[\frac{1}{2C_1}\omega^2\right]_{\omega_i}^{\omega_e}}_{\text{Kinetic energy}} = \underbrace{\int_{\delta_i}^{\delta_e} X_L I_{\rm PCC}\cos(\theta_I) - V_F\sin(\delta)\,d\delta}_{\text{Potential energy}} \quad (30)$$

where i and e denote the initial and ending values of the angular velocity and phase angle of the PLL relative to the grid. From (30), it can be seen that the change in kinetic energy is stored as potential energy and vice versa during a transient situation. This means that the total energy of the system, $E_{\rm tot}$, which is constant, can be obtained from summation of the two sides in (30). The accumulated kinetic energy (acceleration area) originating due to the change in potential energy (V_F and injected current) during a fault is

$$K_{\rm acc} = \int_{\delta_i}^{\delta_a} X_L I_{\rm PCC}\cos(\theta_I) - V_F\sin(\delta)\,d\delta \quad (31)$$

where i denotes the initial prefault stable equilibrium point and a denotes the stable equilibrium point during the fault. The stable operating points can be obtained by solving (14) using the impedance, voltage level, and injected current before and during a fault. The maximum possible deceleration area or the critical energy is

$$K_{\rm max} = -\int_{\delta_a}^{\pi-\delta_a} X_L I_{\rm PCC}\cos(\theta_I) - V_F\sin(\delta)\,d\delta. \quad (32)$$

The accelerating and maximum decelerating areas during the fault are visualized in Fig. 10. If $K_{\rm acc} > K_{\rm max}$ when neglecting damping forces, then the power angle (δ) will exceed the point $\pi - \delta_a$ causing the mechanical power (P_m) to once again

exceed the electrical power (P_e), see Fig. 10. This once again enforces the acceleration power to remain positive, leading to LOS since δ will drift away from the stable operating point during the fault. Said in another way, the kinetic energy which is collected during the acceleration period will be larger than the maximum obtainable decelerating energy used to counteract this change. In the case of a grid fault, reactive current injection is required which means that the mechanical power (v_{q+}) becomes negative which as an analogy to synchronous machines can be seen as power being delivered back to the wind. Hence, as seen in Fig. 8, the stable equilibrium point at $\phi_g - \delta$ is negative, meaning that (31) actually represents a deceleration power instead of the conventional acceleration power.

Likewise, as in the presented case for active power injection during the fault (where v_{q+} is positive), if the deceleration power during capacitive reactive current injection is larger than the acceleration power, transient instability occurs. This can be visualized by showing Fig. 10 with a negative mechanical power and plotted in the interval $-\pi \leq \delta \leq 0$. The derivation of EAC is done for an inductive grid but can easily be extended to a resistive grid simply by letting $C_1 \rightarrow K_i$ and $X_L\cos(\theta_I) \rightarrow R_L\sin(\theta_I)$ in the presented analysis (26)–(32). Since no system exhibits zero damping, this method could introduce a wrong stability prediction in a conservative manner. To assess the stability of the system including damping, the use of phase portraits is examined.

b) Phase portraits: First- and second-order nonlinear differential equations which cannot be solved directly using any analytical tools can be solved graphically using phase portraits [50]. Consider a second-order nonlinear system

$$\dot{\mathbf{x}} = \mathbf{f}(\mathbf{x}) \quad (33)$$

where $\mathbf{x} = (x_1, x_2)$ and $\mathbf{f}(\mathbf{x}) = (f_1(\mathbf{x}), f_2(\mathbf{x}))$. The solution of $\mathbf{x}(t)$ can be presented graphically as a trajectory of the points of the dynamic system in the $(\mathbf{x}, \dot{\mathbf{x}})$ phase-plane for a given initial condition. This is also known as the phase-plane analysis or phase portrait of the problem which has a unique solution given that $\mathbf{f}$ is continuously differentiable [50].

For a resistive line, the second-order nonlinear system can be written as

$$\dot{x}_1 = x_2$$
$$\dot{x}_2 = -K_p V_F\cos(x_1)x_2$$
$$+ K_i\left(R_L I_{\rm PCC}\sin(\theta_I) - V_F\sin(x_1)\right) \quad (34)$$

where $x_1 = \delta$, $x_2 = \dot{x}_1 = \dot{\delta}$, and the initial condition is obtained from (18) to be

$$\dot{\delta}_{i,R} = K_p R_L I_{\rm PCC}\sin(\theta_I)\quad\text{for}\quad \delta_{i,R} = 0 \quad (35)$$

knowing that the PLL integrator cannot change its value instantaneously when the fault occurs. Similarly in the case of an inductive line, the system becomes

$$\dot{x}_1 = x_2$$
$$\dot{x}_2 = x_2 C_1\left(C_2 - C_3 V_F\cos(x_1)\right)$$
$$- C_1\left(\omega_0 C_2 - V_F\sin(x_1)\right) \quad (36)$$

TABLE II
PARAMETERS OF CONSIDERED CASE STUDIES

Symbol	Description	Case 1	Case 2	Case 3
K_p	Proportional gain of PLL	0.4	2	0.4
K_i	Integral gain of PLL	25	25	25
$K_{p,ci}$	Proportional gain of G_{ci}	20	20	20
$K_{r,ci}$	Resonant gain of G_{ci}	10e3	10e3	10e3
$\mathbf{Z_L}$	Line impedance	0.04 pu	0.04 pu	0.1j pu
V_F	Fault voltage magnitude	0.05 pu	0.05 pu	0.05 pu
I_{PCC}	Fault current magnitude	1 pu	1 pu	1 pu

with the initial condition

$$\dot{\delta}_{i,L} = \frac{K_p \omega_0 C_2}{1 - K_p C_2} \quad \text{for} \quad \delta_{i,L} = 0. \quad (37)$$

V. COMPARISON OF STABILITY ASSESSMENT METHODS

To benchmark the different methods, these are tested in simulation and experimentally on a system as shown in Fig. 1. For the simulation model and in the experimental test setup, the grid impedance and fault impedance is not considered since the programmable three-phase ac source, used to emulate the voltage at the fault location directly as shown in Fig. 5(b), has a negligible internal impedance. Due to a limited resolution of both the programmable three-phase ac source and the measurement system of the converter, a low signal-to-noise ratio will occur when considering extremely low voltages. Apart from the programmable source not being able to generate a smooth sinusoidal voltage at any low-voltage level, the resolution of the PCC fault voltage captured with the measurement circuit is low. This will significantly degrade the dynamic performance of the PLL and, consequently, the entire converter behavior during the fault. Therefore, a fault voltage magnitude of 0.05 pu is selected as a trade-off between a desired low-voltage magnitude and an acceptable signal-to-noise ratio of the system.

The grid synchronization is performed using a conventional SRF-PLL (Fig. 2) without any normalization introduced to the measured PCC voltage. In this case, for a decreasing PCC voltage, the equivalent gain and bandwidth of the PLL will be reduced. This choice can both have advantages and disadvantages. Considering a fault voltage magnitude approaching zero, so will the bandwidth of the PLL. This provides a similar response to a frozen/blocked PLL which can be utilized for riding through faults with low voltages as proposed in [31]. However, as mentioned, with a decreased bandwidth of the PLL during a fault, the dynamic response of the converter will be significantly deteriorated which can cause potential challenges with respect to accomplishing a fast reactive current provision alongside an acceptable fault recovery process.

Three case studies are used to compare the different methods which are listed in Table II together with controller parameters for the inner current controller and SRF-PLL. Cases 1 and 2 address a resistive line impedance, whereas an inductive line impedance is considered in Case 3.

To verify the theoretical analysis performed in Section IV, time-domain simulations are carried out using MATLABs,

Simulink, and PLECS Blockset. The main circuit parameters are shown in Table I, whereas the controller parameters and circuit parameters which are varied for different case studies can be seen in Table II.

A. Steady-State Network Analysis

Using (8), it is observed that with reactive current injection of 1 pu, the fault voltage magnitude should be larger than the line resistance in order to have a stable steady-state operating point. As $V_F > R_L$ for Case 1 and Case 2, the fault response of these two cases are predicted to be stable. In case of reactive current injection into an inductive grid, the current transfer limit according to the steady-state analysis is infinite; hence, Case 3 is predicted to be stable as well.

B. Quasi-Static Large-Signal Analysis

Using the constraint of current injection as presented in (16), the stability prognosis would be identical to the one just presented for the steady-state analysis. Therefore, a time-domain simulation is instead performed on the nonlinear system seen in Fig. 7 using $V_{th} = V_F$, $K_g = 1$, $K_c = Z_L$, and $\phi_g = 0$. Alongside the simulation study of the quasi-static large-signal model, two additional simulations with different levels of accuracy are carried out. This is done to visualize the information lost by the assumptions made for the quasi-static model where the converter is modeled as a controlled current source. The additional models comprise an averaged converter model and a detailed switching model of the converter. The averaged model represents a continuous-time average model of the system where the influence of the LCL filter, the current regulator, and delays are included, whereas the PWM operation of the converter is represented as a controlled voltage source. The only difference between the quasi-static model and the averaged model is the inclusion of the dynamics associated with the current controller. The switching model is identical to the averaged converter model but without the assumption of an averaged representation of the converter's PWM operation. The simulation study for Case 1 for the three types of simulations are shown in Fig. 11. Here, it is evident that the quasi-static model is capable of a correct stability prediction with a behavior quite similar to the detailed switching model. Furthermore, the simplified model actually shows a faster decline in estimated frequency, i.e., a more severe LOS, which indicates that the quasi-static model during reactive current injection could result in a tiny conservative stability forecast compared to the detailed simulation model. This is subjected to be due to the fact that the current regulator of the detailed simulation model does not regulate the current error signal to zero immediately. During this time, the loss of stability is actually less severe compared to the case where the injected current is assumed to be equal to its reference value.

The discrepancy between the quasi-static model and the detailed model lies in the disregard of the current controller. This claim is validated by including the actual injected current into the quasi-static model, i.e., including the current controller dynamics. This is equivalent to the averaged model in Fig. 11, which is indistinguishable from the detailed switching model.
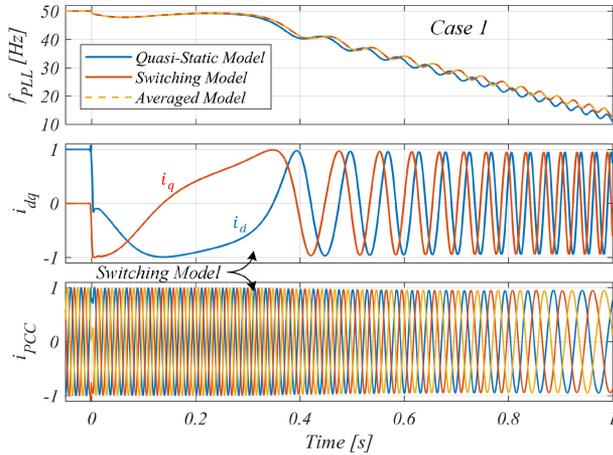
Fig. 11. PLL frequency response for quasi-static model, averaged model, and a detailed switching model for Case 1 where a severe three-phase fault (0.05 pu) appears at 0 s. Subplots 2 and 3 contain the per-unit dq-axes and three-phase injected currents obtained from the switching model.
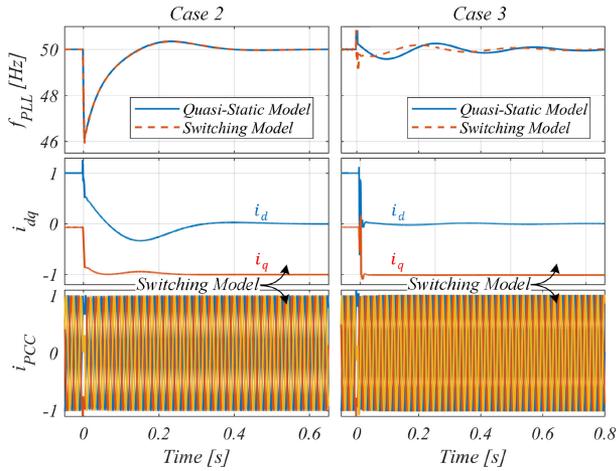

Fig. 12. PLL frequency response for quasi-static model and the detailed switching model for Case 2 and Case 3 where a severe three-phase fault (0.05 pu) appears at 0 s. Subplots 2 and 3 contain the per-unit dq-axes and three-phase injected currents obtained from the switching model.

Besides the PLL frequency, the dq-axes currents and injected three-phase currents are visualized in Fig. 11 for Case 1. Here, it can be seen that the decreasing frequency makes the dq currents to rotate in the negative direction toward -50 Hz as the PLL frequency approaches 0 Hz. Also, as anticipated, the frequency of the injected currents decrease with the decreasing PLL frequency. It must be noted that the dq-axes currents shown in Fig. 11 are referenced to the actual rotating frame of the PCC voltage, when in fact the current controller is fully tracking its reference values but in an incorrectly oriented reference frame established by the PLL.

The response during a severe symmetrical fault for Case 2 and Case 3 is visualized in Fig. 12. As it can be seen for Case 2, which is the resistive grid, the quasi-static model exactly matches the detailed simulation. To that end, as indicated earlier, increasing the damping coefficient of the PLL (increasing K_p) enables the controller to ride through the fault without losing stability. For the inductive grid (Case 3), the stable response quickly settles but discrepancies in the oscillating frequency is seen between
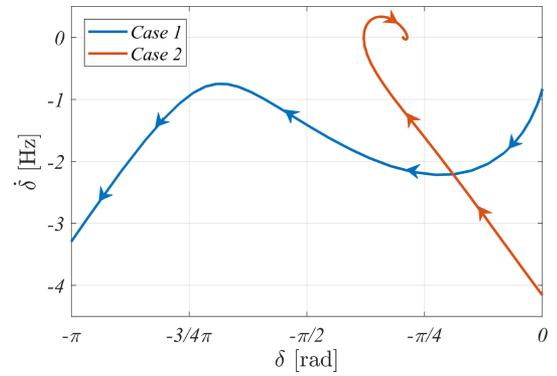
Fig. 13. Stability prediction of Case 1 and Case 2 using phase portraits. Case 2 converges to the stable equilibrium point during the fault.

quasi-static model and the detailed simulation model. This is subjected to be caused by the assumptions made for the current controller since the inductance has a larger influence on the transient response at the fault instant (resist to change in current) than in case of a resistive line. Besides this, the response is seen to be stable as anticipated by the analytical analysis performed earlier. The responses for Case 2 and Case 3 from Fig. 12 are clearly seen to be stable as the grid currents and dq-axes currents track their references and stays at 50 Hz.

C. Equal Area Criterion (EAC)

Calculating the stable operating point before and during the fault (δ_i and δ_a) using (14), one can use (31) and (32) to calculate the accelerating and decelerating power of the transient response during the fault. Inserting the values of each case study as seen in Table II, the EAC forecasts Case 1 to be unstable, Case 2 to be unstable, and Case 3 to be stable. Since damping is neglected using this method and knowing that Case 1 does not possess sufficient damping to remain stable, it is clear that the EAC method is correct in this case. However, for Case 2, the assumption that damping is zero results in a conservative and wrong prediction.

D. Phase Portraits

At last, the three case studies are analyzed using phase portraits where (34) and (35) are used for the resistive line impedance (Case 1 and Case 2) and (36) and (37) are used for the inductive line in Case 3. As it can be seen in Fig. 13, Case 1 is shown to be unstable, whereas increasing the damping coefficient by increasing the proportional gain of the PLL gives sufficient controller robustness to remain stable during the fault. As it is evident for Case 2, the PLL phase arrives at a new stable operating point during the fault. This point matches exactly the stable operating point seen from the corresponding case in Fig. 8 (the dark blue line). Here, it should be mentioned that the stable equilibrium point during the fault is identical for Case 1 and Case 2; nevertheless, for Case 1, the damping of the PLL is not sufficient for the solution to be attracted to the stable equilibrium point. Case 3 is predicted to be stable using phase portraits and it is not included here since the PLL angle deviation was too low to be properly visualized in a graph.
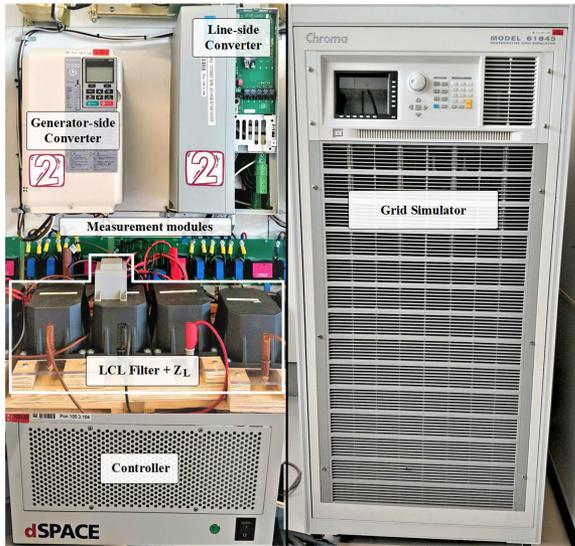
Fig. 14. Laboratory setup used to validate the reviewed methods. The line-side converter is regulated using a dSPACE control platform to inject currents through an LCL filter into a grid simulator.

E. Experimental Verification

In order to validate the simulation model and compare the credibility of the studied methods, experimental tests are conducted on an LCL-filtered VSC connected to the grid through a line impedance, Z_L, which is shown in Fig. 14. The control is performed on a Danfoss frequency converter and a separate converter is installed in a back-to-back configuration to provide a constant dc-link voltage for the VSC. The control system is implemented in a dSPACE DS1007 system which is fully programmable from the block diagram environment in Simulink. A DS2004 high-speed 16-bit A/D board is used for sampling of the voltage and current measurements and a digital output board, DS5101, is used for PWM generation. The grid voltage is established using a regenerative grid simulator manufactured by Chroma. Circuit and controller parameters are identical to the values used for the simulation and theoretical analysis.

The experimental tests of the three case studies are presented in Fig. 15. Here, all three cases can be seen to match the predicted behavior and stability assessment shown for the quasi-static large-signal analysis. It is verified that during a severe symmetrical fault, the synchronization stability of the PLL can be improved by increasing the proportional gain of the PLL as it can be seen in Case 2 in Fig. 15. Nevertheless, it should be noted that even though the damping of the system is increased for Case 2, which permits system stability, any noise and disturbances in the PLL synchronization loop will be amplified which is seen in Case 2 as large steady-state frequency ripples. Furthermore, as pointed out in [51], [52], an increasing proportional gain of the PLL will increase the frequency where the phase characteristics cross $-180°$ which degrades the stability. Therefore, instead of increasing the proportional gain of the PLL, one could increase the system damping by decreasing the integral gain. This is tested and shown in Fig. 16 where the system still remains stable due to the increased damping. As expected, the steady-state frequency ripple is decreased at the cost of a slower dynamic
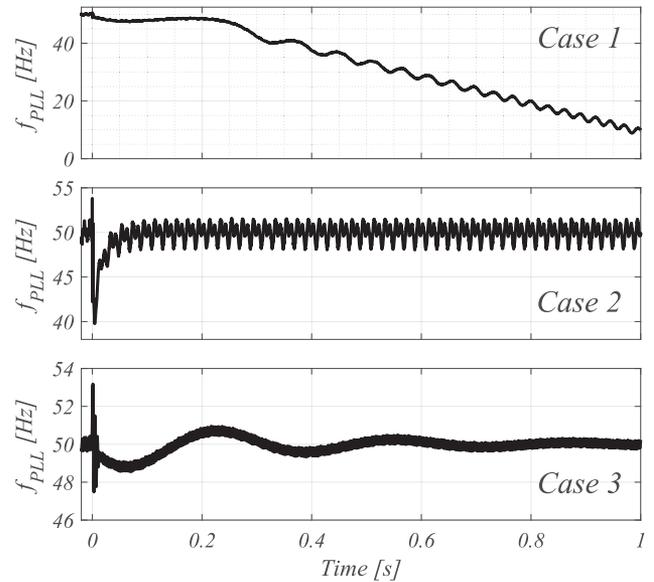

Fig. 15. Experimental results of Cases 1, 2, and 3 showing the estimated frequency performed by the PLL where a severe symmetrical fault occurs at 0 s.
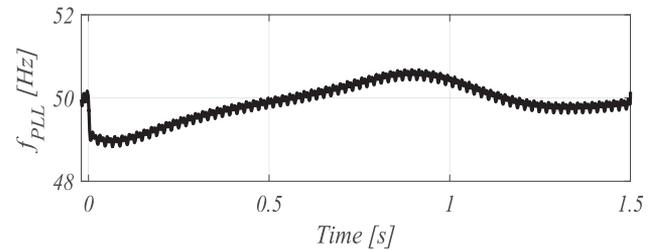

Fig. 16. Experimental result of Case 2 where the integral gain (K_i) is reduced to 5 and the proportional gain (K_p) is kept at 0.4 in order to achieve the same controller parameter ratio but with a slower response. Severe symmetrical fault occurs at 0 s.

performance. Thus, dependent on whether a fast dynamic performance, an accurate steady-state frequency estimation or a mixture of the two is desired, the damping term can be selected accordingly. A zoomed view of the experimental PCC voltages and injected currents from Case 2 are shown in Fig. 17. As it is expected from the frequency response for Case 2, the converter remains synchronized with the grid and quickly prioritizes reactive power injection during the fault. It should be mentioned that since the grid impedance in Case 2 is exclusively resistive, injection of reactive power does not support the PCC voltage which clarifies why these are still 0.05 pu during the fault.

As anticipated, the experimental results of Case 3 shows a stable response with a slow oscillating frequency as seen in Fig. 12.

It should be noted from Fig. 15 that when considering a severe symmetrical fault for up to 150 ms as seen in Fig. 3, the estimated PLL frequency of Case 1 will not have enough time to actually deviate too much from the nominal frequency. Therefore, from a practical application point of view, one might not care if the system is actually unstable if the fault is cleared before the instability becomes too critical. In light of this, the PLL could
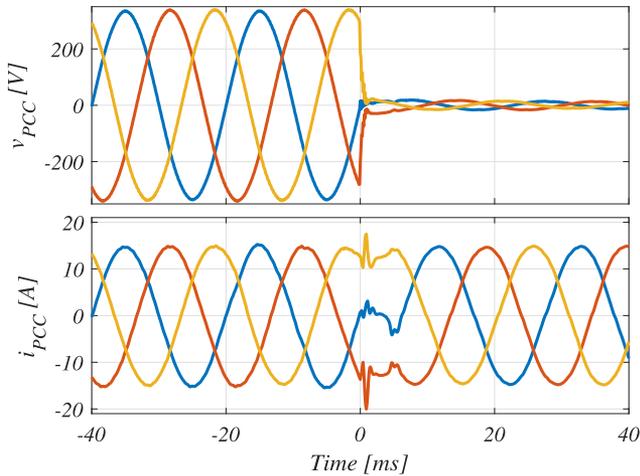
Fig. 17.   Experimental result of Case 2 where the voltages and current at the PCC are shown. The PCC voltage suddenly drops to 0.05 pu during the fault and the converter injects reactive power into the grid.

simply be tuned very slow, such that the estimated frequency would almost not change from its nominal value during a fault. However, in the case of any phase jumps in the PCC voltage during the fault, a slow PLL would not be able to correctly synchronize within 20 ms, which is required by the grid code. Therefore, predictability of the stability of the synchronization process is important in order for the PLL to be able to respond to any further grid disturbances.

Remark for Case 3: For an inductive line impedance during a low-voltage event where it is assumed that the current controller follows its set point and the resistive part of the line is zero, instability will not occur no matter of the voltage sag considered. This is as claimed earlier, that for a purely inductive grid during reactive current injection, synchronization issues are avoided. Nevertheless, none of the aforementioned assumptions that permit this reasoning are fulfilled in general.

At first, whether a stable equilibrium point exists during reactive current injection is determined based on the fault voltage magnitude, the magnitude of the injected current, and the line resistance. Thus, for a nonzero resistance, steady-state instability occurs for some deep voltage sag. Second, the inductance of the line impedance has a large influence on the performance and stability of the inner current controller which in this case can be destabilized even though a stable operating point exists and LOS is avoided.

Moreover, at the fault event instant, the converter is injecting active current which means that the robustness of the current controller is essential for actually arriving at the stable equilibrium point in the first place. Along these lines, even though the PLL might be able to synchronize for any inductive impedance, the inner control loop regulating the injected current might become unstable. This means that the argument presented in Section IV-C, which says that a purely inductive grid will never cause instability during reactive current injection, should be understood with the aforementioned points in mind.

Remark on control solutions for LOS: Throughout this section, the developed methods for assessing synchronization

stability during three cases of a severe symmetrical fault have been tested and experimentally verified. This can then be applied to evaluate the advantages and disadvantages of each method as it will be done subsequently. Apart from this, one may ask, now that the different methods have been tested, what can be done controlwise in order to obtain a stable system considering a case where no steady-state equilibrium point exists during the fault. As mentioned previously, several studies have proposed methods to stabilize such systems [21], [27], [30], [31], [33], which all can provide stability considering such a scenario. As zero current injection described in [33] does not comply with the grid code and that estimation of the X/R ratio of the network impedance is unattractive [27], these methods are not considered as viable methods for a practical implementation. More promising is the method described in [21], [30] where the active current reference is modified based on the PLL frequency error which does not need any additional knowledge of the external network. Perhaps, most compelling is the method of freezing or blocking the PLL as described in [31]. In this case, there is no need for any additional control loop and the state of the PLL is simply frozen at the prefault value in case the voltage decrease is too severe for the stability to be retained. There are, however, several disadvantages of this method including an exacerbated postfault recovery process together with its disability to detect phase jumps, which has a large impact on the actual fault response of the converter. These shortcomings are described in more details in Section VI.

F. Performance Mapping of Reviewed Methods

To allow for a clear and accessible comparison between the different methods, their ability to foresee a correct stability assessment along with a rating of different useful metrics are characterized in Table III. As it can be noted, both the quasi-static large-signal model and phase portraits are able to foresee the correct consequence of the fault, whereas the steady-state model and EAC are unable to correctly predict the stability of Case 1 and Case 2 from the arranged case studies. Besides the stability prediction capability marked with ✔ and ✗, grades are given on the complexity, provision of physical insight, the assumptions needed, and the prediction credibility of each method.

As anticipated, the higher the complexity is of the model used to represent the nonlinear system, a more accurate stability prediction is achieved. Although the quasi-static model and phase portraits are based on the same assumptions and circuit model, the complexity of phase portrait are rated higher due to the direct implementation and manipulation of the nonlinear differential equation when solving the problem. EAC and phase portrait are set to have low physical insight to the problem due to its ability only to guess whether the system remains stable or not. Nevertheless, if the derived equations analogues to a synchronous machine are considered, a high physical insight is achieved since the terms contributing to damping as well as the positive and negative feedback terms discovered in the quasi-static model are revealed. Since the steady-state injection limits and the EAC includes strong assumptions, these are stated as the prediction methods with the least credibility. Along these

TABLE III
COMPARISON OF STABILITY PREDICTION CAPABILITY OF REVIEWED METHODS

Analysis Method	Case 1	Case 2	Case 3	Complexity	Physical Insight	Necessity of Assumptions	Credibility of Prediction
Steady-State	✗	✔	✔	low	medium	high	low
Quasi-Static Large-Signal	✔	✔	✔	medium	high	low	medium
Equal Area Criterion	✔	✗	✔	medium	low	medium	low/medium
Phase Portraits	✔	✔	✔	high	low	low	medium
Actual Response	Unstable	Stable	Stable				

✔: Correct Prediction   ✗: Incorrect Prediction

lines, since the quasi-static model and phase portrait both ignore the effect of the inner current controller and LCL filter, their prediction credibility can be improved.

VI. FUTURE TRENDS AND UNRESOLVED CHALLENGES

As mentioned, none of the presented methods consider the internal converter dynamics including LCL filter and inner current regulator. To improve the credibility of the stability assessment, one could attempt to remove the assumption that the injected current equals its reference value from the model. However, even though the credibility would be improved, the stability assessment model would approach a detailed simulation model which does not provide any additional insight and tuning guidelines.

Instead, it could be desirable to return to the aim introduced for the steady-state model where the injection constraints are derived to ensure stability under some given assumptions. For the quasi-static or an improved version of that, a design guideline of PLL controller parameters which ensures sufficient damping to remain stable would be highly appreciated. Today, the PLL is usually tuned only considering the negative feedback loop (grid-synchronization loop), whereas it might be beneficial to also include the positive feedback loop (self-synchronization loop) in Fig. 7 to improve the overall controller performance. As low-voltage fault events are comparable to weak grid conditions seen from the PLL stability point of view, publications outlining the impact of the tuning procedure for the PLL during weak grid conditions may be applicable here. This includes controllers directed to compensate the destabilizing effect of weak grid conditions as what is here referred to as the self-synchronization loop. For instance, it is described in [53] that for very weak connections, the power transfer capability is significantly reduced and the proportional gain of the PLL should be reduced to avoid instability. In [54], a virtual impedance structure is implemented in the PLL to counteract the destabilizing effect of the self-synchronization loop by canceling the influence of the large grid impedance. This is proven to extend the power transfer capability and consequently improve the synchronization stability due to the converter being virtually synchronized to a stronger point in the system. Alternatively, a PLL-less synchronization mechanism can be applied to improve the robustness against weak grid conditions including power synchronization control [55], or any other control with the objective to emulate a synchronous machine. Here, the synchronization is performed through transient active power transfer which during large disturbances might not be preserved due to converter current limitation. Apart from that, the approach of controller parameters

which can be changed adaptively in the case of grid abnormalities as, e.g., proposed in [56] or by simply applying adaptive voltage normalization, may be profitable to analyze with respect to any potential stability improvements regarding LOS.

Besides including further information regarding the current controller and LCL filter, knowledge about how LOS is influenced in a multiconverter system consisting of various paralleled converter, e.g., in a wind farm string with long cables, is not well documented within prior art. Obviously, if, i.e., the quasi-static model is modified to include the dynamics of the inner current regulator, its complexity increases and its ability for a trained engineer to clearly grasp the stability phenomena is diminished. Thus, for a multiconverter system, it is not necessarily practical or even computationally wise possible to construct a detailed complex model for each converter system in order to assess local and global synchronization issues. So reduced simplified models, which capture only the essential information of the system, could be a more pertinent way to perform LOS assessment of large-scale systems. Although this is still an unresolved problem, several recent publications [57], [58], among others, propose model-order reduction methods within the field of paralleled grid-connected converters and weak grid conditions such as inverter-based microgrids.

In addition to possible improvements and modifications to LOS modeling, a few remarks on how to deal with transient stability in a more solution-oriented manner is given. It was described in Section IV-B that even though a stable operating point exists during the fault period, the dynamics of the PLL might result in an overshoot making the PLL unable to arrive at that equilibrium point. The analysis performed in all of the aforementioned methods state whether a given fault scenario would result in a stable or unstable system. However, considering a short-term fault, the opposite scenario might be possible. This is when the overall converter system is unstable with respect to the steady-state fault condition but due to a short duration of the fault, still able to return to a stable steady-state operation after the fault has been cleared. In such a case, one can identify the critical clearing time, which is the maximum duration of the fault for which the prefault conditions can be reestablished. Therefore, as highly utilized for transient stability analysis for synchronous machines together with relay and circuit breaker coordination, this concept have also been adopted by power electronic based integration of RES [59].

To that end, instead of ensuring a high damping coefficient of the synchronization unit to improve its robustness against LOS, one may apply low bandwidth PLL or simply freeze the PLL during the fault [31]. The meaning of this is of practical interest

since the fault in a lifelike situation is often cleared within a few fundamental cycles. Consequently, it does not matter whether the system is steady-state stable or not during the fault since the PLL will not deviate much from its initial conditions and is, therefore, able to return to a stable operating point after the fault, i.e., the fault duration is less than the critical clearing time of the system. There is, however, one critical issue associated with such a solution. At the instant of a grid fault, phase jumps often occur in the PCC voltage. Thus, considering a frozen or extremely slow PLL, such a change will not be detected and the injected currents will not comply with the reactive current provision required by the grid code. On the other hand, one may argue that if the voltage at the PCC is reaching such extremely low values and taking into account the current limitation of the converter, the system will not be able to support the grid voltage much anyway. Alongside this, it is desired to have a dynamically fast PLL and a slow synchronization unit prolongs the postfault recovery process [60]. Based on this, it is still an open question how LOS should be managed in future power electronic based power systems. Possible solutions comprise careful PLL design based on stability criteria from reviewed methods, adaptive controller modification of the PLL during the fault, or simply using a low/zero bandwidth PLL during the fault.

At last, the equation governing the large-signal stability of the PLL is, as shown, a second-order nonlinear differential equation which does not have any known analytical solution. Therefore, the different methods reviewed throughout this paper comprise the state-of-the-art regarding possible methods to analyze and understand such complicated systems and their transient stability. One method is not described, which is highly used for nonlinear system analysis within the fields of control theory, mechanics, and power system engineering, is the Lyapunov method. Actually, as described in [61], the EAC method, is a special case of Lyapunov's method and the utilization of energy functions. However, this was developed without considering any dissipative forces. In the light of this, it could be fruitful to modify the Lyapunov function to take into account system damping applicable to the studied synchronization unit. As shown in [62], a Lyapunov function exists for a general lossy one-machine-infinite-bus system but how to actually construct such a function may be a challenge. Therefore, how to develop an appropriate Lyapunov function and how to apply it to analyze LOS of grid-connected converters is, to the best knowledge of the authors, still an unresolved challenge interior to the field of direct methods of synchronization stability for VSCs. This may be used to define more accurate conditions for stability including possible tuning guidelines and control actions directed toward an increased system robustness and prevention of system destabilization during severe grid faults.

VII. Conclusion

Grid-connected converters exposed to severe symmetrical fault events are at risk of losing its ability to remain synchronized with the grid which immediately leads to local instability and utmost global destabilization of the power system. This issue is of special concern for future power electronic based power systems which will be dominated by a high integration of converter-based RES. This paper has carried out a comprehensive investigation of methods used to assess synchronization stability together with a description of what causes LOS of grid-connected converters during severe symmetrical faults. State-of-the-art models and methods aiming to reveal the LOS mechanism is rigorously reviewed and a comparison between them is provided to carefully explain how synchronization stability should be understood, what elements are provoking LOS as well as what actions that should be taken to lower the risk of synchronization instability. The reviewed methods aiming to assess the synchronization stability are tested through three case studies exposed to a severe symmetrical grid fault. The first method presented is a model constraining the injected current based on achieving a stable steady-state equilibrium points. This is extended to analysis of the quasi-static large-signal model incorporating the internal dynamics of the SRF-PLL. Hereafter, it is shown that the description of the synchronization process is analogous to the mathematical equations governing a synchronous machine where terms contributing to system damping are identified. From this, it is explicitly disclosed that the stability is degraded under high current injection, low grid voltages, and high grid impedances. Furthermore, it is demonstrated that the damping coefficient of the system, which improves the robustness against instability, can be raised by increasing the proportional gain of the PLL or decreasing the integral gain of the PLL. At last, a nonlinear tool capable of solving the problem graphically is examined. Since most prior art describing LOS are tested during active current injection, this paper exclusively targets the synchronization stability during low-voltage fault events where the converter is enslaved to comply with grid-code requirements, i.e., reactive current injection. The analyzed methods are compared against a detailed simulation model where their individual advantages and disadvantages are mapped. The analytical study is validated through experimental laboratory tests performed on a grid-connected converter exposed to a severe symmetrical fault. From the conducted overview study, there is still a need for a direct method to assess the synchronization stability of grid-connected converters including the damping coefficient of the nonlinear synchronization unit. Such a method might be based on the use of Lyapunov's method and energy functions but additional research is needed in this field to fully answer this question.

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