A 1-MHz Series Resonant DC–DC Converter With a Dual-Mode Rectifier for PV Microinverters

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***Abstract*—The photovoltaic (PV) output voltage varies over a wide range depending on operating conditions. Thus, the PV-connected converters should be capable of handling a wide input voltage range while maintaining high efficiencies. This paper proposes a new series resonant dc–dc converter for PV microinverter applications. Compared with the conventional series resonant converter, a dual-mode rectifier is configured on the secondary side, which enables a twofold voltage gain range for the proposed converter with a fixed-frequency phase-shift modulation scheme. The zero-voltage switching turn-ON and zero-current switching turn-OFF can be achieved for active switches and diodes, thereby, minimizing the switching losses. Moreover, a variable dc-link voltage control scheme is introduced to the proposed converter, leading to a further efficiency improvement and input-voltage-range extension. The operation principle and essential characteristics (e.g., voltage gain, soft-switching, and root-mean-square current) of the proposed converter are detailed in this paper, and the power loss modeling and design optimization of components are also presented. A 1-MHz 250-W converter prototype with an input voltage range of 17–43 V is built and tested to verify the feasibility of the proposed converter.**

***Index Terms*—1-MHz frequency, dc–dc converter, photovoltaic (PV) microinverter, series resonant converter (SRC), wide input voltage range.**

I. Introduction

COMPARED with central and string photovoltaic (PV) inverters, microinverters are favorable in low-power applications, due to the capability of the module-level maximum power point tracking (MPPT), low installation efforts, easy monitoring and failure detection, and low maintenance cost [1]–[3]. Nevertheless, certain challenges remain for PV microinverters, which are as follows.

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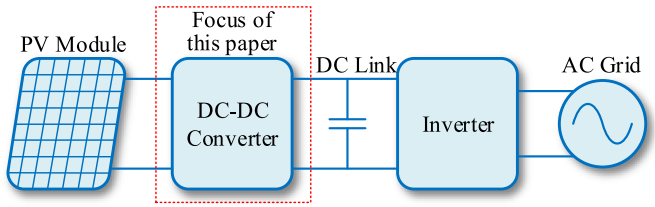

Fig. 1. Configuration of a two-stage grid-connected PV microinverter system.

1) The efficiency performance of microinverters is relatively low compared with string inverters (e.g., the peak efficiency is around 99.2% in [4]).
2) There is a trend that microinverters will be incorporated into PV modules in the future [5], [6], which implies that microinverters should be more compact (i.e., high power density and low profile).
3) Panel-embedded microinverters may be inevitably heated up by the PV panels, accelerating the degradation [7], [8].

Improving the power conversion efficiency and reducing power losses can be an effective way to enhance the energy yield and reliability of PV microinverters [3], [9].

In the literature, three power conversion structures can be found for PV microinverters, i.e., the high-frequency-link (single-stage) microinverter [10], pseudo-dc-link microinverter [11], and dc-link (two-stage) microinverter [12], [13]. The dc-link microinverters have the advantages of simpler structure, lower power decoupling capacitance, and easier performance optimization for each stage; therefore, recently, they attracted much interest [6], [9], [12]–[16]. Fig. 1 shows the configuration of a two-stage grid-connected PV microinverter system. Typically, the front-end dc–dc converter is controlled to achieve the MPPT of the PV module. Depending on the module characteristics and the operating conditions (i.e., the solar irradiance and ambient temperature), the output voltages of PV modules at maximum power points (MPPs) vary over a wide range (e.g., 20–40 V). Therefore, the dc–dc converter should be able to handle a wide input voltage range while maintaining high efficiencies. It is also required that the dc–dc converter should boost the low-voltage (< 50 V [6]) PV module output to a desired high voltage (at the dc link) in order to feed a grid-connected or standalone inverter [17]. Preferably, a high-frequency transformer is inserted into the front-end dc–dc stage to achieve the galvanic isolation, leakage current elimination, and a high voltage-boost ratio [13]. Furthermore, in order to reduce the system profile,

it is required to increase the switching frequency and/or adopt low-profile passive components (e.g., planar magnetics [18] and low-profile decoupling capacitors [19]).

Traditional flyback converters with snubbers or active clamping circuits are simple in topology and low in cost; therefore, they are adopted as the front-end dc–dc stage in some microinverters [20], [21]. However, the voltage stress of the primary switches is high, and thus, low-voltage MOSFETs with low ON-state resistances cannot be used [22], [23]. In the phase-shift full-bridge dc–dc converter, the primary switches can achieve zero-voltage switching (ZVS); however, it is challenged when operating in a wide voltage gain range, e.g., the narrow ZVS range for the lagging leg switches, duty cycle loss, large circulating current, and voltage spikes across the output diodes [24].

The *LLC* resonant converter is a promising topology in terms of high efficiency and high power density [24]–[27]. However, the primary concern for this topology is that the voltage gain range is not wide, and thus, hybrid control schemes [28]–[30] have to be applied, which increases the realization complexity of the MPPT. For instance, a full-bridge *LLC* resonant converter is designed for PV applications in [28]; however, the burst mode control has to be used in addition to the variable frequency control. In [29], a hybrid control combining the pulse-frequency modulation (PFM) and phase-shift pulsewidth modulation (PS-PWM) is employed to a full-bridge *LLC* resonant converter to improve the efficiency, but the control complexity is significantly increased as well.

In addition to the hybrid control schemes, many modified *LLC* resonant converter topologies have been proposed [17], [31]–[41]. Structural modifications can be made to the primary-side inverter [31]–[35], the secondary-side rectifier [36]–[38], and the transformer/resonant tank [39]–[41]. Instead of the conventional half-bridge or full-bridge structure, a variable frequency multiplier is applied to the *LLC* resonant tank to extend the voltage gain range while maintaining high efficiencies [32]. In [33], the primary-side full-bridge inverter is replaced by a dual-bridge inverter; thus, a multi-level ac voltage can be applied to the resonant tank, and a twofold voltage gain range can be achieved; however, the primary-side switches have high turn-OFF currents, and may suffer from high off-switching losses when operating in high step-up applications (e.g., PV microinverters). By combining a boost converter with an *LLC* resonant converter, two current-fed *LLC* resonant converters are proposed in [34] and [35]. Nevertheless, the primary-side switches share uneven current stresses, which may lead to high conduction losses as well as high OFF-switching losses. To avoid the high OFF-switching losses on the high-current primary-side switches, [36]–[38] propose secondary-rectifier-modified *LLC* resonant converter topologies. Specifically, in [36] and [37], two diodes in the full-bridge rectifier (FBR) are replaced with two active switches, yielding a controllable rectifier. In [38], two active switches are utilized to obtain a reconfigurable voltage multiplier rectifier, leading to a squeezed switching frequency range and improved efficiencies over a wide input voltage range; notably, the number of rectifier components is high (eight diodes + two active switches + six capacitors), and thus, this topology may not be cost effective for PV microinverter applications. Furthermore, [39]–[41] modify the transformer and resonant tank to extend the voltage gain range of the *LLC* resonant converter. In [39], an auxiliary transformer, a bidirectional switch (implemented with two MOSFETs in an anti-series connection), and an extra FBR are added to the conventional *LLC* resonant converter. Thus, the equivalent transformer turns ratio and magnetizing inductance can be adaptively changed in order to achieve a wide voltage gain range; however, the component count is high and the transformers utilization ratio is relatively low. To address the issues in [39] as well as to maintain high efficiencies over a wide input voltage range, *Sun et al.* [41] proposed a new *LLC* resonant converter with two split resonant branches; in this way, two operation modes, i.e., the low- and medium-gain modes, are enabled, and the gain range for mode transition is 1.5 times, leading to a smoother efficiency curve over the gain range. Moreover, in [40], a new transformer plus rectifier structure with fractional and reconfigurable effective turns ratios is proposed for a widely varying voltage gain.

As aforementioned, there is a trend to increase the switching frequency and lower the converter profile such that the microinverter can be mechanically and physically integrated with a PV module [5], [6]. Therefore, the megahertz operation and design optimization of resonant dc–dc converters [42]–[48] are becoming attractive to achieve so. Notably, the reported peak efficiency of a 1-MHz *LLC* resonant converter has reached 97.6% with an optimal design of the integrated planar matrix transformer [46]. However, the voltage conversion ratios in these systems are fixed [43]–[48] or vary within a narrow range (±5%) [42], which is not suitable for PV microinverter applications where the dc–dc stage should handle a wide voltage gain range.

In light of the aforementioned, this paper proposes a new dual-mode rectifier (DMR)-based series resonant dc–dc converter for PV microinverter systems. A twofold voltage gain range can be achieved with a fixed-frequency phase-shift modulation scheme. The active switches can turn ON under zero-voltage switching (ZVS) and the rectifier diodes can turn OFF under zero-current switching (ZCS), leading to minimized switching losses. Also, a variable dc-link voltage control is applied, yielding a significant efficiency improvement and input-voltage-range extension. The experimental tests on a 1-MHz microinverter prototype show that the proposed converter can achieve high efficiencies over a wide input voltage range, i.e., 17–43 V.

This paper is an expansion of our previous conference publication in [49] by adding two topology derivatives, detailed characteristics analysis, power loss modeling and design optimization of components, and 1-MHz experimental verifications. The contributions of this paper are summarized as follows.

1) Three DMR-based series resonant dc–dc converter topologies are proposed for PV microinverter systems.
2) The operation principle, critical characteristics (including voltage gain, root-mean-square current, and soft switching), and design optimization of the basic DMR series resonant converter (SRC) are analyzed in detail.
3) A variable dc-link voltage control is introduced to the proposed converter.
4) A 1-MHz microinverter prototype is built and tested to verify the feasibility of the proposed converter.

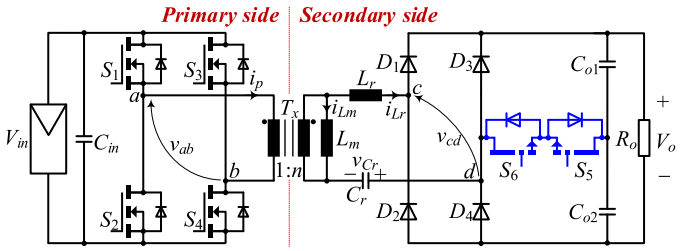

Fig. 2. Schematic of the proposed dual-mode rectifier-based series resonant dc–dc converter.

The remainder of this paper is organized as follows. Section II presents the operation principles of the proposed converter. In Section III, the key operating characteristics are analyzed and parameter design guidelines are presented. Then, the power loss modeling and design optimization of main components are performed in Section IV. After that, the control strategy, modulation implementation, and extensive experimental tests are provided in Section V. Finally, conclusions are drawn in Section VI.

II. Operation Principles of the Proposed Converter

A. Topology Description and Operation Modes

The proposed DMR-based SRC (DMR-SRC) is shown in Fig. 2. The DMR is implemented by adding a pair of anti-series transistors (S_5–S_6) between the midpoints of the diode leg (D_3–D_4) and the output capacitor leg (C_{o1} and C_{o2}). Thus, the following two rectifier modes can be achieved by controlling the anti-series transistors S_5–S_6.

1) *Half-Bridge Rectifier (HBR) Mode*: When the anti-series transistors S_5–S_6 are triggered ON, an HBR (voltage doubler) consisting of D_1, D_2, S_5, S_6, C_{o1}, and C_{o2} presents on the secondary side.
2) *FBR Mode:* When S_5–S_6 are disabled, there is an FBR (D_1–D_4) on the secondary side.

Inspired by the dual-mode rectification concept, two extended series resonant dc–dc converters are derived for high-voltage output applications, as shown in Fig. 3. All the secondary diodes and transistors only need to withstand half of the output voltage V_o. By controlling the secondary-side active switches S_5 and S_6, a dual-mode rectifier can be formed on the secondary side, and therefore, a wide voltage gain can be achieved. Nevertheless, this paper will only focus on the basic topology shown in Fig. 2.

A fixed-frequency phase-shift modulation is applied to the proposed DMR-SRC, as illustrated in Fig. 4. The primary-side diagonal switches are driven synchronously, and the upper and lower switches of each leg are phase shifted by π. On the secondary side, the turn-ON instant of S_5 is synchronized with that of S_2 and S_3, but the turn-OFF of S_5 is lagged by a phase of ϕ with respect to that of S_2 and S_3. The gate signal of S_6 is shifted by a phase of π with that of S_5. It is noted that the fixed-frequency phase-shift modulation scheme is also applicable to the two extended topologies shown in Fig. 3(a) and (b).

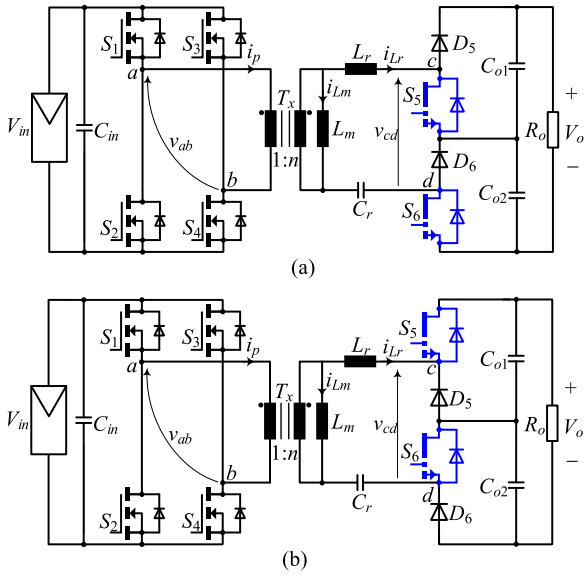

Fig. 3. Schematics of the extended series resonant converter topologies with dual-mode rectifiers for high-voltage output applications. (a) Extended topology A. (b) Extended topology B.

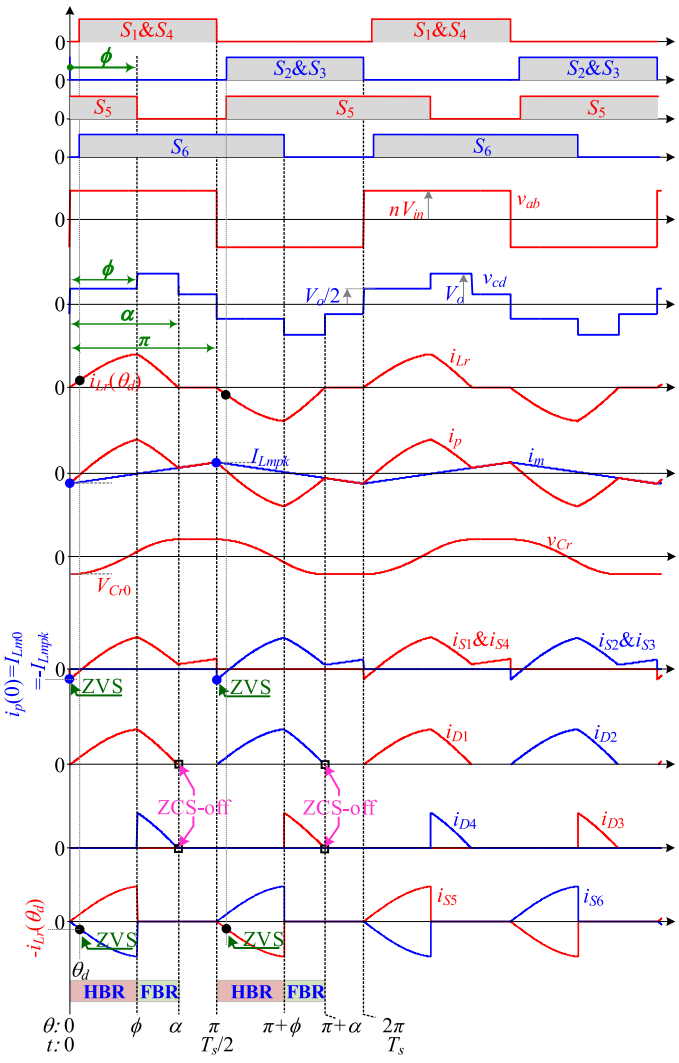

Fig. 4. Fixed-frequency phase-shift modulation for the proposed converter shown in Fig. 2 and key operating waveforms.

With this modulation scheme, the voltage across the midpoints of the two primary-side switch legs, i.e., v_{ab}, is an ac square wave (with an amplitude of V_{in}) that applies to the transformer. In addition, the switching frequency f_s is equal to the series resonant frequency of the resonant inductor L_r and capacitor C_r, i.e., $f_s = f_r = 1/(2\pi\sqrt{L_r C_r})$.

The primary-side transformer current i_p is the sum of the magnetizing current i_{Lm} and the resonant current i_{Lr} referred to the primary side, i.e.,

$$i_p = n(i_{Lm} + i_{Lr}) \tag{1}$$

where n represents the transformer turns ratio.

The waveform of capacitor voltage v_{Cr} has half-wave symmetry, i.e., $v_{Cr}(t) = -v_{Cr}(t + T_s/2)$. Thus, the charge variation of the resonant capacitor over half a switching cycle $[0, T_s/2]$ can be obtained as

$$\begin{aligned} q_{\text{hs}} &= [v_{Cr}(T_s/2) - v_{Cr}(0)]C_r = -2V_{Cr0}C_r \\ &= \int_0^{T_s/2} i_{Lr}(t)\mathrm{d}t = \int_0^{T_s/2} \frac{i_p(t)}{n}\mathrm{d}t - \int_0^{T_s/2} i_{Lm}(t)\mathrm{d}t \\ &= \int_0^{T_s/2} \frac{i_p(t)}{n}\mathrm{d}t = \frac{T_s}{2nV_{\text{in}}}\frac{2}{T_s}\int_0^{T_s/2}[V_{\text{in}} i_p(t)]\mathrm{d}t = \frac{P}{2nf_r V_{\text{in}}} \end{aligned} \tag{2}$$

where V_{Cr0} denotes the initial resonant capacitor voltage at $t = 0$ (see Fig. 4) and P is the transferred power.

The voltage gain of the converter and the inductors ratio of L_m to L_r are defined as $G = V_o/(nV_{\text{in}})$, and $m = L_m/L_r$, respectively. The quality factor is denoted as $Q = Z_r/R_o = P/(V_o^2/Z_r)$, in which the characteristic impedance $Z_r = \sqrt{L_r/C_r}$. Thus, the quality factor Q is also termed as the normalized power.

The initial capacitor voltage V_{Cr0} can be obtained from (2) as

$$V_{Cr0} = \frac{P}{4nf_r C_r V_{\text{in}}} = -\frac{\pi G Q V_o}{2}. \tag{3}$$

The magnetizing current i_{Lm} can be expressed as

$$i_{Lm}(\theta) = I_{Lm0} + \frac{nV_{\text{in}}}{m\omega_r L_r}\theta = I_{Lm0} + \frac{nV_{\text{in}}}{mZ_r}\theta \tag{4}$$

where $\theta = \omega_r t$ with $\omega_r = 2\pi f_r$ being the resonant angular frequency and I_{Lm0} represents the initial magnetizing current at $\theta = 0$. The peak magnetizing current I_{Lmpk} is reached at $\theta = \pi$, i.e., $I_{Lmpk} = i_{Lm}(\pi)$. Due to the half-wave symmetry of the magnetizing current i_{Lm}, we have

$$I_{Lm0} = i_{Lm}(0) = -i_{Lm}(\pi) = -I_{Lmpk}. \tag{5}$$

Substituting (5) into (4) yields the peak and initial magnetizing currents, i.e.,

$$I_{Lmpk} = -I_{Lm0} = \frac{\pi nV_{\text{in}}}{2mZ_r} = \frac{\pi V_o}{2mZ_r G}. \tag{6}$$

B. Operation Principle

The key operating waveforms of the proposed DMR-SRC are shown in Fig. 4. Neglecting the deadtime, six stages can be identified over one switching cycle. Due to the symmetry of operation, only Stages I–III over the first half switching cycle $[0, \pi]$ are described.

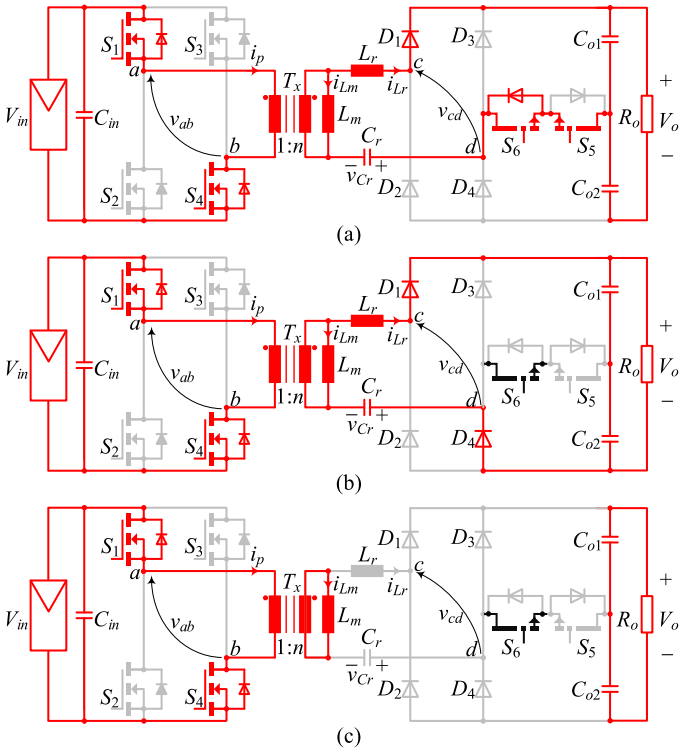

Fig. 5. Equivalent circuits of the proposed converter over the first half switching cycle $[0, \pi]$. (a) Stage I: $[0, \phi]$. (b) Stage II: $[\phi, \alpha]$. (c) Stage III: $[\alpha, \pi]$.

Stage I ($\theta \in [0, \phi]$, see Figs. 4 and 5(a)): Before the time instant 0, S_2, S_3, and S_5 are conducting. At $\theta = 0$, S_2, and S_3 are turned OFF, the negative magnetizing current I_{Lm0} begins to charge/discharge the parasitic output capacitors (C_{oss1}–C_{oss4}) of primary-side switches, such that S_1 and S_4 can achieve ZVS-ON. During this stage, S_5 is turned ON, and an HBR is formed on the secondary side. The voltage v_{cd} is clamped by half of the output voltage $V_o/2$. The resonant inductor L_r and capacitor C_r resonate, and the resonant current i_{Lr} starts increasing from zero. When the parasitic output capacitor of S_6, i.e., C_{oss6}, is fully discharged, the antiparallel diode of S_6 begins to conduct. Thus, ZVS-ON of S_6 can be achieved subsequently by applying the turn-ON gate signal. The governing differential equations in this stage are obtained as

$$\begin{cases} \omega_r L_r \frac{\mathrm{d}i_{Lr}(\theta)}{\mathrm{d}\theta} = nv_{ab}(\theta) - v_{cd}(\theta) - v_{Cr}(\theta) \\ \qquad\qquad = nV_{\text{in}} - V_o/2 - v_{Cr}(\theta) \\ \omega_r C_r \frac{\mathrm{d}v_{Cr}(\theta)}{\mathrm{d}\theta} = i_{Lr}(\theta). \end{cases} \tag{7}$$

Considering the initial conditions $v_{Cr}(0) = V_{Cr0}$ and $i_{Lr}(0) = 0$, (7) can be solved as

$$\begin{cases} i_{Lr}(\theta) = (r_1/Z_r)\sin\theta = A_1 \sin\theta \\ v_{Cr}(\theta) = -r_1\cos\theta + nV_{\text{in}} - V_o/2 \end{cases} \tag{8}$$

where $r_1 = nV_{\text{in}} - V_o/2 - V_{Cr0}$, and $A_1 = r_1/Z_r$.

Stage II ($\theta \in [\phi, \alpha]$, see Figs. 4 and 5(b)): At $\theta = \phi$, S_5 is turned OFF, the resonant current is diverted from S_5–S_6 to D_4,

and an FBR is presented on the secondary side. Thus, the ac voltage v_{cd} is equal to the output voltage V_o, causing the resonant current to decrease sinusoidally. The governing differential equations in this stage are

$$\begin{cases} \omega_r L_r \frac{\mathrm{d}i_{Lr}(\theta)}{\mathrm{d}\theta} = nv_{ab}(\theta) - v_{cd}(\theta) - v_{Cr}(\theta) \\ \qquad\qquad = nV_{\text{in}} - V_o - v_{Cr}(\theta) \\ \omega_r C_r \frac{\mathrm{d}v_{Cr}(\theta)}{\mathrm{d}\theta} = i_{Lr}(\theta). \end{cases} \tag{9}$$

The inductor current and capacitor voltage at $\theta = \phi$, i.e., $i_{Lr}(\phi)$ and $v_{Cr}(\phi)$, can be obtained from (8). Then, (9) can be solved as

$$\begin{cases} i_{Lr}(\theta) = \frac{r_2}{Z_r} \sin(\theta - \phi) + i_{Lr}(\phi)\cos(\theta - \phi) = A_2 \sin(\theta + \delta) \\ v_{Cr}(\theta) = -r_2 \cos(\theta - \phi) + i_{Lr}(\phi) Z_r \sin(\theta - \phi) + nV_{\text{in}} - V_o \end{cases} \tag{10}$$

where $r_2 = nV_{\text{in}} - V_o - v_{Cr}(\phi)$, $A_2 = \sqrt{(r_2/Z_r)^2 + i_{Lr}^2(\phi)}$, and $\delta = \arccos[(r_2/Z_r)/A_2] - \phi$.

Stage III ($\theta \in [\alpha, \pi]$, see Figs. 4 and 5(c)): When the resonant current i_{Lr} falls to zero at $\theta = \alpha$, D_1 and D_4 turn OFF under ZCS. Thus, the resonant tank is prevented from resonance and the resonant current and voltage are kept at 0 and V_{Cr0}, respectively. The output capacitors are discharged to supply the load.

III. Characteristics of the Proposed Converter

In this section, the characteristics of the proposed converter are analyzed in detail in terms of the dc voltage gain, RMS currents, and the soft-switching performance. Additionally, basic design guidelines are also presented.

A. DC Voltage Gain

Because of the half-wave symmetry of both the resonant inductor current i_{Lr} and the capacitor voltage v_{Cr}, we have

$$\begin{cases} i_{Lr}(\pi) = -i_{Lr}(0) = 0 \\ v_{Cr}(\pi) = -v_{Cr}(0) = -V_{Cr0}. \end{cases} \tag{11}$$

Solving (3), (8), (10), and (11) yields the expressions for the voltage gain G and phase angle α as

$$\begin{cases} G = \frac{V_o}{nV_{\text{in}}} = \frac{1}{2\pi Q(3+\cos\phi)} \\ \quad \times \left(K + \frac{4\pi Q(4\pi Q + \sin^2\phi) - \cos^3\phi + 3\cos\phi - 2}{2 + 4\pi Q - \cos\phi - \cos^2\phi} \right) \\ \alpha = \cos^{-1} \left(\begin{array}{c} 4(\sin\phi)^2(1+\cos\phi) \\ -K[3 + 8\pi Q - 2\cos\phi - \cos(2\phi)] \\ \hline 7 + 24\pi Q + 32\pi^2 Q^2 \\ -4(1+4\pi Q)\cos\phi - (3+8\pi Q)\cos(2\phi) \end{array} \right) \end{cases} \tag{12}$$

where $K = \sqrt{8\pi Q(2\pi Q - \cos^2\phi - \cos\phi + 2) + (1 - \cos\phi)^2}$.

According to (12), the voltage gain can be depicted in Fig. 6. It can be seen that the range of the voltage gain is always between 1 and 2 irrespective of the quality factor (i.e., the load). It should be noted that the inductors ratio $m = L_m/L_r$ does not affect the voltage gain. Therefore, the magnetizing inductance can be designed as a large value under the condition that the ZVS-ON of primary-side switches can be achieved. Circuit simulations of the proposed converter are conducted, and the results are also presented in Fig. 6, which validates the obtained analytical gain model (12).

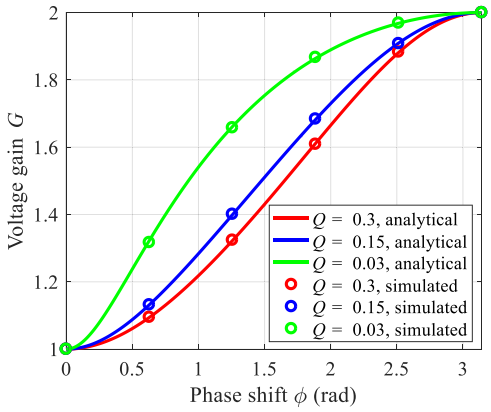

Fig. 6. Analytical and simulated results for the normalized voltage gain G with respect to the phase shift ϕ at different quality factors.

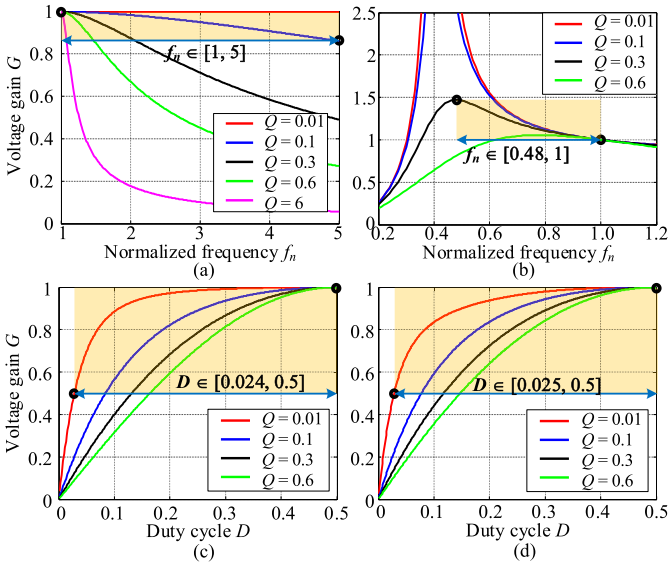

Fig. 7. Voltage gain characteristics of the full-bridge series resonant dc–dc converter and the full-bridge *LLC* resonant dc–dc converter. (a) SRC with PFM. (b) *LLC* resonant converter with PFM. (c) SRC with PWM or PSM. (d) LLC resonant converter with PWM or PSM. In Fig. 7(a) and (b), the normalized switching frequency f_n is based on the series resonant frequency of the resonant tank.

To compare, the voltage gain characteristics of the full-bridge SRC [50] and the full-bridge *LLC* resonant converter [25] are shown in Fig. 7. For the PFM controlled SRC, the light-load gain range is narrow (e.g., 0.85–1 at a light load $Q = 0.1$) even within a wide normalized switching-frequency range $f_n \in [1, 5]$. The PFM-controlled LLC resonant converter has improved gain characteristics. However, the heavy-load gain range is still narrow (e.g., 1–1.47 at a heavy load $Q = 0.3$). In order to have a high full-load gain peak, the characteristic impedance Z_r has to be decreased, resulting in a wider frequency range and/or increased conduction losses.

TABLE I
COMPARISON OF BOMS OF FIVE TOPOLOGIES

Components		Full-bridge SRC [50]	Full-bridge LLC resonant converter [25]	Proposed DMR-based SRC (Fig. 2)	Proposed DMR-SRC derivatives *A* and *B* (Fig. 3)
Primary-side active switch	Count	× 4	× 4	× 4	× 4
	Voltage stress	Input voltage	Input voltage	Input voltage	Input voltage
Secondary-side active switch	Count	0	0	× 2	× 2
	Voltage stress	—	—	Half of output voltage	Half of output voltage
Diode	Count	× 4	× 4	× 4	× 2
	Voltage stress	Output voltage	Output voltage	Output voltage	Half of output voltage
Transformer		× 1	× 1	× 1	× 1
Resonant inductor		× 1	× 1	× 1	× 1
Resonant capacitor		× 1	× 1	× 1	× 1
Output capacitor	Count	× 1	× 1	× 2 in series	× 2 in series
	Voltage stress	Output voltage	Output voltage	Half of output voltage	Half of output voltage

With the fixed-frequency PWM or phase-shift modulation (PSM) control, the gain ranges of the SRC and the *LLC* resonant converter are extended. However, the variation of the duty cycle D is also wide. When the duty cycle D is small, the conduction losses will rise and the soft-switching condition will be lost, because the peak magnetizing current is reduced dramatically in this case. In addition, when controlled with the PWM or PSM scheme, the primary-side (low-voltage and high-current side) switches of the SRC and LLC converter have to turn OFF at a large current, and thus, the OFF-switching loss is large. By contrast, the peak magnetizing current of the proposed resonant converter does not vary significantly with respect to the voltage gain G: the variation range of I_{Lmpk} is twofold according to (6). Therefore, the ZVS-ON of the primary-side switches can be achieved while keeping the magnetizing inductance large. Moreover, the primary-side switches in the proposed converter are turned OFF at the small peak magnetizing current; thus, the OFF-switching loss is small as well.

Furthermore, the bill of materials (BOM) of the five topologies, i.e., the full-bridge SRC [50], the full-bridge *LLC* resonant converter [25], the proposed DMR-based SRC (see Fig. 2), and the derivatives *A* and *B* of the DMR-based SRC (see Fig. 3), is shown in Table I. Compared with the conventional SRC and *LLC* resonant converter, the proposed DMR-based SRC (see Fig. 2) has a higher component count. More specifically, two active switches withstanding half of the output voltage are added on the secondary side, and the output capacitor is split into two low-voltage ones. Likewise, the proposed DMR-SRC derivatives *A* and *B* (see Fig. 3) also employ two secondary-side switches and two output capacitors in series. However, the secondary-side diode count is reduced from 4 to 2, and the voltage stress of the diodes is only half of the output voltage, which is beneficial to cost reduction.

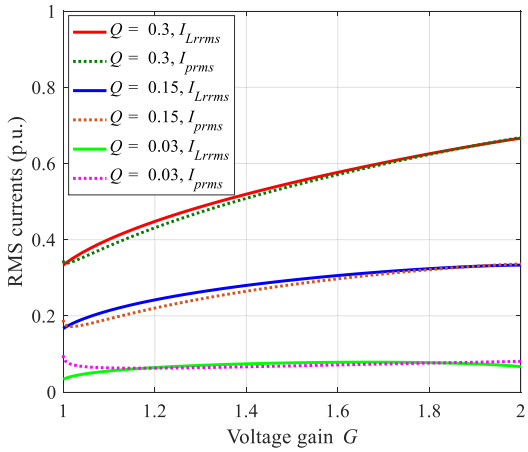

Fig. 8. Primary and secondary transformer RMS currents with respect to the voltage gain at $m = 6$.

B. RMS Currents

The secondary and primary transformer RMS currents can be obtained by

$$\begin{cases} I_{Lr,\mathrm{rms}} = \sqrt{\frac{1}{\pi}\int_0^{\alpha} i_{Lr}^2(\theta)d\theta} \\ I_{p,\mathrm{rms}} = \sqrt{\frac{1}{\pi}\int_0^{\alpha} i_{Lr}(\theta) + i_{Lm}(\theta)^2 d\theta}. \end{cases} \tag{13}$$

The final expressions of $I_{Lr,\mathrm{rms}}$ and $I_{p,\mathrm{rms}}$ are given in Appendix as (39). Fig. 8 shows the normalized RMS currents at different quality factors. The current normalization base is V_o/Z_r. It can be seen in Fig. 8 that at heavy loads, the RMS resonant current $I_{Lr,\mathrm{rms}}$ increases with respect to the voltage gain. The reason is that when the gain increases, the input voltage decreases, and thus, the RMS current increases if the power is fixed. However, at light loads, the RMS current first increases, and then, decreases. This is because the angle α (see Fig. 4) is small at light loads when the voltage gain is in the middle area. A smaller α means a larger RMS current if the power is fixed. For the primary transformer RMS current $I_{p,\mathrm{rms}}$, it is overall rising as the voltage gain G increases. However, at light loads, $I_{p,\mathrm{rms}}$ becomes flat with respect to G. When comparing the two RMS currents, it can be obtained that the difference between them is small. It is because the inductors ratio $m = L_m/L_r$ can be designed to be large for the proposed converter.

For the proposed converter, the characteristic impedance Z_r has a significant impact on the RMS current characteristics when the load is fixed. Fig. 9 shows the full-load RMS current curves under different characterisitc impedances Z_r and voltage gains G. As can be seen, the full-load RMS currents decrease with respect to the increase of the characteristic impedance Z_r except for $G = 1$ and $G = 2$ in Fig. 9(a). Considering the conduction losses, the characteristic impedance Z_r should be designed as large as possible. Moreover, when the resonant frequency is fixed, a larger Z_r means a larger L_r, which is beneficial to

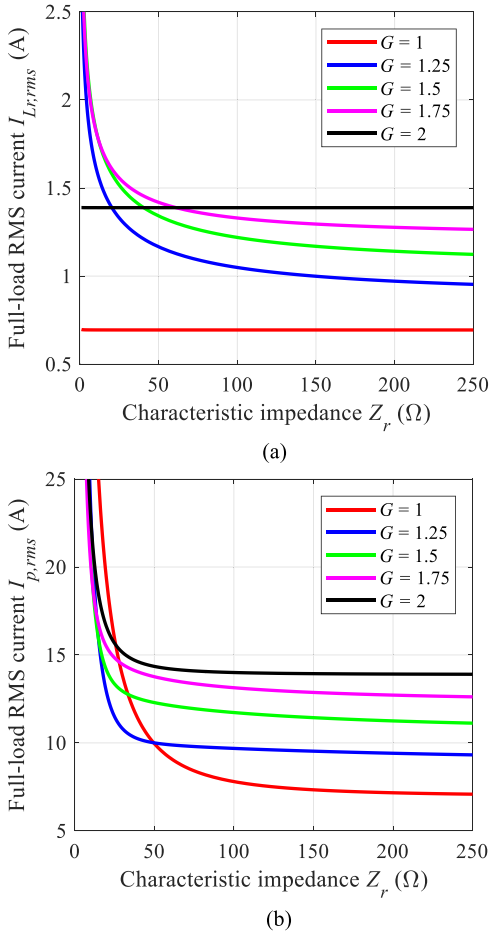

Fig. 9. Full-load RMS currents with respect to the characteristic impedance Z_r at different voltage gains. (a) Secondary-side RMS current $I_{Lr,\mathrm{rms}}$. (b) Primary-side RMS current $I_{p,\mathrm{rms}}$.

the short-circuit current suppression. However, a larger Z_r also leads to a larger ac voltage ripple and a higher voltage peak over the resonant capacitor C_r. Therefore, a tradeoff should be made in practice.

C. Soft Switching

Ideally, the primary and secondary MOSFETs can achieve the ZVS turn-ON if $i_p(0)$ and $-i_{Lr}(\theta_d)$ (see Fig. 4) are negative, as analyzed in Section II-B. This ideal ZVS condition always holds, as indicated by (6) and (8). In practice, however, there are parasitic output capacitances in parallel with MOSFETs and diodes. Therefore, a certain amount of charge is required to fully discharge the output capacitance of the MOSFET during the deadtime interval, such that its antiparallel diode will conduct before the turn-ON signal is applied [51]. Fig. 10 shows the ZVS mechanism of the primary and secondary transistors, and Fig. 11 illustrates the operating waveforms considering the deadtime and output capacitance of transistors. During the deadtime intervals, the output capacitances of the transistors are charged or discharged with i_p, i_{Lm}, and/or i_{Lr}. It is assumed that $C_{oss1} = C_{oss2} = C_{oss3} = C_{oss4} = C_{oss,P}$, $C_{oss5} = C_{oss6} = C_{oss,S}$, and $C_{ossD1} = C_{ossD2} = C_{ossD3} = C_{ossD4} = C_{oss,D}$. Then, the voltage change

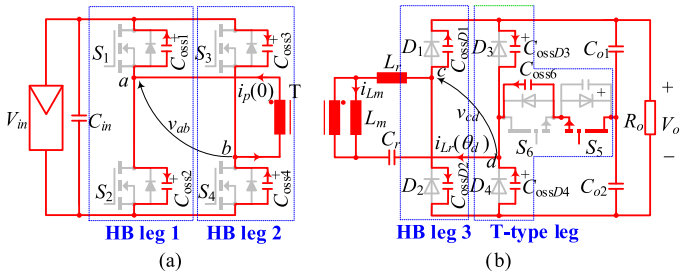

Fig. 10. ZVS mechanism of primary and secondary transistors. (a) ZVS turn-ON of S_1 and S_4 at $t = 0$. (b) ZVS turn-ON of S_6 at $t = 0$. C_{oss1}–C_{oss4}, C_{ossD1}–C_{ossD4}, and C_{oss5}–C_{oss6} are the parasitic capacitances of transistors and diodes.

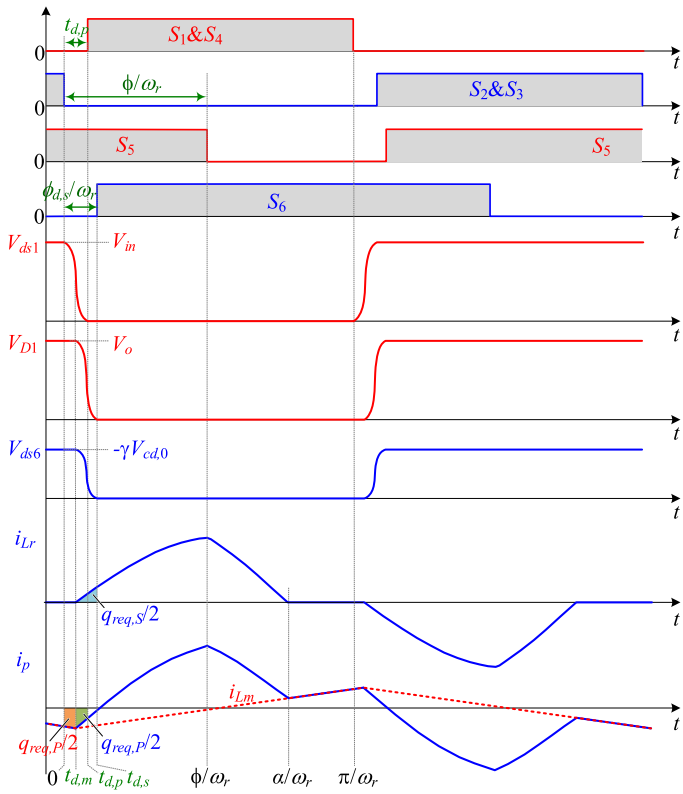

Fig. 11. Operating waveforms of the proposed converter considering the deadtime and output capacitances of transistors and diodes.

and charge required for the ZVS-ON can be obtained, as summarized in Table II.

1) *Primary-Side ZVS:* The ZVS-ON realization of S_1 requires a complete charging of C_{oss1} and a complete discharging of C_{oss2} during the deadtime interval $t_{d,P}$, as shown in Figs. 10(a) and 11. The total required charge $q_{\mathrm{req},P}$ (see Table II) can be divided into $q_{\mathrm{req},P}/2$ within $[0, t_{d,m}]$ and $q_{\mathrm{req},P}/2$ within $[t_{d,m}, t_{d,P}]$, as illustrated in Fig. 11. Due to the high nonlinearity of the parasitic output capacitance with respect to the drain–source voltage, the current waveforms i_{Lm} and i_p will not be distorted significantly during the deadtime interval [52].

To achieve the complete charging and discharging of output capacitances, the charge provided by the currents i_{Lm} and i_p (see

TABLE II
REQUIRED MINIMUM CHARGE TO ACHIEVE ZVS FOR DIFFERENT SWITCH LEGS

Commutation mode	Current to achieve ZVS	Output capacitor		Initial capacitor voltage at $t=0$	Final capacitor voltage at $t=t_{d,p}$ or $t_{d,s}$	Absolute charge variation of a capacitor	Charge variation of an HB/T-type leg	Minimum charge q_{req} for ZVS-ON of all switches
Primary side ZVS (see Fig. 9(a))	i_{Lm} and i_p	HB leg 1	C_{oss1}	V_{in}	0	$V_{in}C_{oss,P}$	$2V_{in}C_{oss,P}$	$q_{req,P}=2V_{in}C_{oss,P}$
			C_{oss2}	0	V_{in}	$V_{in}C_{oss,P}$		
		HB leg 2	C_{oss3}	0	V_{in}	$V_{in}C_{oss,P}$	$2V_{in}C_{oss,P}$	
			C_{oss4}	V_{in}	0	$V_{in}C_{oss,P}$		
Secondary side ZVS (see Fig. 9(b))	i_{Lr}	HB leg 3	C_{ossD1}	$0.5V_o-(1-\gamma)V_{cd0}$	0	$[0.5V_o-(1-\gamma)V_{cd0}]C_{oss,D}$	$[0.5V_o-(1-\gamma)V_{cd0}]C_{oss,D}$	$q_{req,S}=\max\{[0.5V_o-(1-\gamma)V_{cd0}]C_{oss,D}, -\gamma V_{cd0}(2C_{oss,D}+C_{oss,S})\}$
			C_{ossD2}	$0.5V_o+(1-\gamma)V_{cd0}$	V_o	$[0.5V_o-(1-\gamma)V_{cd0}]C_{oss,D}$		
		T-type leg	$C_{oss\,D3}$	$0.5V_o+\gamma V_{cd0}$	$0.5V_o$	$-\gamma V_{cd0}C_{oss,D}$	$-\gamma V_{cd0}(2C_{oss,D}+C_{oss,S})$	
			$C_{oss\,D4}$	$0.5V_o-\gamma V_{cd0}$	$0.5V_o$	$-\gamma V_{cd0}C_{oss,D}$		
			C_{oss5}	0	0	0		
			C_{oss6}	$-\gamma V_{cd0}$	0	$-\gamma V_{cd0}C_{oss,S}$		

Fig. 11) during the deadtime interval $[0, t_{d,P}]$ should satisfy

$$\begin{cases} \int_0^{t_{d,m}} -i_{Lm}(\omega_r t)dt = \int_0^{t_{d,m}} \left(-I_{Lm0} - \frac{nV_{\text{in}}}{mZ_r}\omega_r t\right) dt \geq \frac{q_{\text{req},P}}{2} \\ \int_0^{t_{d,P}-t_{d,m}} -i_p(\omega_r t)dt = \int_0^{t_{d,P}-t_{d,m}} -[A_1\sin(\omega_r t)+i_{Lm}(\omega_r t)]\,dt \\ \approx \int_0^{t_{d,P}-t_{d,m}} -I_{Lm0} - \left(\frac{nV_{\text{in}}}{mZ_r}+A_1\right)\omega_r t dt \geq \frac{q_{\text{req},P}}{2}. \end{cases} \tag{14}$$

From the aforementioned equation, it is obtained that the inductors ratio m should be designed according to

$$m = \frac{L_m}{L_r} \leq \min\left\{\frac{2nt_d V_{\text{in}}(2\pi - t_d\omega_r)}{8q_{\text{req},P}Z_r + nV_{\text{in}}\omega_r t_d^2[G(\pi GQ-1)+2]}\right\}. \tag{15}$$

2) *Secondary-Side ZVS:* Before the output rectifier conducts, e.g., before $t=0$ in Fig. 11, a capacitor network composed of C_{ossD1}–C_{ossD4} and C_{oss6} presents on the secondary side, as shown in Fig. 10 (b). By applying the Kirchhoff's voltage and current laws to the capacitor network, the steady-state capacitor voltages (i.e., the voltages at $t=0$), can be obtained as

$$\begin{cases} V_{D1,0} = V_o/2 - (1-\gamma)V_{cd,0} \\ V_{D2,0} = V_o/2 + (1-\gamma)V_{cd,0} \\ V_{D3,0} = V_o/2 + \gamma V_{cd,0} \\ V_{D4,0} = V_o/2 - \gamma V_{cd,0} \\ V_{dsS5,0} = 0 \\ V_{dsS6,0} = \gamma V_{cd,0} \end{cases} \tag{16}$$

where

$$\begin{cases} \gamma = \frac{2C_{\text{oss},D}}{4C_{\text{oss},D}+C_{\text{oss},S}} \\ V_{cd,0} = -nV_{\text{in}} - V_{Cr0} = V_o\left(\frac{\pi GQ}{2} - \frac{1}{G}\right). \end{cases} \tag{17}$$

The turn-ON of S_6 lags the turn-OFF of S_2 and S_3 with a deadtime $t_{d,s} = \phi_{d,s}/\omega_r$, and the turn-ON of S_5 lags the turn-OFF of S_1 and S_4 with the same deadtime $t_{d,s} = \phi_{d,s}/\omega_r$, as shown in Fig. 11. At $t = t_{d,s}$, the secondary-side capacitors reach new steady states with the final voltages showing in Table II. Then, the absolute charge variation of each capacitor and the minimum charge $q_{\text{req},S}$ required for the secondary-side ZVS-ON can be obtained, as listed in Table II. To achieve the ZVS-ON operation for the secondary transistors S_5 and S_6, the charge provided by the resonant current should be larger than the required one $q_{\text{req},S}$, i.e.,

$$\int_0^{\alpha/(\omega_r t)} i_{Lr}(\omega_r t)dt = \int_0^{\phi/(\omega_r t)} A_1\sin(\omega_r t)dt + \int_{\phi/(\omega_r t)}^{\alpha/(\omega_r t)} A_2\sin(\omega_r t+\delta)dt \geq q_{\text{req},S}. \tag{18}$$

Simplifying the aforementioned equation yields the practical complete ZVS-ON conditions for S_5 and S_6, i.e.,

$$A_1(1-\cos\phi) + A_2[\cos(\delta+\phi) - \cos(\delta+\alpha)] \geq \omega_r q_{\text{req},S}. \tag{19}$$

If the aforementioned equation is not satisfied, S_5 and S_6 will withstand incomplete ZVS-ON. Nevertheless, the drain–source voltage of S_5 and S_6 is low, i.e., $\leq V_o/2$. Therefore, the turn-ON losses are not significant even operating under an incomplete ZVS-ON condition. Based on (19), the areas for the complete ZVS-ON and incomplete ZVS-ON of S_5 and S_6 can be obtained, as shown in Fig. 12. It is seen that the incomplete ZVS-ON occurs only when the quality factor Q (i.e., the load) is very low (e.g., $Q < 0.007$ at $G = 2$).

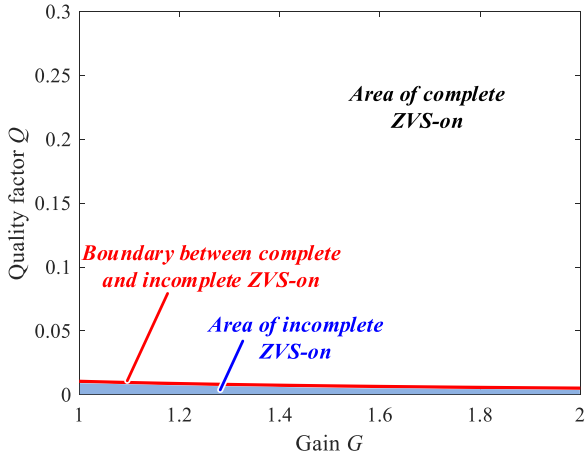

Fig. 12. Ranges of complete ZVS-ON and incomplete ZVS-ON for S_5 and S_6. The shaded area represents the range of incomplete ZVS-ON, and the solid red line is the boundary between the complete and incomplete ZVS-ON ranges.

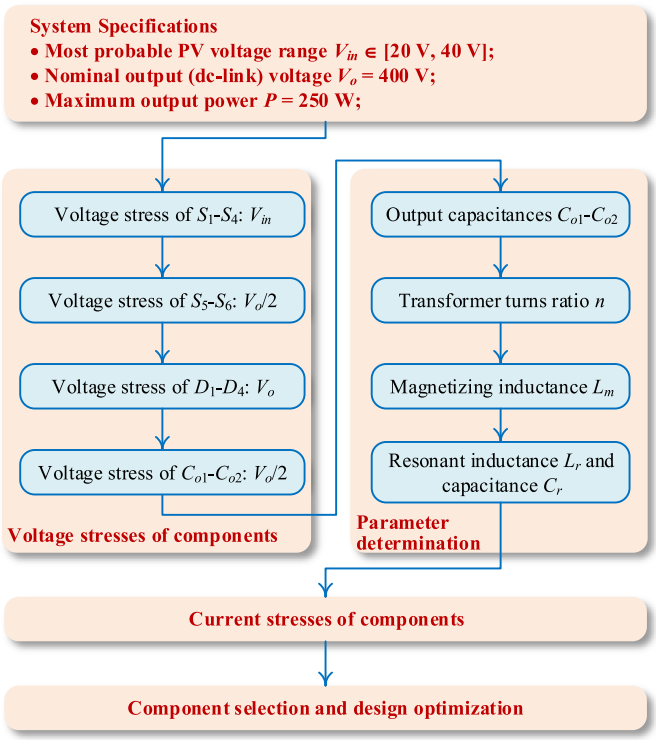

Fig. 13. Flowchart of the design process for the main components of the proposed converter.

D. Design Guidelines

The flowchart of the design process for the main components of the proposed converter is shown in Fig. 13. Before the design, system specifications, e.g., the most possible PV voltage range, nominal output (dc-link) voltage, and maximum output power, are determined. Then, the voltage stresses of semiconductor devices and output capacitors can be obtained based on Table I. After that, the component parameters, e.g., output capacitances C_{o1}–C_{o2}, transformer turns ratio n, magnetizing inductance L_m, and resonant tank (L_r and C_r) can be determined. Subsequently, the current stresses of the main components can be calculated based on the mathematical models built in Sections II and III. Finally, the component selection and design optimization can be performed.

The parameter determination process is detailed as follows.

1) Output (DC-Link) Capacitances: The output capacitors of the proposed dc–dc converter also act as an energy buffer in the two-stage PV microinverter. The instantaneous feeding power to the grid contains a fluctuating power at twice the line frequency, whereas the PV output is dc power. Thus, the output (dc-link) capacitors are used to decouple the power mismatch. The electrical stresses over the dc-link capacitors can be calculated as [53]

$$\begin{cases} \Delta V_o \approx P/(2\pi f_0 C_o V_o) \\ I_{Co,\mathrm{rms}} = P/(\sqrt{2} V_o) \end{cases} \tag{20}$$

where f_0 represents the line frequency, P is the average power injected to the grid, the equivalent output (dc-link) capacitance $C_o = 1/(1/C_{o1} + 1/C_{o2})$, ΔV_o is the peak-to-peak ripple of the output voltage V_o, and $I_{Co,\mathrm{rms}}$ is the RMS current flowing through the output (dc-link) capacitors. Considering a 6%-voltage ripple on the dc-link voltage, the required minimum capacitance output capacitance equals 83 μF. In this design, two low-profile (height: 1.5 cm) 250-V 180-μF electrolytic capacitors are adopted and connected in series.

2) Transformer Turns Ratio and Magnetizing Inductance: The transformer turns ratio n is determined by

$$n = N_s : N_p = \frac{V_o}{G V_{\mathrm{in}}} \tag{21}$$

where N_p and N_s are the numbers of primary and secondary winding turns. Considering the ranges of the voltage gain G (see Fig. 6) and the input voltage V_{in} (see Fig. 13), the transformer turns ratio n is chosen as 10.

For the magnetizing inductance L_m, it is used to assist the primary-side switches achieve the ZVS-ON. A smaller L_m leads to a higher magnetizing current, thereby being beneficial to ZVS-ON. However, the conduction loss will be increased due to the higher circulating current (i.e., magnetizing current). Therefore, the design principle of L_m is that it should be possibly large under the premise that the ZVS-ON of S_1–S_4 can be achieved, as illustrated by (15).

3) Resonant Inductance and Capacitance: As analyzed in Section III-B, a tradeoff between the RMS currents and the resonant capacitor voltage ripple (or peak voltage) should be made for the design of the characteristic impedance Z_r. Meanwhile, it is seen from Fig. 9 that the RMS current curves become flat when Z_r exceeds a certain value (e.g., 175 $\sim$ 225 Ω), which means that increasing Z_r cannot further reduce the conduction losses. Therefore, the design of L_r and C_r follows

$$\begin{cases} f_s = f_r = \frac{1}{2\pi\sqrt{L_r C_r}} = 1\ \mathrm{MHz} \\ 175\ \Omega \le Z_r = \sqrt{\frac{L_r}{C_r}} \le 225\ \Omega. \end{cases} \tag{22}$$

Solving the aforementioned equation and considering the availability of resonant capacitors yield $L_r = 34\ \mu$H and $C_r = 7.5$ nF.

IV. Power Loss Modeling and Design Optimization

A. Power Semiconductors

1) Primary-Side Switches S_1–S_4: All the primary-side switches can achieve the ZVS-ON and are turned OFF at the small peak magnetizing current I_{Lm0}. Therefore, the switching losses of the primary-side switches are small and can be neglected. The total conduction losses of the four switches S_1–S_4 can be calculated as

$$P_{S14,\mathrm{con}} = 4 R_{S14,\mathrm{on}} \left(I_{p,\mathrm{rms}}/\sqrt{2} \right)^2 \tag{23}$$

where $R_{S14,on}$ is the ON-state resistance of the primary-side switches S_1–S_4.

As analyzed in Section III, the voltage stress of S_1–S_4 equals the input voltage V_{in}, which is determined by the PV module properties (e.g., number of cells and material) and environmental conditions (i.e., solar irradiance and ambient temperature).

In this paper, a maximum input voltage of 43 V is considered for the proposed converter, and thus, the 80-V eGaN FETs [54] from Efficient Power Conversion (EPC) Corporation are chosen for a sufficient voltage margin. The maximum RMS current flowing through S_1–S_4 is about $14.1/\sqrt{2} = 10$ A [see Fig. 9(b)]. Considering the availability of 80-V GaN transistors, EPC2029 is finally selected for the implementation of S_1–S_4.

2) Secondary-Side Switches S_5–S_6: The voltage stress of the secondary-side switches S_5–S_6 is half of the output voltage V_o. The maximum output voltage is 430 V in this paper, and the maximum withstanding voltage of S_5–S_6 is about 215 V. Considering a 1.5-2 times voltage margin, the voltage rating of S_5–S_6 should be 322.5–430 V. However, the available voltage ratings of GaN transistors on the market were either below 200 or above 600 V when the PV microinverter was designed in 2017. To the best of our knowledge, the 350- and 400-V GaN transistors [55], [56] have not been commercialized until 2018.

For a series of GaN transistors with the same voltage rating, their current ratings and drain–source ON-state resistances are achieved by employing different numbers of standard die units in parallel. For instance, the numbers of die units inside the 650-V GaN eHEMTs, GS66502B, GS66504B, GS66506T, and GS66508B [57] are 2, 4, 6, and 8, respectively, as shown in Fig. 14(a). Their drain–source ON-state resistances are inversely proportional to the number of die units, whereas the parasitic input and output capacitances of a GaN transistor are proportional to the total die area. Thus, the lower the drain–source ON-state resistance, the higher the parasitic input and output capacitances. In this case, the gate drive loss and incomplete ZVS loss [61] will be increased. For the proposed converter, the incomplete ZVS range of S_5–S_6 is very small, as indicated in Fig. 12. Hence, the conduction loss and cost are the main factors affecting the selection of GaN transistors. Fig. 14(b) shows the market price of the 650-V GaN eHEMTs of GaN Systems. It can be seen that the price of a GaN transistor increases with respect to the number of die units inside. As mentioned before, the ON-state resistance and conduction loss can be reduced with a higher number of die units, but the implementation cost will be increased as well. Therefore, as a tradeoff between the cost and the power conversion efficiency, GS66504B with $N_{\text{unit}} = 4$ is selected for S_5 and S_6.

The secondary switches S_5–S_6 can achieve the ZVS-ON operation, but are turned OFF with a relatively large current, as shown in Fig. 4. Therefore, there may be an amount of turn-OFF losses if the turn-OFF speed is not fast enough. A double-pulse testing setup has been built up in order to explore the turn-OFF power losses of GS66504B devices. The turn-OFF waveforms at $V_{\text{ds}} = 200$ V and $I_{\text{ds}} = 1.43$ A are shown in Fig. 15(a). When the gate voltage V_{gs} falls to below the threshold voltage, the channel is cut off quickly, but the drain–source voltage V_{ds} has not significantly increased. Therefore, the drain–source current is diverted to the output capacitor of the GaN eHEMT, causing V_{ds} to rise from 0 to 200 V. The measured turn-OFF energy loss is approximately equal to the energy stored in the output capacitor C_{oss}, as shown in Fig. 15(b). It should be noted that the calculated turn-OFF energy loss E_{off} ($\approx E_{\text{oss}}$) is not truly dissipated during the turn-OFF period. If the switch is subsequently turned

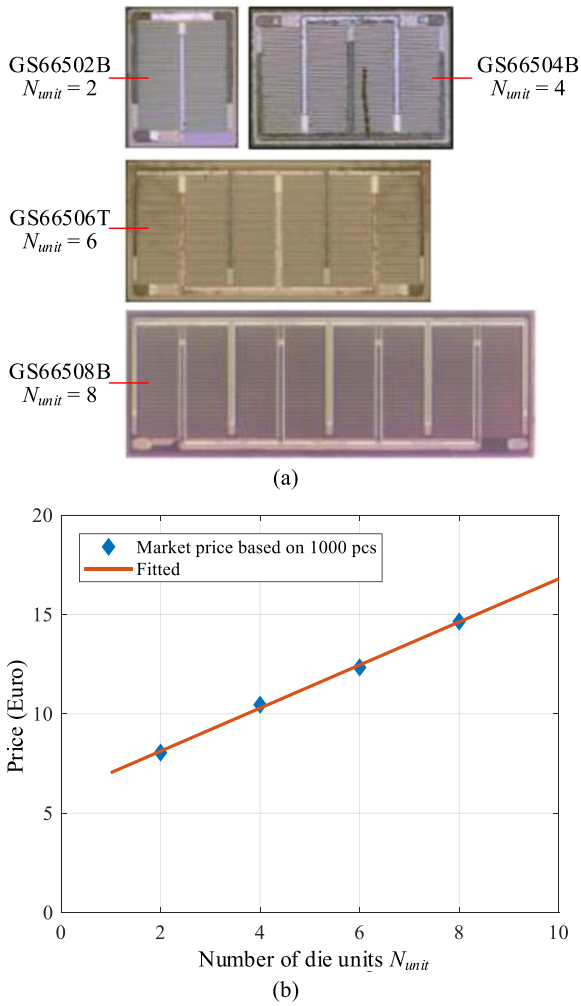

Fig. 14. (a) Microscopy images of four 650-V GaN dies [58]; the total die area of GS66508P (12.3 mm^2 [59]) is almost twice of GS66504B (6.1 mm^2 [60]). (b) Market price of GaN Systems' 650-V GaN eHEMTs with different numbers of die units; the survey was conducted at Mouser Electronics in 2017.

ON under hard switching, then the energy stored in the output capacitor C_{oss}, i.e., E_{oss}, will be dissipated on the channel. However, the switch in this converter can achieve the ZVS-ON, which means that the energy stored in the output capacitor is transferred instead of being dissipated. Therefore, for the proposed converter, the secondary-side switches implemented with GaN HEMTs can achieve a quasi-lossless turn-OFF.

For the conduction loss of S_5–S_6, it can be calculated as

$$P_{S56,\text{con}} = 2R_{S56,\text{on}} I^2_{S56,\text{rms}} \tag{24}$$

where $R_{S56,\text{on}}$ is the ON-state resistance of S_5 and S_6, and $I_{S56,\text{rms}}$ is the RMS current flowing through S_5 and S_6.

3) Secondary-Side Rectifier Diodes: The rectifier diodes D_1–D_4 are operating in the discontinuous conduction mode, and theoretically, the ZCS-OFF can be achieved for D_1–D_4, as shown in Fig. 4. In practice, however, the ZCS condition (i.e., $i_{Lr}(\alpha) = 0$) cannot be always guaranteed due to the resonance of the parasitic output capacitors of rectifier diodes, resonant capacitor C_r, and series inductor L_r. If D_1–D_4 are implemented with silicon ultrafast recovery diodes, the reverse-

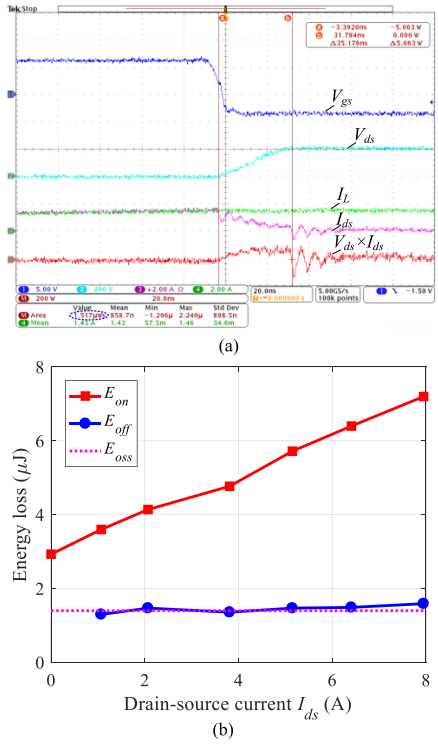

Fig. 15. Double-pulse test on the GaN eHEMT GS66504B. (a) Measured turn-OFF waveforms of GS66504B. (b) Comparison between the measured turn-OFF energy loss and the energy stored in the output capacitance of GS66504B at $V_{ds} = 200$ V.

recovery losses will be high at the 1-MHz switching frequency despite of a quasi-ZCS operation. Hence, four 600-V SiC Schottky diodes, C3D02060E, are utilized in order to ensure a negligible reverse-recovery loss at the 1-MHz switching frequency.

The conduction loss of the rectifier diodes can be calculated as

$$P_{D,\text{con}} = 2(I_{D12,\text{avg}} + I_{D34,\text{avg}})V_F + 2\left(I_{D12,\text{rms}}^2 + I_{D34,\text{rms}}^2\right)R_D \tag{25}$$

where V_F and R_D are the voltage drop at the zero current and the resistance of the diode, respectively; $I_{D12,\text{avg}}$ and $I_{D34,\text{avg}}$ represent the average currents of D_1–D_2 and D_3–D_4, respectively; and $I_{D12,\text{rms}}$ and $I_{D34,\text{rms}}$ denote the RMS currents of D_1–D_2 and D_3–D_4, respectively.

B. Magnetic Components

Planar transformers and inductors are used in this research, and the magnetic core material is ML91S from Hitachi Metal, which has the lowest core loss density at the 1-MHz frequency among all available materials [46], [47]. Fig. 16 presents the power loss density data of the ML91S material under the sinusoidal excitation. With curve fitting, its Steinmetz parameters k, α, and β can be obtained, as shown in Fig. 16.

For the proposed converter, the magnetic cores are excited with nonsinusodial voltages, and therefore, the core loss density can be calculated with the improved generalized Steinmetz equation [62]

$$P_v = \frac{1}{T_s}\int_0^{T_s} k_i \left|\frac{\mathrm{d}B}{\mathrm{d}t}\right|^{\alpha} (\Delta B)^{\beta-\alpha}\mathrm{d}t \tag{26}$$

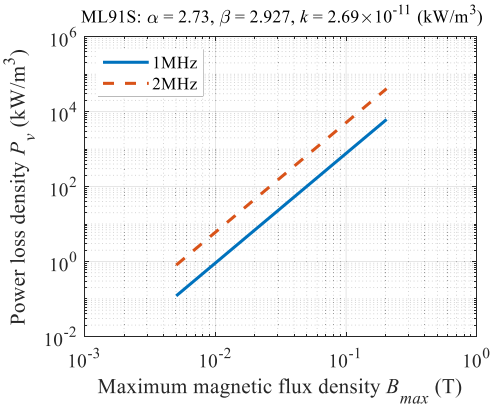

Fig. 16. Power loss density of ML91S material under sinusoidal excitation.

where

$$k_i = \frac{k}{(2\pi)^{\alpha-1}\int_0^{2\pi}|\cos\varphi|^{\alpha}2^{\beta-\alpha}d\varphi}. \tag{27}$$

The ac resistance of the winding increases dramatically with respect to the frequency due to the skin effect and proximity effect, and it can be calculated with the Dowell equation [63], [64] as

$$\frac{R_{\text{ac}}}{R_{\text{dc}}} = \frac{\xi}{2}\left(\frac{\sinh\xi + \sin\xi}{\cosh\xi - \cos\xi} + (2m-1)^2\frac{\sinh\xi - \sin\xi}{\cosh\xi + \cos\xi}\right) \tag{28}$$

where $\xi = h/\delta_s$, h is the thickness of printed circuit board (PCB) traces, δ_s is the skin depth of the conductor, and m is a magnetomotive force (MMF) ratio

$$m = \frac{F(h)}{F(h) - F(0)} \tag{29}$$

in which $F(0)$ and $F(h)$ are the MMFs at the borders of a layer. The winding loss calculation requires the RMS values of the harmonics of the resonant current i_{Lr}. Therefore, the resonant current is expanded based on the Fourier series, as shown in Appendix.

1) Transformer: For the transformer in the proposed converter, applying the Faraday's law to (26) yields a simplified core loss density equation

$$P_v = k_i(2f_s)^{\alpha-\beta}\left(\frac{V_{\text{in}}}{N_p A_e}\right)^{\beta} \tag{30}$$

where N_p is the number of primary turns and A_e is the effective sectional area of the magnetic core.

The planar core ER32/6/25 and two-layer PCB windings (70-μm copper thickness for each layer) are adopted to fabricate the transformer. For the PCB winding layout, three arrangements are explored, as illustrated in Fig. 17. As can be seen, different winding arrangements lead to different MMF distributions, which affect the ac resistance and power loss of windings. Compared with the non-interleaving [see Fig. 17(a)] and interleaving [see Fig. 17(b)] winding arrangements, the arrangement 0.5P-S-P-S-0.5P [see Fig. 17(a)] enables the minimum MMF ratio for windings, and therefore, the ac resistance can be reduced. In addition to the power loss, the intra- and inter-winding

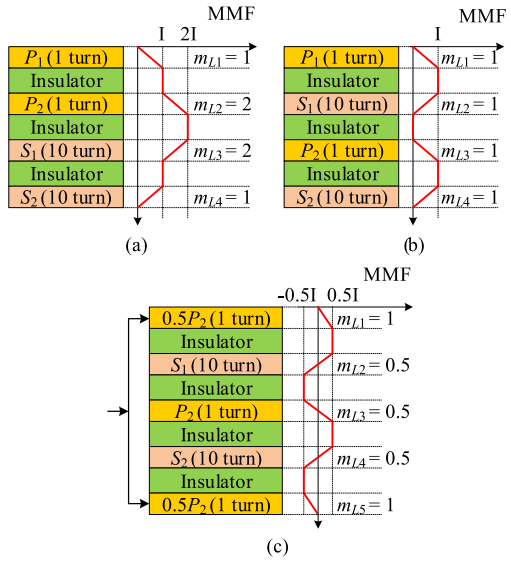

Fig. 17. MMF distribution of different winding arrangements in the case of $N_p = 2$. (a) Non-interleaving winding arrangement: P-P-S-S. (b) Interleaving winding arrangement: P-S-P-S. (c) 0.5P-S-P-S-0.5P. "P" represents the primary winding and "S" denotes the secondary winding.

capacitances of planar transformers will affect the converter operation, and they should be controlled as low as possible for the proposed converter. It is proved in [65] and [66] that the arrangement 0.5P-S-P-S-0.5P can achieve the minimum stray capacitance while maintaining the lowest resistance.

Fig. 18 shows the calculated power losses of the planar transformers with different winding arrangements and different numbers of primary turns N_p. As can be seen, the winding arrangement 0.5P-S-P-S-0.5P can achieve the minimum power losses compared with the other two arrangements. From Fig. 18, it can also be observed that with the increase of the number of primary turns N_p, the core loss decreases, whereas the winding loss rises due to the increased resistance. The case when $N_p = 2$ allows the transformer to achieve the minimum power loss.

2) Resonant Inductor: The voltage across the resonant inductor can be obtained as

$$v_{Lr}(t) = v_{ab}(t) - v_{cd}(t) - v_{Cr}(t). \tag{31}$$

Substituting (8) and (10) into (31) yields v_{Lr} over half a switching cycle $[0\ \pi]$, i.e.,

$$\left|\frac{dB}{dt}\right| = \frac{|v_{Lr}(t)|}{N_{Lr}A_{e,Lr}} = \frac{1}{N_{Lr}A_{e,Lr}} \times \begin{cases} A_1 Z_r \left|\cos\left(\omega_r t\right)\right|, & t \in [0, \phi/\omega_r] \\ A_2 Z_r \left|\cos\left(\omega_r t + \delta\right)\right|, & t \in (\phi/\omega_r, \alpha/\omega_r] \\ 0, & t \in (\alpha/\omega_r, \pi/\omega_r] \end{cases} \tag{32}$$

where

$$\phi = \arccos\left(1 - \frac{4\pi QG(G-1)}{2 - G(1+\pi QG)}\right). \tag{33}$$

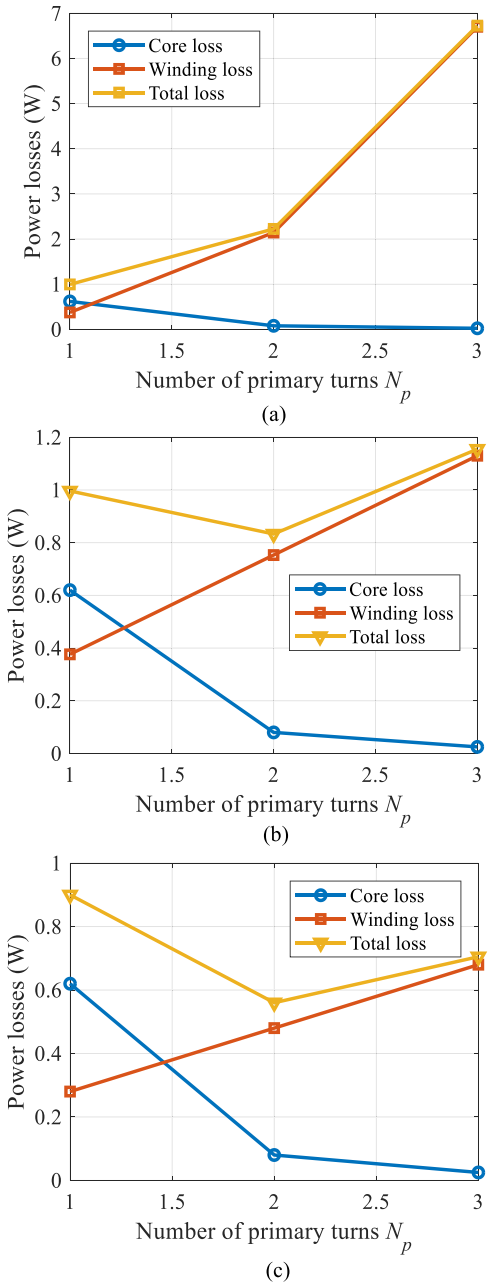

Fig. 18. Calculated power losses of planar transformers with different winding arrangements and different numbers of primary turns N_p. (a) Non-interleaving winding arrangements: P-S for $N_p = 1$, P-P-S-S for $N_p = 2$, and P-P-P-S-S-S for $N_p = 3$. (b) Interleaving winding arrangement: P-S for $N_p = 1$, P-S-P-S for $N_p = 2$, and P-S-P-S-P-S for $N_p = 3$. (c) 0.5P-S-0.5P for $N_p = 1$, 0.5P-S-P-S-0.5P for $N_p = 2$, and 0.5P-S-P-S-P-S-0.5P for $N_p = 3$.

For the magnetic flux density swing of the resonant inductor, it is related to the peak resonant current, which has three different cases, as illustrated in Fig. 19. Then, the flux density swing can be obtained as

$$\Delta B_{Lr} = \frac{L_r \Delta I_{Lr}}{N_{Lr}A_{e,Lr}} = \frac{L_r}{N_{Lr}A_{e,Lr}} \times \begin{cases} 2A_2, 0 \le \phi < \frac{\pi}{2} - \delta \\ 2i_{Lr}(\phi), \frac{\pi}{2} - \delta \le \phi < \frac{\pi}{2} \\ 2A_1, \frac{\pi}{2} \le \phi \le \pi \end{cases} \tag{34}$$

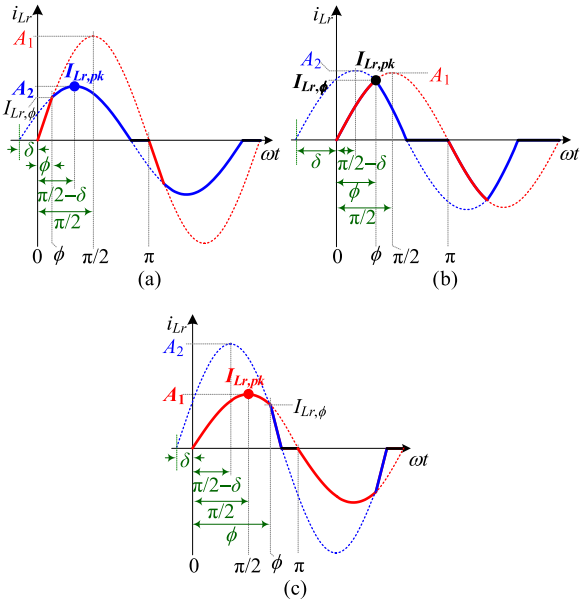

Fig. 19. Positions of the peak resonant current $I_{Lr,pk}$ in different operating conditions. (a) $0 \le \phi < \pi/2 - \delta$. (b) $\pi/2 - \delta \le \phi < \pi/2$. (c) $\pi/2 \le \phi \le \pi$.

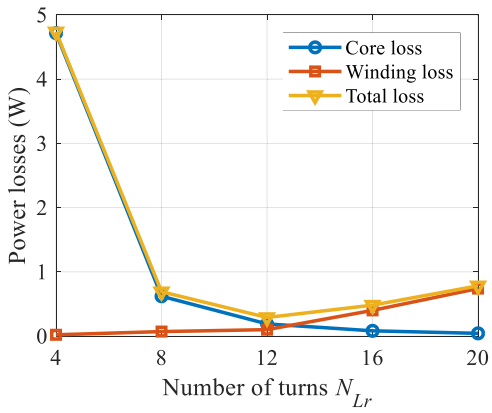

Fig. 20. Calculated power losses of planar inductors with different numbers of turns N_{Lr}.

where $A_1 = r_1/Z_r$, $A_2 = \sqrt{(r_2/Z_r)^2 + I_{Lr,\phi}^2}$, $\delta = \arctan[(r_2/Z_r)/A_2] - \phi$, and $I_{Lr,\phi} = (r_1/Z_r)\sin\phi$. The core loss can be subsequently calculated based on (26).

The magnetic core ER26/6/15 and two-layer PCB windings (70-μm copper thickness for each layer) are used to implement the planar resonant inductor. The calculated power losses of planar inductors with different numbers of turns N_{Lr} are shown in Fig. 20. It is seen that $N_{Lr} = 12$ enables the inductor to achieve the minimum power loss.

C. Capacitors

The power losses in capacitors are generally composed of dielectric losses and thermal losses [67]. The dielectric losses associated with the cycle of charging and discharging of dielectrics are calculated as

$$P_{Cd} = C_r\,|V_{Cr0}|\,f_s \tan\delta \tag{35}$$

where $\tan\delta$ is the dielectric loss factor of the chosen capacitor.

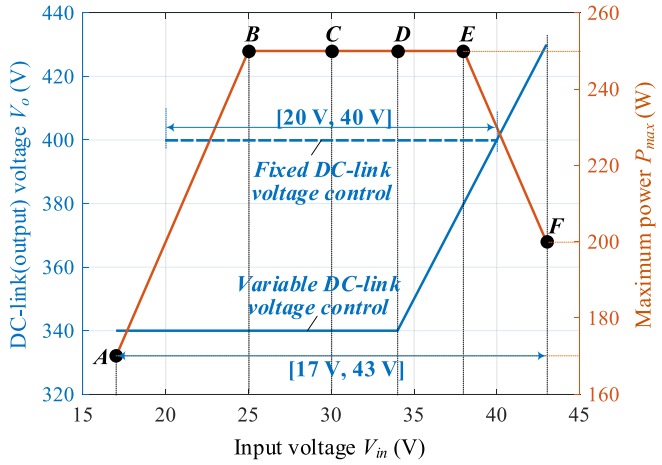

Fig. 21. Operation profile of the PV microinverter with fixed and variable dc-link voltage control schemes. The profile of the PV output power P_{PV} is determined by different PV panels as well as the environmental conditions (i.e., the solar irradiance and ambient temperature).

TABLE III
IDENTIFIED SIX OPERATING POINTS WITH FIXED AND VARIABLE DC-LINK VOLTAGE CONTROL STRATEGIES

Operating point	PV voltage V_{PV}	PV power P_{PV}	DC-link voltage V_o under the variable DC-link voltage control	DC-link voltage V_o under the fixed DC-link voltage control
A	17 V	170 W	340 V	NaN
B	25 V	250 W	340 V	400 V
C	30 V	250 W	340 V	400 V
D	34 V	250 W	340 V	400 V
E	38 V	250 W	380 V	400 V
F	43 V	200 W	430 V	NaN

The thermal losses are derived as

$$P_{Cth} = R_e I_{Lr,\mathrm{rms}}^2 \tag{36}$$

where Re is the equivalent series resistance of the resonant capacitor Cr.

V. CONTROL STRATEGY, MODULATION IMPLEMENTATION, AND EXPERIMENTAL VERIFICATIONS

A. Control Strategy

Depending on the PV panel properties and the environmental conditions (i.e., the solar irradiance and ambient temperature), the PV output voltage and power at the MPPs may change significantly. Fig. 21 depicts a typical operation profile, i.e., the maximum power with respect to the input voltage, for PV microinverter systems. In this case, the maximum power $P_{\max}$ is 250 W when V_{in} is within [25 V, 38 V], but $P_{\max}$ declines when V_{in} is out of this range. Six operating points are identified, as shown in Table III.

In the PV microinverter systems (see Fig. 1), the dc-link voltage can be regulated either by the front-end dc–dc stage or by the dc–ac inverter stage. If the MPPT is implemented with the dc–dc stage, then the dc-link voltage will be regulated by the inverter stage, and vice versa. However, it is not necessary

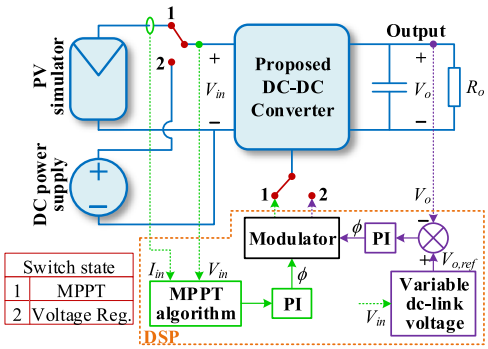

Fig. 22. Control diagram of the proposed dc–dc converter with two operation modes: output (dc-link) voltage regulation or MPPT.

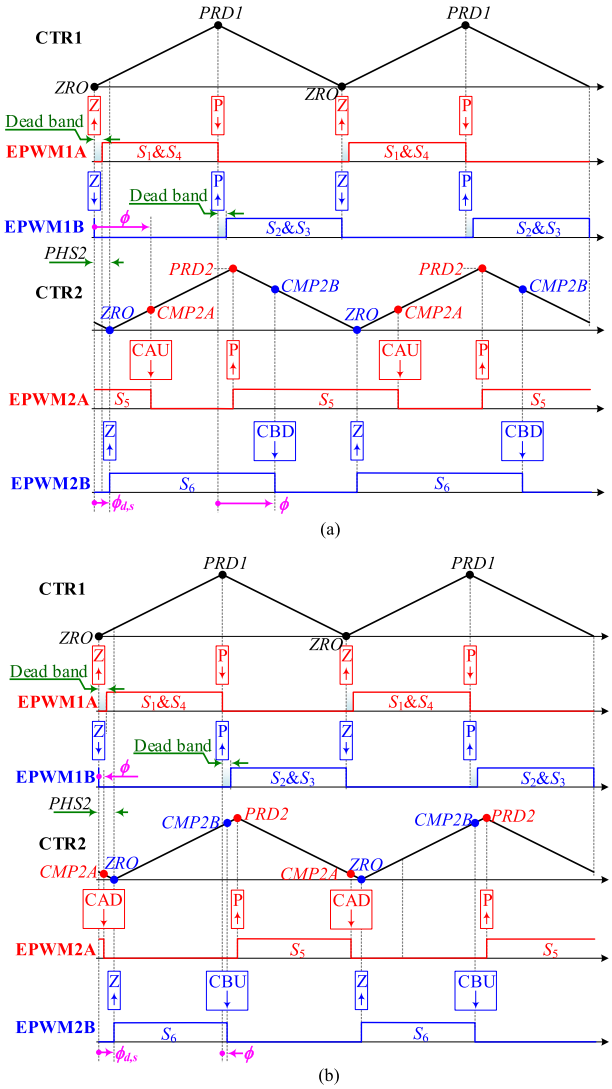

Fig. 23. Modulation waveforms based on TMS320F28075 DSP. (a) $\phi > \phi_{d,s}$. (b) $\phi \leq \phi_{d,s}$. PRD1 and PRD2 represent the period registers of the two ePWM modules (ePWM1 and ePWM2), PHS2 is the phase register of ePWM2, and CMP2A and CMP2B are the counter-compare A and B registers of ePWM2. CAU indicates the event when the counter CTR2 equals the active CMP2A resister and CTR2 is incrementing. CAD indicates the event when the counter CTR2 equals the active CMP2A resister and CTR2 is decrementing. CBU indicates the event when the counter CTR2 equals the active CMP2B resister and CTR2 is incrementing. CBD indicates the event when the counter CTR2 equals the active CMP2B resister and CTR2 is decrementing. Z and P represent the events when the counter equals zero and the period, respectively.

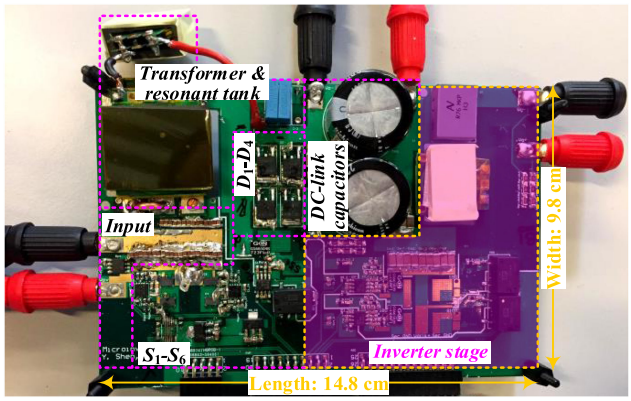

Fig. 24. Photo of the PV microinverter prototype.

TABLE IV
PARAMETERS OF THE CONVERTER PROTOTYPE

Parameters	Values
Input voltage V_{inN}	17-43 V
Nominal input voltage V_{inN}	34 V
Most probable PV (input) voltage range	20-40 V
Output voltage V_o	340-430 V
Rated power P_N	250 W
Transformer turns ratio $n = N_s : N_p$	10
Magnitizing inductance L_m	152 μH
Resonant inductor L_r	34 μH
Resonant capacitor C_r	0.75 nF
Switching frequency f_s	1 MHz
Primary-side switches S_1-S_4	eGaN FET, EPC2029 $R_{ds,on}$ = 3.2 mΩ
Secondary-side switches S_5-S_6	GaN eHEMT, GS66504B $R_{ds,on}$ = 100 mΩ
Rectifier diodes D_1-D_4	SiC Schottky Diode, C3D02060E
DC-link capacitors C_{o1}& C_{o2}	LGJ2E181MELB15, 180 μF/250 V

to always keep the dc-link voltage constant [9]. In this paper, a variable dc-link voltage control is proposed, as shown in Fig. 21. When the input PV voltage V_{in} is lower than 34 V, the dc-link (output) voltage will be always regulated to 340 V; however, when V_{in} is higher than 34 V, then the dc-link (output) voltage reference will rise with the increase of V_{in}. Thus, the input voltage range can be extended from [20 V, 40 V] with the conventional fixed dc-link voltage control to [17 V, 43 V] with the new control. In the meanwhile, the RMS currents under the variable dc-link voltage control are also reduced, which is beneficial to efficiency improvement.

As aforementioned, the proposed dc–dc converter can be controlled either to achieve the MPPT of the PV panel or to regulate the dc-link voltage. In order to demonstrate the feasibility of the proposed converter in both cases, a flexible control scheme is applied, as shown in Fig. 22. If operation mode 1 is enabled, the proposed dc–dc converter will be connected to a PV simulator and it will be controlled to achieve the MPPT; if operation mode 2 is selected, then the proposed converter will be powered by a dc power supply and it will be used to regulate the output voltage to the reference $V_{o,\text{ref}}$.

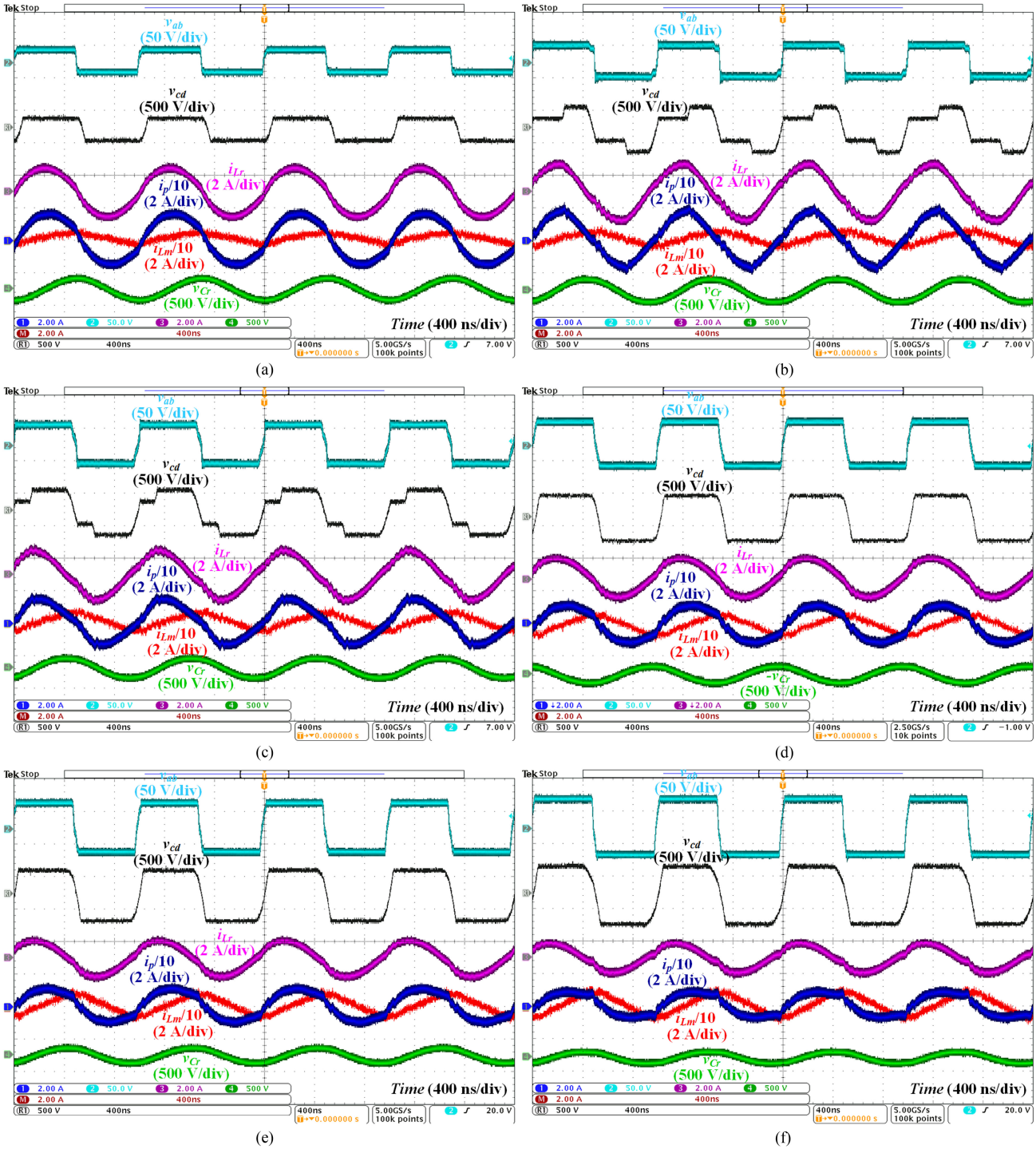

Fig. 25. Steady-state performance of the proposed converter under different conditions (see Fig. 21 and Table III). (a) Operating point A: $V_{\text{in}} = 17\,\text{V}$, $V_o = 340\,\text{V}$, and $P_o = 170\,\text{W}$. (b) Operating point B: $V_{\text{in}} = 25\,\text{V}$, $V_o = 340\,\text{V}$, and $P_o = 250\,\text{W}$. (c) Operating point C: $V_{\text{in}} = 30\,\text{V}$, $V_o = 340\,\text{V}$, and $P_o = 250\,\text{W}$. (d) Operating point D: $V_{\text{in}} = 34\,\text{V}$, $V_o = 340\,\text{V}$, and $P_o = 250\,\text{W}$. (e) Operating point E: $V_{\text{in}} = 38\,\text{V}$, $V_o = 380\,\text{V}$, and $P_o = 250\,\text{W}$. (f) Operating point F: $V_{\text{in}} = 43\,\text{V}$, $V_o = 430\,\text{V}$, and $P_o = 220\,\text{W}$.

B. Modulation Implementation

The modulation waveforms are shown in Fig. 23. Two enhanced pulsewidth modulator (ePWM) peripherals of TMS320F28075 digital signal processor (DSP), i.e., ePWM1 and ePWM2, are utilized, and their output signals are EPWM1A/EPWM1B and EPWM2A/EPWM2B, respectively. EPWM1A and EPWM1B are the gate signals of S_1 and S_4 and S_2 and S_3, respectively. EPWM2A and EPWM2B are used to control S_5 and S_6, respectively. Each time-base counter CTR of the ePWM modules is running in the count-up-and-down

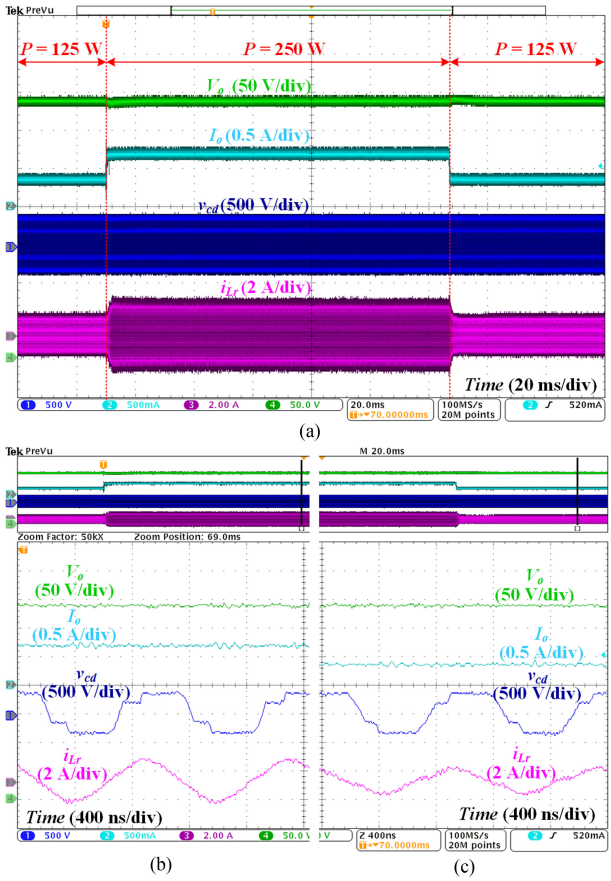

Fig. 26. Transient performance of the proposed converter with the output voltage closed-loop control (the input voltage $V_{\text{in}} = 30$ V and the output voltage reference $V_{o\_\text{ref}} = 340$ V). (a) Transition between $P = 250$ W and $P = 125$ W. (b) Zoomed-in waveforms at $P = 250$ W. (c) Zoomed-in waveforms at $P = 125$ W.

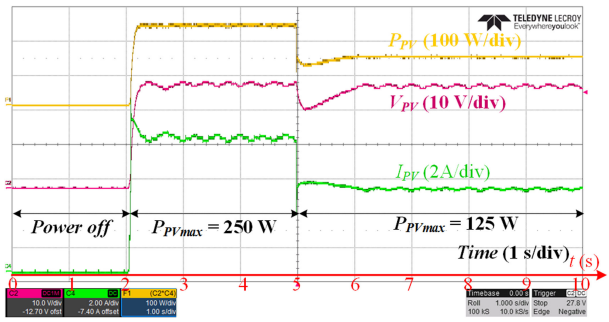

Fig. 27. Measured PV MPPT waveforms of the proposed converter powered by a PV simulator. At $t = 2$ s, the PV simulator is connected with the converter prototype, and the PV simulator operates at its MPP being 250 W after a short transition; at $t = 5$ s, the maximum power of the PV simulator steps to 125 W, and the MPPT controlled converter allows the PV simulator to track its MPP at 125 W.

mode, and the period registers of ePWM1 and ePWM2 are the same. The dead time of EPWM1A (S_1 and S_4) and EPWM1B (S_2 and S_3) is achieved by using the dead-band submodule of ePWM1. There is a phase shift $PHS2$ between the two counters ($CTR2$ and $CTR1$) of ePWM2 and ePWM1. The phase shift is used to generate the turn-ON delay of S_5 and S_6 with respect to the turn-OFF events of S_1 and S_4 and S_2 and S_3, as indicated by $\phi_{d,s}$ in Fig. 11.

The values of the period registers $PRD1$ and $PRD2$ are determined by

$$\text{PRD1} = \text{PRD2} = f_s/(2f_{\text{cpu}}) \tag{37}$$

where f_{cpu} is the clock frequency of the microcontroller. For the two counter-compare registers CMP2A and CMP2B, their values and actions generated by the "CTR2 = CMP2A/B" event are different in two cases

$$\text{CMP2A} = \begin{cases} \text{PRD2} \times (\phi - \phi_{d,s})/\pi \\ \text{Action : EPWM2A clears at CAU} \end{cases}, \phi_{d,s} < \phi \le \pi$$
$$\begin{cases} \text{PRD2} \times (\phi_{d,s} - \phi)/\pi \\ \text{Action : EPWM2A clears at CAD} \end{cases}, 0 \le \phi \le \phi_{d,s}$$

$$\text{CMP2B} = \begin{cases} \text{PRD2} \times \left[1 - (\phi - \phi_{d,s})/\pi\right] \\ \text{Action : EPWM2B clears at CBD} \end{cases}, \phi_{d,s} < \phi \le \pi$$
$$\begin{cases} \text{PRD2} \times \left[1 - (\phi_{d,s} - \phi)/\pi\right] \\ \text{Action : EPWM2B clears at CBU.} \end{cases}, 0 \le \phi \le \phi_{d,s}. \tag{38}$$

The modulation scheme enables the converter control variable, i.e., the phase shift ϕ, to be adjusted from 0 to π.

C. Experimental Verifications

A 250-W converter prototype with the dimension of 14.8 cm × 9.8 cm × 2 cm has been built up, as shown in Fig. 24. The detailed parameters are listed in Table IV. The steady-state performance at the six operating points (see Table III) is shown in Fig. 25. As can be seen, the steady-state waveforms are in close agreement with the theoretical analysis in Section II.

As stated in Section V-A, there are two control options for the dc–dc stage in microinverter applications, i.e., the dc–dc converter can be used either to achieve the MPPT or to regulate the dc-link voltage. Fig. 26 presents the dynamic experimental waveforms of the proposed converter with the output voltage closed-loop control (i.e., operation mode 2 is enabled in Fig. 22). As can be seen, the output voltage V_o can be regulated to the reference being 340 V after the load changes. A good dynamic performance is achieved: the transition time is less than 10 ms and the voltage overshoot and undershoot are quite small, i.e., less than 5 V.

Then, the MPPT control mode (i.e., operation mode 1 in Fig. 22) is selected for the proposed dc–dc converter, and the experimental dynamic performance is tested, as shown in Fig. 27. It is seen that the proposed converter with the MPPT control enables the PV simulator to track its MPPs under different conditions.

The soft-switching performance of the proposed converter is tested at different operating points, as shown in Fig. 28. Due to the symmetry of the topology and the modulation scheme, only the waveforms of S_4 and S_6 are given. As can be seen, the drain–source voltage has fallen to zero before the corresponding

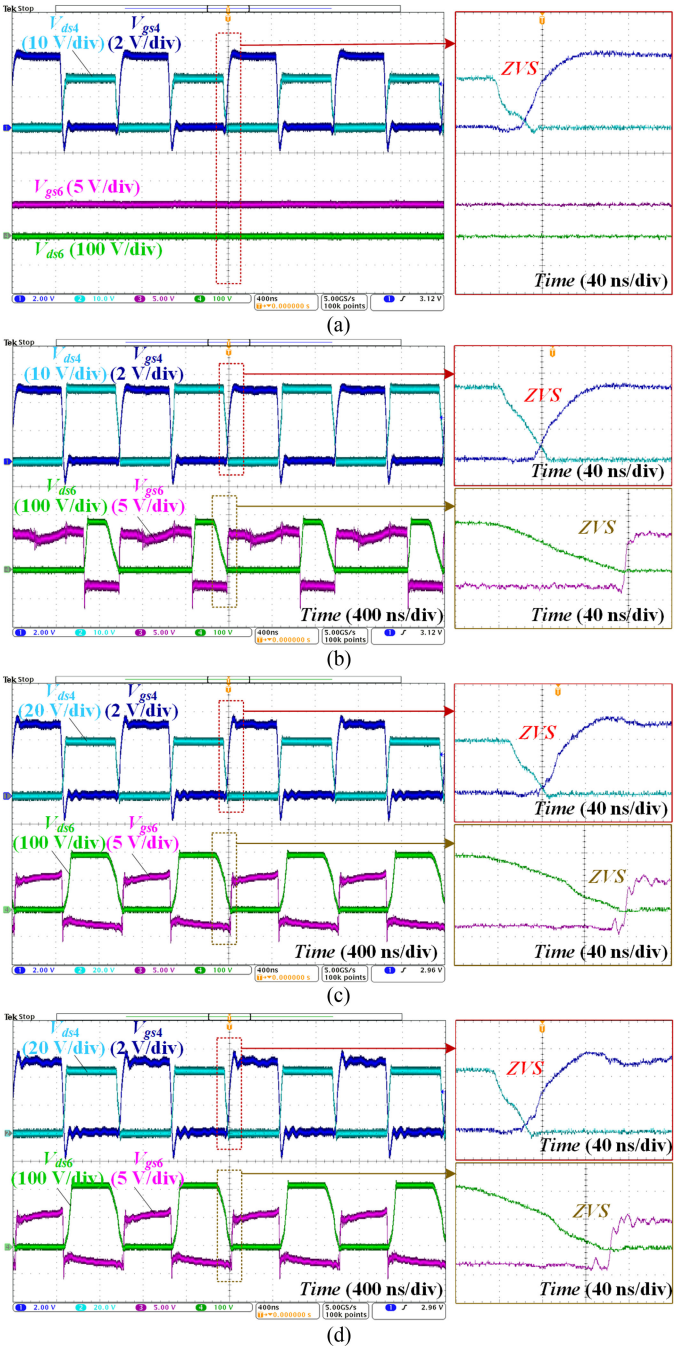

Fig. 28. Soft-switching waveforms of the proposed converter at different operating points. (a) Operating point *A:* $V_{\text{in}} = 17$ V, $V_o = 340$ V, and $P_o = 170$ W. (b) Operating point *B:* $V_{\text{in}} = 25$ V, $V_o = 340$ V, and $P_o = 250$ W. (c) Operating point *E:* $V_{\text{in}} = 38$ V, $V_o = 380$ V, $P_o = 250$ W. (d) Operating point *F:* $V_{\text{in}} = 43$ V, $V_o = 430$ V, and $P_o = 200$ W.

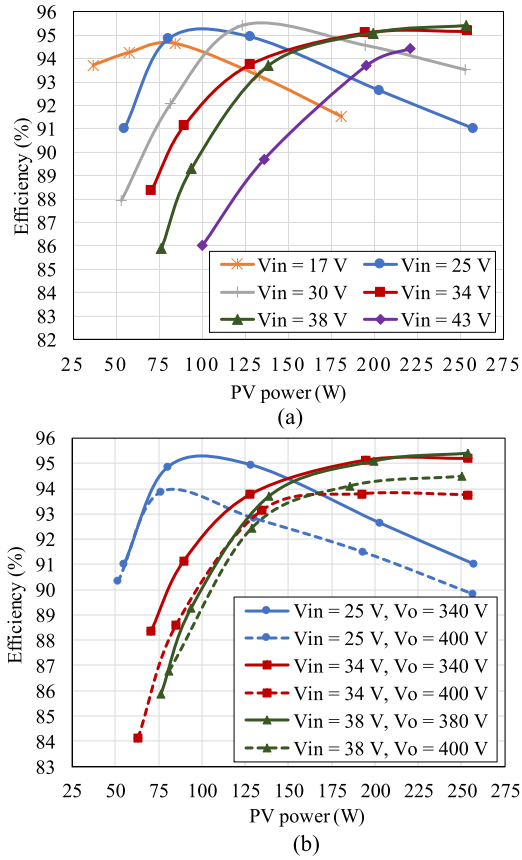

Fig. 29. Measured efficiency of the converter prototype. (a) Efficiency curves at different input voltages with the variable dc-link voltage control. (b) Efficiency comparison between the variable and fixed dc-link voltage control schemes. Solid lines represent the efficiencies with the variable dc-link voltage control and dashed lines are the results with the fixed dc-link voltage control.

gate–source voltage rises to its threshold voltage. That is, the antiparallel diode conducts before the gate signal is applied. Thus, the ZVS-ON is achieved, leading to a negligible turn-ON loss for the switches.

The measured efficiency curves of the proposed converter with the variable dc-link voltage control (see Fig. 21) at different input voltages are shown in Fig. 29(a). As can be seen, peak efficiencies over 95% are achieved for a wide input voltage range, i.e., $V_{\text{in}} = 25$, 30, 34, 38, and 43 V. The measured full-load (250-W) efficiency increases with respect to the input voltage. This is due to the fact that the RMS currents and conduction losses reduce as the input voltage rises. When the proposed converter is controlled to have a constant dc-link (output) voltage 400 V, the efficiency is measured at different input voltages $V_{\text{in}} = 25$ V, 34 V, and 38 V, as shown in Fig. 29(b). It can be seen that the variable dc-link voltage control enables a significant efficiency improvement for the proposed converter. Moreover, the proposed variable dc-link voltage control allows the converter to cope with a more wide input voltage range $V_{\text{in}} \in [17\text{ V}, 43\text{ V}]$ than the conventional fixed dc-link voltage control ($V_{\text{in}} \in [\,20\text{ V}, 40\text{ V}\,]$).

The power losses of the main components are calculated at different input voltages and control schemes, as shown in Fig. 30. Overall, the power semiconductors devices (S_1–S_4, S_5–S_6, D_1–D_4) and magnetic components (transformer T_x and resonant inductor L_r) represent the major power loss sources. The power losses of S_1–S_4, S_5–S_6, D_1–D_4, and L_r decline with respect to the increase of V_{in}, whereas the power loss of T_x rises due to the increased core loss at a higher input voltage V_{in}. Meanwhile, it is seen from Fig. 30 that the power losses of D_1–D_4 become higher with the variable dc-link voltage control; it is because D_1–D_4 suffer from a higher rectifier current in comparison with the fixed dc-link voltage ($V_o = 400$ V)

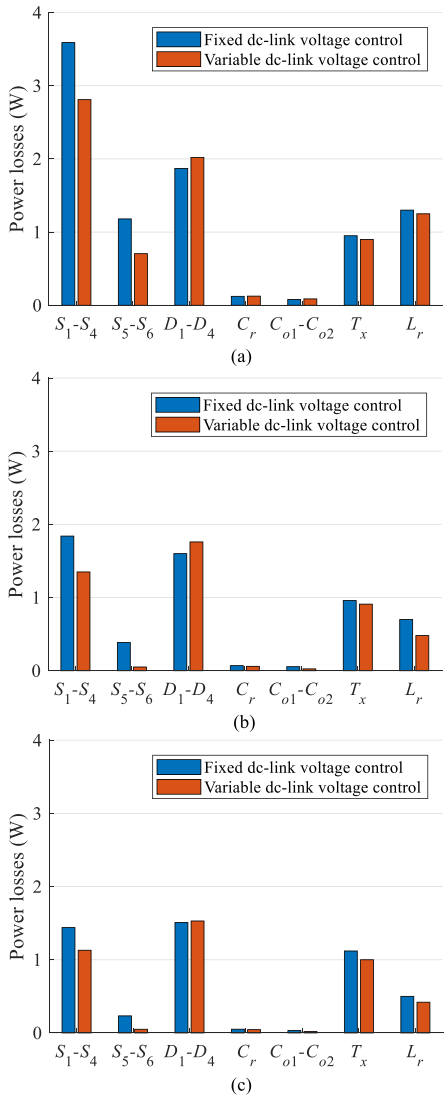

Fig. 30. Power loss breakdown of the proposed converter with different input voltages and control schemes. (a) $V_{\text{in}} = 25$ V and $P = 250$ W. (b) $V_{\text{in}} = 34$ V and $P = 250$ W. (c) $V_{\text{in}} = 38$ V and $P = 250$ W.

control. Nevertheless, the new control scheme enables to reduce the power losses of other main components S_1–S_4, S_5–S_6, T_x, and L_r. Therefore, higher power conversion efficiencies can be achieved for the proposed converter.

VI. Conclusion

In this paper, a new dual-mode-rectifier-based series resonant dc–dc converter was proposed for PV microinverter applications. The modulation, operation principles, and key characteristics were analyzed. A detailed power loss modeling and design optimization of main components were performed, and a variable dc-link voltage control scheme was introduced to the proposed converter. A 1-MHz 250-W converter prototype has been tested and the experimental results have verified the theoretical analysis. The proposed converter with the variable dc-link voltage control can cope with a wide input voltage range, e.g., from 17 to 43 V. The active switches and diodes can achieve ZVS-ON and ZCS-OFF, respectively. Compared with the conventional constant dc-link voltage control, the proposed variable dc-link voltage control enables a remarkable efficiency improvement. High power conversion efficiencies (peak efficiency = 95.5%) can thus be achieved over the wide input voltage range from 17 to 43 V, as tested on the 250-W prototype. Therefore, the proposed topology is a promising converter candidate for PV microinverter systems.

Appendix

The secondary and primary transformer RMS currents are expressed as

$$\begin{cases} I_{Lr,\text{rms}} = \frac{\sqrt{A_2^2(\sigma-\sin\sigma\cos\sigma)+A_1^2(\phi-\sin\phi\cos\phi)}}{\sqrt{2\pi}} \\ I_{p,\text{rms}} = \frac{V_o}{2\sqrt{3\pi}mGZ_r}\left(6\pi\left[(\alpha-\sigma)^2-\phi^2\right]+3\pi^2(-\alpha+\sigma+\phi)\right. \\ \quad \left.-4(\alpha-\sigma)^3+4\phi^3+\pi^3\right) \\ +\sqrt{\frac{3}{\pi}}\begin{pmatrix} mA_2^2\sigma GZ_r/V_o + A_1\left[Gmr_1(\phi-\sin\phi\cos\phi)\right. \\ \quad \left.+2(\pi-2\phi)\cos\phi-2\pi+4\sin\phi\right] \\ +A_2\left[(-2\alpha+2\sigma+\pi)\cos\sigma\right. \\ \left.-\sin\sigma(A_2Gm\cos\sigma Z_r/V_o+4)-2(\pi-2\alpha)\right] \end{pmatrix} \end{cases} \tag{39}$$

where $\sigma = \alpha - \phi$.

The resonant current in (8) and (10) can be expanded into its Fourier series as

$$i_{Lr}(t) = \sum_{n=1,3,\ldots}\left[a_n\sin(n\omega_s t)+b_n\cos(n\omega_s t)\right] \tag{40}$$

where (41) shown at the bottom of this page.

$$\begin{cases} a_1 = \frac{1}{\pi}\left(A_2[(\alpha-\phi)\cos\delta-\sin(\alpha-\phi)\cos(\alpha+\delta+\phi)]+A_1(\phi-\sin\phi\cos\phi)\right) \\ b_1 = \frac{1}{\pi}\left(A_2[\alpha\sin\delta+[\cos(\delta+2\phi)-\cos(\delta+2\alpha)]/2-\phi\sin\delta]+A_1\sin^2\phi\right) \\ a_n = \frac{1}{\pi(n^2-1)}\left(-A_2\begin{pmatrix}(n+1)\sin[\delta-(n-1)\alpha]+(n-1)\sin[\delta+(n+1)\alpha] \\ -2[n\sin(\delta+\phi)\cos(n\phi)-\cos(\delta+\phi)\sin(n\phi)]\end{pmatrix}\right. \\ \qquad \left.+2A_1[n\sin\phi\cos(n\phi)+\cos\phi\sin(n\phi)]\right), n=3,5,\ldots \\ b_n = \frac{1}{\pi(n^2-1)}\left(A_2\begin{pmatrix}(n+1)\cos[\delta-(n-1)\alpha]-(n-1)\cos[\delta+(n+1)\alpha] \\ -2[n\sin(\delta+\phi)\sin(n\phi)+\cos(\delta+\phi)\cos(n\phi)]\end{pmatrix}\right. \\ \qquad \left.+2A_1[n\sin\phi\sin(n\phi)+\cos\phi\cos(n\phi)-1]\right), n=3,5,\ldots. \end{cases} \tag{41}$$

Then, the RMS value of the n_{th} harmonic of the resonant current can be obtained as

$$I_{Lr,\mathrm{rms},n} = \sqrt{\frac{a_n^2 + b_n^2}{2}}. \tag{42}$$

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