A Novel Non-Intrusive Technique for BTI Characterization in SiC MOSFETs

Jose Angel Ortiz González , *Member, IEEE*, and Olayiwola Alatise

***Abstract*—Threshold voltage (V_{TH}) shift due to bias temperature instability (BTI) is a well-known problem in SiC MOSFETs that occurs due to oxide traps in the SiC/SiO_2 gate interface. The reduced band offsets and increased interface/fixed oxide traps in SiC MOSFETs makes this a more critical problem compared to silicon. Before qualification, power devices are subjected to gate bias stress tests after which V_{TH} shift is monitored. However, some recovery occurs between the end of the stress and V_{TH} characterization, thereby potentially underestimating the extent of the problem. In applications where the SiC MOSFET module is turned OFF with a negative bias at high temperature, if the V_{TH} shift is severe enough, there may be electrothermal failure due to current crowding since parallel devices lose synchronization during turn-ON. In this paper, a novel method that uses the forward voltage of the body diode during reverse conduction of a small sensing current is introduced as a technique for monitoring V_{TH} shift and recovery due to BTI. This non-invasive method exploits the increased body effect that is peculiar to SiC MOSFETs due to the higher body diode forward voltage. With the proposed method, it is possible to non-invasively assess V_{TH} shift dynamically during BTI characterization tests.**

***Index Terms*—Bias temperature instability, gate oxide, reliability, SiC MOSFET.**

I. Introduction

Bias temperature instability (BTI) is a well-known reliability hazard in SiC MOSFETs. Despite the improvements of the latest generation of SiC power MOSFETs, a survey of recent literature [1]–[10] on the subject suggests that it continues to be a topic of concern for both academia and industry. Two factors make it a more intractable problem in SiC: First, the increased density of the traps caused by the presence of carbon atoms during the oxidation of SiC [11] and second, the reduced energy band offsets between the SiC semiconductor and the SiO_2 gate insulator [1] (which results from the wider bandgap of SiC compared to silicon). These traps contribute to reduced oxide reliability as assessed by time-dependent-dielectric-breakdown and high-temperature gate bias (HTGB) stress tests as reported in the literature [12].

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When the gate of the SiC MOSFET is subjected to a positive bias, the channel goes into inversion mode, where electrons become the majority carriers in the semiconductor substrate adjacent to the MOS interface. Hence, the traps capture electrons and become net negatively charged. This causes an upward threshold voltage shift, also known as positive bias temperature instability (PBTI). Likewise, when the gate of the SiC MOSFET is subjected to a negative voltage, the channel goes into majority carrier accumulation; hence, the traps capture holes. This causes a decrease in the threshold voltage, which in this case is known as negative bias temperature instability (NBTI). The magnitude of the threshold voltage shift depends on the magnitude of the V_{GS} stress, the duration of the stress, and the temperature of the device [1], [6], [10], [13]–[16], with the latest SiC MOSFETs from different vendors exhibiting better performances under BTI than the vintage SiC MOSFETs [15], [17] since the manufacturing processes have improved. When the gate voltage stress is removed, the traps release the electrons (in the case of a positive V_{GS} stress test) and holes (in the case of negative V_{GS} stress test), in a process known as V_{TH} recovery or trap relaxation [1], [7]. However, it is well known that the V_{TH} recovery may be incomplete, thereby causing a permanent shift in V_{TH}. It has also been shown by different authors that a gate voltage of the opposite polarity to the stress voltage can accelerate V_{TH} recovery [8], [14].

In power electronic converters, where the SiC MOSFET is turned OFF at negative voltages to suppress problems like short-circuits arising from Miller capacitance induced feedback (cross-talk) [18], threshold voltage shift can cause catastrophic failure from loss of current sharing in desynchronized parallel devices [19]. In high power applications, where parallel SiC MOSFETs are held at a negative V_{GS} with high temperature for a long time and are suddenly switched ON, unsynchronized switching caused by variations in V_{TH} drift [1] can cause destructive failure due to current crowding.

The process of measuring the V_{TH} after stress tests can also alter the measured V_{TH}, with factors affecting its measurement including the measurement speed, bias interruption, and stress reapplication [3], [13]. The V_{GS} sweep direction also has an impact on the measured V_{TH} and defines a phenomenon called threshold voltage hysteresis in SiC MOSFETs [1]. Traditional reliability tests like high-temperature gate negative bias may not pick this up since some recovery of the V_{TH} shift may occur between the instant when the stress test ends and when the characterization occurs [2], [20]. This is not detected in the current reliability tests. Hence, new non-intrusive methods of

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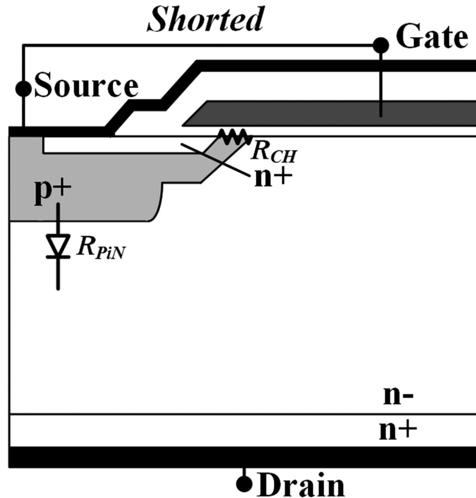


Fig. 1. Cross section of a planar MOSFET cell. Gate and source terminals shorted. Adapted from [22].

monitoring the true V_{TH} shift without altering it are required to properly characterize V_{TH} instability from BTI in SiC MOSFETs. This topic is currently under review by a new JEDEC committee formed in September 2017, the JC-70 Wide Bandgap Power Electronic Conversion Semiconductors Committee [21].

In this paper, a novel method of assessing V_{TH} shift from BTI in SiC MOSFETs is introduced. This method captures V_{TH} shift after the stress is removed and is able to monitor the change of V_{TH} during the relaxation phase. It relies on measuring the forward voltage of the body diode while it is conducting a sensing current in third quadrant operation. Section II explains the theory behind the proposed method, while Section III presents experimental results of BTI in SiC MOSFETs as well as the relationship between the third quadrant characteristics and the V_{TH} shift. The method for characterization of V_{TH} shift due to BTI is presented in Section IV, and Section V concludes the paper.

II. Body Effect and Threshold Voltage in SiC MOSFETs

The method proposed here relies on using the relationship between the body diode forward voltage and the threshold voltage in SiC power MOSFETs. The cross section of a typical planar MOSFET is shown in Fig. 1. During reverse conduction using the body diode, the gate and source are normally shorted as shown in Fig. 1. The physical drain becomes the electrical source and the physical source becomes the electrical drain. Hence, as electrons move from the physical drain to the physical source, the forward voltage of the PN junction causes a negative voltage in the channel/body with respect to the gate thereby lowering the threshold voltage and causing subthreshold conduction through the channel. This phenomenon is known as the body effect [22]–[24] and it is more pronounced in SiC MOSFETs compared to silicon MOSFETs because the forward voltage of the SiC MOSFET body diode is higher due to the lower intrinsic carrier concentration, which in turn is due to the wider bandgap in SiC [25].

Equation (1) is the standard equation for the voltage drop (V_F) across a PiN diode conducting a current density of J_T [25], where T is the temperature, k is Boltzmann's constant, d is half the width of the drift layer, q is the elementary charge, D_a is the diffusion coefficient, n_i is the intrinsic carrier concentration, and F is a complex function depending on the relationship between d and the ambipolar diffusion length L_a

$$V_F = \frac{2kT}{q} \ln\left(\frac{J_T d}{2qD_a n_i F\left(d/L_a\right)}\right). \tag{1}$$

In a MOSFET with potential conduction through the channel due to the body effect, the current density through the body diode J_{PiN} is determined by a current divider between the MOS channel resistance (R_{CH}) and the PiN diode subthreshold resistance (R_{PiN}) which can be expressed using the following equation:

$$J_{\mathrm{PiN}} = \frac{R_{\mathrm{CH}}}{R_{\mathrm{CH}} + R_{\mathrm{PiN}}} J_T. \tag{2}$$

The MOS channel resistance is given by (3) [25]. The equation for the MOS channel resistance is only valid if V_{GS} is greater than V_{TH}. L is the channel length, W is the width of the channel, μ is the mobility of electrons, C_{OX} is the gate oxide capacitance density, V_{GS} is the applied gate–source voltage and V_{TH} is the threshold voltage

$$R_{\mathrm{CH}} = \frac{L}{W\mu C_{\mathrm{OX}}\left(V_{\mathrm{GS}} - V_{\mathrm{TH}}\right)}. \tag{3}$$

During the third quadrant operation, if there is no channel conduction (assuming V_{GS} is less than V_{TH}), the source–drain voltage V_{SD} is equal to the voltage across the PiN diode as defined by (1). However, if V_{GS} becomes larger than V_{TH} (due to a negative channel voltage), V_{SD} falls as a result of a reduction in the current through the body diode since some current flows in the MOS channel. The third quadrant forward voltage can now be expressed using the following equation:

$$V_{\mathrm{SD}} = \frac{2kT}{q} \ln\left(\frac{R_{\mathrm{CH}}}{R_{\mathrm{CH}} + R_{\mathrm{PiN}}} J_T \frac{d}{2qD_a n_i F\left(d/L_a\right)}\right). \tag{4}$$

In silicon power MOSFETs during third quadrant body diode conduction, V_{SD} is usually much smaller than V_{TH}, hence, R_{CH} is much larger than R_{PiN}, meaning that $R_{\mathrm{CH}}/(R_{\mathrm{CH}} + R_{\mathrm{PiN}}) = 1$. However, in SiC MOSFETs, because V_{SD} is larger and V_{TH} is typically smaller, $R_{\mathrm{CH}}/(R_{\mathrm{CH}} + R_{\mathrm{PiN}}) < 1$, thereby causing V_{SD} to reduce due to MOS channel conduction in the third quadrant.

Fig. 2(a) shows the measured third quadrant characteristics for a silicon MOSFET and four different SiC MOSFETs (two planar and two trench devices), measured at ambient temperature (22 °C) using a curve tracer model 371B from Tektronix. It can be seen in Fig. 2(a) that the body diode forward voltage (V_{SD}) is higher for the SiC MOSFETs. Fig. 2(b) shows the measured gate transfer characteristics of the devices, where the threshold voltage can be extracted using a method defined in [26]. With different available methods for measuring V_{TH}, the current-to-square-root-of-transconductance has been selected. The advantages of this method are that it avoids the dependence of the extracted value on parasitic series resistance and mobility degradation. Comparisons of V_{TH} extraction using different methods are presented in [26], [27].

Fig. 3(a) shows the measured body diode forward voltage (V_{SD}) at low current (50 mA) as a function of the V_{GS} applied

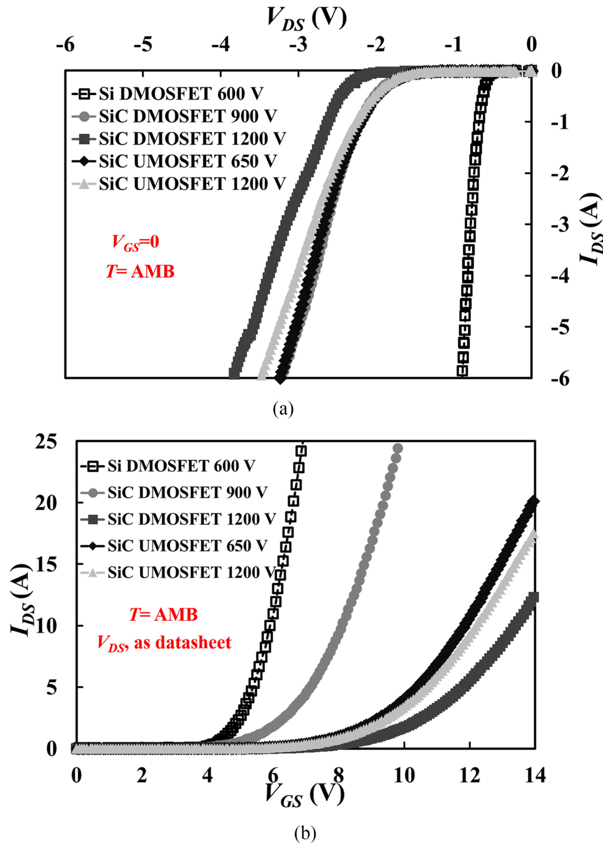


Fig. 2. (a) Third quadrant characteristics for different silicon and SiC MOSFETs. (b) Gate transfer characteristics for different silicon and SiC power MOSFETs.

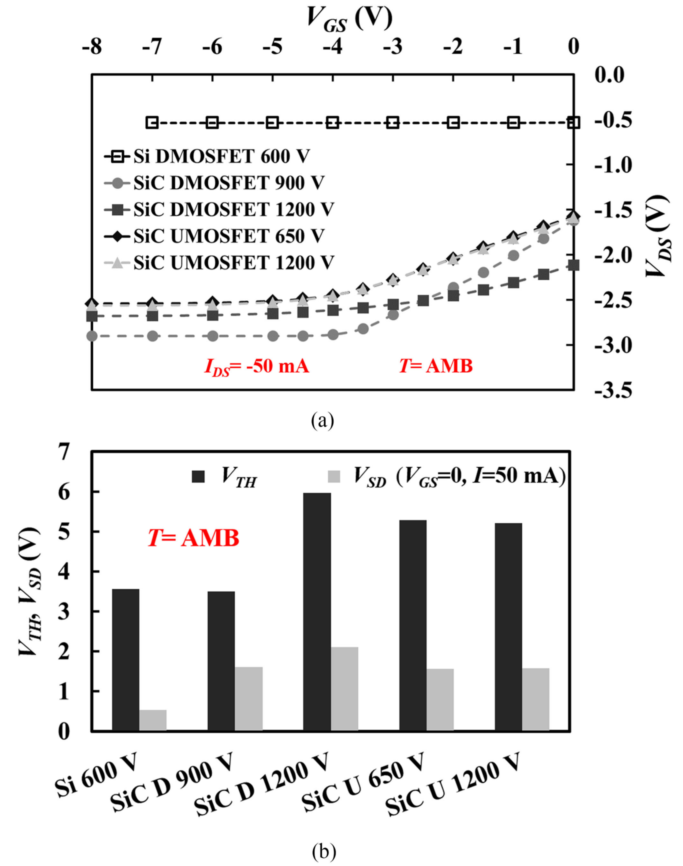


Fig. 3. (a) Measured V_{SD} as a function of negative gate bias. (b) Measured V_{TH} and V_{SD} from different silicon and SiC MOSFETs.

during measurement. This voltage was measured using a digital multimeter model HMC8012 from Hameg. Fig. 3 shows that in the case of the evaluated silicon MOSFET, the measured body diode forward voltage is independent of V_{GS}. It remains at roughly 0.5 V. However, in the SiC power MOSFETs, the absolute value of the measured body diode V_{SD} increases with the absolute value of the V_{GS} negative bias. As shown in (1)–(4), this is due to MOS channel inversion resulting from the coupling between the body diode voltage drop and the gate, i.e., the voltage drop across the PN body diode during third quadrant conduction causes a negative voltage in the p-body with respect to the gate thereby causing some subthreshold current. The overall effect causes a reduction in the absolute value of V_{SD} since there are two current flow paths (the body diode and the MOS channel). This effect does not occur in the evaluated silicon devices because of the low V_{SD} in the third quadrant and can potentially be minimized in devices with high threshold voltages.

Fig. 3(b) shows the measured V_{TH} and V_{SD} for different 600 to 1200 V silicon and SiC planar and trench MOSFETs. It can be seen from Fig. 3(b), that the larger the difference is between V_{TH} and V_{SD}, the less pronounced the body effect is. The low V_{SD} in the evaluated silicon power MOSFET suppresses the body effect while the large V_{SD} in SiC makes it visible. The proposed method for BTI characterization relies on the relationship between V_{SD} and V_{TH} which is developed in Sections III and IV of the paper.

Since the low-current V_{SD} is a well-known temperature-sensitive electrical parameter (TSEP), before introducing the BTI characterization technique, it is important to first analyze the impact of the body effect on V_{SD} as a TSEP. Since the V_{SD} of a PiN diode is the sum of the PN junction voltage and the voltage drop across the voltage blocking drift layer, the temperature coefficient of V_{SD} depends on the current flowing through the diode. At high currents, the V_{SD} has a positive temperature coefficient due to the increase in drift layer resistance with temperature while at low currents V_{SD} has a negative temperature coefficient due to increasing carrier density with temperature at the PN junction. The intersection point between the positive and negative temperature coefficients is called the zero-temperature-coefficient (ZTC) point and is where the increase in carrier density with temperature at the PN junction is counterbalanced by the increase in the drift layer resistance with temperature. Due to the body effect in SiC MOSFETs, the temperature dependency of the V_{SD} will depend on both the negative temperature coefficient of the PN junction (at low currents) and the negative temperature coefficient of the threshold voltage of the MOS channel. Both mechanisms are affected by the increase in the intrinsic carrier concentration due to bandgap narrowing as the temperature increases. Since the p-doping that forms the anode of the intrinsic body diode is typically different from the p-doping of the MOS channel (which is set by the manufacturer according to the target threshold voltage), the two temperature

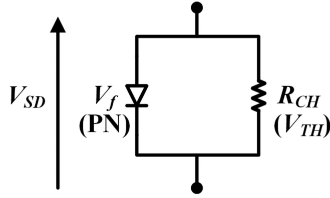


Fig. 4. Temperature sensitive elements affecting the on-state voltage of the body diode of a MOSFET (V_{SD}).

characteristics may differ however both are negative in the sense that the voltages reduce with increasing temperature. In the case of the threshold voltage, the temperature coefficient also depends on the oxide thickness as shown in (5) [28]. Ψ_B is the potential difference between the Fermi level and the intrinsic Fermi level, c_{OX} is the specific gate oxide capacitance, $\varepsilon_{\mathrm{SiC}}$ is the dielectric constant of silicon carbide, N_A is the doping density, q is the electron charge, and $E_g(0)$ is the bandgap energy at $T = 0\,\mathrm{K}$

$$\frac{dV_{\mathrm{TH}}}{dT} = \frac{d\psi_B}{dT}\left(2 + \frac{1}{c_{\mathrm{OX}}}\sqrt{\frac{qN_A\varepsilon_{\mathrm{SiC}}}{\psi_B}}\right) \tag{5}$$

where

$$\frac{d\psi_B}{dT} \approx \frac{1}{T}\left[\frac{E_g\,(0)}{2q} - |\psi_B|\right]. \tag{6}$$

Fig. 4 shows an equivalent circuit highlighting the current divider between the body diode (PN junction) and the MOS channel. The overall temperature coefficient of V_{SD} in SiC MOSFETs depends on the temperature coefficient of the two components depending on which it is dominant. To separate the observable impact of these two mechanisms on V_{SD} as a TSEP, the temperature characteristics of the body diode forward voltage (V_{SD} versus temperature) were extracted under two conditions, one without the body effect present ($V_{\mathrm{GS}} = -10\,\mathrm{V}$) and the other with the body effect present ($V_{\mathrm{GS}} = 0\,\mathrm{V}$).

When the V_{SD} versus temperature characteristics is extracted at $V_{\mathrm{GS}} = -10\,\mathrm{V}$, the channel is fully closed hence there is no MOS channel subthreshold conduction, no body effect, and no current divider in Fig. 4, i.e., all the current flows through the diode. In this case, the measured V_{SD} is the forward voltage of the PN junction and its temperature characteristics are determined solely by the negative temperature coefficient of the PN junction voltage below the ZTC point. When the V_{SD} versus temperature characteristics are extracted at $V_{\mathrm{GS}} = 0\,\mathrm{V}$, the body effect is present and there is a current divider between the MOS channel and the body diode. In this case, the temperature coefficient of the threshold voltage as defined by (5) plays a role depending on which the mechanism between the PN junction and the MOS channel is dominant in temperature sensitivity. By comparing the temperature coefficient of the V_{SD} versus temperature characteristics under both conditions, it is possible to decouple the temperature sensitivity of the two aforementioned mechanisms (the V_{TH} temperature coefficient and PN junction temperature coefficient [29]). This is what is done in Fig. 5. Fig. 5 presents the measured V_{SD} at 50 mA for a 36 A/900 V planar SiC MOSFET and a 39 A/650 V Trench SiC MOSFET at $V_{\mathrm{GS}} = 0$ and $V_{\mathrm{GS}} = -10\,\mathrm{V}$.

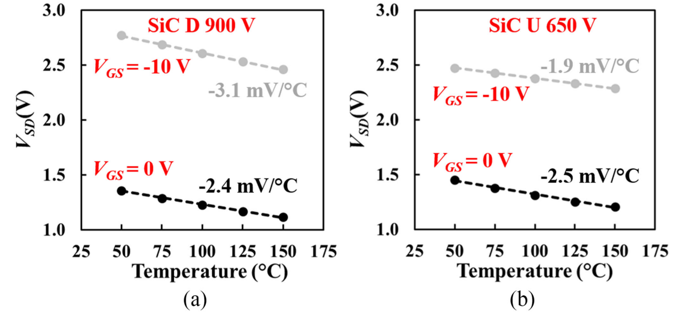


Fig. 5. (a) V_{SD} as a function of temperature for a SIC D MOSFET. $I_{\mathrm{SD}} = 50\,\mathrm{mA}$. (b) V_{SD} as a function of temperature for a SIC U MOSFET. $I_{\mathrm{SD}} = 50\,\mathrm{mA}$).

In Fig. 5(a), for the 900 V SiC planar MOSFET, the temperature sensitivity of V_{SD} reduces from –3.1 mV/°C at $V_{\mathrm{GS}} = -10\,\mathrm{V}$ (no body effect) to –2.4 m V/°C at $V_{\mathrm{GS}} = 0\,\mathrm{V}$ (body effect present). On the other hand, the opposite trend can be observed in the case of the 650 V SiC trench MOSFET shown in Fig. 5(b), where the temperature sensitivity of V_{SD} increases from –1.9 mV/°C (no body effect) to –2.5 mV/°C (body effect present). Since the temperature sensitivity of V_{TH} depends on the channel doping and oxide thickness as shown in (5) and different manufacturers using different fabrication processes will have different parameters, it is difficult to predict the overall characteristics using analytical equations especially since they will vary between planar and trench devices. The recommendation for device technologists using V_{SD} as a TSEP would be to thoroughly characterize its temperature sensitivity over a range of V_{GS} and currents to better understand the specific characteristics peculiar to the device under investigation and to ensure that there is no body effect during V_{SD} measurements.

III. BTI Measurements in SiC MOSFETs

A. *Impact of BTI on the Transfer and Third Quadrant Characteristics*

The physics of both negative and positive threshold voltage shifts from NBTI and PBTI is relatively well understood in silicon and SiC MOSFETs as detailed in several papers [1]–[10]. Hence, what this paper investigates is the relationship between V_{TH} and V_{SD} for devices that have undergone HTGB stresses, and how measuring V_{SD} can be used to characterize V_{TH} shift from BTI. Using the experimental set-up shown in Fig. 6, SiC MOSFETs have been subjected to accelerated positive and negative gate oxide stresses.

After the gate stress phase, the gate transfer and third quadrant characteristics were measured using a curve tracer Tektronix 371B at ambient temperature (22 °C), following a 16-h period to allow time for relaxation/recovery. During the relaxation phase, the gate and source are shorted ($V_{\mathrm{GS}} = 0\,\mathrm{V}$).

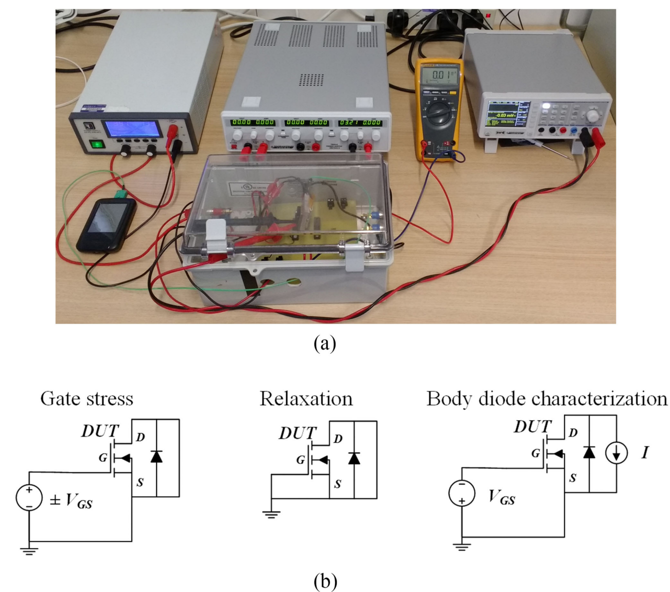


Fig. 6. (a) Picture of the experimental set-up for stressing and characterizing BTI. (b) Schematic of the set-up for the gate stress, recovery/relaxation phase and characterization of V_{SD} as TSEP.

TABLE I
HIGH-TEMPERATURE GATE BIAS STRESSES FOR EVALUATION OF BTI

	Device A (Negative HTGB)	Device B (Positive HTGB)
Stress 1	-25 V, 150 °C, 30 minutes	25 V, 150 °C, 30 minutes
Stress 2	-25 V, 150 °C, 30 minutes	28 V, 150 °C, 30 minutes
Stress 3	-30 V, 150 °C, 30 minutes	30 V, 150 °C, 30 minutes
Stress 4	-30 V, 150 °C, 30 minutes	32 V, 150 °C, 30 minutes

The devices were stressed in four stages of HTGB stress with each stage comprising of 30 min at a defined stress voltage and a junction temperature of 150 °C, which is the maximum operating junction temperature of the selected device. This temperature is limited by the conventional packaging used and not by the material properties of SiC, which allow operating temperatures above 500 °C [30]. The operating temperature is application dependent with some applications like automotive systems having ambient temperatures as high as 140 °C [30]. There is increasing interest in high-temperature electronics, hence ambient temperatures higher than 150 °C are expected [30]. This fact makes the characterization of BTI of SiC MOSFETs more critical.

The stress voltage was progressively increased during the four stages, as summarized in Table I. The objective of these highly accelerated stress tests was to degrade the gate oxide for evaluating the effectiveness of the proposed characterization method and not for lifetime evaluation which has been covered in other studies like [8] and [15]. The device evaluated in this paper was the planar SiC MOSFET, where the body effect was more apparent, i.e., the 900 V planar SiC MOSFET.

The results of the NBTI and PBTI measurements are shown in Figs. 7 and 8, respectively. As can be seen from Fig. 7(a), the negative gate bias stress test has caused the threshold voltage to reduce due to positive charge trapping from tunneling currents.

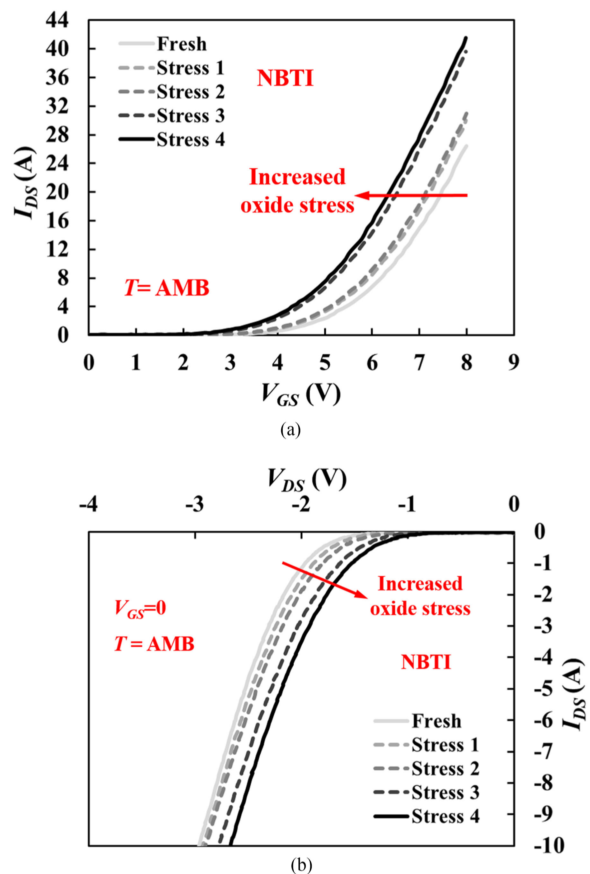


Fig. 7. (a) Gate transfer characteristics showing V_{TH} reduction from NBTI. (b) Third quadrant characteristics showing V_{SD} shift from NBTI.

This is evident from the leftward shift of the transfer characteristic after each stress period that has caused a concomitant reduction in the third quadrant V_{SD} measured at $V_{GS} = 0$ V, as shown in Fig. 7(b). With a lower threshold voltage, the body effect becomes more pronounced, hence, the increased subthreshold current causes a lower V_{SD}. The reverse occurs in the case of PBTI, where an increased in the V_{TH} (rightward shift in the transfer characteristic) is seen in Fig. 8(a) and a concomitant increase in the magnitude of the V_{SD} is seen in Fig. 8(b). As a result of this, using the third quadrant characteristic, it is possible to detect V_{TH} shift due to BTI.

B. Considerations for Condition Monitoring

Condition monitoring is increasingly of interest to academic and industrial researchers as a tool for *in situ* operational management [31]. An option mentioned by different authors is the use of TSEPs [32], [33] for detecting the degradation of the packaging of the device. Different researchers have cited the use of the MOSFET body diode conduction characteristics as a TSEP since there is a well-known temperature dependence of the forward voltage, for example, in [34] and [35]. As it is a widely used TSEP, it is important to evaluate how the stress of the gate oxide will affect its accuracy as temperature indicator.

The temperature dependence of the V_{SD} at low currents has been measured for the evaluated SiC MOSFETs subjected to both

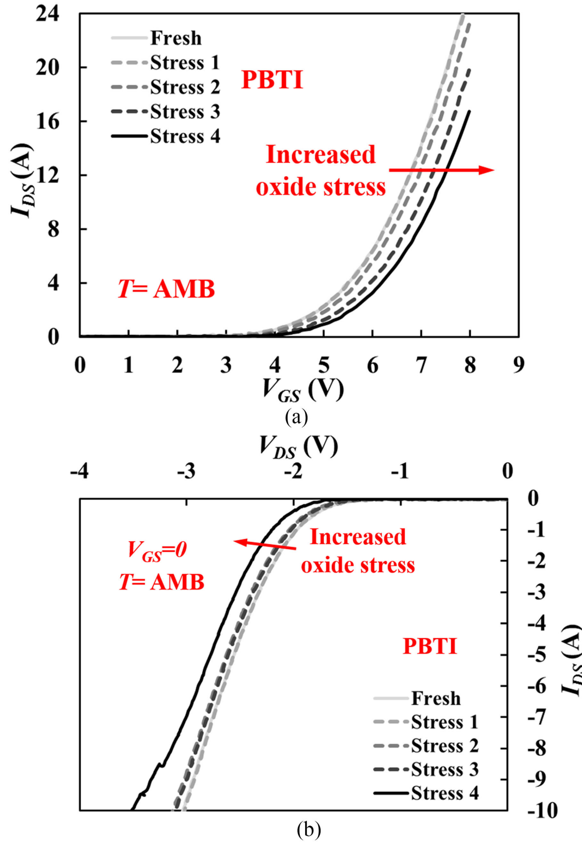


Fig. 8. (a) Gate transfer characteristics showing V_{TH} increase from PBTI. (b) Third quadrant characteristics showing V_{SD} shift from PBTI.

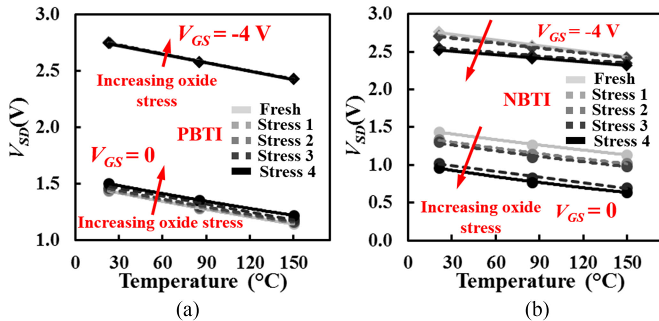


Fig. 9. (a) V_{SD} versus temperature for SiC MOSFETs under PBTI ($I_{\mathrm{SD}} = 50\,\mathrm{mA}$, $V_{\mathrm{GS}} = 0\,\mathrm{V}$ and $V_{\mathrm{GS}} = -4\,\mathrm{V}$). (b) V_{SD} versus temperature for SiC MOSFETs under NBTI, ($I_{\mathrm{SD}} = 50\,\mathrm{mA}$, $V_{\mathrm{GS}} = 0\,\mathrm{V}$ and $V_{\mathrm{GS}} = -4\,\mathrm{V}$).

positive and negative HTGB stress tests. Fig. 9(a) shows the V_{SD} versus temperature characteristics at $V_{\mathrm{GS}} = 0$ and –4 V, measured at different stages of oxide degradation (shown in Table I) for positive HTGB, while Fig. 9(b) shows the measurements for the negative HTGB tests. The current used for this characterization is $I_{\mathrm{SD}} = 50\,\mathrm{mA}$ and the temperature of the device was set using a small dc heater attached to the device. Comparing Fig. 9(a) and (b), it is observed that the impact of PBTI on the V_{SD} is apparently not as pronounced as NBTI. Looking at Fig. 9(a), the V_{SD} increases with positive gate voltage stress (over all temperatures) due to a rise in V_{TH}. However, comparing Fig. 9(a) and (b), the observable stress induced shift in V_{SD} is less apparent as the absolute value of V_{GS} increases from 0 to –4 V.

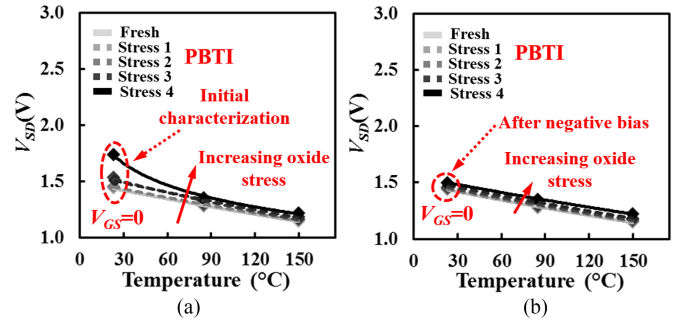


Fig. 10. Impact of the negative bias during characterization on PBTI. (a) Initial characterization. (b) After applying a negative gate bias during characterization.

At $V_{\mathrm{GS}} = 0\,\mathrm{V}$, V_{SD} shifts by +75 mV between the unstressed device and the device that has undergone the four stages of positive HTGB stress as detailed in Table I. At $V_{\mathrm{GS}} = -4\,\mathrm{V}$, the shift in V_{SD} between the unstressed and stressed device can be considered equal to 0. In the case of NBTI, at $V_{\mathrm{GS}} = 0$, the shift of V_{SD} is –490 mV, while at $V_{\mathrm{GS}} = -4$ V the average shift is –177 mV, with the shift being more apparent at lower temperatures than at high temperatures.

During the characterization of V_{SD}, negative voltages were applied to the gate–source for determining the TSEP characteristics (namely $V_{\mathrm{GS}} = -4\,\mathrm{V}$). In the case of the negative HTGB stress, this voltage does not compensate the initial V_{TH} shift caused during the stress. However, in the case of the positive HTGB, the negative gate voltage applied during the characterization sequence partially compensates the V_{TH} shift [8], [14]. Fig. 10(a) shows the measured V_{SD} (at $V_{\mathrm{GS}} = 0\,\mathrm{V}$) as a function of temperature during the different stages of the positive HTGB stress before applying the negative voltage for TSEP characterization. Fig. 10(b) shows the measured V_{SD} (at $V_{\mathrm{GS}} = 0\,\mathrm{V}$) as a function of temperature after applying the negative voltage for TSEP characterization. It can be seen from Fig. 10(b) that the application of the negative gate voltage has partially corrected the V_{SD} shift caused by PBTI.

An important observation, from the results shown in Fig. 10, which has implications from the application and qualification point of view is that the technique used for determining the V_{TH} shift will have an impact on the measured V_{TH} shift and the instantaneous threshold voltage shift can be higher than the measured one. In other words, the process of measuring V_{TH} shift can potentially underestimate the problem and this is more critical for SiC given the reduced reliability of the oxide.

The results presented in Fig. 9 have two implications from the point of view of condition monitoring. First, the degradation of the gate oxide can affect the accuracy of V_{SD} as a TSEP as was already mentioned in [36], especially if it is measured at $V_{\mathrm{GS}} = 0$. Biasing the device at negative voltage minimizes the impact of the threshold voltage shift and the body effect on the temperature sensitivity of V_{SD} [35], [37], [38], however the impact of biasing the device at a negative voltage could be adverse on the reliability of the gate oxide. The change in

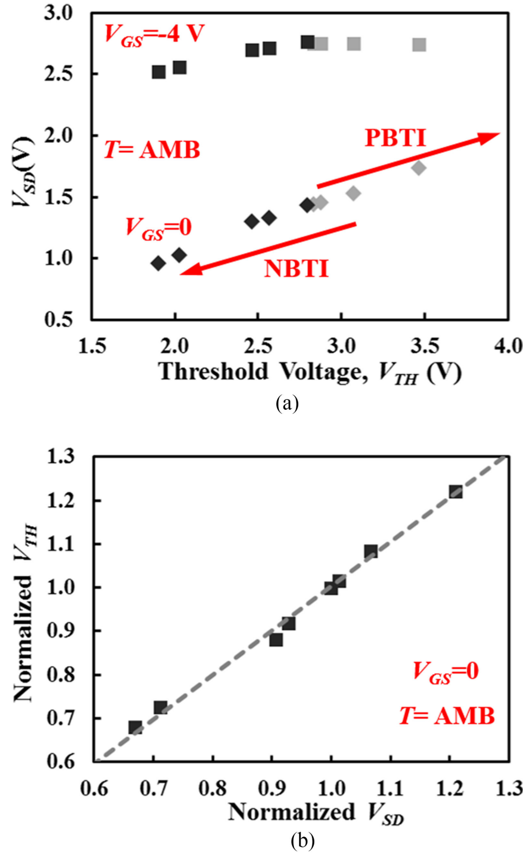
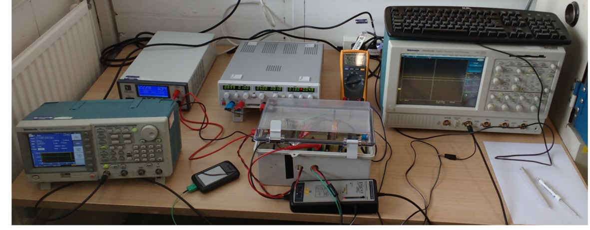
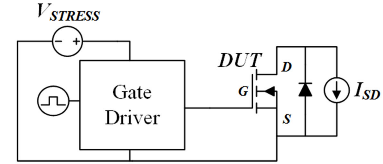


Fig. 11. (a) V_{SD} as a function of threshold voltage V_{TH} during both PBTI and NBTI. (b) Normalized V_{TH} as a function of the normalized V_{SD} (measured at $I = 50\,\mathrm{mA}$).



(a)



(b)

Fig. 12. (a) Experimental setup for characterization of BTI using the body diode. (b) Electrical schematic of the test circuit.

V_{TH} can also affect other TSEPs like the turn-ON *dI/dt* [39] and the threshold voltage itself [24]. Second, if the temperature of the device can be determined using a different technique, then the health/condition of the oxide can be ascertained from the measured V_{SD}. This can be particularly useful as a method for assessing the threshold voltage shift/gate oxide condition in applications, where a standby period allows the devices to settle at high ambient temperature with negative gate voltages.

During the stress/characterization tests, the transfer characteristics were measured at ambient temperature, hence the threshold voltages at ambient temperature can be extracted. Fig. 11 presents the measured V_{SD} as a function of the extracted threshold voltage caused by NBTI and PBTI. Regarding the extraction of the threshold voltages, as mentioned in the introduction, it is important to mention that the measuring method can affect the accuracy of the measured V_{TH}, especially for characterizing the instantaneous V_{TH} shift due to BTI [3], [13]. For the tests performed here, the objective was characterizing a more permanent V_{TH} shift after the accelerated stress test to obtain a relationship between V_{SD} and V_{TH}. The measuring sequence for extraction is given as follows.

1) After the BTI stress test, sufficient time (16 h) is allowed for the recovery to complete, at $V_{GS} = 0$. The objective was to characterize the non-recoverable shift, which can be considered stable during the characterization sequence.
2) Characterization of V_{SD} with a curve tracer Tektronix 371B at $V_{GS} = 0\,\mathrm{V}$ and ambient temperature (22 °C).
3) Characterization of the I_{DS} versus V_{GS} (gate transfer) characteristics using a curve tracer Tektronix 371B, to extract V_{TH} using the current-to-square-root-of-transconductance-ratio method [26]. Positive sweep direction and ambient temperature (22 °C).
4) TSEP characterization with 50 mA sensing current, i.e., V_{SD} versus temperature with V_{GS} = 0, –2, and –4 V. V_{SD} measured with a multimeter Hameg HMC8012.

In the case of PBTI, the values of V_{SD} used in Fig. 11 are the values measured in the initial characterization, before the application of the negative voltage. Analyzing Fig. 11, in the case of PBTI, it can be clearly observed that during the characterization of V_{SD} at $V_{GS} = -4\,\mathrm{V}$, the threshold voltage shift is not observed as the body effect is minimized. This does not happen in the case of NBTI, as the negative voltage used during characterization does not compensate the V_{TH} shift caused during the stress. The V_{TH} reduction makes the body effect apparent at $V_{GS} = -4\,\mathrm{V}$, hence a more negative V_{GS} would be required to fully cut off the channel.

The impact of the body effect and the negative V_{GS} bias can also be analyzed from the results in Fig. 11. For the NBTI measurements, at $V_{GS} = 0$, the V_{SD}/V_{TH} coefficient is 0.55 V/V, and at $V_{GS} = -4\,\mathrm{V}$, it is 0.29 V/V. For the PBTI measurements, at $V_{GS} = 0$, the V_{SD} coefficient can be considered the same as that of NBTI, however at negative V_{GS} values, the shift in V_{TH} and its impact on V_{SD} is compensated during the characterization procedure.

To remove the device-to-device variation, normalized V_{TH} as a function of normalized V_{SD} (at $V_{GS} = 0$ and an ambient temperature of 22 °C) has been calculated and plotted in Fig. 11(b). The relationship between the normalized V_{SD} and V_{TH} is given by (7) and can be used as the calibration characteristic for V_{TH} monitoring using V_{SD}

$$V_{\mathrm{TH,normalized}} = 1.02 \cdot V_{\mathrm{SD,normalized}} - 0.02. \quad (7)$$

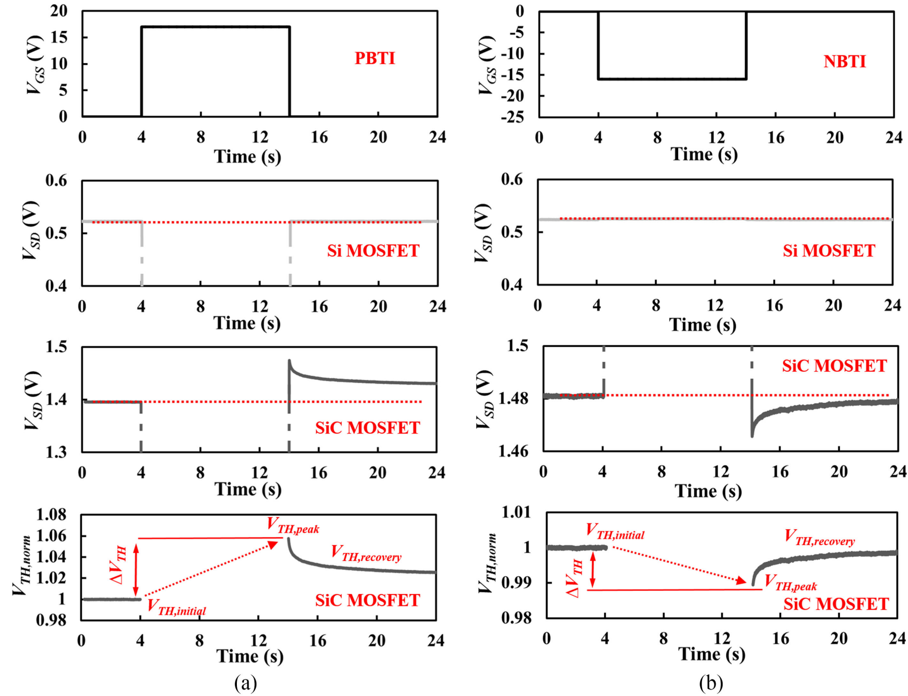


Fig. 13. (a) Evaluation of PBTI using the proposed method. $V_{GS,stress} = 17$ V, $V_{GS,rec} = 0$ V, pulse duration 10 s, $T = 22$ °C and $I_{SD} = 50$ mA, (b) Evaluation of NBTI using the proposed method. $V_{GS,stress} = -16$ V, $V_{GS,rec} = 0$ V, pulse duration 10 seconds, $T = 22$ °C and $I_{SD} = 50$ mA.

The relationship between V_{TH} and V_{SD} determined in this paper is experimental. Modeling of the body effect, which requires knowledge of the manufacturing parameters like channel doping, active area, cell pitch, and oxide thickness, is considered beyond the scope of the study presented in this paper. Further studies of the body effect are presented in [40], where its impact on the reverse recovery and dynamic avalanche is studied, in [41], where the body effect is analyzed for 10 kV SiC MOSFETs, and [42], where initial studies for an analytical model of the channel conduction in the third quadrant are presented.

IV. Novel Characterization Technique of BTI in SiC MOSFETs

As was mentioned in the previous section, the use of the forward voltage of the body diode during reverse conduction of a low current is a well-known TSEP [24], [34]. It can be used for detecting the degradation of the thermal impedance of power modules, based on the increase of the junction temperature due to the increased thermal resistance [33]. Capturing the cooling transient enables the ability of detecting the degraded elements of the packaging [43]. The method presented in this paper is similar in that it uses a sensing current to measure the forward voltage of the body diode during the third quadrant operation. The relationship between the third quadrant forward voltage and the threshold voltage is then used to monitor V_{TH} shift and relaxation during positive and negative gate bias stress tests. The test setup used for evaluating this characterization method is shown in Fig. 12(a) and a simplified electrical schematic is shown in Fig. 12(b). A gate driver with adjustable supply voltages is used for stressing the gate oxide of the device under test at positive and negative gate voltage stresses. The pulse is generated using a Tektronix waveform generator model AFG3022C, a current I_{SD} of 50 mA flows through the MOSFET, while the third quadrant V_{SD} is measured using a differential probe model TA043 from Pico Technology and a Tektronix oscilloscope model TDS5054B.

In the circuit shown in Fig. 12(b), the sensing current I_{SD} flows continuously through the MOSFET during the gate stress and relaxation phases while the body diode forward voltage V_{SD} is measured. During the gate stress phase, V_{SD} will depend on V_{GS} while during the relaxation phase, V_{SD} will depend on V_{TH}. The linear relationship between V_{SD} and V_{TH} shown in Fig. 11 is used to monitor the transient behavior of V_{TH} during the relaxation phase. For a sensing current I_{SD} of 50 mA, the results for NBTI and PTBI characterization of both Si and SiC MOSFETs are shown in Fig. 13.

In the case of PBTI evaluation, as shown in Fig. 13(a), the gate stress voltage was $V_{GS,stress} = 17$ V and the gate recovery/relaxation voltage was $V_{GS,rec} = 0$ V. At $V_{GS} = 0$ V, the MOSFET is OFF hence, the current I_{SD} flows through the body diode, resulting in a V_{SD} voltage of approximately 0.5 V for the Si MOSFET and 1.4 V for the SiC MOSFET (lower than the nominal voltage of a PiN diode due to the body effect, as described previously in Section II). During PBTI evaluation, when the device is turned ON at time $t = 4$ s the current I_{SD} flows through the channel, hence the voltage V_{SD} depends on the ON-state resistance of the MOSFET meaning its value is low, for both Si and SiC MOSFETs. At time $t = 14$ s, when gate voltage is set again to 0 V, the sensing current I_{SD} is commutated to the body diode thereby causing V_{SD} to rise to the initial value in the case of the silicon MOSFET and to a value higher than the initial value in the SiC MOSFET.

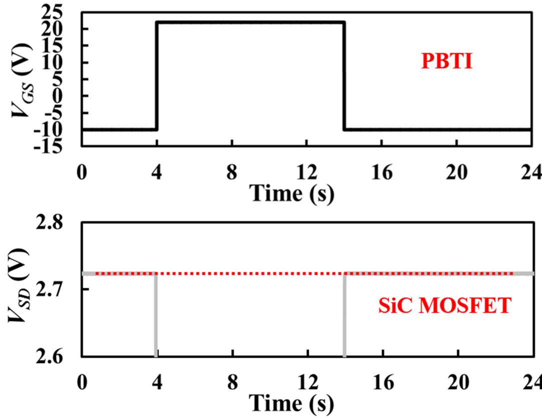


Fig. 14. Impact of the gate voltage used on the body effect. Gate voltage of –10/+22 V.

The difference between the nominal initial value and the peak value is caused by the positive shift of V_{TH} and its impact on the body effect. This peak V_{SD} value is followed by an exponential decay due to the threshold voltage recovery. This is not observable in the silicon MOSFET, not because there is no V_{TH} shift, but because there is no body effect in the evaluated silicon MOSFET. Fig. 13(a) shows the normalized V_{TH} shift and recovery for PBTI calculated using (7).

Fig. 13(b) shows the NBTI characterization, where the stress is $V_{GS,stress} = -16$ V and $V_{GS,rec} = 0$ V is used for the relaxation/recovery phase. In the case of the Si MOSFET, V_{SD} is independent of V_{GS} since the body effect is suppressed. In the case of the SiC MOSFET, during the stress phase, the channel is in accumulation (highly non-conductive) and V_{SD} increases to a higher value, (around 2.7 V, corresponding to a SiC PiN diode forward voltage) as was shown in Section II. After the stress phase, V_{GS} is set to 0 V, in the relaxation phase. In the case of the SiC MOSFET, V_{SD} returns to a value below the prestress value, because of the reduction of V_{TH} and its impact on the body effect. Similar to PBTI, the initial lower peak is followed by the subsequent recovery after the stress has been removed. Fig. 13(b) shows the normalized V_{TH} calculated using (7), where the V_{TH} shift and recovery can be observed for NBTI.

This method of characterizing BTI in SiC MOSFETs is based on the body effect and its impact on the third quadrant characteristics. Hence, if the objective is to observe the V_{TH} shift and recovery using the third quadrant V_{SD}, then it is advised to set $V_{GS} = 0$ V during the recovery phase, as the impact of the body effect is more apparent. Using a negative V_{GS} will disguise the V_{TH} shift under positive HTGB stress tests. This is shown in Fig. 14, where the stress voltage $V_{GS,stress}$ is 22 V and the voltage used during the recovery/characterization phase is $V_{GS,rec} = -10$ V. In Fig. 14, no V_{TH} shift is evident because the negative bias during recovery masks the shift.

For both PBTI and NBTI, using a suitable V_{GS} voltage during reverse conduction of a small current, the difference between the prestress V_{SD} and the poststress V_{SD} is indicative of the threshold voltage shift. The advantage of using the V_{SD} to monitor the V_{TH} is the fact that V_{TH} shift and recovery can be assessed *in situ* without interfering with the physical mechanisms in action, i.e., NBTI and PBTI can be assessed without directly measuring the threshold voltage. The exponential recovery of V_{SD} to its prestress value is indicative of the recovery of the threshold voltage to its prestress value, hence the recovery time can be characterized using this technique in a non-intrusive way.

The heater used for the TSEP characterization in Section III was attached to the device, thereby adding thermal mass and acting as a heatsink in this case, hence the temperature can be monitored during the tests to verify the impact of self-heating during the stress tests. Given that both V_{SD} and V_{TH} are affected by temperature, it is important to ensure that the measurements of V_{TH} shift are solely due to BTI and not self-heating due to the measurement set-up. Since the sensing current used in V_{SD} characterization can cause some self-heating, it is important to quantify its impact and ensure it does not cause error in ascertaining the V_{TH} shift. During the stress phase of the PBTI measurements, self-heating can be neglected for any sensing current (I_{SD}) level due to the very low dissipated power ($V_{SD} \cdot I_{SD}$) since the V_{SD} is low at the ON-state voltage of the device. For example, under PBTI stressing, a sensing current of 50 mA and a V_{SD} of 3 mV leads to a dissipated power of 150 μW which given the heatsink used caused a case temperature change (ΔT_{CASE}) of 0.05 °C. However, during the stress phase of the NBTI measurements, with the sensing current of 50 mA and with the V_{SD} at 2.7 V, the dissipated power due to the self-heating of the device is estimated at 135 mW, which results in a temperature change of 0.1 °C given the heatsink used. For both PBTI and NBTI, there can also be self-heating during the relaxation period. Hence, by ensuring an adequate heatsink was used during the BTI stresses, the experimental measurements in V_{TH} shift due to BTI were not affected by self-heating since the junction and case temperature rise was negligible, i.e., a junction temperature rise of 0.1 °C corresponds to a V_{SD} shift of –240 μV according to the calibration curve shown in Fig. 5(a) which when compared to V_{SD} shifts due to BTI in Fig. 13, which is in the range of several tens of mV, can be considered insignificant.

Fig. 15 shows experimental measurements of the case temperatures during typical NBTI and PBTI stress cycles. The temperatures were logged using a thermocouple data logger TC-08 from Pico Technology, which measured the case temperature of the device. This has been done for a series of stress pulses using a long recovery time and the results are shown in Fig. 15(a) and (b), for PBTI and NBTI stress tests of 15 and –16 V, respectively. The stress duration is 10 s and the monitored time was 100 s, using a sensing current I_{SD} of 50 mA.

During NBTI stresses, V_{SD} can be used as TSEP, thereby the self-heating during the stress phase can be verified using the calibration curve shown in Fig. 5. This is possible given that for both –10 V (calibration) and –16 V (stress) the calibration curve of V_{SD} as TSEP is the same as there is no channel conduction, as described in Section II. The gate stress voltage and V_{SD} (TSEP) during the NBTI stress are shown in Fig. 16. When the channel is fully closed, the temperature sensitivity of V_{SD} is –3.1 mV/°C, hence the measured ΔV_{SD} of –0.8 mV corresponds to a junction temperature increase ΔT_j during the stress equal to 0.26 °C.

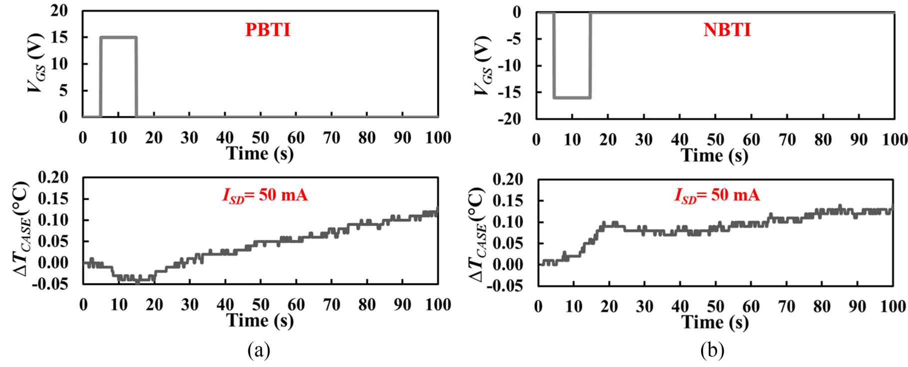


Fig. 15. (a) Evaluation of the self-heating during PBTI evaluation. $V_{GS,stress} = 15$ V, $V_{GS,rec} = 0$ V, stress duration 10 seconds, $I_{SD} = 50$ mA. (b) Evaluation of the self-heating during NBTI evaluation. $V_{GS,stress} = -16$ V, $V_{GS,rec} = 0$ V, stress duration 10 seconds, $I_{SD} = 50$ mA.

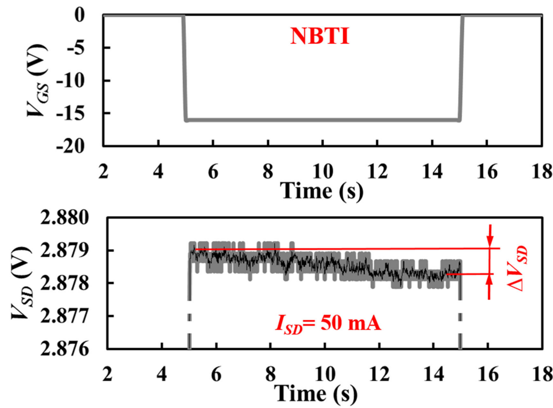


Fig. 16. V_{GS} and V_{SD} (TSEP) during NBTI stress.

The impact of the self-heating for this short evaluation pulse can be considered negligible but longer stress pulses could require further measures, like reducing the sensing current I_{SD} or an improved cooling system.

V. Conclusion

Threshold voltage shift from BTI is now a critical reliability concern in SiC power MOSFETs. The standard methods of assessing BTI in silicon MOSFETs are not applicable in SiC MOSFETs. The reduced oxide reliability in SiC and the need for negative gate biasing during turn-OFF means V_{TH} shift is more critical. Furthermore, the process of characterizing V_{TH} after the high voltage stress test may alter the extent of V_{TH} shift thereby underestimating its extent. This problem is critical in high power applications that use parallel power devices where unsynchronized switching due to non-uniform V_{TH} drift can cause catastrophic failure from current hugging. This paper has introduced a novel method of monitoring threshold shift from BTI using the body effect in SiC power MOSFETs. The body effect is particularly evident in SiC MOSFETs because of the high body diode forward voltage and low threshold voltage compared to silicon. Hence, the third quadrant voltage drop is sensitive to the gate voltage bias and by implication, the threshold voltage. By using a low sensing current through the body diode during the V_{GS} stress and relaxation phase, the third quadrant forward voltage can be used as an indicator for the threshold voltage shift, similar to how the forward voltage is used as a temperature indicator (TSEP). Using this method during qualification of power devices under HTGB will show the true behavior of the threshold voltage since it can assess V_{TH} shift and recovery in-situ without altering it. As V_{SD} is also affected by temperature, it is important to define measures to avoid the self-heating of the device during the tests, in order to consider the shift of V_{SD} caused only by BTI.

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