Miniature High-Power Nanosecond Laser Diode Transmitters Using the Simplest Possible Avalanche Drivers

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Abstract—The state-of-the-art long-distance near-infrared optical radars use laser-diode-based miniature pulsed transmitters producing optical pulses of 3–10 ns in duration and peak power typically below 40 W. The duration of the transmitted optical pulses becomes a bottleneck in the task of improving the radar ranging precision, particularly due to the progress made in developing single photon avalanche detectors. The speed of miniature high-current drivers is limited by the speed of the semiconductor switch, either a gallium nitride field-effect transistor, the most popular alternative nowadays, or a silicon avalanche bipolar junction transistor (ABJT), which was traditional in the past. Recent progress in the physical understanding of peculiar 3-D transients promises further enhancement in speed and efficiency of properly modified ABJTs, but that is not the only factor limiting the transmitter speed. We show here that a low-inductance miniature transmitter assembly containing only a specially developed capacitor, a more advanced transistor chip than that used in commercial ABJTs and a laser diode, has allowed peak power from 40 to 180 W to be reached in optical pulses of 1–2 ns in duration without after-pulsing relaxation oscillations. This finding is of interest for compact low-cost, long-distance decimeter-precision lidars, particularly for automotive applications.

Index Terms—High-speed switching, miniature assembly, nanosecond avalanche drivers, optical radars, peak power.

I. INTRODUCTION

THE-STATE-OF-THE-ART long-distance near-infrared optical radars use laser-diode-based miniature pulsed transmitters producing optical pulses of 3–10 ns in duration and peak power typically below 40 W. A number of recent commercial applications have stimulated a growing demand for generating current pulses of 1–2 ns in length [1] or shorter with an

amplitude of $\sim$10–10^2 A across a low-ohmic load. This concerns particularly the pumping of high-power broad-stripe laser diodes pulsed optical radars (lidars) and other systems [2], [3]. A large variety of commercial generators providing nanosecond and subnanosecond current pulses approaching and even exceeding 100 A are available (see http://www.fidtechnology.com/), but their large sizes and high prices make their use problematic. Much cheaper to use and more compact are avalanche transistor-based Marx circuits [4], which can provide reliable operation after simple modifications [5] in picosecond [6] switching at dozens amperes, or even at several hundred amperes [7] for ten nanoseconds or so. The transmitter in all these examples, however, cannot be considered either low-cost or miniature (i.e., comparable in price and size with an encapsulated laser diode), and these are the criteria of principal importance for most large market applications. The competing state-of-the-art solutions that satisfy these criteria are pulsed switches based on the latest developments in Gallium Nitride (GaN) field-effect transistors (FET) or properly optimized avalanche transistors. Despite very powerful competition from GaN FETs, especially at higher repetition rates ($>$100 kHz), Si avalanche transistors remain a strong competitor in our opinion, thanks to their high switching speed, low price, and simple miniature transmitter circuitry [8], [9]. The relatively large duration of the optical pulse (typically 3–10 ns) becomes a bottleneck in lidars aimed at the longest possible distance (ideally up to several kilometres) with high ranging precision (around a decimetre). Indeed, it has become very popular nowadays to use single photon avalanche detectors (SPADs) gated in a subnanosecond time interval in the receiving channels of lidars, as this allows one to take advantage of 1 ns transmitters and overcome problems of elevated noise in broadband ($>$300 MHz) amplifiers. Thus, the development of a laser diode transmitter emitting optical pulses around 1 ns in duration with as high a peak power as possible (at least several tens of W) is a timely and challenging task, with the main problem lying in high-current nanosecond drivers. In addition, it is worth noting that a reduction in optical pulse duration to well below 1 ns is also possible when the pumping current pulse of the laser diode becomes comparable with the lasing delay, and/or various *transient* gain-and Q-switching picosecond modes [10]–[14] can be realized (SPADs also permit sub-nanosecond, $\sim$200 ps, gating). Gain and Q-switching modes use special laser diodes and/or special pumping conditions, so that they require the deep understanding and unique experience of certain research groups; they

are interesting, but serial production quantities for each particular application has to be analysed separately. Even submicron precision for ∼700-m distance measurements using a femtosecond laser [15] has been demonstrated, but such records do not belong to the realm of simple, miniature, and cost-effective solutions. The practical task we address here can be specified as follows. The driver to be developed should be suitable for any laser diode chip operating in a quasi-steady-state mode, the optical pulse duration should be around 1 ns, and the peak power as high as possible (aiming at ∼100 W). Broad-stripe multijunction high-power pulsed laser diodes reach an efficiency of at least ∼2.3 W/A (see www.lasercomponents.com), which means that current pulses of several tens of amperes with pulse durations around 1 ns should be sufficient. It follows from the measurement results presented here that multijunction 900 nm diodes mentioned above retain 2.3 W/A efficiency at least up to 180 W for a pulse duration of 2 ns. If in other diodes (say, those emitting at around 1500 nm), the efficiency may tend to diminish at high currents, the driver parameters are not the only bottleneck to be considered in this particular instance.

In this work, we show that miniature assemblies fitting into the packages of commercial laser diodes and providing ∼1 ns/40 W or, alternatively, 2 ns/180 W can be manufactured using commercial laser diodes and bipolar junction transistor (BJT) Si transistors operating in avalanche mode. The main contribution to the parameters achieved is provided by proper development of the miniature single-layer capacitors, allowing a transmitter assembly with its total parasitic inductance loop reduced to ∼1 nH and the dielectric permitting effective release of the accumulated charge in a large-signal subnanosecond switching transient. The total inductance of ∼1 nH aimed at here is a really challenging task, since the typical inductance of a commercial encapsulated laser diode is 5 nH at a minimum, that of a commercial surface-mounted transistor is about 2 nH, and that of a ceramic NP0 50-V capacitor is about 1.5–2 nH, resulting in a total circuit loop inductance of at least 10 nH. Second in priority is smart selection of the avalanche transistor chip based on the recently achieved understanding of the three-dimensional (3-D) dynamics of avalanche BJTs (ABJTs). We show here that a properly developed capacitor permitting miniature ∼1 nH assembly and a correctly selected ABJT chip layout allows us to practically record parameters to be achieved for nanosecond miniature optical pulse transmitters.

II. DRIVING CIRCUIT AND ROLE OF EACH COMPONENT

For a given electrical switch, the simplest circuit (see discussion in [16]), as shown in Fig. 1, provides the maximum ratio of the current amplitude (I_m) to the current pulse duration (t_W), which is the quality criterion (I_m/t_W) in our task. Indeed, replacement of capacitor C_0 with any other energy accumulator (e.g., a transmission line aimed at rectangular pulse shaping) would reduce the current amplitude and increase the assembly size, while the presence of a parasitic inductance L_P is unavoidable in any circuit, as well as presence of some kind of load (with the lowest possible impedance). It is precisely this
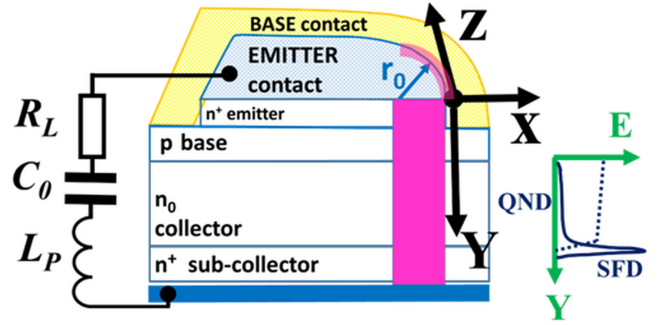

Fig. 1. Simplest possible current driver used in the miniature assembly in this work. The switch is a BJT operating in the "second breakdown" avalanche mode. The capacitor C0 accumulates energy between the pulses (charges) and discharges across the switch. The load is a laser diode or a resistor (RL used alternatively for current pulse measurement). LP is the entire parasitic inductance of the circuit loop. Application to the base of the current pulse exceeding ∼20 mA in amplitude and a dozen nanoseconds in duration is sufficient for avalanche transistor triggering. The unavoidable LP limits the current ramp and should obviously be as small as possible. The value $RL = 1$ Ω was selected for measuring the voltage pulse for its further recalculation in current waveform by an iteration procedure that accounts for the parasitic inductance of the resistor chip. A real-time 6-GHz digital oscilloscope with a passive 500-Ω probe was used for reducing the band limitation caused by the inductance of the 50-Ω probe. In the case of an optical transmitter, the load resistor is replaced with a laser diode chip only, which has an even lower inductance than the sub-mm surface-mounted load resistor. The fairly good fit between the optical and current waveforms achieved on account of the 2.3 W/A laser efficiency proved the acceptability of our approach as a solution to the nontrivial problem of nanosecond/sub-nanosecond current pulse measurement in a miniature (below 2 nH) low-ohmic transmitter assembly. Various elements on the transistor chip draft illustrate the 3-D transient peculiarities, which have been found in ABJTs within the last few years, and these will be used in Section III to interpret the results obtained here. The magenta channel shows the initial position of the switching region at the corner of the emitter finger with a curvature of radius r0. The size of this region changes with time. Y is the longitudinal coordinate in the current direction, X is the transverse coordinate perpendicular to the emitter–base (e–b) interface on the top plane of the transistor chip, and Z is the direction along this interface (Obviously this coordinate system alters for different points on the e–b interface so that the plane X–Y is always perpendicular to this curved line). The graph on the right-hand side represents the electric field profile in the direction Y before the switching (dot line), and in the switching channel at a sufficiently high current density. The abbreviations QND and IFD mark the positions of the characteristic regions discussed below in Section III.

low-inductance circuit loop that is used in our *transmitter* when replacing the load resistor R_L with the laser diode.

The goal of this paper is to find bottlenecks that prevent maximization of the quality criterion I_m/t_W and to suggest simple solutions. Such bottlenecks can be associated with the *circuit* or with the *switch*, and we use a simplified but illustrative way *of separating their contribution*. Fairly instructive are the simple formulas available for estimating the amplitude I_m and duration t_w (FWHM) of the current pulse that are valid for an "ideal" switch with an infinitely short switching time between the levels U_0 (initial C_0 biasing) and U_R (residual voltage across the switch by the end of the switching transient):

$$t_w = 2.2 \times \sqrt{L_P \times C_0} \qquad (1)$$

and

$$I_m = \frac{U_0 - U_R}{\sqrt{\frac{L_P}{C_0}} + R_L}. \qquad (2)$$

Given that $U_R = 0$ and $R_L = 0$ (the load resistor is replaced with a laser diode with zero impedance), we obtain the maximum of the "quality criterion" permitted by the ideal circuit

$$(I_m/t_w)_{\max} = \frac{U_0}{2.2 \times L_P}. \qquad (3)$$

This relation overestimates the ratio I_m/t_W, since at zero losses $(R_L = 0)$ relaxation oscillations in the current in *LC* will inevitably cause after-pulsing that can be suppressed only by losses equivalent to at least $R_L = (L_P/C_0)^{1/2}$, and therefore this R_L value has to be substituted in (2), thus reducing the quality criterion twice. Furthermore, including an additional resistor in the transmitter for dumping the oscillations will increase the parasitic inductance, which will reduce the I_m/t_W ratio still further.

As will be seen below, an extremely interesting option of *increasing the quality criterion toward its fundamental limit* can be provided in some cases by the very *fortunate ability of ABJT to dump the relaxation oscillations by means of a time-dependent transistor impedance after switching in the absence of resistor R_L.* If this case were realized, the *simplest assembly* with the minimum possible L_P would contain only the transistor chip, the capacitor, and a laser diode emitting a clean, single optical pulse.

As follows from the relations (1) and (2) for an ideal switch, an increase in the quality criterion I_m/t_w will require maximization of the biasing U_0 (with subtracted residual voltage U_R) and minimization of the inductance L_P. In reality, the biasing voltage U_0 is determined by a compromise between maximization of the value of I_m/t_w and the minimum switching time, which for an Si ABJT is smaller for a transistor with a thinner n_0 collector and thereby, unfortunately, a lower voltage U_0. The parasitic inductance L_P has to be reduced, and its fundamental limit is determined by the minimum possible size and an "assembly-friendly" shape of the semiconductor (or ceramics) components, permitting a compact 3-D construction (Note that the requirement of 3-D assembly inside a laser diode package with four pins, for example, does not contradict the technological and commercial requirements acceptable for mass production technology).

III. Results and Discussions

A. Effect of the Circuit and Transistor Switching Time on the Current Pulses Generated

Among the commercially available avalanche transistors FMMT 413, 415, and 417 (ZETEX Semiconductors Inc.), the maximal quality criterion (I_m/t_W) was found in FMMT-415, since it provided the best compromise between a sufficiently high collector-base breakdown voltage (maximal biasing $U_0 \sim 300\,\text{V}$) and a relatively short switching time in our amplitude/duration range (see data in Figs. 2 and 3, and related discussions).

The dependences of the current pulse amplitude on the pulse duration measured using commercially available components: NP0 ceramic capacitors and three types of ABJT produced by ZETEX Semiconductors, are presented in Fig. 3. Each of the
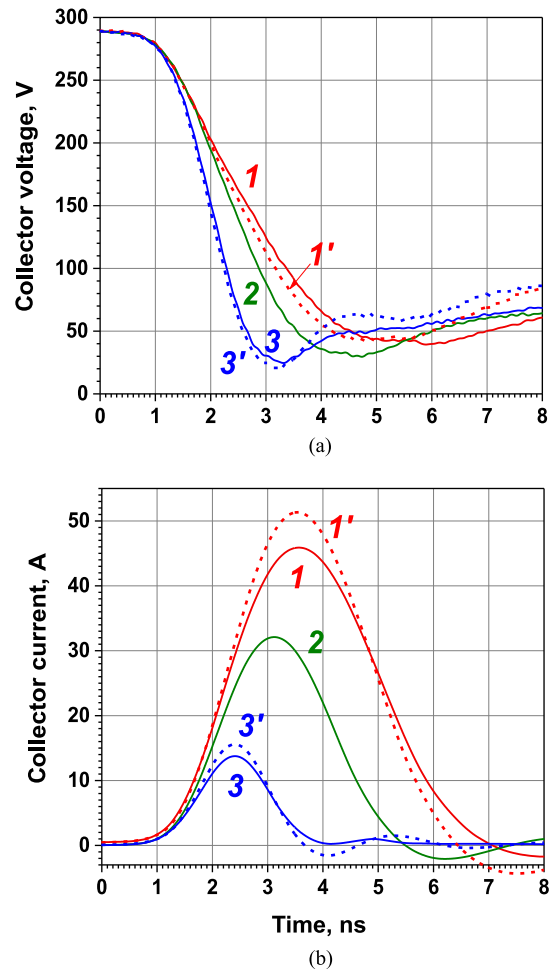

Fig. 2. Examples of voltage (a) and current (b) waveforms measured during the switching transient of the commercial avalanche transistor FMMT415/ZETEX Semiconductors (curves 1–3) in the circuit shown in Fig. 1 for different multilayer ceramic capacitors with NP0 dielectric type. The total inductance of the circuit of LP ~4 nH cannot be reduced further when an NP0 capacitor, a surface-mounted transistor, and a load resistor are used. The current pulses shown are computed from the measured voltage waveforms across the load by a numerical procedure [17], [18] accounting for a 0.8-nH parasitic inductance of the load resistor ($RL = 1\,\Omega$). In order to reduce the error caused by the voltage drop across the internal inductances, the voltage between the emitter and the collector was measured by probing the potential difference between the metal contacts to the semiconductor chip reached by polishing the plastic transistor package. The 500-Ω passive probe of the oscilloscope was connected between the emitter and the collector contacts (across a separating capacitor), bypassing the parasitic inductance of the surface-mounted transistor assembly, thus permitting correct measurement of the voltage across the emitter and the collector ohmic contacts. Polishing the plastic package of the surface-mounted transistor also allowed its contribution to the total loop inductance to be reduced to below 2 nH; the inductance associated with the laser diode chip was below 0.5 nH, and the main contribution to the total inductance was made by the geometry and size of the NP0 capacitor. The capacitor C0 values (pF) being 1–470, 2–270, and 3–82. Curves 1′ and 3′ show, for the sake of comparison, the current and voltage waveforms measured under the same conditions using a BJT of type FMMT 493. This transistor was selected as an analogue of the FMMT 415 with its semiconductor layers as closely similar as possible but with a different emitter-base finger layout, for the reasons discussed in Section III below. The particular FMMT 493 transistor chips used here were preselected using curve-tracer measurements of the base-collector breakdown voltage, aiming at ~300 V (as for the FMMT415), an emitter-base breakdown voltage of ~7 V, and a common emitter current gain β ~60–70. Assuming similar BJT technology from the same manufacturer, this should apparently mean similar doping and thickness of the n0-collector layer and the base region, which are (according to experimental and numerical studies) the most critical structural parameters affecting high-current ("second breakdown mode") avalanche switching [17]–[19].
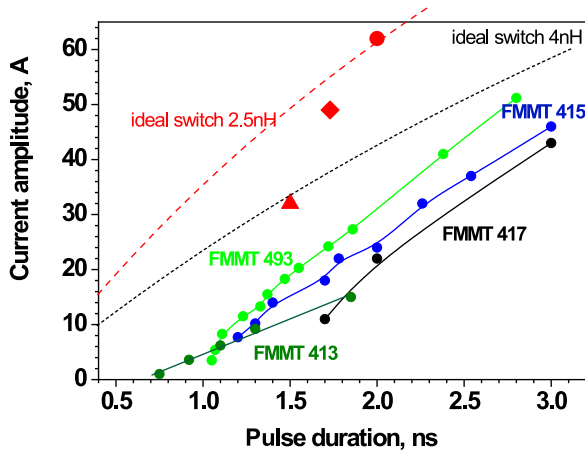
Fig. 3. Solid lines show the measured peak current against the pulse duration obtained for three types of commercial avalanche transistors in the circuit containing multilayer ceramic NP0 capacitors of different values, and the same total inductance LP ≈ 4 nH in all cases as in the measurement results shown in Fig. 2. Each capacitor value provides its own pulse duration. Somewhat better results were obtained for FMMT 493 BJT, which we selected as a certain analogue of FMMT415, aiming at a similar semiconductor structure (see captions to Fig. 2) but a different chip layout, according to the reasoning discussed in Section 3. The dashed black curve shows for comparison the expected results for an ideal switch obtained using formulas (1) and (2) at an assumed residual voltage UR = 60 V (determined mainly by the voltage across the high-field ionizing collector domain [17]–[19], see IFD in Fig. 1). The dashed red curve represents expectations at a lower inductance LP = 2.5 nH. The red dots denoted by special symbols were measured for FMMT 493 at LP ≈1.8 nH using specially developed capacitors C0 (see Section III.3): ball −470 pF, rhomb −300 pF, and triangle −165 pF. The differences between the measurements and expectations for an ideal switch are obviously larger with shorter pulses due to the limited switching speed of an ABJT.

experimental points connected by solid lines corresponds to a particular capacitor value, so that the larger the capacitor value is, the longer will be the pulse and the higher the amplitude.

Let us interpret main results presented in Figs. 2 and 3.

1) Pulse Amplitude I_m and Duration t_W Determined by the Circuit: The current amplitude for shorter pulses is always smaller, even for an ideal switch, due to growth in the characteristic *LC* circuit impedance $\rho = (L_P/C_0)^{1/2}$ (see formulas (1) and (2) and dashed lines in Fig. 3). However, the reduction in the measured current amplitude for shorter pulses is more significant than that determined by the circuit . We should trust the approach of infinitely fast switch as long as the current pulse duration t_W, defined by relation (1), is much longer than the switching time t_{sw} of the transistor. The approach can be still useful if those times are comparable: the switching can excite oscillation(s) in the *LCR* circuit, the pulse duration can anyway be evaluated using formula (1), but the pulse amplitude becomes lower than is predicted by formula (2) (see Fig. 3). Finally, noticeable oscillation(s) in an *LCR* circuit cannot be excited if $t_W \ll t_{sw}$ at all. Using "device" terminology, a fast avalanche switching mechanism (a few ns) will *not* occur at excessively low capacitor values. Indeed, fast switching requires a high current density (at least exceeding the critical value [17]–[19]) that provides ("second breakdown") as represented by quasi-neutral domain (QND) and ionizing field domain (IFD) in the E(Y) profile in Fig. 1. The charge accumulated in a small capacitor becomes insufficient for such field reconstruction. In this case,

only fairly slow avalanche switching (many tens of nanoseconds) may take place ($t_W \ll t_{sw}$) and nanosecond pulse generation fails. One can see from Fig. 3 that the shortest achievable pulses range between 0.7 and 1.5 ns depending on the transistor type, while generation of even shorter pulses is prevented by the small capacitor values.

2) Switching Time: The interpretation placed upon the present experimental results depends on *how we would define the switching time t_{sw} of a particular ABJT. There are two possible definitions*, and finding the correct relation between them is critically important for interpreting our experimental results. According to the first definition (let us call it the "circuit definition"), the switching time is a *characteristic time for the voltage reduction across the switch* (say, 90%–10% of U_0–U_R) that is directly measurable [see Fig. 2(a)], and determines the excitation efficiency of the current oscillation(s) in the *LRC* transmitter circuit. This definition is not sufficient, however, and *must be compared with the other one, which is typical of the device physics*. Following this "physical definition," we note that the voltage-blocking n_0 collector *becomes highly conductive within a certain time, thanks to the appearance of a large number of carriers in the earlier depleted layer*. We mean here by the *switching time* of the ABJT the characteristic timing of the carrier avalanche generation, affected by a number of complicated physical processes investigated experimentally and numerically in [17]–[23].

Further consideration is hardly possible without a brief listing of what we know from previous publications about the processes (some of which compete with each other) that determine the switching scenarios. Let us define X, Y, and Z coordinates as shown in Fig. 1 and explained in the figure captions.

1) A one-dimensional switching scenario [17]–[19] consists of a reconstruction of the Y-profile of the collector field, as shown schematically in Fig. 1. The initial biasing U_0 corresponding to complete depletion of the n_0-collector region [dotted line in graph E(Y)] changes during the *"circuit" switching time* to the residual voltage $U_{R,}$ determined mainly by the area of the narrow, powerfully IFD situated at the collector/subcollector interface. In the switched-ON state, the electric field is practically removed by the electron-hole (e–h) plasma from the major n_0-collector part, termed QND. This QND spreads from the p-base toward the subcollector during the switching transient, thanks to compensation of the negative charge of the electrons injected from the emitter by the positive charge of the holes *avalanche injected* from the IFD. The switching speed accelerates as the avalanche injection of holes from the IFD, which determines also the electron injection and the total current density, increases.

2) The IFD and QND regions are formed within the area $\Delta X \times \Delta Z$, where the time-dependent quantity ΔX (t) denotes the size of the conducting channel along the X coordinate and ΔZ (t) denotes that along the Z coordinate. Our vision of the processes investigated in [20]–[23] is as follows. The size of the initial switching area $\Delta X_0 \times \Delta Z_0$ is determined by the current spread in a transverse direction ($\Delta X_0 \sim 15$–$20\,\mu m$) in the base and by the curvature

of the emitter figure corner ($\Delta Z_0 \sim r_0$). However, both ΔX and ΔZ will have shrunk then to ~ 5 μm, during the subnanosecond switching interval, at which point the competing process of turn-on spread will have started.

3) ΔX may return to ~ 15–25 μm only, while the spreading in the longitudinal direction depends critically on the current pulse duration, and may reach a velocity of ~ 50 μm/ns, increasing at a large capacitor the size of ΔY to ~ 200 μm (around the single finger corner).

4) Let us use those approximate values to obtain instructive estimates. Previous research has shown that the current density j during avalanche switching typically ranges between 100 kA/cm^2 and 1 MA/cm^2, and the fastest switching (fastest spreading of the QND region in the Y-direction, with a velocity of ~ 10 μm/ns) corresponds to the highest j (~ 1 MA/cm^2). This means that the fastest carrier generation for the narrowest switching channel ($\Delta X \times \Delta Z \sim 25$ μm^2) can already be realized at a current as low as 25 μm^2 $\times$ 1 MA/cm^2 ~ 0.25 A, which is sufficient for the fastest possible "physical switching" [compare this miserable current value with the currents at the beginning of the transient in Fig. 2(b)]. After the ~ 2 ns of the switching transient, the turn-on spreading increases the switching area drastically, and the same rate of carrier generation (the same j) would require a collector current as high as several tens of amperes. Last but not least, we have to take account of the fact that we are most probably dealing with the simultaneous switching of several channels [20] at the emitter finger corners, and one apparently has to divide the current values in Fig. 2(b) by a factor of 5 or 10 when comparing them with the estimates suggested here.

The nontrivial conclusion follows from this consideration. Namely, with the longest (high amplitude) pulses *the peak current density* (and thus the highest switching speed) will *not* reach as high values as for short pulses.

To summarize, given a smaller capacitor (and accordingly a smaller and shorter current pulse) shrinking of the switching channel will cause high current densities, while the competing turn-on spread mechanism is interrupted by the limited capacitance. Accordingly, faster "physical" switching (a higher j and more powerful ionization due to the growth in the IFD amplitude) will take place. This will be accompanied by fast "circuit" switching, because the slight increase in the IFD amplitude causes its fast shrinking, thus reducing the collector voltage [see Fig. 2(a)]. By contrast, at a larger capacitor, the turn-on spread will limit the peak current density (despite the larger current!) and accordingly the ionization rate will be lower and the switching time larger.

All in all, a "physical" definition of the switching time on account of peculiarities in the 3-D transient allows an interpretation to be given for faster switching with smaller capacitors (and accordingly lower currents). Both "physical" and measurable [see Fig. 2(a)] "circuit" switching times show the same tendencies, due to properties of the IFD, i.e., domain shrinkage (a lower voltage) is accompanied by an increased ionization rate,

and thus faster conductivity modulation causes faster collector voltage reduction.

It is worth noting that various special features of 3-D avalanche switching have been investigated [20]–[23] using quasi 3-D physics-based numerical modeling and experimentation. The general conclusions are certain, but quantitative numerical study of a particular circuit, transistor structure, and layout would consume much effort in each particular case. The point is that rigorous 3-D transient modeling is impossible nowadays, while "smart approaches" utilizing a 2-D simulator face various difficulties, and are an art rather than a universal engineering tool.

3) Minimal and Maximal Switching Times for a Particular Transistor: One can see from Fig. 2(a) that the switching time is not a fixed value intrinsic to a particular transistor and biasing voltage, but it depends also on the capacitor value, which is not surprising in view of the switching peculiarities discussed above. The shortest switching time, ~ 1.2 ns, is observed for FMMT 493 with small capacitors [curve 3′ in Fig. 2(a)], while with a larger capacitance the switching requires a longer time, ~ 2.7 ns [curve 1′ in Fig. 2(a)], the time which it takes for complete formation and spreading of the QND in a much broader switching channel, and accordingly with reduced current densities (and impact ionization rates). With even larger capacitors, further channel broadening (turn-on spread [22]) mostly ceases and the switching time practically stops growing. This marks the *upper limit of the switching time*. In the opposite case of minimal size of the region of initial switching, any further reduction in the capacitor value cannot reduce this region any further but quits switching instead due to the insufficiency of the charge for the collector field reconstruction (see E(Y) in Fig. 1). Then, the switching quenches completely instead of undergoing any further reduction in the switching time below ~ 1.2 ns, which thus marks the *lower limit of the switching time*.

For each transistor, a certain range exists in which the switching time varies from a minimum of 1.2 ns to a maximum of 2.7 ns (for FMMT 493). For the generation of current pulses with a duration well above the maximum switching time, the transistor should provide the same current amplitude as an infinitely fast (ideal) switch, while the generation of pulses significantly shorter than the minimal switching time is rendered impossible. The minimal/maximal switching times measured for the transistors FMMT 413 and 417 are $\sim 0.7/1.6$ ns and $\sim 1.6/3.4$ ns, respectively, while for FMMT 415 the values are slightly larger ($\sim 1.3/2.9$ ns) than for FMMT 493, implying a small but still noticeable difference in the demand for 1–1.5 ns current pulse generation.

Let us compare the predictions of formula (1) with the measured pulse durations and switching times for curves 1–3 in Fig. 2(a) and (b). In all three cases (capacitors 470, 270, and 82 pF), the estimated and measured pulse durations are the same (3.0, 2.3, and 1.35 ns), and comparable with the switching times for FMMT 415 (2.9, 2.0, and 1.3 ns). We would conclude that using relation (1) measured and estimated pulse duration fit fairly well with each other, while current pulse amplitude found from relation (2) for an ideal switch overestimates measured

peak current significantly since the condition of a much shorter switching time relative to the pulse duration fails to materialize: compare the experimental curves with the estimate for the ideal switch for 4 nH inductance in Fig. 3.

Each transistor has its own shortest pulse duration, and as one can see from Fig. 3, the cut-off value is smaller for a low-voltage transistor. This is no surprise, since the switching time that is determined by the QNR spreading across the n_0-collector is smaller in a structure with a thinner collector, while the QNR spread velocity along the Y coordinate is about the same at the same current density. The smallest value for the capacitance C_0 below which the current amplitude diminishes can be evaluated using the minimum switching time and formula (1).

B. Physical Motivations for Selecting BJT Type FMMT 493

The conclusion mentioned above that follows from [17]–[23] is that the highest current density (up to $\sim 10^6$ A/cm^2) provides the most favourable switching scenario with the minimum switching time. This means that any measure that allows reduction of the switching area for the same structure and the same collector current should improve the transient characteristics as long as the level of heat generation is not harmful. Lateral (Z-direction) transient shrinkage of the switched-ON area followed by turn-ON spread will occur inherently in the device, and the only parameter that apparently may be controlled technologically is the lateral size (ΔZ_0) of the initial switching region. This size, according to [20], is determined by the curvature radius r_0 of the emitter finger corner. The reason lies in the experimentally proven crowding of the current of electrons injected at the corner of the emitted figure, which causes initial avalanche switching near its location. It is our opinion that the layout of commercial avalanche transistors FMMT 413, 415, 417 has not been properly optimized for nanosecond pulses, as they utilize fairly large radius $r_0 \sim 60 \, \mu m$. An attempt undertaken here is to improve the transient behavior of an FMMT 415 BJT by reducing its r_0 value. Since we had no access to the manufacturing technology, we decided to select a structure that was apparently analogous to that of the FMMT 415 but with a different chip layout, providing a significantly smaller r_0 value. Relatively minor but still noticeable switching enhancement with respect to FMMT 415 was achieved here using preselected FMMT 493 transistor chips (see selection criteria in the caption to Fig. 2). The chip selection was aiming at using a BJT structure similar to that of FMMT 415, while the enhancement can be ascribed to two features of the chip layout of the FMMT 493 transistor.

The most important difference, in our opinion, concerns in the multiple ($\sim$10) emitter fingers with "sharp corners" (curvature radius $\sim$5 μm), unlike the single finger in FMMT 415 with four corners having a fairly large curvature radius of $\sim$60 μm (see details for BJT FMMT 417 in [23], as this has the same chip layout as the FMMT 415).

Another difference concerns the device area in FMMT 493, which is larger by a factor of $\sim$5, which may in principle also accelerate the switching transient. The point is that the collector-base capacitance discharges inside the transistor structure across the avalanching channel. This process is not affected by an

external inductance and the ionization in the IFD may be increased. This effect has been proved in *GaAs* ABJTs [24], [25] with a different avalanche switching mechanism, but a similar effect can be expected in Si ABJTs as well. This second scenario requires numerical and experimental verification for *Si* ABJT, however, and *a priori*, we trust the dominating effect of the emitter fingers with sharp corners more when interpret better switching efficiency of FMMT 493 with respect to that of FMMT 415.

To summarize, the shortest current pulses were measured for FMMT 413, the transistor with the thinnest collector, but its biasing voltage was so small that relation (2) did not allow an increase in the current amplitude above $\sim$10 A. Highest in breakdown voltage FMMT417 loses out to FMMT415 due to slower switching, while highest in amplitude 1.5–2 ns current pulses were achieved using BJT FMMT493. We assume that both FMMT493 and FMMT 415 have similar structure optimal for our application, but the first one has more advanced chip layout containing sharp corners of the emitter fingers. A convincing quantitative interpretation would require further complex experimental and quasi-3-D numerical studies.

C. The Problem of a Miniature Low Inductance Transmitter Assembly Using Commercial Capacitors

More impressive than the advantage brought about by proper transistor selection (FMMT 493 instead of 415) is the improvement predicted by relation (2) for a halving of the inductance ($L_P = 2.5$ nH), which is challenging but realistic provided an assembly of minimal size were to be designed using a sub-mm (sub-nH)-sized transistor and sub-nH laser diode chips combined with a single-layer capacitor of size $\sim$1 mm with a geometry appropriate for miniature 3-D construction. The dashed red curve in Fig. 3 presents this estimate for an infinitely fast switch with $U_0 \sim 300$ V and $U_R \sim 60$ V (values characteristic of FMMT 493), while the three experimental points highlighted in red that are somewhat related to those calculations show the actual current amplitudes measured using the most successful assembly discussed below.

The multilayer NP0 ceramic capacitors used earlier in this work, which can withstand more than 300 V and demonstrate satisfactory behavior in the nanosecond range were of length 1.6 mm and their geometry did not allow us to obtain noticeably less loop inductance in the transmitter than the 4 nH achieved using a miniature laser diode and transistor chips. At first glance, the problem can be solved using a commercial COMPEX single layer CSM capacitor (http://www.compexcorp.com/csm-series) that is square in shape and slightly exceeds 1 mm in size. We have made, indeed, the improved assembly with a total inductance of about 2–3 nH by using the FMMT 493 transistor, CSM capacitor, and 1 Ω/0.8 nH load resistor (for current measurement), but the results shown in Fig. 4 were discouraging. The capacitors used not only enlarged the pulse duration with respect to that estimated using formula (1) and showed significant pulse spreading near the bottom (see Fig. 4), but even showed smaller amplitude than was achieved for NP0 despite the larger inductance (of around 4 nH) in the latter case. This definitely
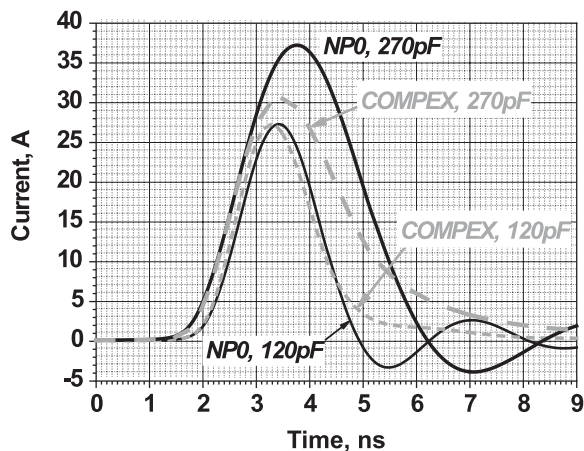
Fig. 4. Current pulses measured in a low-inductance assembly using an FMMT 493 transistor with two NP0 capacitors and two COMPEX CSM capacitors with the same values: dielectrics C-90 (120 pF) and C-100 (270 pF); capacitor size 1.27×1.27 mm in both cases.

proves that the COMPEX CSM capacitors used by us have *internal losses in large signal mode in the nanosecond range and cannot be recommended for this application*.

We have to conclude that the bottleneck now consists of the lack (to the best of our knowledge) of any suitable commercial capacitors, and further efforts have to be concentrated on this problem.

D. Specially Developed Capacitor: An Si3N4 Dielectric Deposited on a Highly Conductive Si Substrate by a Plasma-Chemical Method (PECVD)

The properties of the silicon nitride layer used as the dielectric in the capacitors developed here depend on a number of technical parameters involved in the deposition process. A special investigation into the effect of the processing regimes (substrate temperature, composition, and rate of entry of the reagents into the chamber) on the electro-physical parameters of dielectric films (breakdown voltage, specific capacitance, and high-frequency losses) was undertaken [26], and main outlines of the development are as follows. One technically controllable parameter is the configuration of hydrogen bonds in a silicon nitride molecule, which determines the refractive index of the material and is related in a complex manner to the breakdown voltage, specific capacitance, and dielectric loss tangent (see Fig. 5). It follows from the measured dependences that the refractive index of 1.85 corresponds to an optimal dielectric for a capacitor with minimal dielectric losses, maximum breakdown voltage, and a still acceptable specific capacitance value. Indeed, when as large a value of C_0 as $\sim$400 pF was required for generating $\sim$1.5–2 ns optical pulses at a maximum biasing voltage of 300 V (0.4 μm dielectric thickness selected), the size of the capacitor determined by its area of 4 mm^2 still allowed us to perform the assembly with a total inductance loop as low as $\sim$1–2 nH. This eventually resulted in optical pulses approaching $\sim$150–180 W. For shorter pulses ($\sim$1 ns), the performing of a $\sim$1 nH assembly with an appropriate capacitor (200 pF)
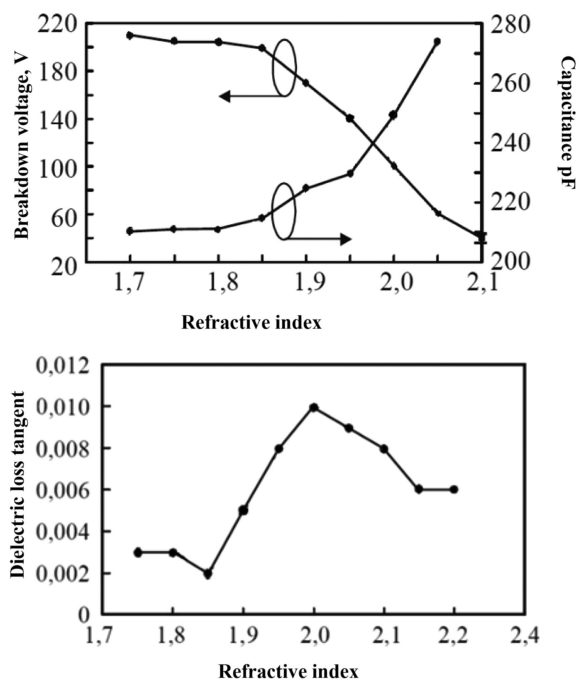

Fig. 5. Dependences of (top) breakdown voltage and capacitance for a film of thickness 0.2 μm and area 1 mm^2, and (bottom) dielectric losses tangent on the refractive index in an Si_3N_4 dielectric.

for achieving 1 ns/40 W optical pulses becomes a relatively routine task.

E. High-Power Nanosecond Transmitters: The Result of New Capacitor Development and Miniature Assembly

The most instructive comparison of all three capacitor types, shown in Fig. 6, answers the question: which type of capacitor provides the highest possible current pulse with duration of 2 ns using the optimal transistor chip for our task, FMMT 493, and the lowest inductance (as achieved by us), which is mainly determined by the geometry of each capacitor. The result for the COMPEX capacitor presented by curve 1 in Fig. 6, shows such a small amplitude and so unexpectedly large pulse duration (also extended near the bottom) that this circuit is of no practical interest. We would attribute this behavior to a slow change in the dielectric polarization or slow recharging of the interface states at the metal-dielectric interface.

Both NP0 and the specially developed capacitors provided pulse durations similar to those predicted by relation (1) on account of the inductance values (see figure caption) estimated for them from the assembly geometries. A comparison of curves 2 and 3 provides the expected tendencies for an effect of a 1.4 times *capacitor increase at the same inductance*: factor $\sim$(1.4)$^{1/2}$ increase in the pulse duration, a slight increase in the amplitude and a certain reduction in the relaxation oscillations. Comparison of the *same capacitor values for curves 3 and 4 but with the a difference in the inductance* by a factor of $\sim$1.5 provides the expected $\sim$(1.5)$^{1/2}$ difference in pulse duration and obvious tendencies with respect to relaxation oscillations.
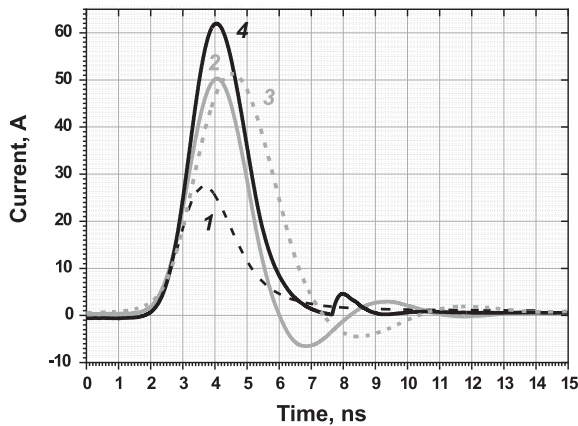
Fig. 6. Current pulses computed from voltage waveforms measured across a 1 Ω/0.8 nH load resistor using an FMMT 493 transistor chip and various capacitors. Curve 1 - COMPEX CSM 270pF (C-100, 1.27 mm ×1.27 mm) and total parasitic inductance of the circuit $L_p \approx 1.8$ nH. Curve 2 - NP0 capacitor 330 pF and total parasitic inductance $L_p \approx 2.8$ nH (thanks to the transistor chip used). Curve 3 - NP0 capacitor 470 pF and about the same parasitic inductance as in curve 2. Curve 4 - specially developed single layer Si_3N_4 470pF and inductance $L_p \approx 1.8$ nH. The inductance values were the minimum possible permitted for each assembly by the corresponding capacitor geometry, while the capacitor values for curves 1, 2 and 4 were empirically selected in order to obtain the same current pulse duration (FWHM) of 2 ns in all cases. Curve 3 is shown for comparison with curve 2 (the same capacitor type and of a different value and roughly the same inductance), and curve 4 (the same capacitance and different inductance).

The clear advantage of newly developed capacitor lies not only in the increased quality criterion I_m/t_W due to smaller inductance values (which would be even smaller if the 1 Ω/0.8 nH resistor in the transmitter were replaced with a laser diode), but equally important is the fact that in the circuit using new capacitor, the relaxation oscillations are absent unlike the situation in that utilizing NP0.

Let us make simple estimates in order to understand the role of the impedance of a switched-ON transistor. Suppression of the relaxation oscillations requires the presence in the switching loop of an active resistance R (or equivalent dissipative losses) equal to or larger than the characteristic impedance $\rho = (L_P/C_0)^{1/2}$ of the LC circuit. For simplicity, let us ascribe to the switched-ON transistor unchanged with time internal resistance R_i. For the new capacitor (curve 4 in Fig. 6) $\rho = 2 \Omega$, $R_L = 1 \Omega$ and thus the minimum value required for the transistor impedance to suppress the oscillations is $R_i = \rho$ and $R_L \approx 1 \Omega$. For NP0 capacitors (curves 2 and 3), ρ ranges from 2.9 to 2.6 Ω, and assuming the same internal resistance $Ri \approx 1 \Omega$, we obtain a noncompensated value of $\rho - R_L - R_i = 0.6 - 0.9 \Omega$, which indeed corresponds to the presence of oscillations in the experiment. The same estimates made using the data of Figs. 2 and 4 arrive at the same conclusions: the assumption of internal resistance R_i in the switched-ON transistor of 1 Ω leaves noncompensated LC impedance in the circuit loop and causes relaxation oscillations, and only a reduction in the inductance to 1.8 nH (curve 4 in Fig. 6) together with $R_L = 1 \Omega$ will suppresses the relaxation oscillations.

Fig. 7 illustrates an attempt at achieving a 2 ns optical pulse with peak power exceeding 100 W (see curve 1 in Fig. 7) using
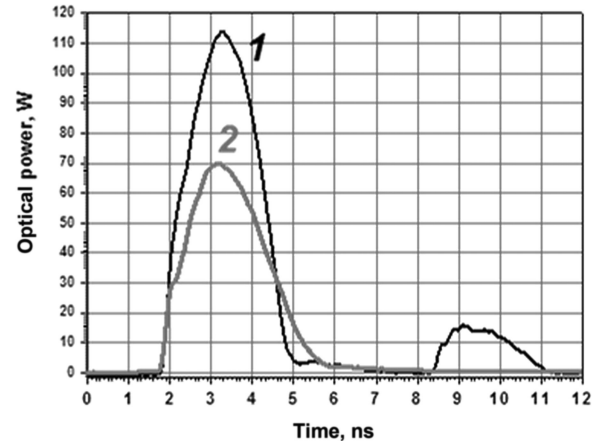

Fig. 7. Optical responses for the circuit using an FMMT 493 transistor, the NP0 capacitor 330pF, and a laser diode; parasitic inductance Lp ≈ 2.8 nH. Curve 1 presents a 114 W/2.1 ns optical response with the unfortunate presence of a second pulse caused by the relaxation oscillation of the pumping current. The oscillation is dumped (curve 2) using an additional 2-Ω serial resistor, which suppressed the second optical pulse at the expense of a reduction in the peak power to 70 W.

an assembly as compact as possible, including a commercial NP0 capacitor, a transistor, and laser diode chips. The problem here lies in the relaxation oscillation, suppression of which was in that case achieved only by using a serial 2-Ω resistor at the expense of a power reduction to 70 W together with increased assembly complexity and size. The impedance balance was as follows: in the assembly without a 2-Ω resistor (2.8 nH, 0.33 nF), the noncompensated impedance $\rho - R_i = 2.9 - 1 = 1.9 \Omega$ caused oscillations, while in the assembly that included a 2-Ω resistor (3.4 nH, 0.33 nF), the characteristic impedance was practically compensated for $\rho - R_i - R_L = 3.2 - 1 - 2 = 0.2 \Omega$, and no oscillations, at least in the optical response, were recorded (see curve 2 in Fig. 7). One can conclude that no attractive solutions were found in this work using any of the commercial capacitors.

The best results shown in Fig. 8 were achieved in this work using specially developed capacitors, FMMT493 transistor chips, and miniature assembly, the total inductance of which was estimated to be below 2 nH.

1) Suppression of Relaxation Oscillations: Importance and Special Features: The newly developed capacitors allow overcoming (or softening) of the after-pulsing problem, since the same pulse duration combines lower inductance and larger capacitance, resulting in a reduced characteristic impedance ρ. If the internal resistance R_i (losses) in the switched-ON transistor compensates for this impedance completely, this will create a very favourable synergy effect: the simplest possible assembly will contains only three essential components (a laser, a capacitor, and a transistor), with the absence of any specially added dumping resistance (and any additional inductance associated with it) minimizing the characteristic impedance ρ still further and simultaneously maximizing the ratio I_m/t_W.

By a first glance, the experimentally observed relaxation oscillations (see data in Figs. 2, 4, 6, and 7 and estimates given above in this section) can be interpreted using the assumption
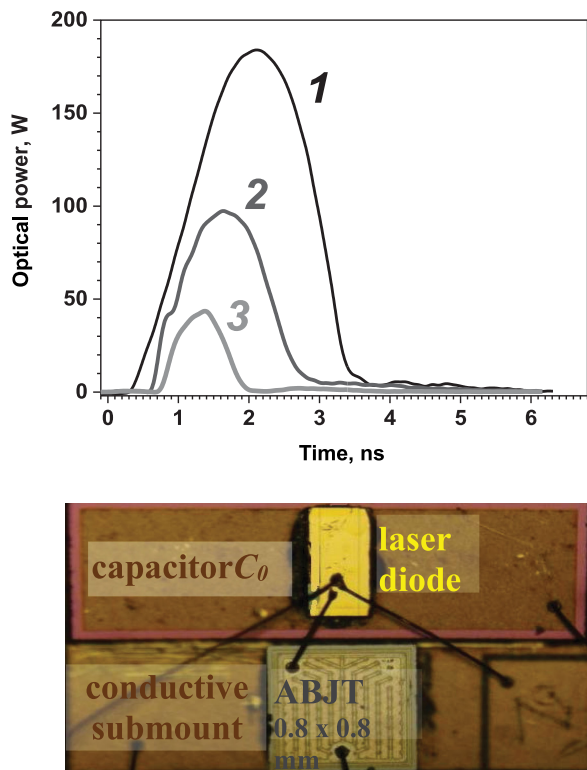
Fig. 8. Measured optical pulses (184 W/1.92 ns; 98 W/1.35 ns; 43 W/0.78 ns) from three miniature transmitters using the transistor FMMT 493 biased to 290 V, a laser diode and three specially developed capacitors of different values C_0: 1–470 pF, 2–165 pF, and 3–70 pF. The photo shows the assembly used in one of the transmitters: the cathode of the laser diode is placed on top of the capacitor, while the transistor collector and the other capacitor plate are mounted on a conductive heatsink. The total loop inductance is mostly determined by a bonding wire ($\sim$0.5 nH) of length $\sim$0.5 mm connecting the top (anode) of the laser diode chip with the transistor emitter, while the other contribution to the inductance is provided by a broad lateral current spreading along the transistor collector, capacitor electrodes, and conductive submount. The geometry of the current spreading is fairly complicated, which makes it difficult to estimate the inductance from the geometry of the assembly. A guess concerning the total inductance following from formula (1) gives 1.5–2.2 nH (Unfortunately we cannot provide completely reliable proof of the inductance values. The limited switching speed of the transistor might increase the pulse duration with respect to the "ideal switch" estimate, and the shape and duration of the current pulse may also differ from those of the optical pulse because of the possible effect of lasing delay). On account of a number of other experimental estimates using similar assemblies but faster switches we would more inclined to trust the inductance values in the range 0.8–1.5 nH, depending on the capacitor value (and thereby its size).

of a time-independent internal resistance in the switched-ON transistor $Ri \approx 1\,\Omega$. The situation is not that simple, however. Indeed, even assuming an inductance as low as 1 nH for curves 1, 2, and 3 in Fig. 8, we obtain $\rho \approx 1.5$, 2.5 and 3.8 Ω, respectively, which cannot be compensated for by $Ri \approx 1\,\Omega$ and seems to contradict the experimental data shown in Fig. 8.

Is it possible for Ri to reach a value as high as $\sim$4 Ω? The only ohmic region in the switched-ON transistor structure is the QND region (see E(Y) profile in Fig. 1). We know from the modeling reported in [17]–[23] that for high-currents ($\sim$10–100–A), the e–h concentration in the QND can be in the range $\sim$(3–8) $\times$ 10^{17} cm^{-3}, while the typical switching area with 1–2 ns pulses is in the range (100–200) μm $\times$ 10 μm $\sim$ (1–2)$\times 10^{-5}$ cm^2. Then, on account of the electron mobility $\sim$1500 cm^2/V$\times$s and thick-

ness of an n_0 collector $\sim$10 μm (comparable to the QND length), we obtain a resistance for the QND in the range $Ri \sim 0.2$ –1.4 Ω (here smallest values are more probable). We see that the value $Ri \approx 1\,\Omega$ assumed earlier for interpreting the observed oscillations is fairly realistic but still a little high, while the damped oscillations in the curves shown in Fig. 8 cannot be ascribed to the QND at all. Interpretation would most probably requires detailed study of the dynamics of IFD decay and its interaction with the current relaxation (apparently on account of 3-D effects), which has not been investigated so far. On view of the data in Fig. 8, the losses, which we ascribe to IFD decay, should be equivalent to at least 4 Ω and manifest themselves within the current relaxation time interval. Fortunately, the switching-ON process is free of those losses, and thus I_m/t_W ratio can be maximized in ABJT-based driver without induced relaxation oscillations. Found peculiarity of ABJT transient manifests itself only at extremely low ($<$2nH) parasitic inductances, which is apparently the reason why it was not found earlier.

New phenomenon is of considerable practical importance, but has not been interpreted so far and undoubtedly requires further experimental and numerical investigations from the viewpoint of ABJT physics.

The repetition rate of the pulses shown in Fig. 8 was 1 kHz. The questions of the maximum possible repetition rate, emitter reliability, and durability will require further technical and experimental investigations. We merely point out here that the average heat of the transmitter is very low, and the maximum repetition rate is limited by the thermal diffusion time from the hottest zone of the transistor to the heat sink. The same factor should affect reliability, which requires further study as well. The selection of a faster (lower voltage) transistor for operating with 1 ns pulses would be preferable for lower power consumption and a higher repetition rate, although at the expense of limitation of the peak power to $\sim$100 W.

IV. CONCLUSION

We demonstrated here the possibility of realizing very simple, miniature, and potentially low cost assemblies fitting into standard laser diode packages and able to generate pulses from 0.8 ns/43 W (about 20 A peak current) to 1.9 ns/180 W (about 80 A). These assemblies use commercial multijunction laser diodes with an efficiency of around 2.3 W/A. Main contribution is the unique Si ABJT driver originated from the high-current, subnanosecond properties of single-layer capacitors specially developed for the present purpose, which permits miniature assemblies with low parasitic inductance (1–2 nH), and a properly selected transistor chip.

Fairly powerful is the competition from 20 A/2 ns [27] and from the especially impressive subnanosecond 25–30 A [28] GaN FET-based drivers. They definitely surpass Si avalanche drivers in having a higher repetition rate, but should lose out in the simplicity of assembly (including the realization of low inductance), miniaturization, the expected price of a transmitter, and the compactness of the electronics driving the transmitter (a Si ABJT can be triggered by a pulse of only $\sim$20 mA, while the requirements for controlling a GaN driver are very strict). It

is worth noting that Si avalanche transistors have a good chance of operating up to 100–200 kHz, although this would require additional technical and research efforts.

All in all, very detailed comparison is required for really smart selection of the right transmitter for each particular application, despite the common opinion nowadays that GaN FETs have completely replaced Si ABJTs in long-distance nanosecond Li-DARs based on pulsed high-power laser diodes.

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