An Adaptable Interface Circuit With Multistage Energy Extraction for Low-Power Piezoelectric Energy Harvesting MEMS

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***Abstract*—This paper presents a self-powered interface circuit to extract energy from ambient vibrations for powering up microelectronic devices. The circuit interfaces a piezoelectric energy harvesting micro electro-mechanical systems (MEMS) device to scavenge acoustic energy. Synchronous electric charge extraction (SECE) technique is deployed through the implementation of a novel multistage energy extraction (MSEE) circuit in 180 nm HV CMOS technology to harvest and store energy. The circuit is optimized to operate with minimum power losses when input power is limited, and adapts well to operating conditions with higher input power. The highly accurate peak detector was validated for a wide piezoelectric frequency range from 20 Hz to 4 kHz. A charging efficiency of about 84% has been achieved for 4.75 V open-circuit piezoelectric voltage excited at 390 Hz input vibration under nominal input power range of 30–80 μW. Power optimizations enable the circuit to maintain a conversion efficiency of 47% at input power level as low as 3.12 μW. MSEE provides up to 15% efficiency improvement compared to traditional SECE, and maintains power efficiency as high as possible for a wide input power range.**

***Index Terms*—Interface circuit (IC), multistage energy extraction (MSEE), piezoelectric energy harvester (PEH), power efficiency, self powered, vibration.**

I. Introduction

PIEZOELECTRIC energy harvesters (PEH) have recently attracted interest as a solution for self-powered microelectronic devices, such as implantable microdevices and wireless sensor networks. Piezoelectric transducers provide higher power density than the electrostatic harvesters, and provide ease of integration, planarity, and higher output voltage in comparison with electromagnetic counterparts [1]. PEHs can supply power from μW to mW using ambient vibrations. Besides, there has been tremendous development in microfabrication processes [2], [3] and power density of micro electro-mechanical systems (MEMS) transducers [4]. The MEMS harvesters gain importance in volume- and weight-constrained applications such as bioimplantable devices [5]–[7] where battery replacement is impractical and costly. For example, an MEMS piezoelectric harvester has been utilized to generate rms output power range up to 160 μW under different vibration levels [8].

PEHs supply ac power with significant output impedance; consequently, an interface circuit (IC) is required to efficiently extract and convert piezoelectric ac voltage to usable dc voltage. Two conventional rectifiers, full-bridge rectifier and voltage doubler are the most common ac–dc converters, which have been demonstrated in several works [9], [10]. Passive and active rectifiers [11], [12] suffer from low extraction efficiency due to significant power losses during intermittent vibrations. The main reason for the low efficiency is that the rectifier has to charge and discharge the piezoelectric capacitor (C_p) of the piezoelectric harvester each cycle, which dissipates considerable power. A maximum power point sensing circuit [13] is utilized to match load impedance of the full-bridge rectifier to the real part of the source impedance, which improves power efficiency. The piezoelectric open-circuit voltage $(V_{\rm OC})$ sensing method is implemented to fix output voltage of the full bridge at half of $V_{\rm OC}$. The circuit nevertheless wastes most of the generated charge at the piezoelectric capacitance. Furthermore, this method is only effective for periodic vibrations.

Beside standard rectification, switching approaches based on nonlinear processing of the voltage across PEH are used to enhance the extracted power, including synchronized switching [13], [14], single supply prebiasing [15], and synchronous electric charge extraction (SECE) [16], [17] techniques. Synchronized switch harvesting on inductor (SSHI) [18], [19] benefits from charge inversion on C_p through recycling inductor. In this way, opposite charge generation is initiated close to conduction threshold of the rectifier. In this method, the power improvement strongly depends on the output load. Prebiasing and energy recycling methods boost extracted power through investing portion of the stored energy into the piezoelectric capacitor to step-up

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electrostatic force of the piezoelectric actuator. Optimization of invested energy requires high battery voltage and cumbersome adjustments.

Operation principle, power gain, and efficiency analysis of switching techniques are detailed in [20]. It is shown that the harvested power can be increased up to 400% through the SECE [21] scheme, wherein the generated charge at peak displacement is transferred to the output buffer through *LC* resonant circuits. SECE is an efficient approach among switching techniques for facilitating charge delivery and achieving load matching at the same time. The main challenge in this approach is extracting maximum power for a wide input power and frequency range. Energy extraction and transfer in several successive charge packages enables reduction in the size of off-chip electromagnetic components and increased power efficiency [22]. The SECE circuit implemented in [22] is efficient only for mechanical frequency range below 100 Hz, and depends on digital inputs for establishing critical time constants associated with piezoelectric and output storage capacitances, to regulate extraction and transfer durations. High input voltage and low input frequency operation necessitates a large harvester, which is impractical for deployment in implantable microdevices.

The aim of this work is to realize an autonomous harvesting circuit that is compatible with MEMS energy harvesters used to power-up biomedical devices. This paper presents a power-optimized SECE IC that improves the minimum required input power and frequency range of MEMS PEHs with low voltage output. In particular, an original multistage energy extraction technique has been implemented through a unique energy-based multistage generator circuit in an integrated SECE converter system to simultaneously achieve low cost and high power conversion efficiency. IC introduced briefly in [23], is optimized, prototyped, and evaluated in this study. The principle of circuit operation, power optimization approach, and implementation details are presented in the following section. Section IV summarizes test setup and experimental results. Finally, the study is concluded in Section V.

II. IC Design

SECE is an effective topology to interface piezoelectric harvesters operating at low voltages. Low power and high mechanical frequency of MEMS PEH requires careful design of the ac–dc IC to achieve high efficiency. In [22], a flyback SECE uses multistage technique to handle highly charged PEH with a package inductor, but the high series resistance of the relatively large inductor constrains power conversion efficiency. The proposed multistage energy extraction (MSEE) on conventional SECE architecture allows shrinking the external inductor without affecting power conversion efficiency. The multistage extraction can efficiently transfer the harvested energy over a relatively low-profile inductor (100 μH–1 mH). In the previously reported multistage circuits, timing is calculated by multiplying digital inputs set by user and predefined coefficients, which requires measurements and hand-calculations. Compromises between mechanical frequency and power consumption cannot be avoided. Although the core configuration

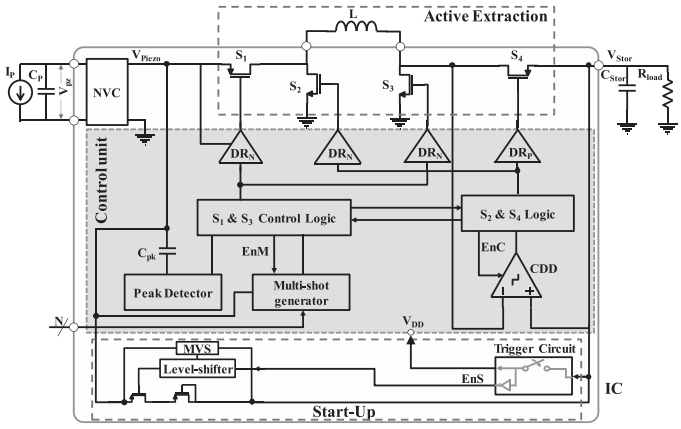


Fig. 1. System architecture of the integrated PEH IC; modified version of [23].

of the circuit in this paper is similar to SECE-integrated circuits proposed in [17] and [24], our design is adaptable to minimize power losses with the help of the multistage technique that does not require explicit calculation of extraction time duration. The circuit enhancements, which include a high accuracy peak detector and ultralow power control, play a significant role in extracting power more efficiently from MEMS PEH with few microwatts of capacity and high excitation frequency compared to previous approaches. Furthermore, implementation of the multistage generator with energy sensing capability eliminates efficiency and cost limitations arising from high mechanical frequency, additional digital inputs, and timing problems

A. Operation Principle

The proposed circuit comprises a control unit and three processing stages including a negative voltage converter (NVC), active extraction, and energy storage with start-up circuit, as shown in Fig. 1. The positive voltage from NVC charges the storage capacitor C_{stor}, at wake-up, through a diode and a control switch. The startup circuit decouples the supply voltage of the control unit (V_{DD}) and storage voltage (V_{stor}) as long as $V_{\text{stor}} < V_{\text{trig}}$, and switches the storage voltage to power-up the active components in the control unit $(V_{\text{DD}} = V_{\text{stor}})$ when $V_{\text{stor}} > V_{\text{trig}}$. The power extraction stage is designed based on the SECE technique. Active power extraction is realized through three phases managed by switch control circuitry, as shown in Fig. 2. In the first phase, all switches in Fig. 1 are turned OFF to bias the PEH at open-circuit condition until its output peaks. After peak detection, energy stored on the PEH capacitor is transferred to the inductor through C_p–L resonant circuit by turning S_1 and S_3 ON. The third phase is entered when PEH voltage reaches zero. At this point, S_1 and S_3 are turned OFF, S_2 and S_4 switches are turned ON, and the stored energy on the inductor is transferred to the storage capacitor C_{stor}. Charging of the capacitor continues until the inductor current reaches zero.

Then, the circuit goes back to the first phase, and starts a new cycle by turning all switches OFF. In the case of the multistage extraction, the second and third phases are repeated in sequence according to the defined stage number *N*, as shown in Fig. 2. The IC extracts generated energy in *N* successive packets. The

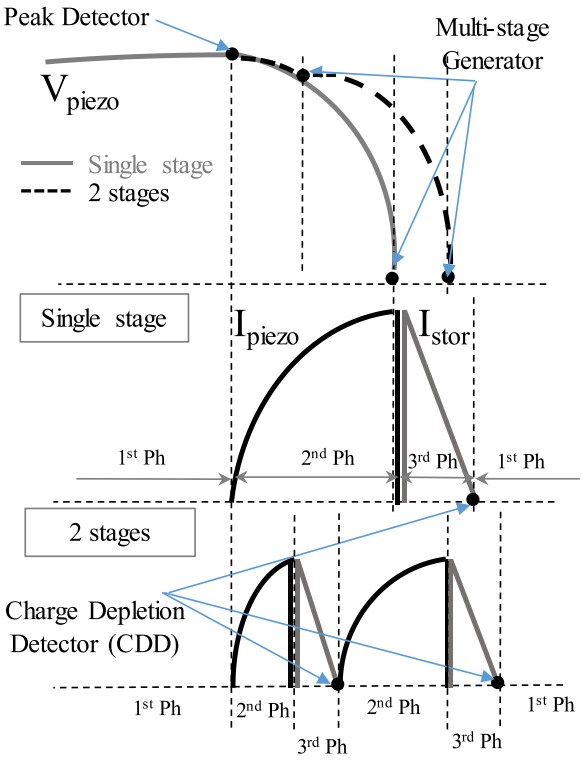


Fig. 2. Extraction phases and critical switching points of the SECE in time domain for single- and two-stage transfers.

energy transferred at each stage n through inductor is equal to $\frac{1}{2}C_pV_{\rm OC}^2/N$, where $V_{\rm OC}$ is the generated open-circuit voltage at piezoelectric capacitor C_P. Thus, the magnitude of the oscillation current depends on the total stage number N through the following relationship:

$$i_{{\rm peak},n} = V_{\rm oc}\sqrt{\frac{C_p}{L\times N}}. \tag{1}$$

The extraction time duration $T_{p,n}$ is worked through energy conservation to derive the same quantity of energy at the inductor in each stage

$$T_{p,n} = \frac{1}{\omega_p}\cos^{-1}\sqrt{\frac{N-n}{N-n+1}}. \tag{2}$$

During $T_{s,n}$, the energy of the inductor is transferred to the buffer capacitor. This period can be obtained by solving *LC* resonant circuit with initial the capacitor and the inductor values. $T_{s,n}$ is approximated as follows by assuming $C_{\rm stor} \gg C_p$:

$$T_{s,n} = L\frac{i_{{\rm peak},n}}{V_{\rm stor}}. \tag{3}$$

In our proposed approach, energy packet size is determined with energy sensing method that does not require explicit calculation of extraction time duration. The generated energy in the first phase is sensed through a downscaling circuit, and is divided by N with the help of a capacitor network. It is then compared with the energy extracted in the second phase, which is measured through a current sensing and energy converting circuit to determine the magnitude of the energy packet.

Eventually, the current magnitude in each stage is reduced by $\sqrt{1/N}$. Therefore, the conduction loss of the power switches and the inductor is decreased in proportion to the current reduction passed through an inductor–switch network. In addition, this approach allows utilizing a low volume inductor with small series resistance, which is desired for reduced system footprint and cost. Power analysis is discussed in the next part.

B. Power Optimization

The energy generated on a piezoelectric capacitor C_p as the beam vibrates, due to the mechanical excitation of the harvester, is obtained as

$$E_{\rm Coupled} = \frac{1}{2}C_pV_{\rm OC}^2. \tag{4}$$

The coupled energy is extracted through discharging the piezoelectric capacitor and transferred to output buffer capacitance. The pure energy harvested $E_{\rm Harv}$ is calculated as

$$E_{\rm Harv} = E_{\rm Coupled} - E_{\rm loss}. \tag{5}$$

There are four sources of power dissipation in the switching circuit. Resistive conduction losses in the inductors and MOSFET switches $(P_{\rm cond})$; charge redistribution losses at MOSFET parasitic capacitances during phase changes $(P_{\rm sw})$; capacitive switching losses at the gates of power switches $(P_{\rm driv})$; and leakage current associated with any MOSFET in OFF state $(P_{\rm leak})$

$$P_{\rm loss} = P_{\rm cond} + P_{\rm sw} + P_{\rm driv} + P_{\rm leak}. \tag{6}$$

With regard to circuit configuration and stage number, four dynamic power losses are expressed as follows:

$$P_{\rm cond} = (R_{\rm ind} + R_{\rm sw1\&sw3}) \times \sum\nolimits_N \int_0^{Tp,n} i_{p,n}^2\,dt + (R_{\rm ind} + R_{\rm sw2\&sw4}) \times \sum\nolimits_N \int_0^{Ts,n} i_{s,n}^2\,dt \tag{7}$$

$$P_{\rm driv} = (Q_{g,{\rm sw2,3,4}}V_{\rm stor} + Q_{g,{\rm sw1}}V_{\rm oc})f_{\rm exc} \tag{8}$$

$$P_{\rm sw} = C_{\rm ds,sw2}V_{pz,n}^2 f_{\rm exc} + C_{\rm ds,sw3}V_{\rm stor}^2 f_{\rm exc} \tag{9}$$

$$P_{\rm leak} = i_{\rm leak}w_{\rm sw1}V_{\rm oc} + i_{\rm leak}w_{\rm sw4}V_{\rm stor} \tag{10}$$

where $I_{\rm leak}$ is the leakage current per width specified in the technology datasheet.

In the above equations, ON-resistance $R_{\rm ON}$, gate-charge Q_g, drain-source capacitance, and $C_{\rm ds}$ are approximated by the following equations:

$$R_{\rm on} = 1/\mu C_{\rm ox}\frac{W}{L}(V_{gs} - V_{\rm th}) \tag{11}$$

$$Q_q = 2C_{\rm ov}WV_{gs} + C_{\rm ox}WL(V_{gs} - V_{\rm th}) + C_{\rm ov}WV_{\rm ds} \tag{12}$$

$$C_{\rm ds} = WL_DC_j\left(1 - \frac{V_{\rm ds}}{P_B}\right)^{-M_j} + (W + L_D) \times C_{j\rm sw}\left(1 - \frac{V_{\rm ds}}{P_{B\rm sw}}\right)^{-M_{j\rm sw}} \tag{13}$$

where μ is the mobility of electron or hole, $C_{\rm OX}$ is the gate oxide capacitance per unit area, $C_{\rm OV}$ is the gate overlap capacitance per

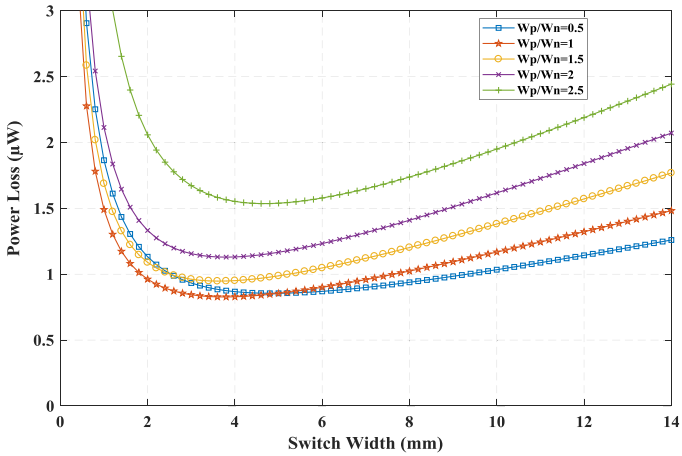


Fig. 3. Total power losses versus power switch sizes at $V_{OC} = 1.5$ V.

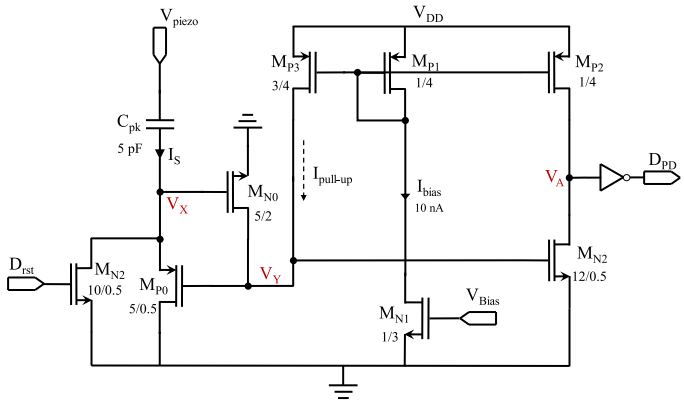


Fig. 4. Schematic of the implemented peak detector.

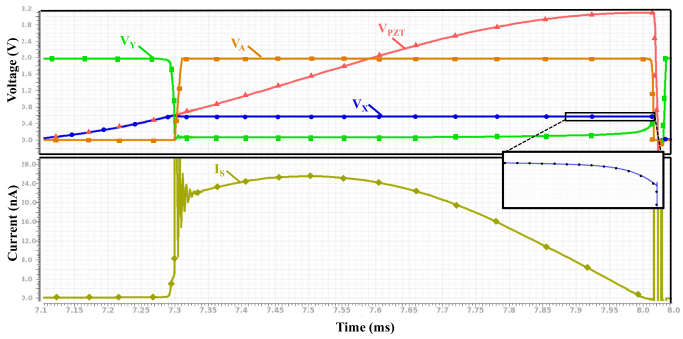


Fig. 5. Voltage and current waveforms of the peak detector.

unit length, C_J is the drain bottom junction capacitance per unit area at zero bias, $C_{J\mathrm{SW}}$ is drain sidewall junction capacitance per unit length at zero bias, P_{B} is the drain bottom junction built-in voltage, $P_{B\mathrm{sw}}$ is drain sidewall junction built-in voltage, M_j is the drain bottom junction grating coefficient, L_D is the lateral diffusion length, and $M_{j\mathrm{sw}}$ is the drain sidewall junction grating coefficient.

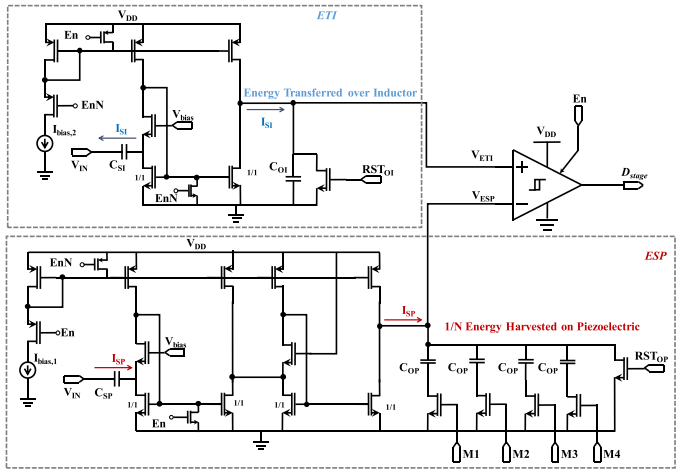
The above equations indicate that ON-resistance and gate-charge of the switch S_2 vary with input piezoelectric voltage, while the same parameters are sensitive to the storage voltage for the other switches. The substitution of (12)–(14) into (8)–(11) shows that all four power-dissipation sources depend on power switch size, input piezoelectric voltage, and storage voltage (V_{stor}).

In implemented technology, 180 nm HV CMOS, N-MOSFET, and P-MOSFET power switches tolerate up to 12 and 17 V at their terminals, respectively. The MSEE chip requires minimum supply voltage of 1.1 V to drive power switches and achieve proper operation of the MSEE. The maximum storage voltage is limited to 3.3 V, which is defined by 3.3 V MOSFETs utilized in the control unit. After thorough investigation of losses, within 180 nm HV CMOS, the total power loss is obtained as a function of N-MOSFET power switch sizes and corresponding aspect ratio of the P-MOSFET switches, as shown in Fig. 3. Since efficient extraction in low-power outputs of the MEMS PEHs are intended, minimum input voltage is set to 1.5 V and storage voltage is set to maximum allowable value $V_{\mathrm{stor}} = 3.3$ V. The power switch $(\mathrm{S}_1 - \mathrm{S}_4)$ sizes have been optimized, as $W = 4$ mm for a minimum power loss of 0.86 μW at just above the lowest allowable PEH voltage $V\mathrm{oc} = 1.5$ V. This optimization improves power efficiency for the low input power scenario, while maintaining the control of the higher input power levels through MSEE.

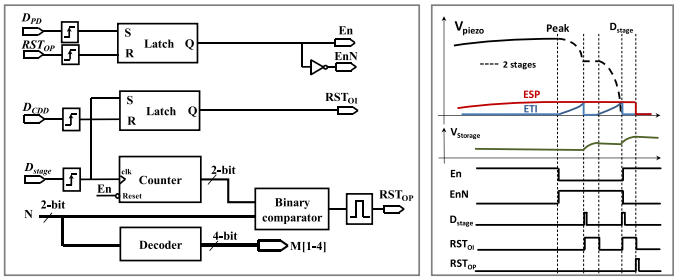
C. Control Unit

Peak detector, multistage generator, and charge-depletion detector (CDD) in the control unit sequence the switch drivers according to the phases described in the previous section, in order to realize the multistage synchronous charge extraction.

1) *Peak detector:* The proposed peak detector, shown in Fig. 4, is designed to operate at PEH voltage levels higher than supply voltage V_{DD}. The circuit operates in the current mode with internal negative feedback. A series capacitor C_{PK} converts piezoelectric voltage to current I_S, where Node V_X is reset to the ground, previously. Negative feedback action on M_{N0} and M_{P0} forces Node V_X to be charged just around the threshold voltage of the M_{N0} MOSFET. As PEH voltage peaks, I_S crosses zero, and voltage drop of the node V_X over M_{P0} turns M_{N0} OFF. As M_{N0} turns OFF, the node V_Y is pulled up by mirroring reference current through the node. Common source amplifier and digital inverters in the output stage deliver a high edge rate. Fig. 5 illustrates the operation of the peak detector through the voltage and current simulation waveforms. The accuracy of the peak detector is critical in viewpoint of power conversion efficiency. The previous current-mode peak detectors suffer from offsets due to reference-current level and device mismatch of the current comparator. The proposed circuit resolves above issues using an active switch (M_{N0}) instead of the current comparator. With increasing piezoelectric voltage, switch M_{N0} turns ON, and consequently M_{P0} starts conducting to regulate voltage at node V_X due to feedback between V_X and V_Y. When I_S reaches zero, M_{P0} dissipates accumulated charge at node V_X, turning OFF M_{N0}. The applied



(a)



(b)

Fig. 6. (a) Implemented multistage generator. (b) Operation principle and related signals.

method alleviates the sensitivity of the circuit to process variation and mismatches in MOSFETS. The proposed circuit pulls up node V_Y through $I_{\text{pull-up}}$ without contending with peak I_S, which results in significant improvement in response time. The upper limit of the input frequency determines the reference-current value, while the minimum detectable amplitude determines the value of the series capacitor C_{PK}. D_{rst} goes high to connect node V_X to ground as the extraction phase is entered. This suppresses I_S oscillation that is caused by the resonant switching in the second phase.

2) *Multistage generator circuit:* The multistage generator, depicted in Fig. 6(a), relies on energy drain without any calibration requirement. This circuit comprises two energy sensing circuits and a comparator. The energy generated on piezoelectric capacitor is sensed by the energy sensing circuit called energy stored in piezoelectric (ESP) in the first phase. The ESP utilizes a capacitor to convert piezoelectric voltage to current with the help of flipped voltage follower (FVF). The FVF provides almost constant voltage on the negative terminal of the capacitor through feedback connection of two cascaded transistors. Through two current mirrors, the sensed voltage is regenerated over sensing capacitors. The number of extraction steps (N) determines the capacitors connected in parallel to divide sensed energy by N. Four equally sized capacitors are controlled to obtain desired value, $C_{T,\text{op}} = C_{\text{op}} \times \text{M}_1 + C_{\text{op}} \times \text{M}_2 + C_{\text{op}} \times \text{M}_3 + C_{\text{op}} \times \text{M}_4$, with minimum voltage downscaling of C_S/C_{op}. When PEH voltage peaks, ESP circuit switches to hold state by lowering enable signal in order to save the measured voltage. During the second phase, energy transferred to the inductor is sensed through energy transferred on inductor (ETI) circuit based on the same principle, and the same size of the capacitances $C_{\text{SI}} = C_{\text{SP}}$ and $C_{\text{OI}} = C_{\text{OP}}$. Finally, sensed energy with ETI through V_{ETI} is compared with N-division of generated energy, determined through V_{ESP}, using a hysteresis comparator to determine energy packet size transferred to the inductor. This guarantees constant energy extraction at each stage, as shown in Fig. 6(b). Multistage output signal initiates the third phase to harvest the generated energy, and C_{OI} is reset for next extraction. The operation principle and related signals are illustrated in Fig. 6(b). The number of extraction stages is controlled through M_{1-4}, generated from two digital bits (labeled N in Fig. 1) and a decoder.

3) *CDD:* Depletion of stored energy in the inductor to storage capacitance is controlled by a charge-depletion comparator as shown in Fig. 7, with a relatively high bandwidth. The comparator monitors the voltage across S_4 switch to detect the end of inductor discharging. The CDD is only activated in the fourth phase to save power.

III. Experimental Results

The IC is designed in 180 nm HV CMOS technology from X-FAB company. The IC is implemented in an active area of 2 mm^2 within 1.5 mm × 1.5 mm die. The setup for experimental measurements is shown in Fig. 8 with micrograph of the chip. A custom MEMs piezoelectric harvester [25], fabricated in METU_MEMS center, is mounted on a holding board. The MEMS harvester with footprint of 9 mm × 4 mm has a capacitor of 4 nF. The MEMS harvester is excited at its resonance frequency with a shaker table consisting of a control unit, an amplifier, a feedback accelerometer, and an interface computer.

The maximum operation frequency of the MSEE is determined by the peak detector. A delay in detecting peak instant may cause significant energy loss as the energy transfer is initiated at lower piezoelectric voltage. The accuracy of implemented peak detector has thus been experimentally evaluated as a function of the input frequency. Fig. 9 shows piezoelectric and peak detector output waveforms for three different excitation frequencies. The accuracy of the peak detector is obtained as $(|V_{\text{max}} - V_{\text{meas}}|)/V_{\text{max}}$, which has been illustrated in Fig. 10 up to 4000 Hz, which is the maximum design frequency of the MSEE circuit. Peak point is detected with more than 98% accuracy for excitation frequency range of 20 to 4000 Hz with $I_{\text{pull-up}} = 30$ nA. High accuracy of the peak detector alleviates degradation of the power efficiency due to peak detection latency. The peak point can be detected with higher precision and operation frequency range can be extended by increasing the reference current.

The performance of the IC has been measured using an MEMs piezoelectric harvester with $C_P = 4$ nF attached to a shaker ta-

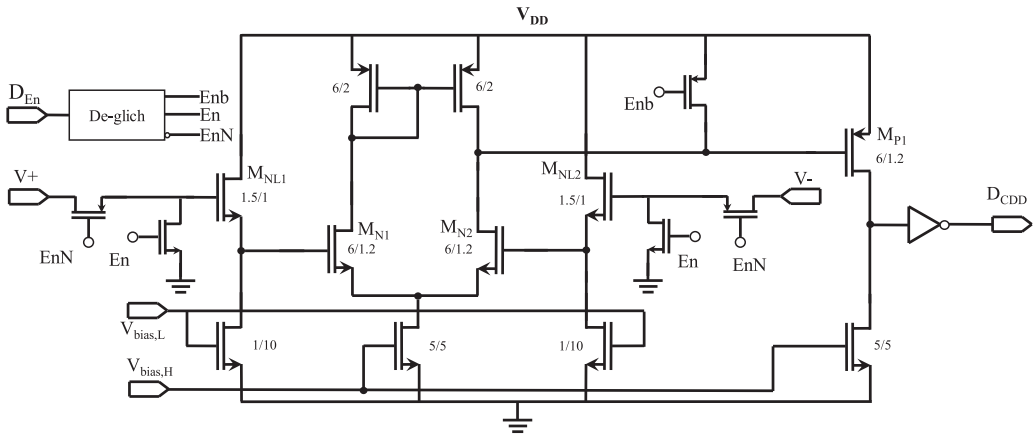


Fig. 7. CDD.

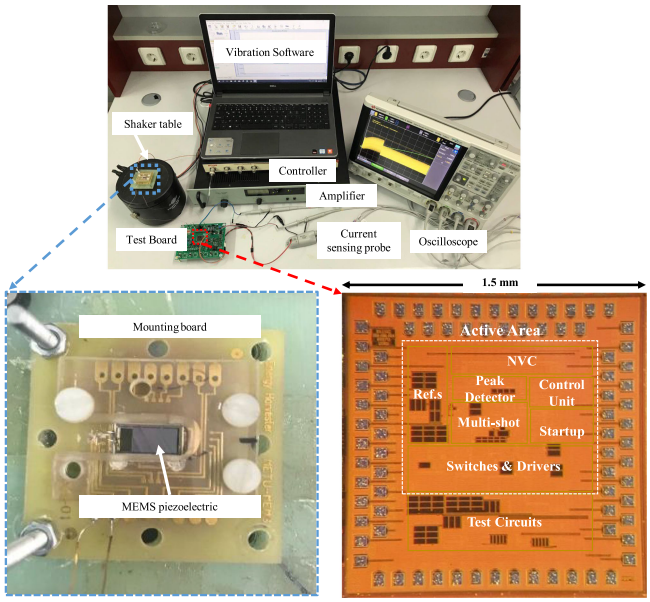


Fig. 8. Test setup for experiments, based on an IC, test board, and MEMS PEH.

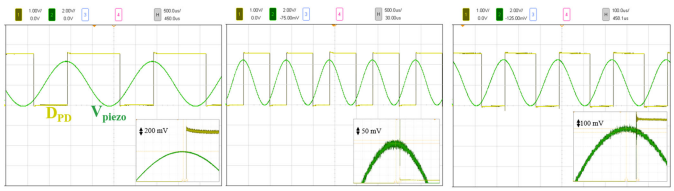


Fig. 9. Measured input and output waveforms of the peak detector for (a) 500 Hz, (b) 1 kHz, and (c) 4 KHz input frequencies.

ble. An inductor ($L = 1\,\text{mH}/\,5.1\,\Omega$) is connected to the chip to charge a 1 μF storage capacitance in parallel with a variable load resistance. Minimum piezoelectric peak voltage of 700 mV is required for operating start-up of the circuit. Fig. 11 depicts operation of the circuit for an excitation frequency of 390 Hz with 17 μW input power, and 290 kΩ load resistance. The storage capacitance is initially charged through the start-up circuit. Then, energy is extracted from PEH in three stages ($N = 3$).

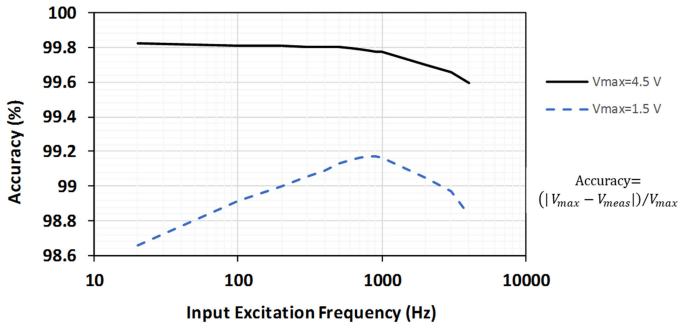


Fig. 10. Accuracy of the peak detector versus input excitation frequency with 1.5 and 4.5 V input peak voltages.

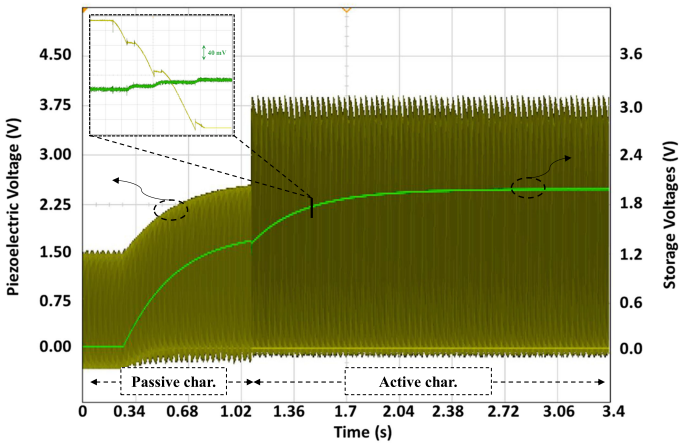


Fig. 11. Measured input–output waveforms during multistage extraction ($N = 3$) with highlighted periods for passive and active charging.

The voltage waveform during charging of the storage capacitor in three stages is shown in Fig. 11. Fig. 12 illustrates measured piezoelectric voltage and inductor current waveforms when different number of stages are used in the circuit. The magnitude of the current passing through inductor and switches is divided by the square-root of the number of stages. Consequently, conduction power loss is decreased with the current reduction. As seen in Fig. 12, there is a harvesting time variation among different number of stages. This variation is partly related to the extraction time duration $T_{p,n}$ that depends on the number of

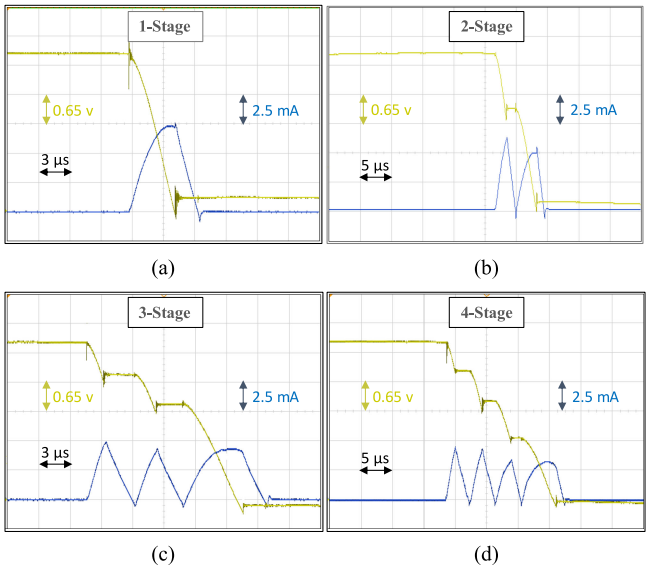


Fig. 12. Experimental piezoelectric voltage and inductor current waveforms using the multistage method. (a) Single stage. (b) Two stages. (c) Three stages. (d) Four stages.

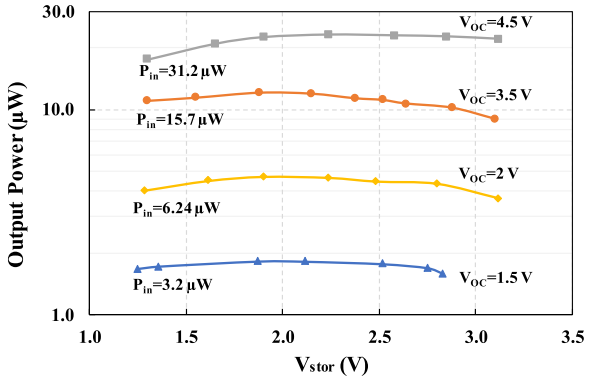


Fig. 13. Experimental output power versus output dc storage voltage for four values of V_{OC} with single-stage extraction.

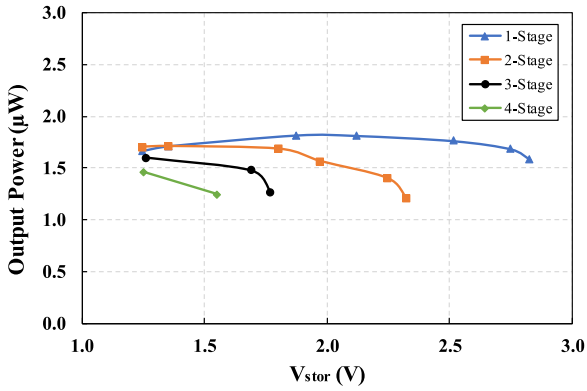


Fig. 14. Experimental output power at $V_{OC} = 1.5$ V for four different staging configurations versus output dc storage voltage.

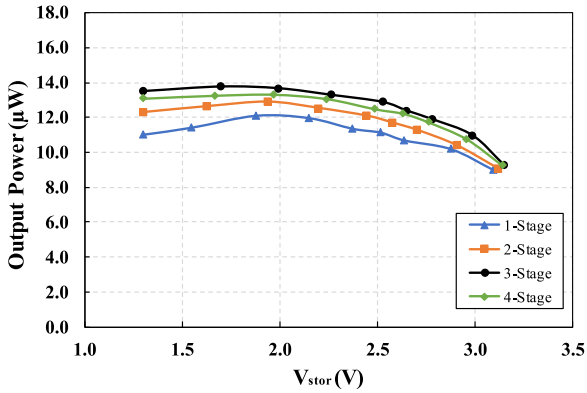


Fig. 15. Experimental output power at $V_{OC} = 3.5$ V for four different staging configurations versus output dc storage voltage.

stages as in (2). Another variation comes from the difference in storage voltage V_{stor}, which makes charge transfer duration $T_{s,n} = L \times i_{\text{peak},n}/V_{\text{stor}}$, variant. Summing the extraction and transfer durations determines total time, which is distinct for different N.

Initially, the output power extracted within a single stage has been measured as a function of the storage voltage. Fig. 13 depicts the outcome for several values of V_{OC}. The dependence of the extracted output power on storage voltage is low, as expected, due to SECE technique. Ratio of V_{OC} to V_{stor} affects efficiency at lower storage voltage levels, as it takes longer to transfer energy to storage. Losses due to switching at higher storage voltage are more dominant for lower input power. For lower storage voltage as ratio of V_{OC} over V_{stor} increases, the output power dependence on the storage voltage V_{stor} is shown in Figs. 14 and 15 for $V_{\text{oc}} = 1.5$ V and $V_{\text{oc}} = 3.5$ V, respectively, as the number of stages is varied. Single charge extraction shows the best performance for lower power limit, since excess switching dissipates dramatically higher power especially at higher output voltage. For higher input power, multistage extraction increases the output power due to the reduction of conduction losses on switches. Moreover, influence of the multistage extraction degrades with the increase of the output voltage due to high switching loss and the increase of quiescent current.

The charging efficiency η is obtained as the ratio of the effective power delivered to the storage capacitance over the average input power. The effective power is calculated as energy increment on the storage capacitance over the charging time, $\frac{1}{2}C_{\text{stor}}(V_{\text{Final}}^2 - V_{\text{trig}}^2)/\Delta t$ where V_{Trig} is the voltage trigging the active extraction. V_{Final} is the final stabilized voltage, 3.3 V at which extraction is deactivated. The input power is obtained through measured input voltage and current of the harvester connected to the proposed circuit. Fig. 16 depicts the charging efficiency of the circuit as a function of the piezoelectric open-circuit voltage

$$\eta = \frac{P_{\text{eff}}}{P_{\text{in}}} = \frac{\frac{1}{\Delta t}C_{\text{stor}}\left(V_{\text{Final}}^2 - V_{\text{trig}}^2\right)}{\frac{1}{\Delta t}\int V_{pz}.I_{\text{piezo}}.dt}. \tag{14}$$

It is expected that multistage power extraction will improve power efficiency with increasing input power. The maximum power efficiency was measured at 84.4%. As it stands, the op-

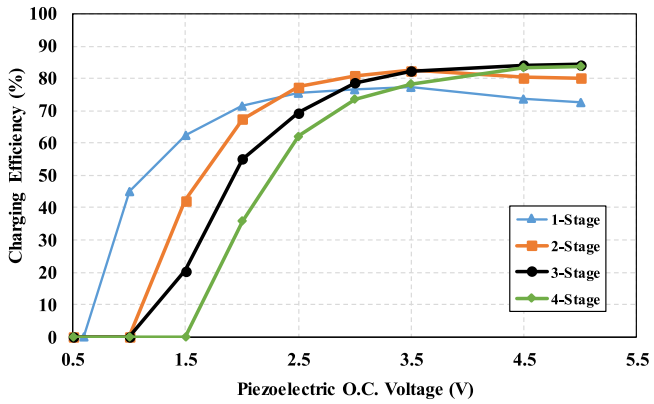


Fig. 16. Experimental power-conversion efficiency of the IC for four different staging configurations versus piezoelectric OC voltage.

TABLE I
COMPARISON OF IMPLEMENTED IC WITH OTHER SECE CIRCUITS

Parameters	Hehn, 2012 [17]	Gasnier, 2014 [22]	Dini, 2016 [24]	**This work**
Technology	0.35 µm	0.35 µm (off-chip MOSFETS)	0.32 µm	**180 nm HV**
Static Power loss	< 4 µW	< 1 µW	> 0.4 µW*	**< 0.7 µW**
Max. input voltage	< 20 V	> 200 V	< 5 V	**< 12 V**
Operation Frequency range	<600 Hz**	< 100 Hz**	< 100 Hz**	**< 4 kHz**
Excited Frequency	174 Hz	100 Hz	60 Hz	**390 Hz**
Inductor (Volume)	10mH ($630mm^3$)	10mH/25uH ($125mm^3$)	10mH/560uH (-)	**1 mH ($67mm^3$)**
Max. Efficiency	85% @V_p=12.8V	61% @V_p=40V	85.3% @V_p=4.7V	**84.4% @Vp=4.75V**
Output. Power @Max. Eff.	477 µW	560 µW	51.33 µW	**78 µW**

* Equivalent Static power loss estimated from reported quiescent current.
** Frequency range estimated form reported efficiency limitations.

timum stage number can be determined through input power or corresponding open-circuit piezoelectric voltage. The stage number N can be adjusted automatically through input power measurement at the end of the first phase of the extraction. The power efficiency can consequently be maximized for all input power levels in an autonomous manner.

Table I compares the experimental results of the implemented IC with recent integrated SECE converters. The maximum operation frequency of the previous studies has been limited to achieve high conversion efficiency for harvester energy. This has resulted in the use of large piezoelectric harvesters with low resonance frequency, which is not practical in integrated and implantable electronic devices. Additional volume restriction follows from the size of the external inductor. Hehn *et al.* [17] utilized 10 mH inductor with large package (630 mm^3) to constrain the oscillation current. Dini *et al.* [24] utilized a 560 μH inductor in addition to 10 mH to remove residual charge effect. Gasnier *et al.* [22] used two off-chip MOSFETs in addition to small sized inductor (125 mm^3); however, high series resistances of the inductor (72 Ω) adversely affected the power conversion efficiency. Our system benefits from both wide frequency operation range that is capable of harvesting energy from MEMS piezoelectric harvesters, and small size inductor (66.8 mm^3). As a result of optimization, minimum dynamic power loss has reduced below 1 μW. The multistage extraction circuit has limited oscillation current, while improving the power efficiency to 84.4%.

IV. CONCLUSION

An autonomous CMOS IC has been designed and fabricated for the efficient utilization of PEH resources. An adaptable MSEE circuit has been proposed to enhance the efficiency of the circuit for wide range of inputs. 98% accuracy has been measured up to 4 kHz for peak detector circuit. The performance of the IC has been evaluated through MEMS piezoelectric harvester with 9 mm × 4 mm footprint. The charging efficiency of the IC goes above 47% for an input power of 3.12 μW, while the maximum charging efficiency is recorded as 84.4% for an input power of 78 μW. The presented PEH interface IC delivers the means to supply power to microelectronic devices more efficiently, regardless of the variation in the available PEH energy.

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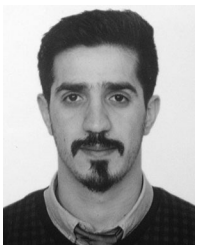

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