# General Control Scheme for a Dual-Input Three-Level Inverter

Cheng Yan, Dehong Xu, *Fellow, IEEE*, and Wenjie Chen

***Abstract*—This paper proposes a general control scheme for the dual-input three-level inverter, which comes from a neutral point clamped three-level inverter. It can be used for photovoltaic (PV) systems or battery storage systems with two dc sources. The dual-input three-level inverter can be connected with two PV arrays, which are able to realize maximum power point tracking independently. First, the dynamic model of the dual-input three-level inverter is established, which describes the relationship between the dual-input voltages and the duty cycle. After discussing the control theory of the dual-input voltages, a typical control scheme is proposed. The design of a control loop is introduced in details. Afterward, modulation and restriction of the proposed method are discussed. Finally, experiment on a 125 kW dual-input three-level PV inverter is implemented to verify the validity and feasibility of the proposed method.**

***Index Terms*—Inverters, power control, pulsewidth modulation (PWM), voltage control.**

## I. Introduction

CURRENTLY, three-level inverters have been widely used for PV generations [1]. With regards to a PV inverter, if the PV array can be divided into two subarrays, which are connected to the upper and lower dc bus of the three-level inverter, then each subarrays can be controlled independently and work at its maximum power point (MMP). Therefore, independent control of the upper and lower dc bus of the three-level inverter is able to increase solar energy harvesting. This concept can be extended to a battery energy storage system. In these cases, decoupling control of dual-input of the three-level inverter is needed.

Since the voltages of upper and lower half dc bus in the three-level inverter can be controlled independently, it is called the dual-input three-level inverter in this paper. There have already been important developments with respect to control of dual-input three-level inverters.

Front-end dc–dc converter stages are added between the PV array and the three-level inverter [2]. The dc–dc converters are used to regulate the terminal voltage of two PV strings independently. Thus, independent maximum power point tracking (MPPT) control is realized even for both PV strings with different output characteristics. Similarly, an auxiliary converter is used to the dual-input three-level inverter in [3]–[5]. Compared to a full-power capacity front-end dc–dc converter method, the auxiliary converter only needs to deal with the power deviation between the two inputs. Although both methods mentioned above can realize independent MPPT control of two PV strings, extra hardware is needed. It not only increases circuit complexity but also results in extra power conversion loss in the added dc–dc conversion stage. Therefore, dual-input voltage control methods without extra power stages are preferred.

Voltage control methods without extra additional power stages have been extensively investigated in the literature [6]–[29]. Though most of them are concentrated on neutral point (NP) voltage balance for the three-level inverter, it shares the similar control concepts for the dual-input three-level inverter. These methods can be classified according to the pulsewidth modulation (PWM) methods.

For dual-input three-level inverter control methods based on carrier-based PWM (CBPWM) schemes, positive or negative zero sequence voltage is injected according to the NP voltage and direction of instantaneous output three-phase current [6]–[8]. If the accurate function between NP current and the added zero sequence voltage is revealed, the active control methods with a linear model can be established. In [9]–[13], the accurate needed zero sequence voltage is derived online according to the deviation of dc-link voltage, the instantaneous current, and the capacitance of dc link. It can completely control the dc-link voltage of the three-level inverter without any low-frequency NP voltage oscillations. Since the exact calculation of added zero sequence voltage in these methods is quite complicated, so the curve fitting is applied in [14] to simplify the calculation. Based on this control concept, an asymmetrical voltage control for dual-input three-level based on CBPWM is proposed in [15]. The NP current is indirectly controlled by the zero sequence voltage. Correlation between NP current and zero-sequence voltage is mathematically analyzed. The performance of all these methods depends on the accurate relationship between the zero sequence voltage and NP current. In [16]–[18], NP voltage control methods based on double-signal PWM (DSPWM) are able to completely remove low-frequency oscillation appearing in NP. The relationship between changed modulation signal and the NP current is easy to be calculated. Besides, this method is suitable for any load over the full range of converter output volt-

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age and for all load power. But the switching frequency of the power devices is higher than with the standard CBPWM, and the high-frequency harmonic component of the output voltages increases.

For dual-input three-level inverter control methods based on space vector modulation (SVM) since one pair of redundant small vectors have opposite effect on the NP voltage, thus the NP voltage is controlled by selecting proper small vector or adjusting dwell time of redundant small vectors [19]–[21]. Independent voltage control methods based on SVM are proposed in [22]–[24]. The dwell time of two redundant vectors is rearranged according to instantaneous voltage deviation. Output voltage distortion due to the deviation of two capacitor voltages is taken into consideration. In [24], the influence of all active vectors in a switching sequence is taken into consideration before their activation. Similar control methods based on the discontinuous PWM (DPWM) are realized by selecting small vector properly [25]–[27]. Methods based on the traditional SVM or DPWM are easy to be implemented. But the control performance has not been deeply investigated. Independent voltage control method based on virtue space vector PWM (VSVPWM) is proposed in [28]. This method is similar to DSPWM and can completely remove low-frequency oscillation. However, the switching loss and high-frequency harmonics of output voltage/current will increase.

All these methods mentioned above are all derived from specific PWM or SVM schemes. Up to now, we lack a general model to explicitly describe the relationship between the dual-input voltages and PWM duty cycles for the dual-input three-level inverter. Analysis of dual-input voltage control restriction has not been deeply investigated yet.

In this paper, we hope to generalize the basic concept of independent control beyond the specific PWM modulation. The control is based on power concept rather than the instantaneous output ac current. An independent control scheme of the dual-input three-level inverter is proposed. The dual-input three-level inverter can be connected with two PV arrays, which are able to realize MPPT independently. The paper is arranged as follows. In Section II, the dynamic model of the dual-input three-level inverter is established. The relationship between the dual-input voltages and the duty cycle is revealed. After discussing the control theory of the dual-input voltages, a typical control scheme is proposed. In Section III, the design of the control loop is implemented in details. In Section IV, modulation and restriction of the proposed method are discussed. The proposed method is verified via experimental results in Section V, and the conclusion is given in Section VI.

## II. Modeling of the Dual-Input Three-Level Inverter

A dual-input three-level inverter connected with two independent PV arrays is shown in Fig. 1. It is mainly composed of a neutral point clamped (NPC) or T-type three-level inverter, which is connected to the grid with *L* filter and step-up transformer.

It is assumed that power devices in Fig. 1 are ideal switches, and each arm of the bridge has three states (positive, negative, and neutral). So each arm can be simplified by three switches

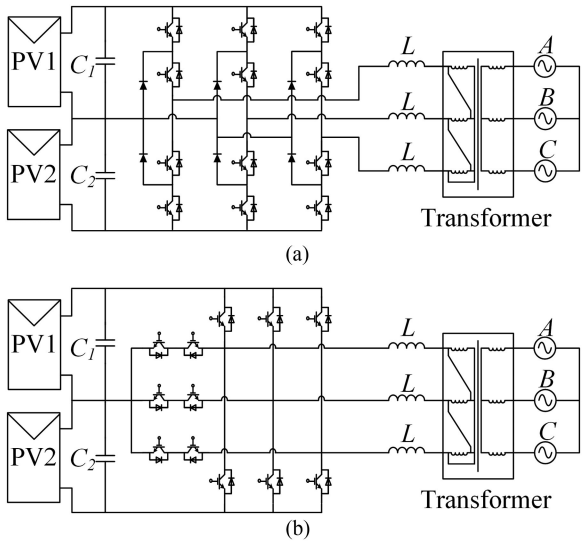


Fig. 1. Dual-input three-level inverter. (a) NPC. (b) T-type.

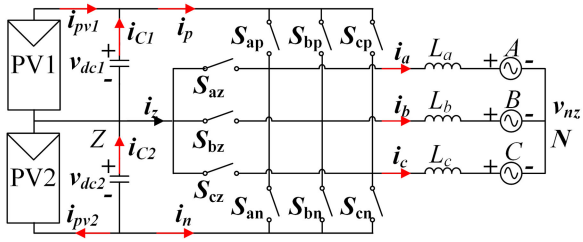


Fig. 2. Equivalent circuit of the dual-input three-level inverter.

(the upper, lower, and neutral switches), shown in Fig. 2. PV1 and PV2 represent two independent PV arrays. $i_{pv1}$ and $i_{pv2}$ are the current of PV1 and PV2, respectively. $i_p$ is the positive bus current between the dc capacitance and the three-phase bridge. $i_n$ is the negative bus current between the dc capacitance and the three-phase bridge. $v_{dc1}$ and $v_{dc2}$ are the voltage of PV1 and PV2, respectively. $v_{ga}$, $v_{gb}$, $v_{gc}$ are the grid phase voltage and $i_a$, $i_b$, $i_c$ are the grid current. *L* is the inductance of the filter, and its parasitic resistance is *r*.

### A. Power Control Model

According to the equivalent circuit, a state average model in a three-phase stationary coordinate frame is derived as follows for the ac side:

$$L\frac{d}{dt}\begin{bmatrix} i_a \\ i_b \\ i_c \end{bmatrix} = \begin{bmatrix} d_{ap} \\ d_{bp} \\ d_{cp} \end{bmatrix} v_{\mathrm{dc1}} - \begin{bmatrix} d_{an} \\ d_{bn} \\ d_{cn} \end{bmatrix} v_{\mathrm{dc2}} - r\begin{bmatrix} i_a \\ i_b \\ i_c \end{bmatrix} - \begin{bmatrix} v_{ga} \\ v_{gb} \\ v_{gc} \end{bmatrix} - \begin{bmatrix} v_{nz} \\ v_{nz} \\ v_{nz} \end{bmatrix} \tag{1}$$

where $v_{nz}$ is the voltage from utility neutral point *N* to neutral point *Z* of the dc bus in the three-level inverter. $d_{xp}$, $d_{xn}$, $d_{xz}$ are the switching duty cycles of upper, lower, and neutral switches in phase *x*, respectively (*x* can be *a*, *b*, or *c*).

To reveal the relationship between the dc power and ac current, the power of PV1 and PV2 is derived as follows:

$$P_{\rm dc1} = v_{\rm dc1} \cdot i_p = v_{\rm dc1} \cdot (d_{ap} i_a + d_{bp} i_b + d_{cp} i_c)$$
$$P_{\rm dc2} = v_{\rm dc2} \cdot (-i_n) = v_{\rm dc2} \cdot (d_{an} i_a + d_{bn} i_b + d_{cn} i_c). \quad (2)$$

The duty cycles in one phase, duty cycles $d_{xp}$, $d_{xn}$, $d_{xz}$ need to satisfy the relationship in

$$d_{xp} + d_{xn} + d_{xz} = 1. \quad (3)$$

The model in (1) and (2) under the stationary coordinate frame can be converted into that under a rotating coordinate frame as follows:

$$L\frac{d}{dt}\begin{bmatrix} i_d \\ i_q \\ i_0 \end{bmatrix} = \begin{bmatrix} d_{dp} \\ d_{qp} \\ d_{0p} \end{bmatrix} v_{\rm dc1} - \begin{bmatrix} d_{dn} \\ d_{qn} \\ d_{0n} \end{bmatrix} v_{\rm dc2} - \begin{bmatrix} v_{gd} \\ v_{gq} \\ v_0 \end{bmatrix} - r\begin{bmatrix} i_d \\ i_q \\ i_0 \end{bmatrix} - \begin{bmatrix} \omega L i_d \\ -\omega L i_q \\ i_0 \end{bmatrix} \quad (4)$$

$$P_{\rm dc1} = v_{\rm dc1} \cdot (d_{dp} i_d + d_{qp} i_q)$$
$$P_{\rm dc2} = v_{\rm dc2} \cdot (d_{dn} i_d + d_{qn} i_q) \quad (5)$$

where $v_{gd}$, $v_{gq}$ are the components of grid voltage in the *dq*0 frame. $i_d$, $i_q$ are the components of grid current in the *dq*0 frame. $d_{dp}$, $d_{qp}$, $d_{0p}$ are the duty cycles for upper switches in the *dq*0 frame, $d_{dn}$, $d_{qn}$, $d_{0n}$ are the duty cycles of lower switches, and $d_{dz}$, $d_{qz}$, $d_{0z}$ are the switching duty cycles for neutral switches. The relationship between the duty cycles in the *dq*0 frame and the duty cycles in the stationary coordinate frame is derived as

$$\begin{bmatrix} d_{dp} & d_{dn} & d_{dz} \\ d_{qp} & d_{qn} & d_{qz} \\ d_{0p} & d_{0n} & d_{0z} \end{bmatrix} = T \begin{bmatrix} d_{ap} & d_{an} & d_{az} \\ d_{bp} & d_{bn} & d_{bz} \\ d_{cp} & d_{cn} & d_{cz} \end{bmatrix} \quad (6)$$

where *T* is the matrix of park transformation

$$T = \sqrt{\frac{2}{3}} \begin{bmatrix} \cos\omega t & \cos\left(\omega t - \frac{2\pi}{3}\right) & \cos\left(\omega t + \frac{2\pi}{3}\right) \\ -\sin\omega t & -\sin\left(\omega t - \frac{2\pi}{3}\right) & -\sin\left(\omega t + \frac{2\pi}{3}\right) \\ \frac{1}{\sqrt{2}} & \frac{1}{\sqrt{2}} & \frac{1}{\sqrt{2}} \end{bmatrix}. \quad (7)$$

According to (3) and (6), duty cycles in the *dq* frame satisfy the relationship

$$d_{dp} + d_{dn} + d_{dz} = 0$$
$$d_{qp} + d_{qn} + d_{qz} = 0. \quad (8)$$

The factor $\omega L$ in (4) can be decoupled, so the model in each *dq*0 frame is composed of three decoupled parts. Among them, the zero-sequence equation can be ignored for a three-phase three-wire system.

*Q*-axis voltage $v_{gq}$ is regulated to be zero. The three-level PV inverter is controlled with unit power factor, i.e., $i_q = 0$. The power loss of the inverter is ignored, and the grid power is equal to the sum of the dual-input power

$$P_{\rm sum} = P_{\rm dc1} + P_{\rm dc2} = v_{gd} \cdot i_d. \quad (9)$$

Therefore, the total power $P_{\rm sum}$ can be controlled by regulating the *d*-axis grid current $i_d$. The different power $P_{\rm dif}$ of the dual-input $P_{dc1}$ and $P_{dc2}$ is derived from (5) and (8)

$$P_{\rm dif} = P_{\rm dc1} - P_{\rm dc2} = v_{\rm dc1} \cdot i_d \cdot d_{dp} + v_{\rm dc2} \cdot i_d \cdot d_{dn}$$
$$= (v_{\rm dc1} - v_{\rm dc2}) \cdot i_d \cdot d_{dp} - v_{\rm dc2} \cdot i_d \cdot d_{dz}. \quad (10)$$

Diagram of a dual-input three-level inverter model is shown in Fig. 3. The duty cycle in *d*-axis $d_{dp}$ and $d_{dz}$ can control the output power of the three-level inverter. The duty cycle $d_{dz}$ plays a more important role than $d_{dp}$ in controlling the power deviation $P_{\rm dif}$ because $v_{dc1}$ and $v_{dc2}$ are approximately equal. In other words, the *d*-axis duty cycle of neutral switches $d_{dz}$ determines the power deviation $P_{\rm dif}$. Therefore, the duty cycle $d_{dp}$ is used to control the *d*-axis current $i_d$, i.e., total power. The rest duty cycle in *d*-axis $d_{dn}$ can be decided by (8). For duty cycle in the *q*-axis, $d_{qp}$ is used to control *d*-axis current $i_q$, i.e., the power factor. There is redundancy in remaining two duty cycles $d_{qz,}$ and $d_{qz}$, which brings freedom in generalizing the PWM scheme.

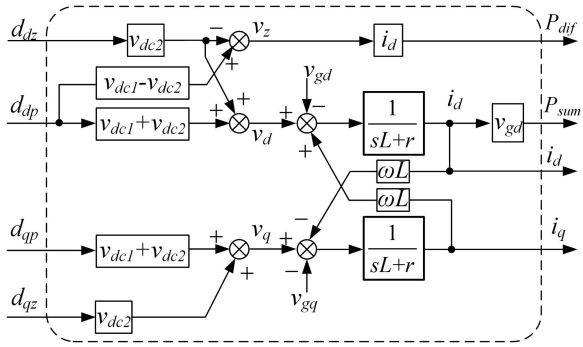


Fig. 3. Power dynamic model of the dual-input three-level inverter.

### B. Voltage Control Model

In PV application, the dc voltage is the controlled target. It is essentially controlled by the output power of each PV array. As the control relationship between and power and the duty cycle is established, the relationship between the voltage and its output power can be written as

$$C_1 \frac{dv_{\rm dc1}}{dt} = i_{\rm pv1} - i_p = i_{\rm pv1} - \frac{P_{\rm dc1}}{v_{\rm dc1}}$$
$$C_2 \frac{dv_{\rm dc2}}{dt} = i_{\rm pv2} + i_n = i_{\rm pv2} - \frac{P_{\rm dc2}}{v_{\rm dc2}}. \quad (11)$$

The voltage of each PV array can be controlled by regulating its output power. So the dynamic model of the dual-input three-level inverter for voltage control is shown in Fig. 4.

### C. Voltage Control Scheme

Based on the model mentioned above, the voltage control scheme for the dual-input three-level inverter is shown in Fig. 5.

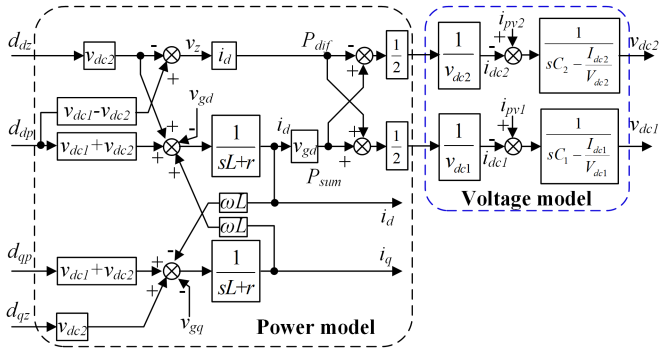


Fig. 4. Voltage control model of the dual-input three-level inverter.

It is composed of outer dc voltage control loop and inner grid current control loop. Each voltage of the dc bus is controlled by a PI regulator with dc voltage feedback. The output of the voltage regulator is used as the power reference of the inner current loop. And the output of the current regulator is the duty cycle for the three-level inverter.

Besides, necessary decoupling between duty cycles with dc bus voltage is added. The factor $\omega L$ between current $i_d$ and $i_q$ is also decoupled similar to the traditional *dq* dual controller [30]. The modulation is produced with the demand of certain duty cycle analyzed above.

## III. Control Loop Designed and Analysis

From the analysis in the previous section, the power control can be divided into two parts: the total power is control by the *d*-axis current, which is determined by duty cycle $d_{dp}$, and the different power is mainly controlled by $d_{dz}$, the *d*-axis duty cycle of neutral switches. Replace the dual-input three-level inverter in Fig. 5 with a mathematical module. The fundamental control loop is shown in Fig. 6.

### A. Design of the Current Inner Control Loop

The *d*-axis current $i_d$ is controlled by the duty cycle $d_{dp}$. The *q*-axis current $i_q$ is controlled by the duty cycle $d_{qp}$. There are several coupling factors between $d_{qz}$ and $d_{dp}$ in Fig. 6. The coupling is eliminated as (12). Besides, the inductor factor decoupling, dc voltage, and grid voltage feed forward are also implemented here [31], [32]. So the duty cycle reference $d_{dp}^*$ is designed

$$d_{dp}^* = \frac{\left(i_d^* - i_d\right) G_{\mathrm{PI\_}i}(s) + v_{gd} - v_{\mathrm{dc2}} \cdot d_{dz} - \omega L \cdot i_q}{v_{\mathrm{dc1}} + v_{\mathrm{dc2}}} \quad (12)$$

where $G_{\mathrm{PI\_}i}(s)$ is the PI regulator for the current control loop.

So the inner control loop can be simplified as Fig. 7 without any coupling factors with the other loop. $e^{-\tau s}$ is the time delay of the control loop. Besides, the disturbance of grid voltage is neglected. The transfer function of the current control loop can be written as

$$i_d = H_i(s)\, i_d^*,$$
$$H_i(s) = \frac{G_{\mathrm{PI\_}i}(s) \cdot e^{-\tau s}}{sL + r + G_{\mathrm{PI\_}i}(s) \cdot e^{-\tau s}}. \quad (13)$$

The inner control loop is similar to the traditional current control in the *dq*0 frame.

### B. Design of the Voltage Control Loop

Similar to the *d*-axis duty cycle $d_{dp}$, the duty cycle reference $d_{dz}^*$ can be designed as follows:

$$d_{dz}^* = \left(\left(P_2^* - P_1^*\right) \cdot K + \left(v_{\mathrm{dc1}} - v_{\mathrm{dc2}}\right) \cdot d_{dp}^*\right) / v_{\mathrm{dc2}} \quad (14)$$

$$\begin{cases} P_1^*(s) = \left(v_{\mathrm{dc1}}(s) - v_{\mathrm{dc1}}^*(s)\right) G_{\mathrm{PI\_}v}(s) \\ P_2^*(s) = \left(v_{\mathrm{dc2}}(s) - v_{\mathrm{dc2}}^*(s)\right) G_{\mathrm{PI\_}v}(s) \end{cases} \quad (15)$$

where $K$ is the proportion coefficient. $P_1^*$ and $P_2^*$ are the output of the PV1 and PV2 voltage regulators, respectively. $G_{\mathrm{PI\_}v}(s)$ is the PI regulator for the voltage control loop.

According to Fig. 6, the sum of $P_1^*$ and $P_2^*$ is set as reference of *d*-axis current $i_d^*$. And the total output power $P_{\mathrm{sum}}(s)$ and power deviation $P_{\mathrm{dif}}(s)$ of the inverter can be written as

$$\begin{cases} P_{\mathrm{sum}}(s) = \left(P_1^*(s) + P_2^*(s)\right) \cdot H_i(s) \cdot V_{gd} \\ P_{\mathrm{dif}}(s) = \left(P_2^*(s) - P_1^*(s)\right) \cdot K \cdot (-i_d). \end{cases} \quad (16)$$

According to (11), (15), and (16), the voltage of dc1 can be expressed as

$$v_{\mathrm{dc1}}(s) = \frac{A \cdot v_{\mathrm{dc1}}^*(s) - B\left(v_{\mathrm{dc2}}(s) - v_{\mathrm{dc2}}^*(s)\right) + \frac{1}{sC_1} \cdot i_{\mathrm{pv1}}(s)}{A+1} \quad (17)$$

$$A = \frac{G_{\mathrm{PI\_}v}(s)\left(K \cdot i_d + H_i(s)\, v_{gd}(s)\right)}{2 \cdot sC_1 \cdot V_{\mathrm{dc1}}}$$
$$B = \frac{G_{\mathrm{PI\_}v}(s)\left(K \cdot i_d - H_i(s)\, v_{gd}(s)\right)}{2 \cdot sC_1 \cdot V_{\mathrm{dc1}}}. \quad (18)$$

The control performance of $v_{dc1}$ will be affected by $v_{dc2}$ or $v_{dc2}^*$ due to the coefficient *B*, which will lead to unexpected disturbance and poor dynamic control performance. In order to control the voltage of dc1 and dc2 independently, the coefficient *B* should be set approximately to be zero. So the coefficient *K* is designed as

$$K = H_i(s)\, v_{gd}(s) / i_d. \quad (19)$$

As traditional control loop design, the inner loop is much faster than the outer loop [33], $H_i(s)$ can be regarded as 1 in designing the outer voltage loop.

Then, the voltage control of dc1 is only related to its voltage reference and disturbance of PV current

$$v_{\mathrm{dc1}}(s) = \frac{A}{1+A} v_{\mathrm{dc1}}^*(s) + \frac{1}{sC_1} \frac{1}{1+A} i_{\mathrm{pv1}}(s). \quad (20)$$

It is similar to voltage control of dc2. As long as *K* is set as (19), the coupling between the voltage of dc1 and voltage of dc2 can be suppressed. The voltage of dc1 and dc2 can be controlled

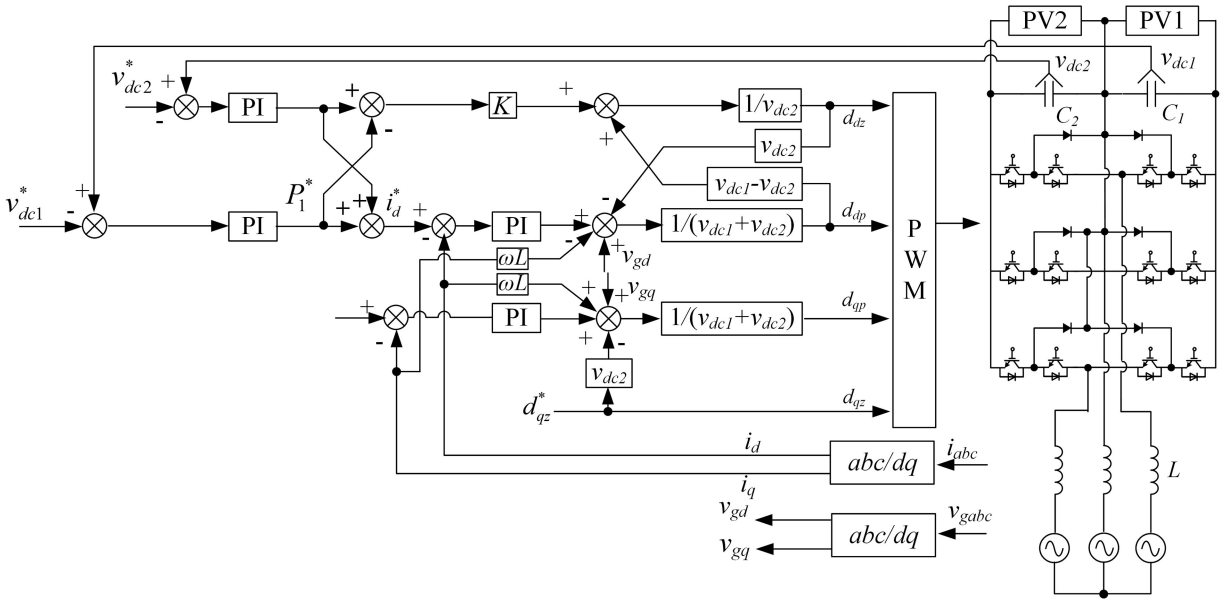


Fig. 5. Voltage control scheme for the dual-input three-level inverter.

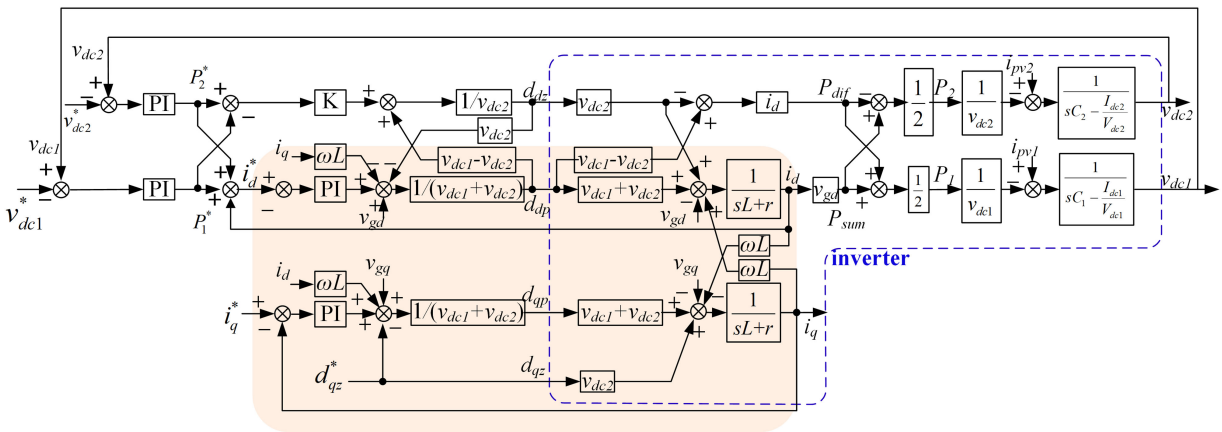


Fig. 6. Voltage control loop.

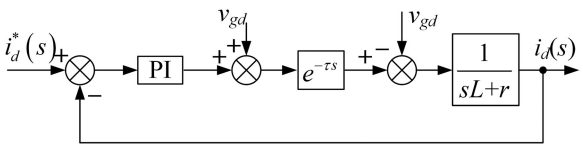


Fig. 7. Current inner loop and total power outer loop.

independently. The voltage control of dc2 is only related to its voltage reference and disturbance of PV current

$$v_{\mathrm{dc2}}(s) = \frac{A}{1+A} v^{*}_{\mathrm{dc2}}(s) + \frac{1}{sC_2}\frac{1}{1+A} i_{\mathrm{pv2}}(s). \quad (21)$$

### C. Bode Plot

The current control loop is designed to ensure that the output currents meet the grid code. The bandwidth of the current control loop should be high enough to deal with the dynamic situation such as low voltage ride through. But the control bandwidth is limited by the switching frequency. In this paper, the switching frequency is 5 kHz. The cross-over frequency of the current control loop is designed to 500 Hz, which is much lower than the switching frequency to achieve quite good stability. The bode diagram before and after the PI regulator is shown in Fig. 8. The cross-over frequency before control is 1000 Hz. The zero-point frequency of the PI controller is designed to 50 Hz. The cross-over frequency of the control loop is 500 Hz and the phase margin is 49°.

The voltage control loop is designed to control the dc/PV voltage. According to a traditional control loop design, the outer voltage control loop should be much slower than the inner current control loop. On the other hand, the voltage control speed should be faster than the MPPT speed. The MPPT interval in the inverter of this paper is 1 s. So the bandwidth of the voltage control loop is designed to 50 Hz, which is much slower than the inner current control loop (500 Hz), and faster than the MPPT control speed (1 Hz). The bode diagram before and after the PI regulator is shown in Fig. 9. The cross-over frequency before

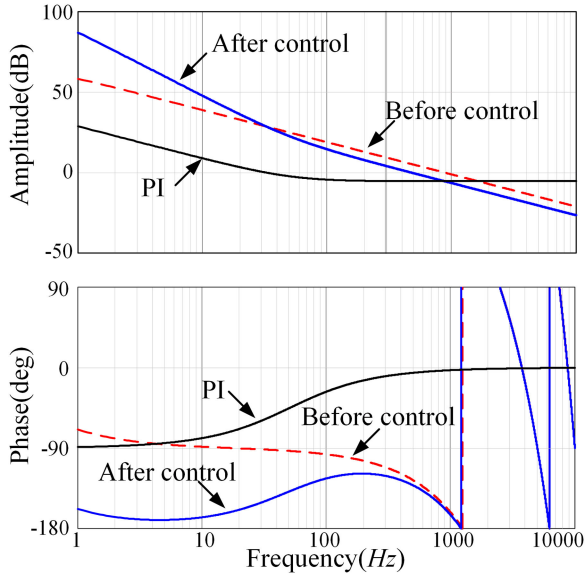


Fig. 8. Bode diagram of the current control loop.

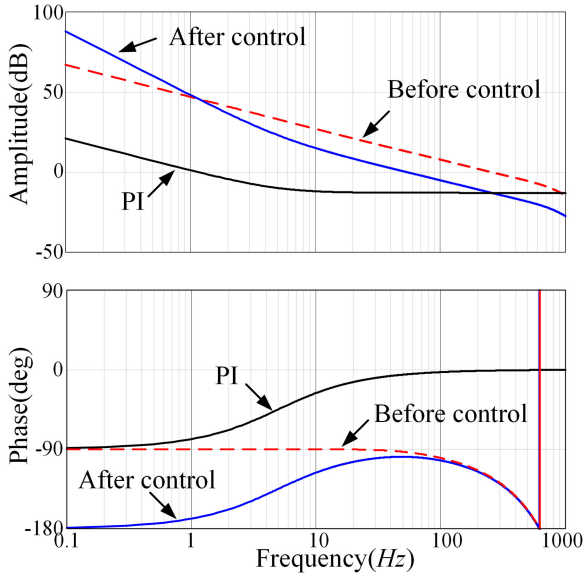


Fig. 9. Bode diagram of the voltage control loop.

control is 250 Hz. The zero-point frequency of the PI controller is designed to 5 Hz. The cross-over frequency is 50 Hz and the phase margin is 81°.

Based on the analysis and design aforementioned, the inverter has enough dynamic performance. Meanwhile, the stability of the system is satisfactory.

## IV. Modulation and Restriction in the Dual-Input Three-Level Inverter

According to the analysis aforementioned, the basic control scheme has been established. Some duty cycles in the *dq* frame ($d_{dp}$, $d_{dz}$,$d_{qp}$) have been determined by the control regulator, and the rest duty cycles bring free degree for a modulation signal. In this section, the final modulation scheme will be discussed and the control restriction of the dual-input three-level inverter will be revealed.

### A. PWM Modulation Generator

When four duty cycles $d_{dp}$, $d_{qp}$ $d_{dz}$, $d_{qz}$ are assigned by control scheme, the rest duty cycles in the *dq* frame $d_{dn}$, $d_{qn}$ can be derived by (8). The final modulation signal in the stationary frame can be derived from the duty cycles in the *dq* frame with inverse Park transformation $T^{-1}$

$$\begin{bmatrix} d_{ap} \\ d_{bp} \\ d_{cp} \end{bmatrix} = \sqrt{\frac{2}{3}} \begin{bmatrix} \cos\theta & -\sin\theta & \frac{1}{\sqrt{2}} \\ \cos\left(\theta - \frac{2}{3}\pi\right) & -\sin\left(\theta - \frac{2}{3}\pi\right) & \frac{1}{\sqrt{2}} \\ \cos\left(\theta + \frac{2}{3}\pi\right) & -\sin\left(\theta + \frac{2}{3}\pi\right) & \frac{1}{\sqrt{2}} \end{bmatrix} \begin{bmatrix} d_{dp} \\ d_{qp} \\ d_{0p} \end{bmatrix} \tag{22}$$

$$\begin{bmatrix} d_{an} \\ d_{bn} \\ d_{cn} \end{bmatrix} = \sqrt{\frac{2}{3}} \begin{bmatrix} \cos\theta & -\sin\theta & \frac{1}{\sqrt{2}} \\ \cos\left(\theta - \frac{2}{3}\pi\right) & -\sin\left(\theta - \frac{2}{3}\pi\right) & \frac{1}{\sqrt{2}} \\ \cos\left(\theta + \frac{2}{3}\pi\right) & -\sin\left(\theta + \frac{2}{3}\pi\right) & \frac{1}{\sqrt{2}} \end{bmatrix} \begin{bmatrix} d_{dn} \\ d_{qn} \\ d_{0n} \end{bmatrix}. \tag{23}$$

The zero-sequence duty cycles $d_{0p}$ in (22) and $d_{0n}$ in (23) represent the common-voltage components produced by the upper and low bus, respectively.

The modulation signal generated by (22) and (23) is called dual-input PWM in this paper. The dual-input PWM is more than a specific modulation scheme. The redundant duty cycles bring a free degree in generating a modulation signal. So there are infinite kinds of modulation signals that can be used in the dual-input three-level inverter. It provides the opportunity to choose the best PWM scheme.

### B. Control Restriction for Power Deviation

Total power control restriction in the dual-input three-level inverter is quite similar to that in a conventional inverter. Modulation index is the basic restriction of the total output power. We should pay more attention to control restriction of power deviation in the dual-input three-level inverter. There must be a boundary for the power deviation of two dc input among all possible PWM modulation signals, which can be derived from the duty cycles of each switch.

First, the duty cycle of upper three switches should be between 0 and 1

$$d_{ap}, d_{bp}, d_{cp} \in [0, 1]. \tag{24}$$

Substituting (22) into (24), the restriction of $d_{dp}$ and $d_{qp}$ is

$$\begin{cases} |d_{qp}| \le \dfrac{1}{\sqrt{2}} \\ \left| d_{dp} \pm \dfrac{1}{\sqrt{3}} d_{qp} \right| < \sqrt{\dfrac{2}{3}}. \end{cases} \tag{25}$$

It shows that the vector of $d_{dp}$ and $d_{qp}$ is located in a hexagon, which is similar to the traditional SVM space vector hexagon diagram.

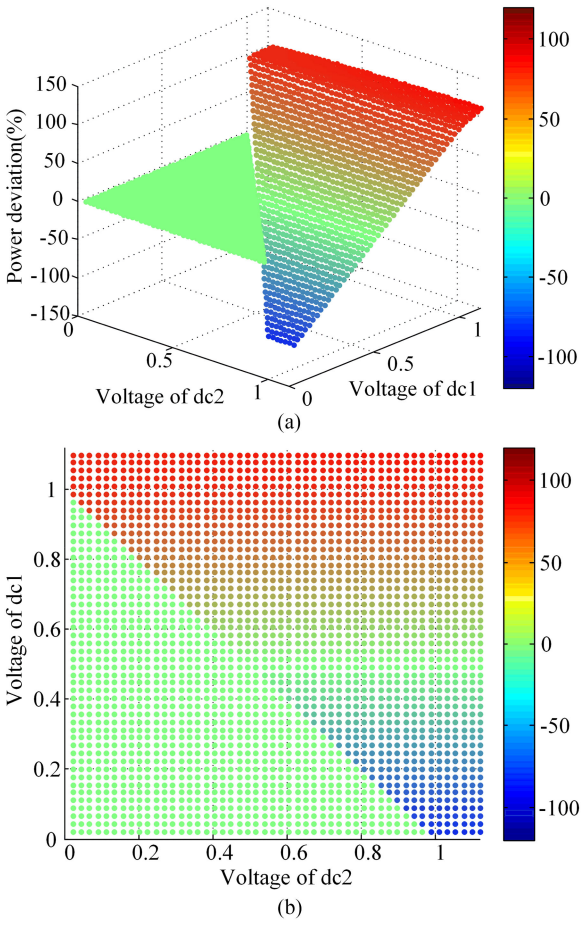


Fig. 10. Maximum limit of the power deviation. (a) 3-D view. (b) *X–Y* view.

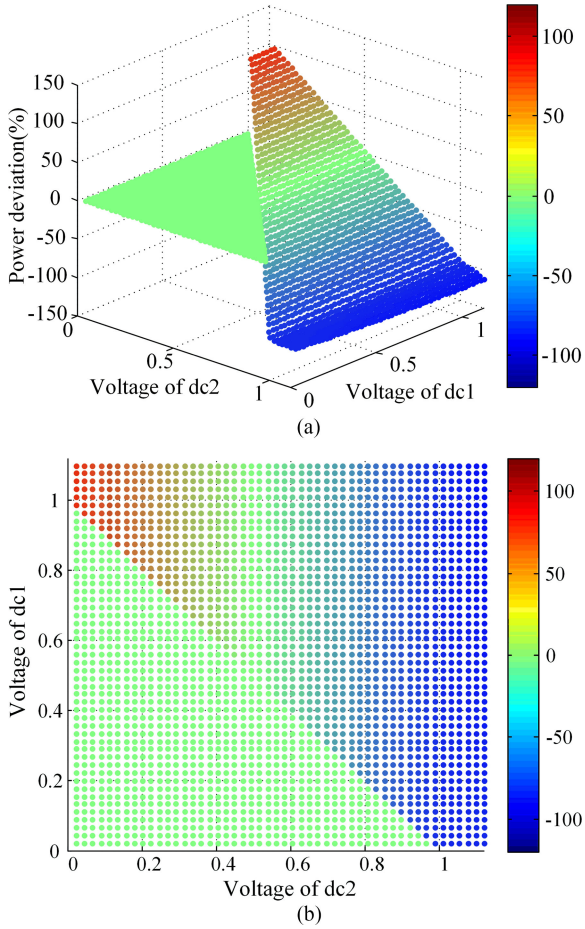


Fig. 11. Minimum limit of the power deviation. (a) 3-D view. (b) *X–Y* view.

Similarly, the boundary of duty cycles $d_{dn}$ and $d_{qn}$ is

$$\begin{cases} |d_{qn}| \le \dfrac{1}{\sqrt{2}} \\ \left| \frac{\sqrt{3}}{2} d_{dn} \pm \frac{1}{2} d_{qn} \right| < \dfrac{1}{\sqrt{2}}. \end{cases} \tag{26}$$

Besides, there is another restriction for the duty cycles, the sum duty cycle of upper and bottom switches for every phase should be between 0 and 1

$$d_{ap} + d_{an}, d_{bp} + d_{bn}, d_{cp} + d_{cn} \in [0, 1]. \tag{27}$$

Equations (25)–(27) are the main restriction for duty cycles; in other words, the power control in the dual-input three-level input is restricted by these equations. According to the boundary of the duty cycle in the *dq* frame and the power deviation of the dual-input written as (10), the boundary of the power deviation is revealed.

Fig. 10 shows the maximum limit of the power deviation in three-dimensional (3-D) space based on two bus voltages ($v_{dc1}$, $v_{dc2}$), the *y*-axis is the voltage of the upper dc-bus voltage $v_{dc1}$, and the *x*-axis is the voltage of the lower dc-bus voltage $v_{dc2}$. The value of $v_{dc1}$ and $v_{dc2}$ in Fig. 10 represents the ratio of dc-bus voltage to output line voltage. In other words, $v_{dc1}$ is equal to 1 in Fig. 10 meaning that $v_{dc1}$ is equal to the amplitude of output line voltage. As shown in the *X–Y* view in Fig. 10(b), when the sum of $v_{dc1}$ and $v_{dc2}$ is below 1, the inverter cannot output essential grid voltage, so it has no ability to regulate the power deviation. When $v_{dc2}$ is fixed, the maximum power deviation is approximately proportional to $v_{dc1}$. And when $v_{dc1}$ is fixed, $v_{dc2}$ has little effect on the maximum power deviation.

Fig. 11 shows the minimum limit of the power deviation in 3-D space based on two bus voltages ($v_{dc1}$, $v_{dc2}$), the *y*-axis is the voltage of the upper dc-bus voltage $v_{dc1}$, and the *x*-axis is the voltage of the lower dc-bus voltage $v_{dc2}$. The value of $v_{dc1}$ and $v_{dc2}$ in Fig. 11 represents the ratio of dc-bus voltage to output line voltage. As shown in the *X–Y* view in Fig. 11(b), when the sum of $v_{dc1}$ and $v_{dc2}$ is below 1, the inverter cannot output essential grid voltage, so it has no ability to regulate the power deviation. When $v_{dc1}$ is fixed, the minimum power deviation is approximately proportional to $v_{dc2}$. And when $v_{dc2}$ is fixed, $v_{dc1}$ has little effect on the minimum power deviation.

The PWM generator contains all possible PWM signals, including traditional PWM methods such as SPWM and SVM. For comparison, traditional PWM methods are taken into considerations, especially. There is an additional restriction for traditional SPWM or SVM. Only one pair of switches is operating in one switching period. In other words, during every switching period,

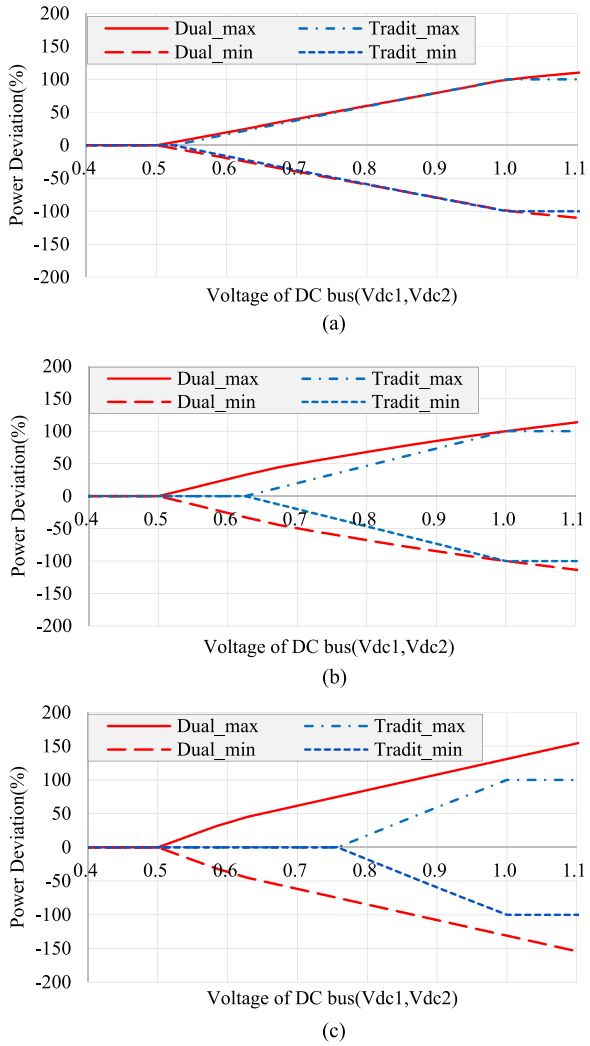


Fig. 12. Power deviation comparison when $v_{dc1}$ is equal to $v_{dc2}$. (a) $\varphi = 0°$. (b) $\varphi = 30°$. (c) $\varphi = 60°$.

there must be

$$\begin{aligned} d_{ap} \cdot d_{an} &= 0 \\ d_{bp} \cdot d_{bn} &= 0 \\ d_{cp} \cdot d_{cn} &= 0. \end{aligned} \tag{28}$$

To prevent complexity in viewing and analysis, Fig. 12 shows the comparison of dual-input PWM and traditional PWM under the situation when $v_{dc1}$ is equal to $v_{dc2}$. The horizontal axis is the voltage of the dc bus. The vertical axis is the power deviation of two inputs. The value of $v_{dc1}$ and $v_{dc2}$ represents the ratio of dc-bus voltage to output line voltage.

Fig. 12(a) shows the situation when the power factor is 1, i.e., the power factor angle $\varphi = 0$. The red and blue lines represent the maximum power deviation of dual-input PWM and traditional PWM, respectively. And the red and blue dash lines represent the minimum power deviation of dual-input PWM and traditional PWM, respectively. If the voltage of half-bus is below 0.5, all PWM modulations cannot be able to work properly for the three-level inverter. It is the same to the conclusion from Figs. 10 and 11. With the increase in the dc voltage, the power deviation capability increases proportionally. The relation between the dc voltage and maximum or minimum power deviation is approximately linear.

As shown in Fig. 12(a), the traditional PWM method power deviation capability is slightly weaker than the dual-input PWM method. One difference is that the lowest controllable dc voltage of dual-input PWM is smaller. The other difference is under the situation when dc voltage is high enough, the maximum power deviation of traditional PWM is equal to 100%. While the maximum power deviation of dual-input PWM can be larger than 100%.

Fig. 12(b) shows the power deviation under the situation when the power factor angle $\varphi$ is 30°. The controllable area of the dual-input PWM method is much larger than that of traditional PWM. The lowest controllable dc voltage $v_{dc1}$ and $v_{dc2}$ in dual-input PWM is around 0.5, while the lowest voltage in traditional PWM is around 0.63. With the increase in the dc voltage, the dual-input PWM method always has a wider controllable range.

Fig. 12(c) shows the power deviation under the situation when the power factor angle $\varphi$ is 60°. The controllable area of the dual-input PWM method is significantly larger than that of traditional PWM. The lowest controllable dc voltage $v_{dc1}$ and $v_{dc2}$ in dual-input PWM is around 0.5, while the lowest voltage in traditional PWM is around 0.76. With the increase in the dc voltage, the dual-input PWM method always has a wider controllable range.

Fig. 13 shows the comparison of dual-input PWM and traditional PWM under a specific situation that $v_{dc1}$ is 20% larger than $v_{dc2}$. The horizontal axis is $v_{dc1}$, while $v_{dc2}$ is 20% less than the voltage of $v_{dc1}$. The value of $v_{dc1}$ and $v_{dc2}$ represents the ratio of dc-bus voltage to output line voltage.

Fig. 13(a) shows the situation when the power factor is 1, i.e., the power factor angle $\varphi = 0$. The red and blue lines represent the maximum power deviation of dual-input PWM and traditional PWM, respectively. And the red and blue dash lines represent the minimum power deviation of dual-input PWM and traditional PWM, respectively. Similar to the situation when $v_{dc1}$ is equal to $v_{dc2}$, if $v_{dc1}$ (horizontal axis) is below 0.55, all PWM modulation cannot be able to work properly for the three-level inverter. With the increase in the dc voltage, the control capability of power deviation increases proportionally. As $v_{dc1}$ is larger than $v_{dc2}$, the control capability of positive power deviation is stronger than that of negative power deviation. For example, when $v_{dc1}$ reaches 1, maximum power deviation of traditional PWM is equal to 100%. On the other hand, minimum power deviation of traditional PWM reaches –100% until $v_{dc1}$ is equal to 1.2 ($v_{dc2}$ is equal to 1). The relationship between the dc voltage and maximum or minimum power deviation is approximately linear. Besides, control capability of the traditional PWM method power deviation is slightly weaker than that of the dual-input PWM method.

Fig. 13(b) shows the power deviation under the situation when the power factor angle $\varphi$ is 30°. The controllable area of the dual-input PWM method is much larger than that of traditional PWM. The lowest controllable dc voltages $v_{dc1}$ and $v_{dc2}$ in dual-input PWM are around 0.55, while the lowest voltage in traditional PWM is around 0.69. With the increase in the dc voltage, the

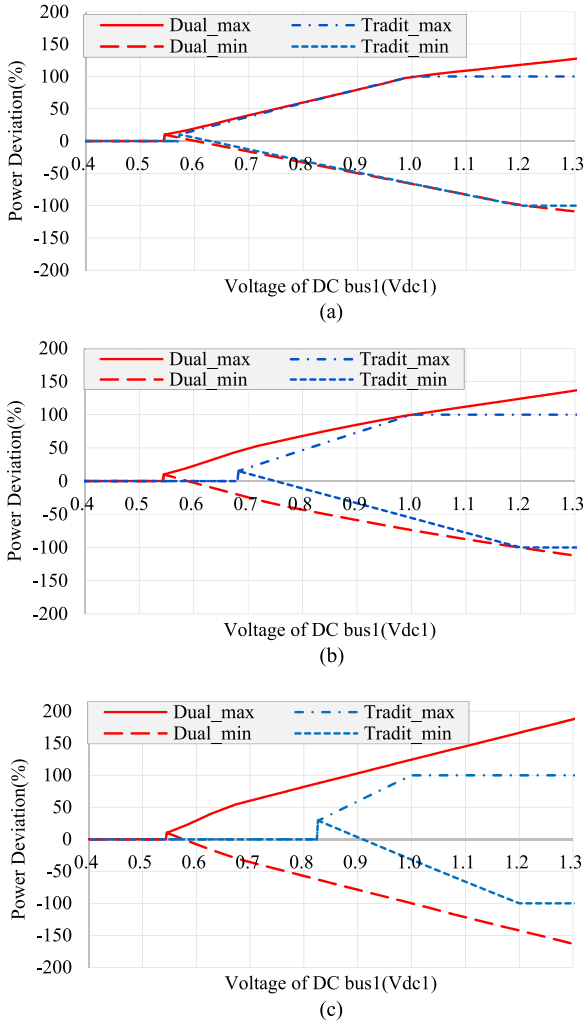


Fig. 13. Power deviation comparison when $v_{dc1}$ is 20% larger than $v_{dc2}$. (a) $\varphi = 0°$. (b) $\varphi = 30°$. (c) $\varphi = 60°$.

dual-input PWM method always has a wider controllable range. Besides, as $v_{dc1}$ is larger than $v_{dc2}$, the control capability of positive power deviation is stronger than that of negative power deviation.

Fig. 13(c) shows the power deviation under the situation when the power factor angle $\varphi$ is 60°. The controllable area of the dual-input PWM method is significantly larger than that of traditional PWM. With the increase in the dc voltage, the dual-input PWM method always has a wider controllable range. Besides, as $v_{dc1}$ is larger than $v_{dc2}$, the control capability of positive power deviation is stronger than that of negative power deviation.

One drawback of the dual-input PWM method is that the number of turn-ON and turn-OFF switching transient may slightly increase in every switching frequency period. But it is quite effective to enhance the control capability of power deviation. So in some extraordinary operation situation, such as PV application, when the PV panels are partially shadowed, large unbalance power deviation of two input arrays appears in dual-input PWM. Though the switching loss may increase, more PV energy can be harvested.

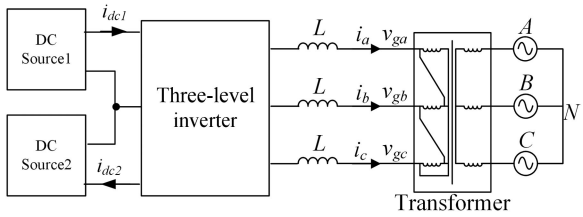


Fig. 14. Experimental system.

TABLE I
PARAMETERS OF THE DUAL-INPUT INVERTER

| Parameters | Value |
|---|---|
| Rated power | 125kW |
| Switching frequency | 5kHz |
| Grid voltage | 315V/50Hz |
| Filter Inductance | 0.05mH |
| Upper and lower DC capacitance | 1260uF |

TABLE II
PARAMETERS OF THE PV ARRAY

| Parameters | Value |
|---|---|
| Open circuit voltage | 350V |
| Short circuit current | 25A |
| MPP voltage | 271.6V |
| MPP current | 22.1A |
| MPP power | 6kW |

For practical application, when the inverter is operating under a normal condition, the three-level inverter can operate with PWM with less switching times, which is similar to SPWM or SVM, and when the required power deviation exceeds its controllable limit, the three-level inverter can transit into dual-input PWM with more switching times to enhance the control capability of power deviation.

## V. EXPERIMENTAL RESULTS

The implementation is carried out on a 125 kW T-type three-level PV inverter to verify the proposed control method. Fig. 14 shows the experimental system and its main parameters are listed in Table I.

The dual-input PV arrays of the three-level inverter are produced by two Chroma dc power supply 62150H-1000s. Each one operates as a PV array listed in Table II.

Fig. 15 shows the steady-state waveform with the proposed method at 20 kW. The dc voltages $v_{dc1}$, $v_{dc2}$ and currents $i_{dc1}$, $i_{dc2}$ are constant without low-frequency fluctuation, while switching frequency of dc current exists, and $i_a$, $i_b$, $i_c$ are the grid current with low total harmonic distortion (THD), so the power of DC1 and DC2 is controlled to be constant with high output power quality.

Fig. 15(a) shows the steady waveform when voltages of dc1 and dc2 are the same. Channels 1 and 2 are the voltage of dc1 and dc2, channels 3–5 are the three-phase grid current. The voltages of dc1 and dc2 are both 320 V. The three-phase grid current is symmetrical, and the power quality is as good as that under

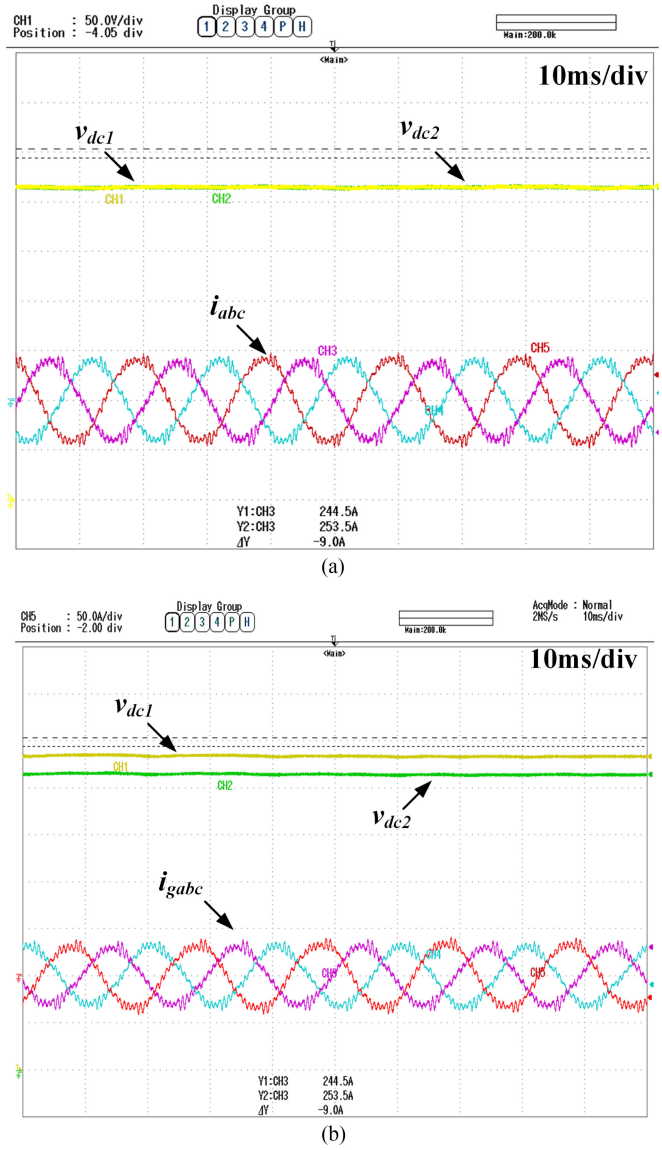


Fig. 15. Steady waveform [$v_{dc1}$ (50 V/div, center 200 V), $v_{dc2}$ (50 V/div, center 200 V), $i_{dc1}$ (12 A/div, center 0 A), $i_{dc2}$ (12 A/div, center 0 A), and $i_{abc}$ (20 A/div, center $-40$ A)]. (a) With the same dc voltage. (b) With different dc voltages.

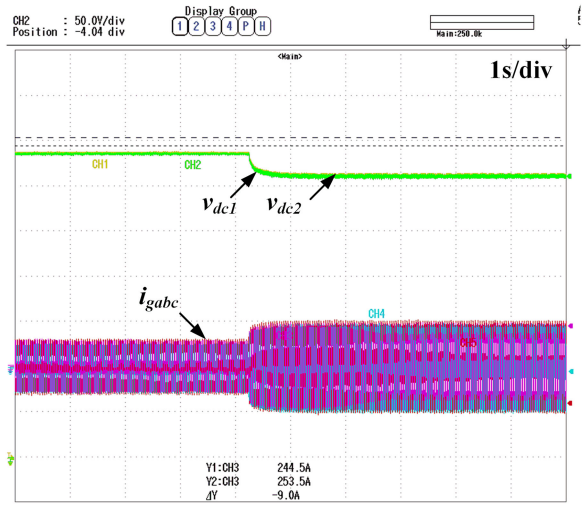


Fig. 16. Total voltage control [$v_{dc1}$ (50 V/div, center 200 V), $v_{dc2}$ (50 V/div, center 200 V), $i_{dc1}$ (12 A/div, center 0 A), $i_{dc2}$ (12 A/div, center 0 A), and $i_{abc}$ (20 A/div, center $-40$ A)].

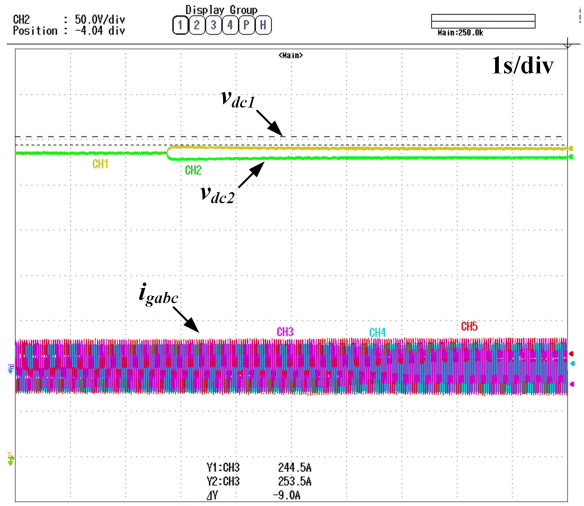


Fig. 17. Different voltage controls [$v_{dc1}$ (50 V/div, center 200 V), $v_{dc2}$ (50 V/div, center 200 V), $i_{dc1}$ (12 A/div, center 0 A), $i_{dc2}$ (12 A/div, center 0 A), and $i_{abc}$ (20 A/div, center $-40$ A)].

traditional control with single PV input. Besides, there is nearly none of the low-frequency oscillation on half bus voltage.

Fig. 15(b) shows the steady waveform when the voltage of dc1 is higher than the voltage of dc2 by 20 V. The three-phase grid current is symmetrical, and the power quality is as good as that under traditional control with single PV input. Besides, there is nearly none of the low-frequency oscillation on single dc1 or dc2 voltage. So the control method will not affect the steady performance of the three-level inverter.

Fig. 16 shows the dynamic voltage control waveform when both voltages of dc1 and dc2 are changed. At time $t_0$ in Fig. 16, the voltages of dc1 and dc2 are controlled from 340 to 320 V at the same time. It can be seen that the control speed of $v_{dc1}$ and $v_{dc2}$ is almost the same. The control time is around 100 ms. When the voltages of dc1 and dc2 are controlled toward MPP, the grid current increases with the decrease in voltage and increase in output power. There is no surge in voltage and current. The total voltage control is implemented.

Fig. 17 shows the dynamic voltage control waveform when the voltage of dc1 increases and dc2 decreases. The control performance is similar to that of total voltage control. The control speed of $v_{dc1}$ and $v_{dc2}$ is almost the same. There is no surge on voltage and current. The different voltage controls are implemented.

Fig. 18 shows the performance of single voltage control of PV1. At time $t_0$, the voltage of dc1 is reduced by 20 V, while the voltage of dc2 keeps constant. The working point of PV1 alters with the decrease in voltage and the increase in current. Meanwhile, the operation state of dc2 keeps the same. Both current and voltage of PV2 are not changed.

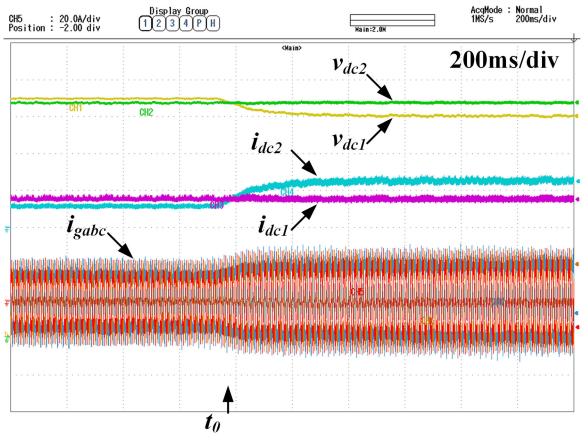


Fig. 18. Voltage control of PV1 [$v_{dc1}$ (50 V/div, center 150 V), $v_{dc2}$ (50 V/div, center 150 V), $i_{pv1}$ (12 A/div, center 0 A), $i_{pv2}$ (12 A/div, center 0 A), and $i_{abc}$ (20 A/div, center $-40$ A)].

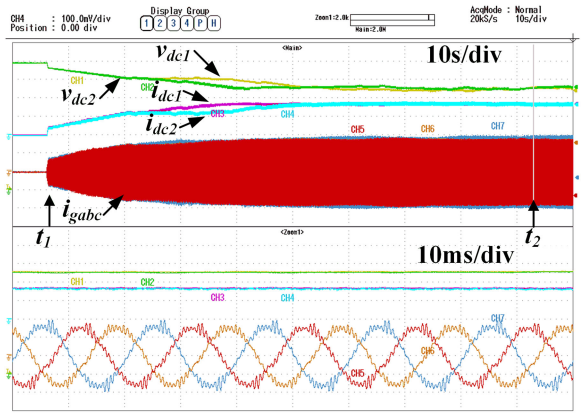


Fig. 19. Waveform with the same PV array [$v_{dc1}$ (50 V/div, center 150 V), $v_{dc2}$ (50 V/div, center 150 V), $i_{pv1}$ (12 A/div, center 0 A), $i_{pv2}$ (12 A/div, center 0 A), and $i_{abc}$ (20 A/div, center $-40$ A)].

Fig. 19 shows the MPPT waveform of dual PV input. Both PV1 and PV2 are set as Table II. The maximum point power is 6 kW. At time $t_1$, the three-level inverter is connected to the grid, and the grid current increases. The voltage controller with MPPT is working properly. Both voltages of DC1 and DC2 can be tracked down to the MPP. At last time $t_2$ in Fig. 19, each PV array works at its MPP. The bottom of Fig. 19 is the enlarged waveform of time $t_2$. The grid current is controlled with good quality.

Fig. 20 shows the tacking path of PV1 and PV2 with the same PV array. The blue and red dots are the working state of PV1 and PV2 every 2 s. The slash lines are the *P–V* curve of PV1 and PV2 in theory. The three-level input can track both of the PV arrays for upper and lower dc side. The power of PV1 and PV2 is 6 kW as expected. The dual-input three-level inverter can work effectively to achieve maximum power from two-series PV array with power deviation.

Fig. 21 shows the MPPT waveform of dual PV inputs. PV1 is set as Table II. PV2 is set operating at 80% illumination in Table II. Its maximum power is 4.8 kW. At time $t_1$, the three-level inverter is connected to the grid, the voltage controller with

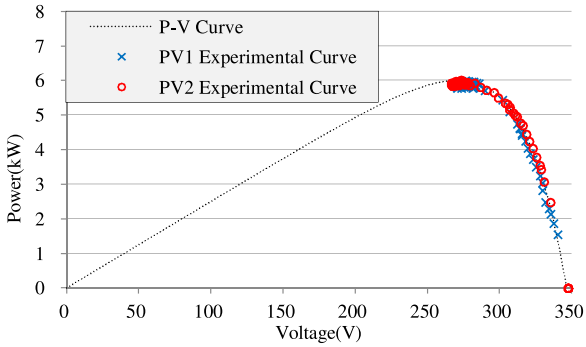


Fig. 20. Comparison of experiment curve and designed *P–V* curve with the same dual PV array.

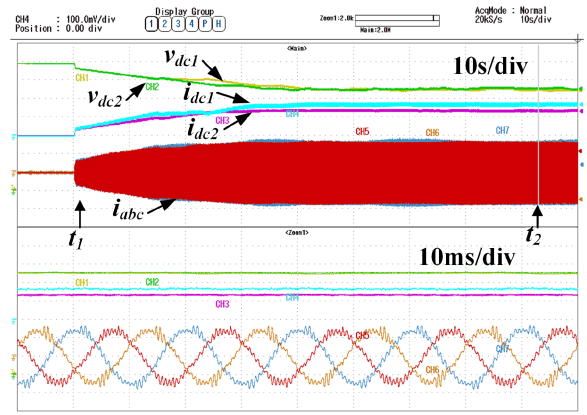


Fig. 21. Waveform with the same PV array [$v_{dc1}$ (50 V/div, center 150 V), $v_{dc2}$ (50 V/div, center 150 V), $i_{pv1}$ (12 A/div, center 0 A), $i_{pv2}$ (12 A/div, center (0 A), and $i_{abc}$ (20 A/div, center $-$ 40 A)].

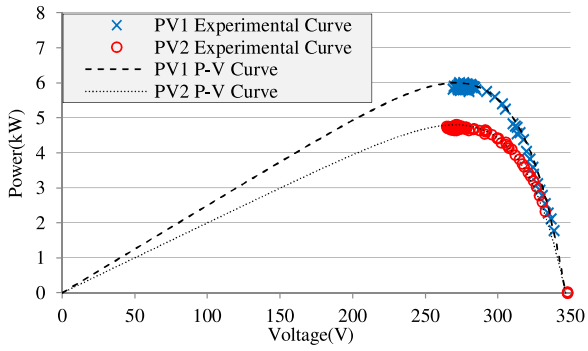


Fig. 22. Comparison of experiment curve and designed *P–V* curve with different PV arrays.

MPPT is working, and both voltages of DC1 and DC2 can be tracked down to the MPP. At last time $t_2$ in Fig. 21, each PV array works at its MPP. The bottom of Fig. 21 is the enlarged waveform of time $t_2$. The grid current is controlled with good quality.

Fig. 22 shows the tacking path of PV1 and PV2, and the blue and red dots are the working state of PV1 and PV2 every 2 s. The slash lines are the *P–V* curve of PV1 and PV2 in theory. The three-level input can track both of the PV arrays for upper and lower dc side. The dual-input three-level inverter can work

effectively to achieve the maximum power from the two-series PV array with power deviation.

From the experimental results, the voltage of PV1 and PV2 can be controlled separately. Each PV array can reach its MPP when the PV arrays are operating under different circumstances. More power is harvested with good power quality.

## VI. Conclusion

This paper proposed a general control scheme for the dual-input three-level inverter. A dynamic model of the dual-input three-level inverter is established, which represents the relationship between the voltage/power and specific duty cycle. With the proposed method, dual-input voltages of the three-level inverter can be controlled independently with good quality of grid current. Each PV array can achieve its maximum power when the PV arrays are operating under different circumstances. It increases energy harvesting for the PV array. Besides, modulation and restriction of the proposed method are discussed. The power deviation control capability of dual-input PWM is much stronger than that of traditional PWM.

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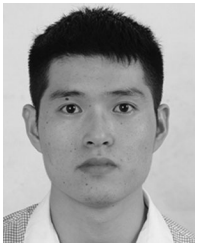

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