A Three-Phase Active Rectifier Topology for Bipolar DC Distribution

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***Abstract*—A new three-phase active rectifier topology is proposed for bipolar dc distribution, which can achieve the independent dc-pole control, with only one two-level voltage source converter and an ac-side grounding inductor. The averaged large-signal model and linearized small-signal model of the rectifier are derived in the stationary reference frame. Moreover, a control system is proposed with proper controller parameters. Besides, the rectifier is tested on an experiment platform. Comprehensive experiment results are given and analyzed to validate the function of the proposed rectifier under different operation conditions, including the rectifier start-up performance, rectifier dynamics with unbalanced dc loads for two poles, and rectifier dynamics with asymmetrical dc voltages for two poles. Finally, the proposed rectifier is compared with other two existing ac–dc conversion approaches, in terms of required number and rating of components as well as power losses with different load imbalance levels, which further highlight some potential benefits of the proposed topology.**

***Index Terms*—AC–DC power converters, current control, inductors, modeling, power distribution.**

I. Introduction

THE use of dc in high power applications is growing over the years as better power semiconductors become available and potential solutions to the main technical challenges of dc power systems (e.g., efficient ac–dc [1] and dc–dc [2] conversion, fault dc current interruption [3]). For example, the voltage-source-converter high-voltage dc (VSC-HVDC) transmission technology has undergone a rapid growth over the past decade [1], and low-voltage dc (LVDC) is used in kilowatt-scale applications for power trains [4] and charging systems in electric vehicles [5]. With the number of power-electronic-interfaced loads and generation systems increasing over the years, the idea of using dc in low-voltage distribution is gaining interest. Some of the potential benefits of the dc distribution are [6]–[13]: 1) no need for reactive current; 2) easier interfacing of certain loads such as LED lighting, battery storage, variable speed drives, and photovoltaic; 3) more power-dense converters; and 4) simpler voltage regulation and power balancing control.

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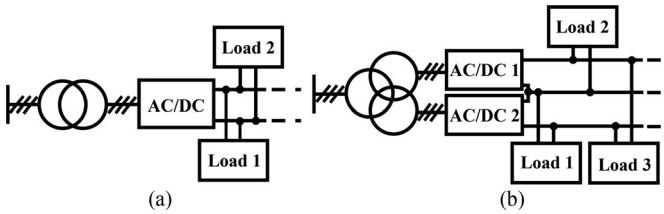

Fig. 1. Examples of dc distribution systems. (a) Unipolar dc systems. (b) Bipolar dc systems.

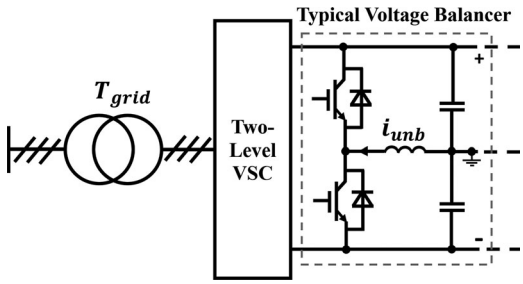

Fig. 2. Two-level voltage-source converter with a voltage balancer.

There are two types of dc distribution systems [13]: unipolar distribution and bipolar distribution, as shown in Fig. 1. This paper focuses on the bipolar system due to its prominent advantages. A bipolar dc system can provide different voltage levels to loads in a similar way as a three-phase ac system does [13]. Meanwhile, the reliability is increased due to the two available poles [9], [11]. Moreover, the grounding for bipolar distribution is also better and simpler than that of the unipolar distribution, because the faults can be easily detected and quickly cleared, and an unambiguous pole-to-ground voltage can be defined [13], [14].

However, as shown in Fig. 1(b), a bipolar dc system is normally implemented using two rectifiers in series at dc side in order to handle possible unbalanced loads. This in turns requires double secondary windings in the transformer rated to withstand a dc voltage offset caused by the series connection. Some novel ideas have been proposed to solve this problem in [5], [11], [15], and [16]. For these approaches, one converter is used only, however, with the help of a voltage balancer (or the forth bridge), which still requires extra power switches, as shown in Fig. 2. Besides, the voltage balancer also consumes power and needs extra auxiliary systems. Here a new rectifier topology is

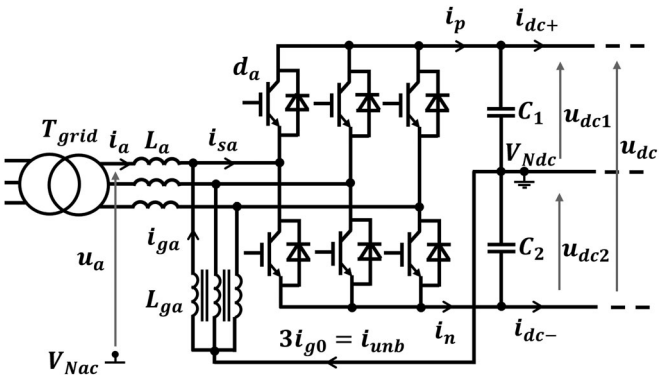

Fig. 3. Proposed rectifier topology.

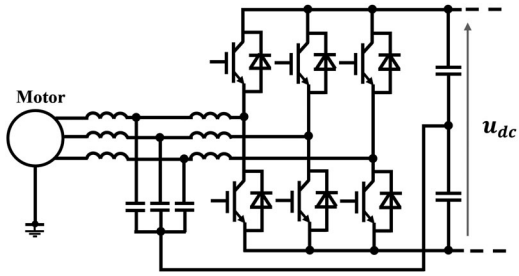

Fig. 4. Virtually-grounded voltage-source converter.

proposed, which is constructed based on a two-level VSC with an ac-side grounding reactor, as shown later in Section II.

This paper is organized as follows: Section II introduces the proposed rectifier topology. Section III gives the detailed derivation of the rectifier large- and small-signal models, followed by a proposed control system. The experiment results of the proposed rectifier are illustrated and analyzed in Section IV. Then in Section V, the proposed rectifier is compared with other two existing ac–dc conversion approaches for bipolar dc distribution.

II. Rectifier Topology Overview

The proposed rectifier topology is shown in Fig. 3. The basic idea is to provide a current-injection path from the ac side to the dc-side neutral line by a grounding inductor (i.e., L_g), so that the dc bus voltages for positive and negative poles (i.e., $u_{\rm dc1}$ and $u_{\rm dc2}$) can be controlled independently. When the loads are perfectly balanced, the rectifier behaves like a conventional active rectifier, and no dc current is injected through the grounding reactor. When the loads are unbalanced, zero-sequence dc current flows through the grounding reactor in order to maintain the voltage balance between two dc poles.

It is worth noting that the proposed topology has certain similarities with the one proposed in [17], [18], as shown in Fig. 4, where the ac side is connected to the middle point of dc bus by using capacitors. This topology provides a path for the high-frequency current in order to alleviate the dv/dt stress at motor terminals. Besides, the grounding capacitors can also be used to help with the balance of dc-bus capacitors in a three-level neutral-point-clamped (NPC) VSC [19], as shown in Fig. 5. However, when feeding unbalanced dc loads, compared with

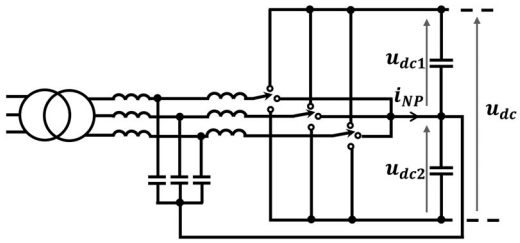

Fig. 5. Virtually-grounded three-level voltage-source converter.

the dc path given by the grounding inductor (see Fig. 3), the dc current in the NPC VSC (see Fig. 5) cannot flow through the virtually-grounded path due to the blocking of capacitors, and has to be injected through the clamped-neutral point (i.e., $i_{\rm NP}$). But as discussed in [5], [20], and [21], for ensuring a high modulation index and avoiding the over modulation, the unbalanced power provided by $i_{\rm NP}$ is quite limited, which makes the NPC VSC only possible to handle the imbalance of dc-bus capacitors, but unfit for the bipolar operation with unbalanced dc loads, unless a forth bridge is added.

III. Rectifier Model and Control System

Pulse width modulation (PWM) is widely used to generate the switching signals in VSCs, which is also used for the proposed rectifier topology in this paper. Different modeling techniques for three-phase two-level PWM VSCs have been discussed in the past [22]–[24]. These approaches are often originally meant for VSCs where the zero-sequence current could be considered to be zero. However, the proposed rectifier in Fig. 3 has an ac-side grounding reactor connected to the dc bus, which enables the zero-sequence current to flow from the branches of the rectifier. This makes the aforementioned models unfit. Hence, the large- and small-signal models of the proposed rectifier are derived next.

A. Stationary Reference Frame

Three variable reference frames are normally used when analyzing the dynamics of three-phase VSCs and designing their controllers [25]: natural (*abc*) frame, stationary reference ($\alpha\beta 0$) frame, and synchronous rotating (*dq0*) frame. The operation of the proposed rectifier requires zero-sequence current control through a grounding reactor, which benefits the use of the $\alpha\beta 0$ and *dq0* variables over *abc*. Further, *dq0* control requires the cross decoupling of currents in *d*- and *q*-axis, but the zero-sequence current in *dq0* frame is exactly same to that of $\alpha\beta 0$ frame. This gives no superiority but more complexities to *dq0* frame. Therefore, $\alpha\beta 0$ frame will be used for the current control. A *PR* controller can be used to eliminate the tracking error of the sinusoidal current in $\alpha\beta 0$ frame [26].

B. Voltage Equations for Source Inductors

The reference directions of currents and voltages are displayed in Fig. 3. (For the ac side, only the physical quantities of phase *a* are demonstrated.)

If the source inductors for three phases are exactly same, i.e., $L_a = L_b = L_c = L$ and $R_a = R_b = R_c = R$, then the average voltage equations for them are

$$\begin{bmatrix} u_a \\ u_b \\ u_c \end{bmatrix} = R \begin{bmatrix} i_a \\ i_b \\ i_c \end{bmatrix} + L\frac{d}{dt}\begin{bmatrix} i_a \\ i_b \\ i_c \end{bmatrix} + \begin{bmatrix} d_a \\ d_b \\ d_c \end{bmatrix} u_{\mathrm{dc}} - \begin{bmatrix} 1 \\ 1 \\ 1 \end{bmatrix} u_{\mathrm{dc2}} + \begin{bmatrix} 1 \\ 1 \\ 1 \end{bmatrix} V_N \quad (1)$$

where d_a, d_b, and d_c are the duty cycles for three-phase high-side power switches; $V_N = V_{\mathrm{Ndc}} - V_{\mathrm{Nac}}$ is the voltage difference between the neutral points of dc and ac sides. By adding the three-phase equations together, the following expression is found:

$$\sum_{k=a,b,c} u_k = R \sum_{k=a,b,c} i_k + L\frac{d}{dt}\sum_{k=a,b,c} i_k + u_{\mathrm{dc}} \sum_{k=a,b,c} d_k - 3u_{\mathrm{dc2}} + 3V_N. \quad (2)$$

Further, if the grid-interface transformer is in delta connection (or in star connection with a floating neutral) on the converter side, the transformer will not have the zero-sequence current, i.e., $i_0 = 0$, which leads to

$$V_N = -u_{\mathrm{dc}} d_0 + u_{\mathrm{dc2}} + u_0 \quad (3)$$

where d_0 is the zero-sequence duty cycle for each high-side power switch; and u_0 is the zero-sequence grid voltage. The voltage equations for source inductors can be rewritten by combining (1) and (3):

$$\begin{bmatrix} u_a \\ u_b \\ u_c \end{bmatrix} = R \begin{bmatrix} i_a \\ i_b \\ i_c \end{bmatrix} + L\frac{d}{dt}\begin{bmatrix} i_a \\ i_b \\ i_c \end{bmatrix} + \begin{bmatrix} d_a - d_0 \\ d_b - d_0 \\ d_c - d_0 \end{bmatrix} u_{\mathrm{dc}} + \begin{bmatrix} 1 \\ 1 \\ 1 \end{bmatrix} u_0. \quad (4)$$

By applying the Clarke transformation to this equation, voltage equations in $\alpha\beta 0$ frame are obtained as follows:

$$\begin{bmatrix} u_\alpha \\ u_\beta \end{bmatrix} = R \begin{bmatrix} i_\alpha \\ i_\beta \end{bmatrix} + L\frac{d}{dt}\begin{bmatrix} i_\alpha \\ i_\beta \end{bmatrix} + \begin{bmatrix} d_\alpha \\ d_\beta \end{bmatrix} u_{\mathrm{dc}} \quad (5)$$

where the zero-sequence equation is removed as $i_0 = 0$.

C. Voltage Equations for Grounding Inductors

Clearly, grounding inductors would see the full ac voltages and hold sustained ac currents, which would incur unnecessary losses. Increasing the inductance value is a natural idea to limit these currents. However, large inductance also results in very slow response of the zero-sequence current, which has negative effects for the current injection and the control of the two dc poles. Besides, if three independent inductors were used, the need to carry high dc current would make their core sizing costly due to the high dc flux. Alternatively, a coupled structure is used for the grounding reactor, i.e., the three-phase windings are wound at a balanced three-phase magnetic core, as shown in Fig. 6 [27]. In this case, the inductor core cannot carry the zero-sequence dc flux, which reduces the chances for core saturation, similarly to what happens in the design of cores for dc chokes. Meanwhile, the inductance of the zero sequence can be much lower than those of α and β sequences. The inductance matrix for the coupled reactor is of the form:

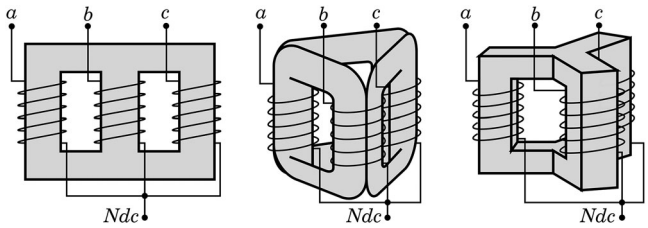

Fig. 6. Examples of suitable core shapes with low zero-sequence impedance.

$$L_{g,\mathrm{abc}} = \begin{bmatrix} L_g & -M_g & -M_g \\ -M_g & L_g & -M_g \\ -M_g & -M_g & L_g \end{bmatrix}. \quad (6)$$

By applying the Clarke transformation

$$L_{g,\alpha\beta 0} = \begin{bmatrix} L_{g\alpha} & 0 & 0 \\ 0 & L_{g\beta} & 0 \\ 0 & 0 & L_{g0} \end{bmatrix} = \begin{bmatrix} L_g + M_g & 0 & 0 \\ 0 & L_g + M_g & 0 \\ 0 & 0 & L_g - 2M_g \end{bmatrix}. \quad (7)$$

Similarly, the winding resistors in *abc* and $\alpha\beta 0$ frames are represented by $R_{g,\mathrm{abc}}$ and $R_{g,\alpha\beta 0}$, respectively.

The average voltage equations for coupled grounding inductors are

$$\begin{bmatrix} 0 \\ 0 \\ 0 \end{bmatrix} = R_{g,\mathrm{abc}} \begin{bmatrix} i_{\mathrm{ga}} \\ i_{\mathrm{gb}} \\ i_{\mathrm{gc}} \end{bmatrix} + L_{g,\mathrm{abc}}\frac{d}{dt}\begin{bmatrix} i_{\mathrm{ga}} \\ i_{\mathrm{gb}} \\ i_{\mathrm{gc}} \end{bmatrix} + u_{\mathrm{dc}} \begin{bmatrix} d_a - \frac{1}{2} \\ d_b - \frac{1}{2} \\ d_c - \frac{1}{2} \end{bmatrix} + \frac{1}{2}\Delta u \begin{bmatrix} 1 \\ 1 \\ 1 \end{bmatrix} \quad (8)$$

with

$$\Delta u = u_{\mathrm{dc1}} - u_{\mathrm{dc2}}. \quad (9)$$

By applying the Clarke transformation

$$\begin{bmatrix} 0 \\ 0 \\ 0 \end{bmatrix} = R_{g,\alpha\beta 0} \begin{bmatrix} i_{g\alpha} \\ i_{g\beta} \\ i_{g0} \end{bmatrix} + L_{g,\alpha\beta 0}\frac{d}{dt}\begin{bmatrix} i_{g\alpha} \\ i_{g\beta} \\ i_{g0} \end{bmatrix} + u_{\mathrm{dc}} \begin{bmatrix} d_\alpha \\ d_\beta \\ d_0 - \frac{1}{2} \end{bmatrix} + \begin{bmatrix} 0 \\ 0 \\ \frac{1}{2}\Delta u \end{bmatrix}. \quad (10)$$

TABLE I
AVERAGED LARGE-SIGNAL EQUATIONS IN STATIONARY REFERENCE FRAME

Voltage Equations for Source Inductors	$\begin{bmatrix} u_\alpha \\ u_\beta \end{bmatrix} = R \begin{bmatrix} i_\alpha \\ i_\beta \end{bmatrix} + L \frac{d}{dt} \begin{bmatrix} i_\alpha \\ i_\beta \end{bmatrix} + \begin{bmatrix} d_\alpha \\ d_\beta \end{bmatrix} u_{\mathrm{dc}}$
Voltage Equations for Grounding Inductors	$\begin{bmatrix} 0 \\ 0 \\ 0 \end{bmatrix} = R_{g,\alpha\beta 0} \begin{bmatrix} i_{g\alpha} \\ i_{g\beta} \\ i_{g0} \end{bmatrix} + L_{g,\alpha\beta 0} \frac{d}{dt} \begin{bmatrix} i_{g\alpha} \\ i_{g\beta} \\ i_{g0} \end{bmatrix} + u_{\mathrm{dc}} \begin{bmatrix} d_\alpha \\ d_\beta \\ d_0 - \frac{1}{2} \end{bmatrix} + \begin{bmatrix} 0 \\ 0 \\ \frac{1}{2}\Delta u \end{bmatrix}$
Current Equations for High-Side Capacitor	$C_1 \frac{du_{\mathrm{dc1}}}{dt} = i_p - i_{\mathrm{dc}+}$ with $i_p = 3d_0\, i_{s0} + \frac{3}{2}(d_\alpha i_{s\alpha} + d_\beta i_{s\beta})$
Current Equations for Low-Side Capacitor	$-C_2 \frac{du_{\mathrm{dc2}}}{dt} = i_n - i_{\mathrm{dc}-}$ with $i_n = 3i_{g0} - i_p$

When ignoring the switching harmonics of i_{g0} and the zero-sequence inner resistance R_{g0} of the grounding inductor, the steady state relationship between d_0 and Δu can be derived as

$$d_0 = \frac{1}{2} - \frac{\Delta u}{2u_{\mathrm{dc}}} \tag{11}$$

which leads to $d_0 = 0.5$ at steady state if no dc voltage imbalance is desired (i.e., $\Delta u = 0$).

D. Current Equations for DC Capacitors

The average current equation for the high-side capacitor is

$$C_1 \frac{du_{\mathrm{dc1}}}{dt} = i_p - i_{\mathrm{dc}+} \tag{12}$$

with

$$i_p = d_a\, i_{\mathrm{sa}} + d_b i_{\mathrm{sb}} + d_c i_{\mathrm{sc}}. \tag{13}$$

For transferring this current equation in $\alpha\beta 0$ frame, we note that

$$i_p = \begin{bmatrix} d_a \\ d_b \\ d_c \end{bmatrix}^T \cdot \begin{bmatrix} i_{\mathrm{sa}} \\ i_{\mathrm{sb}} \\ i_{\mathrm{sc}} \end{bmatrix} = \begin{bmatrix} d_a \\ d_b \\ d_c \end{bmatrix}^T \left(C_{3s\to 2s}^{-1} C_{3s\to 2s}\right) \begin{bmatrix} i_{\mathrm{sa}} \\ i_{\mathrm{sb}} \\ i_{\mathrm{sc}} \end{bmatrix}. \tag{14}$$

where $C_{3s\to 2s}$ is the matrix for the Clarke transformation. By investigating the matrix $C_{3s\to 2s}^{-1}$, we get

$$\left\{ \left(C_{3s\to 2s}^{-1}\right)^T \begin{bmatrix} d_a \\ d_b \\ d_c \end{bmatrix} \right\}^T = \frac{3}{2} \begin{bmatrix} d_\alpha \\ d_\beta \\ 2d_0 \end{bmatrix}^T. \tag{15}$$

Therefore, the current equation in $\alpha\beta 0$ frame is

$$\begin{aligned} C_1 \frac{du_{\mathrm{dc1}}}{dt} &= \frac{3}{2} \begin{bmatrix} d_\alpha \\ d_\beta \\ 2d_0 \end{bmatrix}^T \cdot \begin{bmatrix} i_{s\alpha} \\ i_{s\beta} \\ i_{s0} \end{bmatrix} - i_{\mathrm{dc}+} \\ &= 3d_0\, i_{s0} + \frac{3}{2}(d_\alpha i_{s\alpha} + d_\beta i_{s\beta}) - i_{\mathrm{dc}+}. \end{aligned} \tag{16}$$

Similarly, the current equation for low-side capacitor can be derived as

$$-C_2 \frac{du_{\mathrm{dc2}}}{dt} = i_n - i_{\mathrm{dc}-} \tag{17}$$

with

$$i_n = 3i_{g0} - i_p = 3i_{g0} - d_a i_{\mathrm{sa}} - d_b i_{\mathrm{sb}} - d_c i_{\mathrm{sc}} \tag{18}$$

and in $\alpha\beta 0$ frame

$$\begin{aligned} -C_2 \frac{du_{\mathrm{dc2}}}{dt} &= 3i_{g0} - \frac{3}{2} \begin{bmatrix} d_\alpha \\ d_\beta \\ 2d_0 \end{bmatrix}^T \cdot \begin{bmatrix} i_{s\alpha} \\ i_{s\beta} \\ i_{s0} \end{bmatrix} - i_{\mathrm{dc}-} \\ &= 3(1-d_0)\, i_{s0} - \frac{3}{2}(d_\alpha i_{s\alpha} + d_\beta i_{s\beta}) - i_{\mathrm{dc}-}. \end{aligned} \tag{19}$$

E. Conclusions of Rectifier Modeling

The averaged large-signal equations in (5), (10), (16), and (19) are resummarized in Table I. By applying the perturbation and linearization [28] to these equations, the linearized small-signal equations can be obtained, as summarized in Table II.

In order to facilitate the control system design and the rectifier analysis, the zero-biased duty cycle s (i.e., with a range from –0.5 to 0.5) is used to replace the duty cycle d (i.e., with a range from 0 to 1). The relationship between them is

$$\begin{cases} d_a = s_a + 0.5 \\ d_b = s_b + 0.5 \\ d_c = s_c + 0.5 \end{cases} \text{and} \begin{cases} d_\alpha = s_\alpha \\ d_\beta = s_\beta \\ d_0 = s_0 + 0.5. \end{cases} \tag{20}$$

Based on the derived equations, the large- and small-signal models in $\alpha\beta 0$ frame are constructed, as shown in Figs. 7 and 8, respectively, where

$$u_{g0} = s_0 u_{\mathrm{dc}} + \frac{1}{2}\Delta u \tag{21}$$

and

$$\begin{cases} \hat{u}_{g1} = S_0 \hat{u}_{\mathrm{dc}} + \frac{1}{2}\Delta\hat{u} \\ \hat{u}_{g2} = S_0 U_{\mathrm{dc}} + \frac{1}{2}\Delta U + \hat{s}_0 U_{\mathrm{dc}}. \end{cases} \tag{22}$$

F. Proposed Control Structure

Based on the linearized small-signal model, a control structure is proposed, as shown in Fig. 9, which includes: 1) an outer loop for the dc-bus voltage control, with an inner loop for the

TABLE II
LINEARIZED SMALL-SIGNAL EQUATIONS IN STATIONARY REFERENCE FRAME

Voltage Equations for Source Inductors	$\begin{bmatrix}\hat{u}_\alpha\\ \hat{u}_\beta\end{bmatrix}=\begin{bmatrix}R_\alpha & 0\\ 0 & R_\beta\end{bmatrix}\begin{bmatrix}\hat{\imath}_\alpha\\ \hat{\imath}_\beta\end{bmatrix}+\begin{bmatrix}L_\alpha & 0\\ 0 & L_\beta\end{bmatrix}\frac{d}{dt}\begin{bmatrix}\hat{\imath}_\alpha\\ \hat{\imath}_\beta\end{bmatrix}+U_{dc}\begin{bmatrix}\hat{s}_\alpha\\ \hat{s}_\beta\end{bmatrix}+\hat{u}_{dc}\begin{bmatrix}S_\alpha\\ S_\beta\end{bmatrix}$
Voltage Equations for Grounding Inductors	$\begin{bmatrix}0\\0\\0\end{bmatrix}=\begin{bmatrix}R_{g\alpha} & 0 & 0\\ 0 & R_{g\beta} & 0\\ 0 & 0 & R_{g0}\end{bmatrix}\begin{bmatrix}\hat{\imath}_{g\alpha}+I_{g\alpha}\\ \hat{\imath}_{g\beta}+I_{g\beta}\\ \hat{\imath}_{g0}+I_{g0}\end{bmatrix}+\begin{bmatrix}L_{g\alpha} & 0 & 0\\ 0 & L_{g\beta} & 0\\ 0 & 0 & L_{g0}\end{bmatrix}\frac{d}{dt}\begin{bmatrix}\hat{\imath}_{g\alpha}\\ \hat{\imath}_{g\beta}\\ \hat{\imath}_{g0}\end{bmatrix}+U_{dc}\begin{bmatrix}\hat{s}_\alpha\\ \hat{s}_\beta\\ \hat{s}_0\end{bmatrix}+\hat{u}_{dc}\begin{bmatrix}S_\alpha\\ S_\beta\\ S_0\end{bmatrix}+U_{dc}\begin{bmatrix}S_\alpha\\ S_\beta\\ S_0\end{bmatrix}+\begin{bmatrix}0\\0\\\frac{1}{2}(\Delta\hat{u}+\Delta U)\end{bmatrix}$
Current Equations for High-Side Capacitor	$C_1\frac{d\hat{u}_{dc1}}{dt}=\hat{\imath}_{p1}+\hat{\imath}_{p2}-\hat{\imath}_{dc+}$ with $\begin{cases}\hat{\imath}_{p1}=3(S_0+\frac{1}{2})\hat{\imath}_{g0}+\frac{3}{2}\left[S_\alpha(\hat{\imath}_\alpha+\hat{\imath}_{g\alpha})+S_\beta(\hat{\imath}_\beta+\hat{\imath}_{g\beta})\right]\\ \hat{\imath}_{p2}=3\hat{s}_0 I_{g0}+\frac{3}{2}\left[\hat{s}_\alpha(I_\alpha+I_{g\alpha})+\hat{s}_\beta(I_\beta+I_{g\beta})\right]\end{cases}$
Current Equations for Low-Side Capacitor	$-C_2\frac{d\hat{u}_{dc2}}{dt}=\hat{\imath}_{n1}+\hat{\imath}_{n2}-\hat{\imath}_{dc-}$ with $\begin{cases}\hat{\imath}_{n1}=3\hat{\imath}_{g0}-\hat{\imath}_{p1}\\ \hat{\imath}_{n2}=0-\hat{\imath}_{p2}\end{cases}$

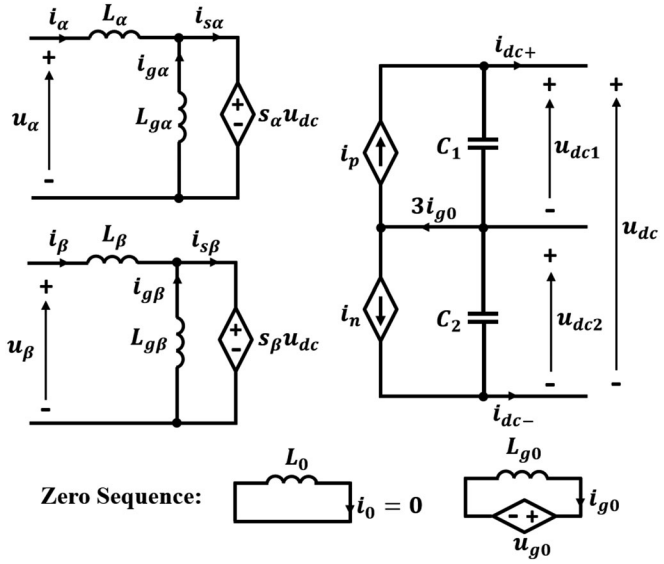

Fig. 7. Large-signal model.

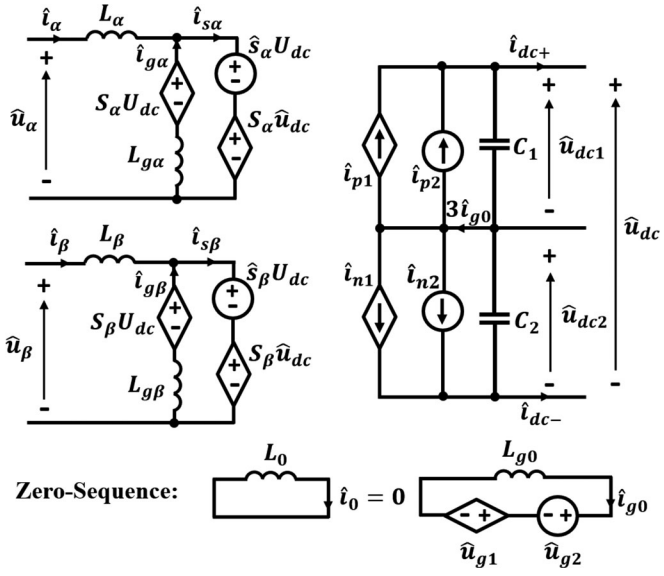

Fig. 8. Small-signal model.

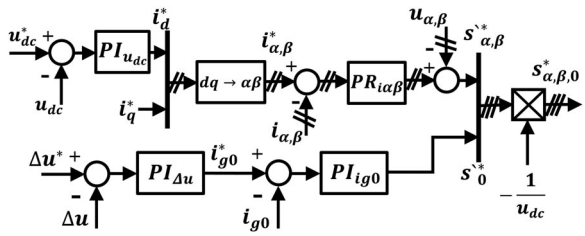

Fig. 9. Proposed control structure.

ac-inductor current control, which generates the duty cycles in α and β sequences; and 2) an outer loop for the voltage difference control of two dc poles, with an inner loop for the zero-sequence current control of the grounding inductor, which gives the duty cycle in zero sequence. For the $\alpha\beta$-sequence current control, a controller with sufficient gain at both dc- and ac-grid frequency should be used to eliminate the steady state error for tracking the current reference. This can be achieved either with a *PR* [26] or a *PIR* controller. As for the zero-sequence current control, a nonzero resonant part should be added into a *PI* controller for the more reliable rectifier performance in practice, as shown later in Section IV.

In addition to that, a conventional phase locked loop (PLL) is used, for measuring the phase angle and angular frequency of the ac-grid voltages [29].

IV. EXPERIMENT TEST

The experiment platform shown in Fig. 10 is used to test the proposed rectifier topology. A transformer is used to implement the coupled grounding inductor, due to its appropriate coupled structure. The schematic of the platform is shown in Fig. 11. For reducing the volume of the filter and improve the ac-grid power quality, an *LCL* filter rather than an *L* filter is used at the ac side. The parameters of the controllers and the test equipment are illustrated in Tables III and IV, respectively.

The rectifier is tested under three scenarios: 1) start-up with balanced dc loads; 2) dynamics with unbalanced dc loads; and 3) dynamics with asymmetrical dc voltages. The test results are presented and discussed next.

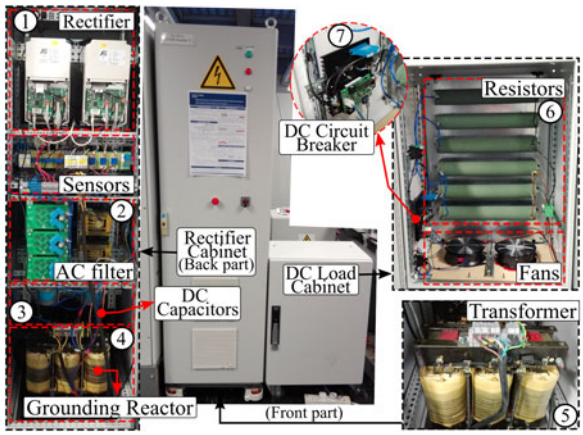

Fig. 10. Experiment platform for the proposed rectifier test.

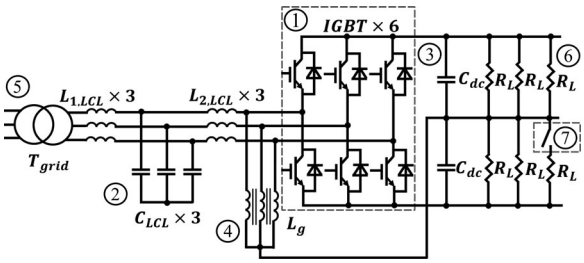

Fig. 11. Schematic of the experiment platform.

TABLE III
CONTROL PARAMETERS

Current Controller	$PR_{i\alpha\beta}$ Alpha/Beta Sequence	PI_{ig0} Zero Sequence
	$K_p = 10;\ K_r = 100;$ $K_i = 10$ $\omega_r = 2\pi \cdot 50$ rad/s $\omega_c = 8$ rad/s	$K_p = 30;\ K_i = 300$ $K_r = 10$ $\omega_r = 2\pi \cdot 50$ rad/s $\omega_c = 8$ rad/s
Voltage Controller	$PI_{u_{dc}}$ DC Bus Voltage Regulation	$PI_{\Delta u}$ Voltage Balance for Two DC Poles
	$K_p = 0.8;\ K_i = 1.2$	$K_p = 0.3;\ K_i = 0.6$
PLL Controller	PI_{PLL}: $K_p = 8.9, K_i = 1336$	
Others	Switching Frequency $f_s = 10$ kHz Sample Frequency $F_s = 10$ kHz	

TABLE IV
EXPERIMENT EQUIPMENT PARAMETERS

AC-Grid Voltage	Line-to-Line RMS Voltage 415V
AC-Grid Transformer	Tap Ratio 415V – 330V
LCL Filter	$L_{1,LCL} = 0.93$mH, $R_{1,LCL} = 0.3\Omega$ $L_{2,LCL} = 2.3$mH, $R_{2,LCL} = 0.4\Omega$ $C_{LCL} = 8.8$uF
Grounding Reactor	$L_{g\alpha} = L_{g\beta} = 1.362H;\ L_{g0} = 13.231mH$ $R_{g\alpha} = R_{g\beta} = 644.013\Omega;\ R_{g0} = 1.281\Omega$
DC Bus Capacitor	$C_{dc} = 5305\mu$F
DC Bus Rated Voltage	$V_{dc} = 600$V
DC Load	$R_L = 220\Omega$

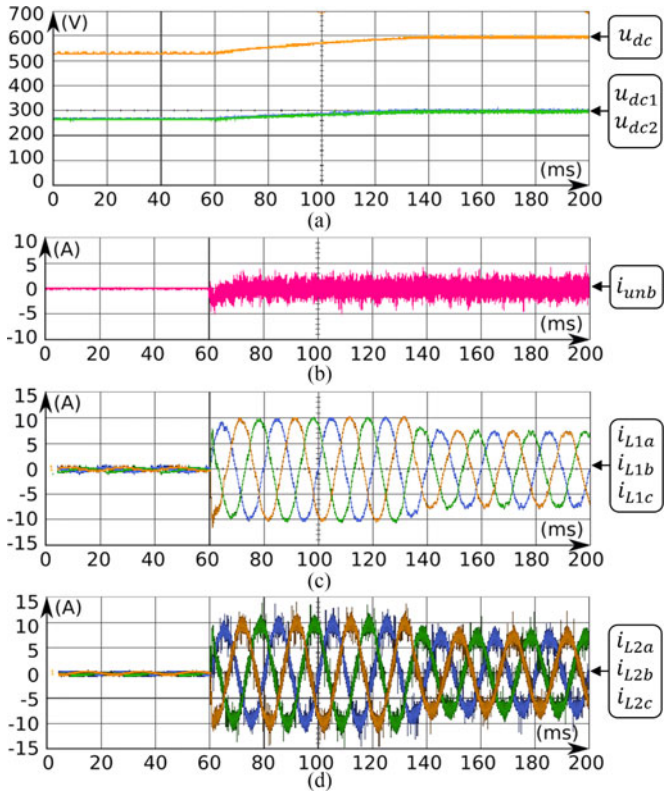

Fig. 12. Rectifier start-up performance with balanced dc loads. (a) DC bus voltages. (b) Total of injected three-phase zero-sequence currents. (c) Transformer-side inductor currents. (d) Converter-side inductor currents.

A. Rectifier Start-Up With Balanced DC Loads

Fig. 12 displays the rectifier start-up performance with balanced dc loads. The starting sequence of the proposed rectifier is same as a conventional VSC: 1) the dc bus is precharged through diodes with current limiting resistors, followed by a controlled boost up to the rated dc voltage; and 2) the ac-side capacitors of the *LCL* filter are precharged by the grid transformer in order to track the transformer voltages before switching the IGBTs.

As shown in Fig. 12(a), at a certain point in time, the rectifier starts to boost the dc bus voltage from the precharged value (about 530 V) to the rated value (600 V). The voltages for two poles increase concurrently and they are balanced all the time. Besides, it is noticeable that the PWM switching of the IGBTs also causes ripples flowing through the grounding inductor, as shown in Fig. 12(b).

In Fig. 12(c) and (d), both the transformer- and converter-side inductor currents are controlled to their upper limits, so that the dc bus voltage can be boosted as fast as possible, while maintaining the current below the maximum rating of the converter. When finishing the voltage boost, ac currents fall back to their rated values quickly. Remarkably, the transformer-side currents hold much less harmonics than the converter-side currents, due to the *LCL* filter, which contributes to the high ac-grid power quality.

The neutral current flowing through the grounding inductor is illustrated in Fig. 13(a), which is the summation of three-phase currents and holds zero-sequence dc component and high-

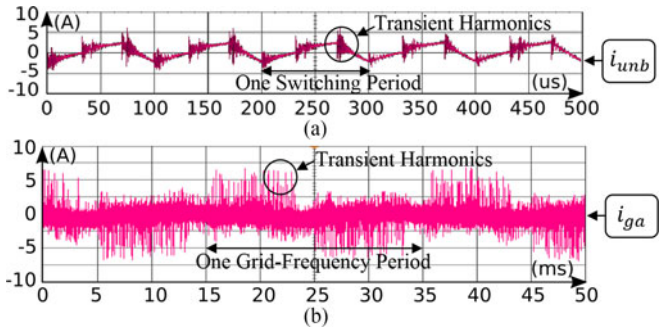

Fig. 13. Close-up plots of the currents flowing through the grounding inductor. (a) Total of three-phase currents. (b) One-phase current.

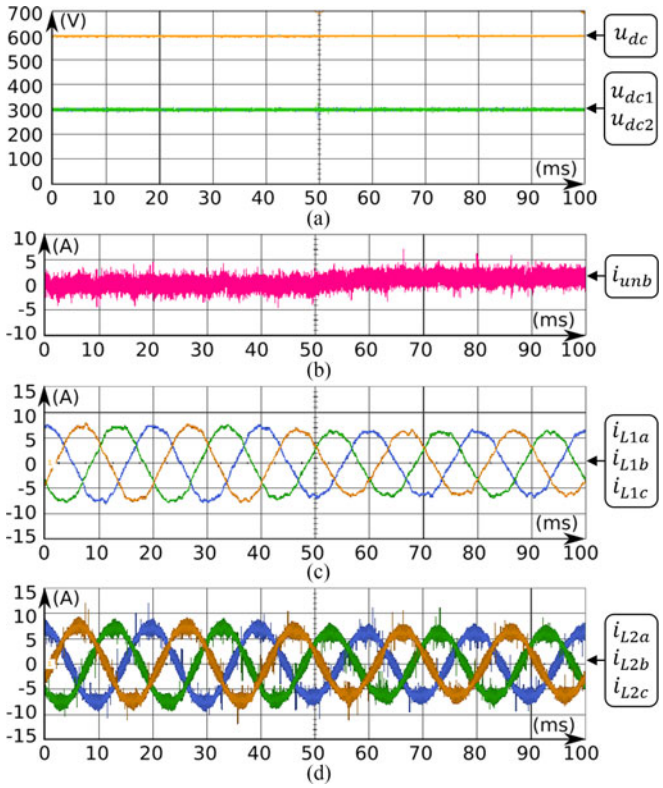

Fig. 14. Rectifier dynamics with a step change of load imbalance from 0% to 20% by disconnecting one dc load of the negative pole. (a) DC bus voltages. (b) Total of injected three-phase zero-sequence currents. (c) Transformer-side inductor currents. (d) Converter-side inductor currents.

frequency harmonics only. Transient harmonics appear due to the switching event of each IGBT. All zero-sequence harmonics can be filtered easily due to their low magnitude and high frequency. The one-phase current of the grounding inductor is also displayed in Fig. 13(b), where the grid-frequency sinusoidal component can barely be seen because of the large inductance in $\alpha\beta$ sequence.

B. Rectifier Dynamics With Unbalanced DC Loads

The rectifier dynamics with a step change of dc loads are illustrated in Figs. 14 and 15. Initially, the rectifier operates with balanced dc loads. At a certain point in time in Fig. 14, one load of the negative dc pole is disconnected and a load imbalance

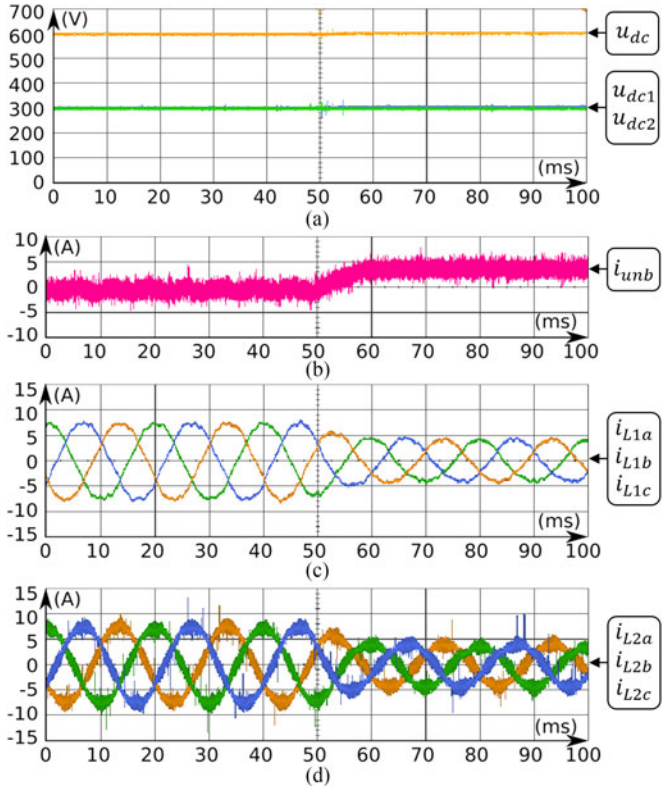

Fig. 15. Rectifier dynamics with a step change of load imbalance from 0% to 100% by disconnecting all dc loads of the negative pole. (a) DC bus voltages. (b) Total of injected three-phase zero-sequence currents. (c) Transformer-side inductor currents. (d) Converter-side inductor currents.

of 20% is given. As for Fig. 15, all loads of the negative pole are disconnected leading to a load imbalance of 100%. Upon removing the loads in both Figs. 14 and 15, the voltages of two dc poles are going to split because of the unbalanced dc-load current. Owing to the voltage balancing controller and zero-sequence current controller, the zero-sequence current is quickly regulated to its new steady state and makes the dc voltages balanced again [about 10 ms in Figs. 14(b) and 15(b)]. The voltage fluctuations in Figs. 14(a) and 15(a) are small enough to be hard to see in the figures. This not only shows the good dynamics of zero-sequence voltage and current controllers, but also validates the high voltage quality ensured by the proposed control structure. In Fig. 14(b) and (c) as well as Fig. 15(b) and (c), ac currents reduce and reach their new steady states within one sinusoidal period, which shows good performance of the $\alpha\beta$-sequence current controller.

C. Rectifier Dynamics With Asymmetrical DC Voltages

The proposed rectifier can work with asymmetrical dc voltages, by simply changing the value of Δu^* in the control structure in Fig. 9. Based on (11), a nonzero steady state Δu requires a nonzero dc offset (i.e., $s_0 = d_0 - 0.5 \neq 0$) of there-phase duty cycles. Hence, the overmodulation should be carefully avoided for this operation mode. As displayed in Fig. 16, at a certain instant, the value of Δu^* is changed from 0 to 40 V. As a result, the outer-loop voltage balancing controller makes the inner-loop

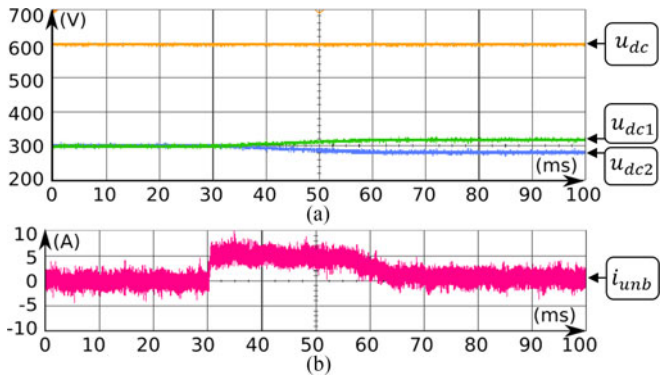

Fig. 16. Rectifier operation with unbalanced dc voltages. (a) DC bus voltages. (b) Total of injected three-phase zero-sequence currents.

TABLE V
REQUIRED NUMBER OF COMPONENTS

Item	Case 1	Case 2	Case 3
Transformer	1 or 2	1	1
Inductor	2	2	2
Power Switch	$6+6=12$	$6+2=8$	6

zero-sequence current controller absorb the current from the dc-side neutral line actively, which causes the voltage difference between two poles to increase steadily for around 35 ms.

This operation is a natural generalization of the voltage balancing control and can obviously provide three different voltage levels and more flexibilities to the loads. The fourth rail system currently used in the London Underground is a typical application of the asymmetrical dc-bus voltage distribution [30].

V. COMPARISON OF AC–DC CONVERSION APPROACHES

In previous sections, the proposed rectifier was analyzed and tested. Nevertheless, as mentioned earlier, two other existing ac–dc topologies are also available for the bipolar dc distribution, as shown in Figs. 1(b) and 2. In order to show the benefits of the proposed rectifier further, all three cases are compared in detail next: 1) Case 1 – two two-level VSCs; 2) Case 2 - one two-level VSC with a voltage balancer; 3) Case 3 - one two-level VSC with a grounding inductor, i.e., the topology proposed in this paper.

A. Comparison of Required Number of Components

The characteristics of required number of components for all three cases are organized in Table V.

Cases 2 and 3 require one transformer each, while case 1 requires one transformer with two secondary windings and the insulation rated to withstand a dc voltage offset.

Regarding the inductors required in the converters, two three-phase inductors are needed in the two rectifiers of case 1. For case 2, besides the three-phase grid inductor, an extra balancing inductor is required by the voltage balancer. As for case 3, an extra three-phase grounding inductor is necessary.

TABLE VI
REQUIRED RATING OF COMPONENTS

Item	Case 1	Case 2	Case 3
Grid Voltage: $U_{ph,RMS}$	$M\frac{u_{dc}}{4}\frac{1}{\sqrt{2}}$	$M\frac{u_{dc}}{2}\frac{1}{\sqrt{2}}$	
Current Rating of Power Switch with Balanced Loads: I	$\frac{2\sqrt{2}S_{ac}}{3Mu_{dc}}$		
Voltage Rating of Power Switch: U	$\frac{u_{dc}}{2}$	u_{dc}	
Current Rating of L Filter with Balanced Loads: I	$\frac{2\sqrt{2}S_{ac}}{3Mu_{dc}}$		
Sizing of L Filter: L	$\frac{u_{dc}}{4}\frac{\Delta t}{\Delta i_{ac}}$	$\frac{u_{dc}}{2}\frac{\Delta t}{\Delta i_{ac}}$	
Current Rating of Balancing/Grounding Inductor: I	-	i_{unb}	$i_{unb}+i_{\alpha\beta}$
Sizing of Balancing/Grounding Inductor: L	-	$\frac{u_{dc}}{2}\frac{\Delta t}{\Delta i_{unb}}$	$L_0=\frac{u_{dc}}{2}\frac{\Delta t}{\Delta i_{g0}}$ $L_{\alpha\beta}=\frac{U_{ph,RMS}}{2\pi f_{ac} I_{\alpha\beta,RMS}}$

Note: M is the modulation index; S_{ac} is the total ac-side apparent power; u_{dc} is the positive-to-negative dc bus voltage; Δi indicates the corresponding current ripple; and f_{ac} is the ac-grid power frequency.

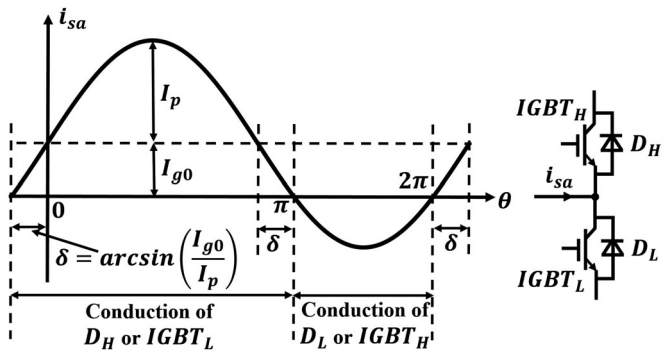

Fig. 17. Current flow analysis for phase a of the proposed rectifier.

As for the number of power switches, the proposed topology, i.e., case 3, only needs six power switches, which are less than the requirements for case 2 (eight power switches) and case 1 (12 power switches). The ratings of these components are discussed next.

B. Comparison of Required Rating of Components

The component ratings for all three cases are summarized in Table VI. The voltage and current ratings for case 2 are equivalent to those of a conventional two-level active rectifier. As for case 1, each rectifier requires almost half ac-grid voltage but same current as case 2, which leads to a worse conversion efficiency as shown later in Section V-C. By contrast in case 3, the ac-grid voltage might be around 15% lower than that of case 2 because of the inapplicability of third harmonics injection [31], which results in slightly higher currents in case 3 as well.

The inductor sizing equations for all three cases are also organized in Table VI. Regarding to L filters, the inductance value required by case 1 is only the half of that for case 2 or 3, due to its lower PWM voltages. As for the grounding inductor in

TABLE VII
IGBT POWER LOSSES CALCULATIONS OF THE PROPOSED RECTIFIER

Conduction Losses	$P_{C,ph} = P_{C,IGBT,ph} + P_{C,D,ph}$ with $\begin{cases} P_{C,IGBT,ph} = u_{CE0}(\underbrace{I_{IGBT,H,avg} + I_{IGBT,L,avg}}_{I_{IGBT,ph,avg}}) + r_{IGBT}(\underbrace{I^2_{IGBT,H,rms} + I^2_{IGBT,L,rms}}_{I^2_{IGBT,ph,rms}}) \\ P_{C,D,ph} = u_{D0}(\underbrace{I_{D,H,avg} + I_{D,L,avg}}_{I_{D,ph,avg}}) + r_D(\underbrace{I^2_{D,H,rms} + I^2_{D,L,rms}}_{I^2_{D,ph,rms}}) \end{cases}$ $\begin{cases} I_{IGBT,ph,avg} = \frac{I_p}{\pi}\sqrt{1-\frac{I_{g0}^2}{I_p^2}} + \frac{I_{g0}}{\pi}\arcsin\left(\frac{I_{g0}}{I_p}\right) - \frac{I_p M\cos(\phi)}{4} \\ I_{D,ph,avg} = \frac{I_p}{\pi}\sqrt{1-\frac{I_{g0}^2}{I_p^2}} + \frac{I_{g0}}{\pi}\arcsin\left(\frac{I_{g0}}{I_p}\right) + \frac{I_p M\cos(\phi)}{4} \end{cases}$ $\begin{cases} I^2_{IGBT,ph,rms} = I_p^2\left(\frac{1}{4} - \frac{2M\cos(\phi)}{3\pi}\sqrt{1-\frac{I_{g0}^2}{I_p^2}}\right) + I_{g0}^2\left(\frac{1}{2} - \frac{M\cos(\phi)}{3\pi}\sqrt{1-\frac{I_{g0}^2}{I_p^2}}\right) - \frac{I_p I_{g0} M\cos(\phi)}{\pi}\arcsin\left(\frac{I_{g0}}{I_p}\right) \\ I^2_{D,ph,rms} = I_p^2\left(\frac{1}{4} + \frac{2M\cos(\phi)}{3\pi}\sqrt{1-\frac{I_{g0}^2}{I_p^2}}\right) + I_{g0}^2\left(\frac{1}{2} + \frac{M\cos(\phi)}{3\pi}\sqrt{1-\frac{I_{g0}^2}{I_p^2}}\right) + \frac{I_p I_{g0} M\cos(\phi)}{\pi}\arcsin\left(\frac{I_{g0}}{I_p}\right) \end{cases}$
Switching Losses	$P_{sw,ph} = P_{on,IGBT,ph} + P_{off,IGBT,ph} + P_{sw,D}$ with $\begin{cases} P_{on,IGBT,ph} = \frac{V_{cc} t_{rN} f_s}{4 I_{CN}}(2I_{g0}^2 + I_p^2) \\ P_{off,IGBT,ph} = \frac{V_{cc} t_{fN} f_s}{12 I_{CN}}\left(2I_{g0}^2 + I_p^2 + \frac{8 I_{CN} I_p}{\pi}\sqrt{1-\frac{I_{g0}^2}{I_p^2}} + \frac{8 I_{CN} I_{g0}}{\pi}\arcsin\left(\frac{I_{g0}}{I_p}\right)\right) \\ P_{sw,D} = \frac{1}{4} Q_{rr} V_{cc} f_s \end{cases}$
Total Power Losses	$P_{loss,ph} = P_{C,ph} + P_{sw,ph}; \quad P_{loss,total} = 3P_{loss,ph}$
Auxiliary Equations	$i_{sa} = I_p \sin(\theta) + I_{g0}$ and $s_a = \frac{1}{2} M \sin(\theta + \phi)$ or $d_a = \frac{1}{2}(M \sin(\theta + \phi) + 1)$ with $\theta = \omega t = 2\pi f_{ac} t$

case 3, the total zero-sequence current flowing through it is simply the unbalanced load current (i.e., i_{unb}), which equals to the current of the balancing inductor of case 2. Besides, the zero-sequence grounding inductance of case 3 is also sized similarly to the balancing inductance of case 2. However, compared with the balancing inductor in case 2 (e.g., a dc choke), the grounding inductor of case 3 should be three-phase coupled and the $\alpha\beta$-sequence inductance is required to be large enough to limit the $\alpha\beta$-sequence current and power losses, as explained earlier in Section III-C. As for the dc bus capacitors for all three cases, they can be sized similarly based on the ripple analysis in [32]–[34].

C. Comparison of Power Losses

Based on [35], [36], the power losses of case 1 and case 2 can be obtained directly. For case 3, by analyzing the current flow in Fig. 17 and adapting the formulation in [35], [36], the power losses equations of IGBTs are derived and organized in Table VII.

For calculating the power losses, the parameters of "CM75TJ-24F Trench Gate Design Six IGBTMOD$^{\mathrm{TM}}$ 75 Amperes/ 1200 Volts" [37] are used, as summarized in Table VIII, which is also the IGBT used in the experiment test. Further, the assumed rated comparison conditions are organized in Table IX.

For getting more reliable results, the losses of inductors (including ac-side L filters of three cases, the balancing inductor of case 2, and the grounding inductor of case 3) are also considered. The equivalent inner resistance for an L filter in one phase is evaluated with a rated efficiency of around 99%, as shown in Table X. Remarkably, the inner resistance of the L filter for case 1 is only the half of that for case 2 or 3, due to the lower inductance value and the probably shorter conductor, as explained in Section V-B and Table VI earlier. Besides, for case 2, it is assumed that the inner resistance of the balancing inductor equals to that of an L filter, according to the similar PWM voltages faced by both of them. Moreover, the losses of dc-bus capacitors are omitted. Further, it is temporarily assumed that the zero-sequence inner resistance (i.e., $R_{\mathrm{in,Lg0}}$) of the grounding inductor equals to $R_{\mathrm{in,bal}}$ of the balancing inductor, i.e., $k = 1$ in Table X, and the losses caused by the $\alpha\beta$-sequence currents are small enough to be ignored. These two assumptions will be discussed in detail later.

With the fixed modulation index value of 0.8, the power losses for all three cases with different dc-load imbalance levels are shown in Fig. 18. When the load imbalance increases (e.g., more and more dc loads are connected to the positive pole), the power losses of both cases 1 and 2 grow considerably. Specifically, 100% of load imbalance causes the power losses increase of 35.9% (213.6 W) and 71.0% (287.8 W) for cases 1 and 2, respectively. For case 1, the losses of two L filters and IGBT conduction losses contribute to the increase of power losses mainly. As for case 2, the switching losses and balancing inductor losses increase dramatically, caused by the rising current flowing through the voltage balancer. By contrast, for case 3, only a slight change of 17.7% (71.4 W) is noticed and the total power losses are lower than those of cases 1 and 2 for an almost arbitrary load imbalance.

However, the third harmonics injection is not applicable for the proposed rectifier in case 3 due to the grounding reactor, which makes the maximum modulation index value of case 3 (i.e., "$M_{\max} = 1$") lower than those of cases 1 and 2 (i.e., "$M_{\max} = 1.15$") [31]. Besides, as explained in Section III-C, the $\alpha\beta$-sequence grounding inductance of case 3 should be large enough and would probably lead to a longer conductor, and therefore, a larger zero-sequence inner resistance than the balancing inductor in case 2, i.e., $R_{\mathrm{in,Lg0}} \geq R_{\mathrm{in,Lbal}}$ and $k \geq 1$ in

TABLE VIII
PARAMETERS OF CM75TJ-24F TRENCH GATE DESIGN SIX IGBT MOD TM 75 AMPERES/1200 VOLTS

Item	Value
IGBT on-state zero-current collector-emitter voltage	$u_{\mathrm{CE0}} = 1.3$ V
IGBT on-state resistance	$r_{\mathrm{IGBT}} = 6.7$ mΩ
Diode on-state zero-current voltage	$u_{\mathrm{D0}} = 1.7$ V
Diode on-state resistance	$r_D = 11.2$ mΩ
Rated collector current	$I_{\mathrm{CN}} = 75$ A
IGBT rated rise time	$t_{\mathrm{rN}} = 50$ ns
IGBT rated fall time	$t_{\mathrm{fN}} = 300$ ns
Diode reverse recovery charge	$Q_{\mathrm{rr}} = 3.1\ \mu$C

TABLE IX
RATED COMPARISON CONDITIONS

Item	Value
Positive-to-negative dc-bus voltage	$U_{\mathrm{dc}} = 600$ V
AC-grid frequency	$f_{\mathrm{ac}} = 50$ Hz
Switching frequency	$f_s = 10$ kHz
DC-side balanced load current	$I_{\mathrm{bal}} = 30$ A
DC-side unbalanced load current	$I_{\mathrm{unb}} = 0$ A
Modulation index	$M = 0.8$
Active power	$P_{\mathrm{ac,rated}} \approx P_{\mathrm{dc,rated}} = 600\ \mathrm{V} \cdot 30\ \mathrm{A} = 18$ kW
Reactive power	$Q_{\mathrm{ac,rated}} = 0$ Var
Apparent power	$S_{\mathrm{ac,rated}} = 18$ kVA

TABLE X
EQUIVALENT INNER RESISTORS OF INDUCTORS

	Item	Value
Case 1	For one-phase L filter	$R_{\mathrm{in},L,\mathrm{case1}} = 0.015\ \Omega$
Case 2	For one-phase L filter	$R_{\mathrm{in},L,\mathrm{case2}} = 0.03\ \Omega$
	For balancing inductor	$R_{\mathrm{in,Lbal}} = 0.03\ \Omega$
Case 3	For one-phase L filter	$R_{\mathrm{in},L,\mathrm{case3}} = 0.03\ \Omega$
	For grounding inductor	$R_{\mathrm{in,Lg0}} = k \cdot R_{\mathrm{in,Lbal}}$ where k is a positive coefficient

Table X. Hence, the power losses with maximum modulation index values and different values of zero-sequence resistance of the grounding inductor are compared in Fig. 19. For balanced loads, the improved ac-grid voltage of case 2 makes its losses lower than case 3. By contrast, for the increase of the load imbalance, case 3 is found to be better under some conditions. Noticeably, the total IGBT losses of case 3 are lower than those of both cases 1 and 2 when the load imbalance is over about 25%. But the inductor losses of case 3 are higher than other two cases in most cases: one reason is the lower modulation index of case 3, which leads to lower ac voltages, higher ac currents, and consequently higher L filter losses; the other is the higher zero-sequence grounding resistance that results in higher losses. Noticiably, when $R_{\mathrm{in,Lg0}} \geq 6 \times R_{\mathrm{in,bal}}$, case 3 is worse than case 2 in power losses. Hence, for a better effciency of case 3, the zero-sequence resistance of the grounding inductor should be designed as small as possible.

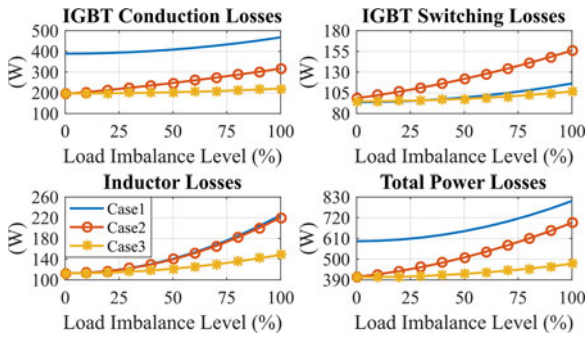

Fig. 18. Power losses for three cases with different dc-side load imbalance levels when modulation index $M = 0.8$ and $R_{\mathrm{in,Lg0}} = R_{\mathrm{in,Lbal}}$.

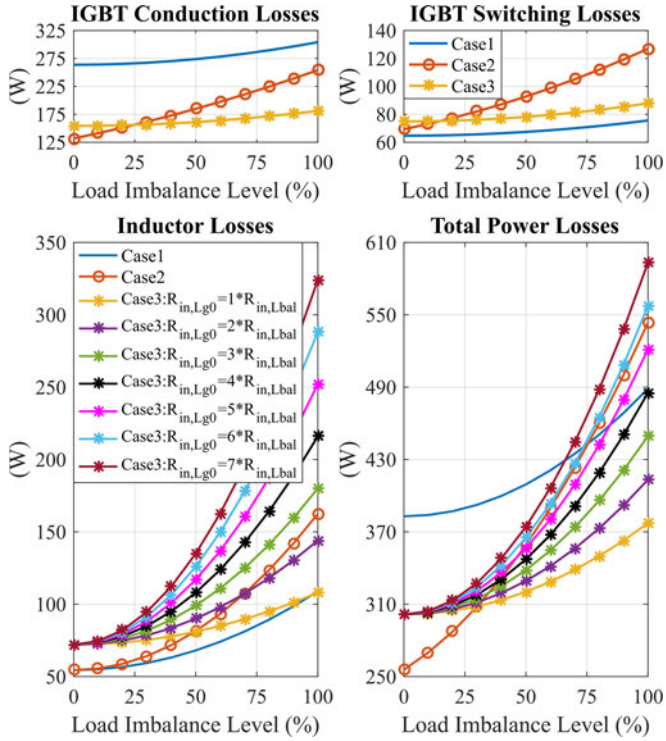

Fig. 19. Power losses for three cases with different dc-side load imbalance levels when modulation index $M = M_{\max}$ and $R_{\mathrm{in,Lg0}} \geq R_{\mathrm{in,Lbal}}$.

Next, the losses caused by $\alpha\beta$-sequence current of the grounding inductor will be discussed. The margin of power losses of case 3 when compared with case 2 is calculated, which is defined as

$$\mathrm{Margin} = \left(\frac{P_{\mathrm{Tol,Loss,Case2}} - P_{\mathrm{Tol,Loss,Case3}}}{P_{\mathrm{Lg0,Loss,Case3}}} \right)_{100\%\ \mathrm{Load\ Imbalance}} \quad (23)$$

That is, the margin gives the upper limit of the $\alpha\beta$-sequence losses of the grounding inductor, if the efficiency of case 3 is required to be better than that of case 2 with 100% load imbalance, as shown in Fig. 20. Remarkably, the larger zero-sequence resistance, the lower margin for the $\alpha\beta$-sequence losses, and consequently the lower $\alpha\beta$-sequence current and larger $\alpha\beta$-sequence inductance required for the grounding inductor. There-

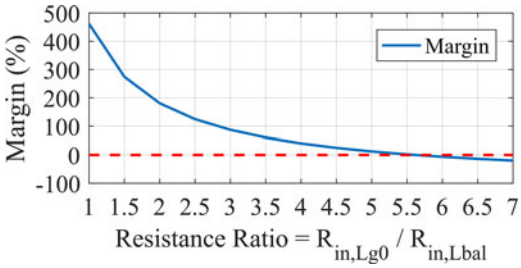

Fig. 20. Margin for $\alpha\beta$-sequence losses of the grounding inductor of case 3.

fore, in addition to the design requirement of low zero-sequence resistance, the $\alpha\beta$-sequence inductance should be large enough for a good efficiency of case 3. These two design requirements might increase the system costs of case 3. But as long as the grounding inductor in case 3 costs less than the voltage balancer in case 2 (mainly including one balancing inductor, two IGBTs, and corresponding gate-driving signals given by an auxiliary control system), case 3 is still cost-benefit with a satisfactory conversion efficiency.

VI. Conclusion

A new three-phase active rectifier topology for bipolar dc distribution has been proposed and analyzed. This topology has the ability to feed two dc poles independently and control two dc-pole voltages actively, by using an ac-side three-phase coupled grounding inductor to achieve the current injection to the dc neutral line. The proposed rectifier has been tested on an experiment platform. Compared with other two existing ac–dc conversion approaches for bipolar LVDC distribution, the proposed topology uses less IGBTs and potentially holds less power losses when feeding unbalanced dc loads. But meanwhile, the coupled grounding inductor is required with high $\alpha\beta$-sequence inductance and low zero-sequence resistance, which closely influence the efficiency of the proposed topology.

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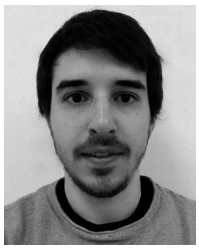

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