A 6.7-GHz Active Gate Driver for GaN FETs to Combat Overshoot, Ringing, and EMI

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Abstract—**Active gate driving has been demonstrated to beneficially shape switching waveforms in Si- and SiC-based power converters. For faster GaN power devices with sub-10-ns switching transients, however, reported variable gate driving has so far been limited to altering a single drive parameter once per switching event, either during or outside of the transient. This paper demonstrates a gate driver with a timing resolution and range of output resistance levels that surpass those of existing gate drivers or arbitrary waveform generators. It is shown to permit active gate driving with a bandwidth that is high enough to shape a GaN switching during the transient. The programmable gate driver has integrated high-speed memory, control logic, and multiple parallel output stages. During switching transients, the gate driver can activate a near-arbitrary sequence of pull-up or pull-down output resistances between 0.12 and 64 Ω. A hybrid of clocked and asynchronous control logic with 150-ps delay elements achieves an effective resistance update rate of 6.7 GHz during switching events. This active gate driver is evaluated in a 1-MHz bridge-leg converter using EPC2015 GaN FETs. The results show that aggressive manipulation of the gate-drive resistance at sub-nanosecond resolutions can profile gate waveforms of the GaN FET, thereby beneficially shaping the switch-node voltage waveform in the power circuit. Examples of open-loop active gate driving are demonstrated that maintain the low switching loss of constant-strength gate driving, while reducing overshoot, oscillation, and EMI-generating high-frequency spectral content.**

Index Terms—**Active gate driver, electromagnetic interference (EMI), gate signal profiling, GaN FETs, gate overshoot, oscillation, programmable gate resistance.**

I. INTRODUCTION

ACTIVE gate driving dynamically changes the gate resistance [1]–[6], gate voltage [7]–[9], or gate current [10]–[16], with the intention of controlling switching waveforms of power semiconductor devices, as opposed to conventional gate drives that apply a voltage step function to the gate via a fixed resistance. Benefits that have been demonstrated in MOS-gated silicon devices include current balancing in parallel devices [3], voltage balancing in series devices [10], [11], reduction of current and voltage overshoot [4]–[7], [13], suppression of EMI generation without significantly affecting power loss [8], [9], [12]–[15], and optimization of power efficiency under constantly changing load conditions [7], [16].

With the move to faster wide-bandgap devices, the need for shaping the switching waveforms increases. Two commonly reported challenges encountered in the application of wide-bandgap devices are voltage overshoots and oscillation [8], [17]–[19]. Conventional methods to address these issues at the source can be divided into two categories:

1) Minimizing parasitic inductances introduced by device packaging and PCB layout: As di/dt and dv/dt increase dramatically in wide-bandgap devices, the amount of parasitic inductance necessary to generate voltage overshoots or oscillation is greatly reduced [17]. Optimized PCB layout techniques cannot eliminate parasitic inductance completely and may even conflict with the requirements for thermal and mechanical design [18].

2) Slowing down the switching speed: With conventional gate drivers, overshoots and oscillation are traded off for increased switching loss, thus undoing some of the benefit of using wide-bandgap devices [8]. In bridge-leg topologies, it also implies an increase in the dead time that further increases power loss [19].

Another reported challenge is that commercially available low-voltage GaN devices exhibit a low margin between the gate-source voltage required to enhance the channel, and the absolute maximum gate-source voltage above which the gate is permanently damaged [20]. Maximum switching speed is thereby limited under conventional gate driving, as there is a minimum gate resistance requirement to avoid overshoot at the gate (see [21], eq. (3.1)]), as illustrated in Fig. 1. By contrast, active gate driving can achieve the switching speed of a constant gate resistance lower than this minimum requirement, without incurring any gate overshoot (see Fig. 1), as demonstrated later. To fully take advantage of wide-bandgap devices, active gate driving that accommodates more degrees of freedom for shaping the switching waveforms is therefore highly desirable.
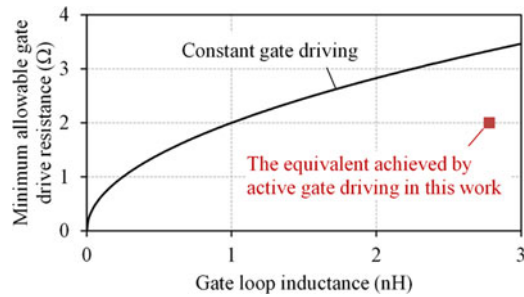
Fig. 1.   Minimum allowable gate resistance versus gate loop inductance for a GaN FET with 1-nF input capacitance under conventional (according to [21], eq. (3.1)]) and active gate-driving scenarios.
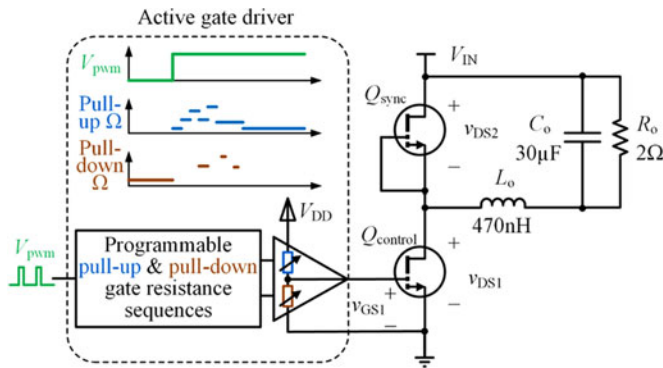

Fig. 2.   Active gate driving for GaN FET in bridge-leg topology.

While some studies in gate voltage profiling for SiC power devices have been reported [1], [5], it remains unclear to what extent GaN devices are controllable via the gate. Reported variable gate driving for GaN devices has been limited to local dead-time management [22], single change in driving strength [23], and the use of three gate voltage levels for loss reduction during dead time [24]. Two particular challenges arise: first, the time resolution or bandwidth of the active gate driver must be commensurate with the sub-10-ns-level switching time of GaN devices; second, the low-pass filter composed of driver package, PCB tracks and the input capacitance of the GaN FET makes it harder to deliver a shaped gate signal—high-frequency shaping components may be filtered out, while components around the resonant frequency of the gate-drive loop will be emphasized and give rise to underdamped parasitic oscillation.

In this paper, the first gate driver [25] capable of open-loop active gate driving of GaN devices is demonstrated, and driving strategies are developed. The integrated active gate driver, as illustrated in Fig. 2, can be programmed to vary its output resistance every 150 ps, which is shown using a 10-V, 4-A, 1-MHz GaN FET bridge leg.

This paper focusses on three example objectives:
1) turning GaN gates on faster, without incurring gate voltage overshoot;
2) eliminating overshoot in switch-node voltage waveforms;
3) attenuating high-frequency components of switch-node voltage spectra.

A SPICE modeling technique and a gate driving strategy are proposed, which permit the accurate evaluation of active gate driving for GaN FETs. This modeling takes into account driver, interconnect, layout, and component parasitics, and is validated by experiment. It provides insight into the high-bandwidth circuit currents, which are difficult to measure in compact GaN-based circuits without a significant increase in layout parasitics [21]. The model allows the calculation of switching loss per transient, which is useful in the search for optimized switching waveforms with improved balances of switching loss and power-circuit overshoots, oscillation, and EMI-generating, high-frequency spectral content.

This paper is organized as follows: Section II presents the 150-ps high-speed programmable resistance gate driver for GaN FETs. In Section III, this gate driver is modeled and simulated in a GaN-based switching circuit, and gate driving strategies for shaping the turn-on and turn-off switching waveforms are provided. Section IV describes the test circuit and measurement methods used. Section V shows measured switching waveforms for constant-strength gate driving contrasted against active gate driving that target the aforementioned three objectives. The corresponding spectra and power losses are also provided. Section VI draws conclusions on the potential and limitations of the presented method of active gate driving for GaN FETs.

II. HIGH-SPEED ACTIVE GATE DRIVER WITH PROGRAMMABLE OUTPUT RESISTANCE

A. Overview of the Driver Architecture

On arrival of a pulsewidth-modulated (PWM) edge, the driver activates a sequence of pull-up and pull-down resistances. This programmable sequence contains the desired output resistances, the polarities (direction of pull, up or down), and the timing values. The driver's architecture, shown in Fig. 3, comprises three main circuit blocks:
1) An output stage consisting of two parallel drivers: a "main" driver with 2^8 output resistance levels and a time resolution adjustable between 1.6 and 2.5 ns, and a "fine" driver with 2^6 output resistance levels and a time resolution of 150 ps. The main driver pulls up when the input PWM control signal is logic high and pulls down when PWM is low. In either case, it can alternatively be programmed to be in a high-impedance state if required. Apart from its higher time resolution, the fine driver differentiates itself from the main driver by being able to either pull up or pull down regardless of the logic stage of the input PWM signal.
2) Memory that holds the gate drive sequences and logic that controls the output stages during transients that are triggered by the PWM signal. This block is controlled by a system clock, and programmed with sequences from external circuitry.
3) A subclock pulse generator that is triggered by the clock and then runs asynchronously to set delays and pulse widths for the fine driver according to the stored sequence.
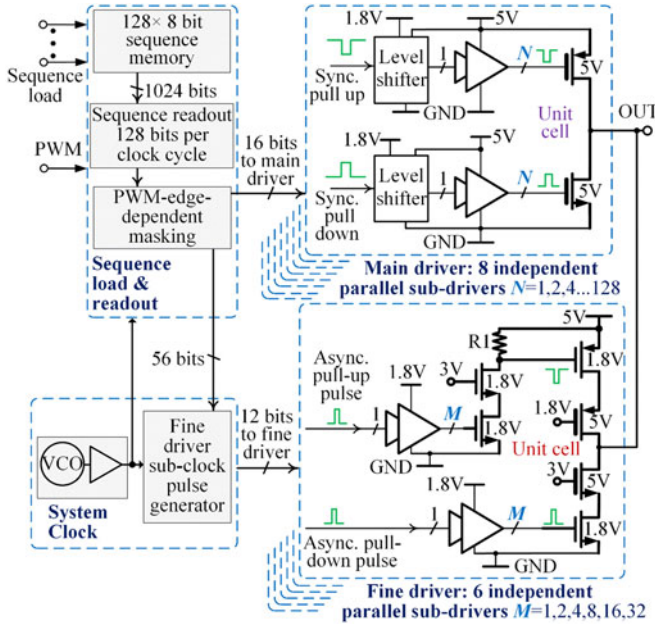
Fig. 3. Architecture of the gate driver chip with programmable output resistance.

TABLE I
GATE DRIVER SPECIFICATION

	Main Driver	Fine Driver
Resistance range	0.14–36 Ω	1–64 Ω
Resistance levels	2^8 (0x01-0xFF)	2^6 (0x01-0x3F)
Time steps	8	11 per main driver step
Time resolution	1.6–2.5 ns	150 ps
Output polarity	Same as PWM	Selectable

tively, thus allowing any number of unit cells between 0 and 255 to be selected using 8 bits.

The fine driver is an asynchronous system, controlled by 12 pulse signals with programmable delay and pulse length. These control six parallel-connected subdrivers, which buffer and distribute their two input signals to M parallel identical unit cells (shown in thick line in Fig. 3). These unit cells are cascode connections of fast 1.8-V transistors and slower 5-V in order to attain the required fast resistance change-over. A cascode in the high-side inverts and shifts its input A V to $(5 - A)$ V, to enable level-shifting with a delay of only 80 ps. The six subdrivers of the fine driver stage contain $M = 1$, 2, 4, 8, 16, and 32 identical unit cells, respectively, thus allowing any number of unit cells between 0 and 63 to be selected using 6 bits.

D. Output Resistance Values and Drive Strength

The selectable drive resistances are 0.14 to 36 Ω for the main driver and 1 to 64 Ω for the fine driver (see Table I). The combined minimum nominal output resistance is 120 mΩ.[1]

These nominal resistances are defined here as the on-state resistances of the pull-up and pull-down branches of the unit driver cells when 5 V is applied to the respective branches. Under these conditions, the transistors are saturated, and the cell acts as a current source. The resistance against output voltage of a main driver pull-down NMOS transistor, determined by prelayout simulation using Cadence Spectre, is shown in Fig. 4. The transistor is seen to reduce its on-state resistance from 5 to 2 V, where it is seen to enter the ohmic region. The instantaneous resistance thus varies significantly during active gate driving from the stored programmed nominal resistance. Therefore, simulations in Section III use this characteristic.

In the following sections, for simplicity, resistance sequences are provided using nominal resistances. The maximum resistance, where all driver transistors are off, is denoted as "High Ω."

E. Degrees of Freedom in the Generation of Drive Resistance Sequences

In each of the eight clock cycles following the PWM edge, the main driver pulls with a constant nominal resistance in the

B. Signal Generation to Control the Output Stage

The desired turn-on and turn-off sequences are loaded into a 1024-bit memory by an external controller. The two sequences contain resistances for the main driver and the resistances, timings, and polarities for the fine driver. The data required for the main driver are less, as the fast internal system clock provides its timing, and the PWM edge defines the polarity of pull. Resistance sequences are triggered by the PWM signal edges and last for eight clock cycles. An on-chip, voltage-controlled oscillator (VCO) generates the system clock, variable from 1.6 ns (625 MHz) to 2.5 ns (400 MHz), to permit use for different rise and fall times of the gate transient. The main driver changes resistance on each clock edge. The subclock pulse generator is triggered on each clock edge to produce six pulses of controlled delay and duration for the fine driver, during a single clock period. Delay and duration are controllable in increments of 150 ps (equivalent to 6.7 GHz sampling), using selectable delay elements. This allows the sampling frequency to exceed the nominal maximum clock frequency for a given fabrication process. After the eight clock cycles, both drivers retain their final resistance setting until the next PWM transition.

C. Main and Fine Driver

The main driver is a synchronous system, controlled by eight pull-up and eight pull-down signals, which control eight parallel-connected subdrivers, as indicated in Fig. 3. Each subdriver level-shifts its two input signals from 1.8 to 5 V (~500 ps delay) and buffers them to control N parallel identical unit driver cells comprising HV PMOS and NMOS FETs (shown in thick line in Fig. 3). The use of identical unit cells ensures consistent timing. The eight subdrivers contain $N = 1$, 2, 4, 8, 16, 32, 64, and 128 identical cells, respec-

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[1]The driver is thermally capable of driving continuously into a short circuit, as well as the main and the fine driver pulling in opposite directions with minimum resistance. The on-chip wires have been designed to avoid electromigration failures up to 10 A. Thus, the driver can accommodate a wide range of driving requirements.
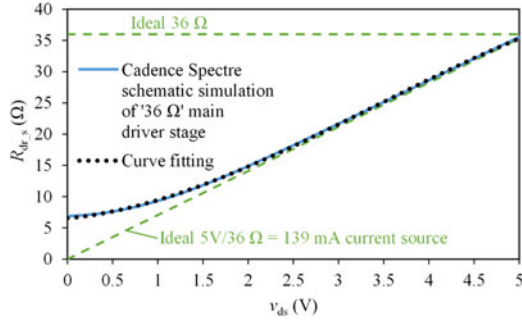
Fig. 4.   Simulated output characteristics of a single pull-down NMOS transistor in the main driver.
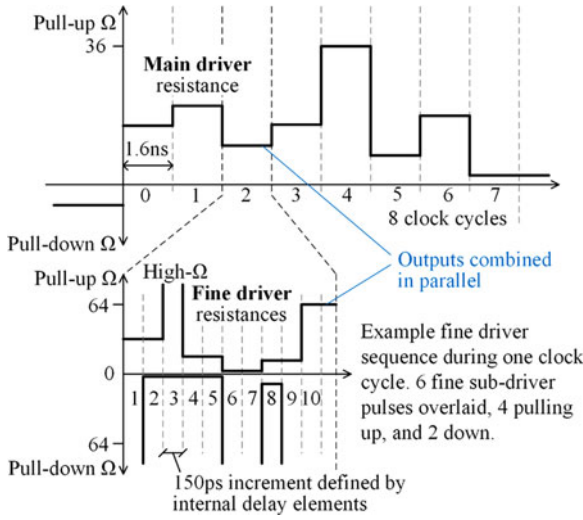

Fig. 5.   Example of an output resistance sequence.

Fig. 6.   Circuit model of the experimental GaN-based bridge-leg circuit used in Section V. Parasitic circuit elements are shown in thick lines.

direction indicated by the PWM signal. In each of these eight clock cycles, the six fine driver substages can be individually delayed (by 0 to 7 × 150 ps) and then activated for a selectable duration (0, 1, 2, 4, or 6 × 150 ps), to either pull up or down. This provides many degrees of freedom for the nominal driving sequence, one of which is illustrated in Fig. 5.

The parallel connection of the fine subdrivers forms a sequence of up to 11 resistance changes per clock cycle. The sequence for each of the eight clock cycles is independently programmable. In the example of Fig. 5, the gate driver is shown transitioning from pull down that holds a power device off to pulling up to a variable degree to shape a turn-on transient.

III. MODELING OF ACTIVE GATE DRIVING OF GaN FETS

This section studies whether the programmable driver output can adequately profile the gate-source voltage of a GaN power device despite the effect of the driver package, PCB tracks, and gate impedances of the GaN FETs creating a parasitic low-pass filter between the driver and the GaN FET, and further, whether the achievable profiling is adequate to shape the power-circuit switching waveforms with appreciable benefits.
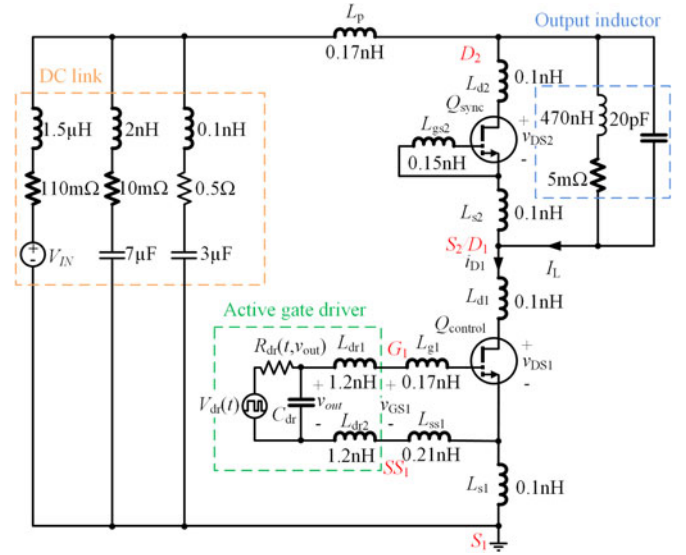
A GaN FET bridge-leg topology is selected as an evaluation platform for waveform shaping, as it incorporates a hard-switched control device and a soft-switched synchronous device in one circuit. Active gate driving can be applied to either or both devices. In this paper, the active gate driver is used to drive the control device only. The gate and source terminals of the synchronous device are shorted, resulting in the equivalent behavior of a body diode. It is reasonable to hold the gate of the synchronous device off, as both turn-on and turn-off current and voltage commutations happen between the control device and the equivalent body diode of the synchronous device.

A. Circuit Model and Extraction of Parasitics

The SPICE model equivalent to the real bridge-leg circuit in Fig. 2 and used in Section V is shown as in Fig. 6, with a view to investigating hard-switched GaN FET switching behavior under the influence of gate signal profiling. An active gate driver controls the low-side control GaN device. The parasitic elements considered are shown in thick lines.

The active gate driver is modeled as follows: A voltage source $V_{dr}(t)$ steps to 5 V for pull-up and back to 0 V for pull-down. There is an on-chip decoupling capacitance whose parasitic inductance is negligible; therefore, the parasitic inductance in the gate driver decoupling loop is neglected. $R_{dr}(t, v_{out})$ models the varying equivalent output resistance of the active MOS transistors. During pull-down, R_{dr} equals a third-order polynomial approximation of the voltage-dependent resistance R_{dr_s} of a single NMOS transistor, as shown in Fig. 4, divided by the time-varying number of driver unit cells in parallel (see Fig. 3). During pull-up, the scaled voltage-dependent output resistance of a unit pull-up PMOS transistor is used. In conventional gate drivers, this resistance includes an external gate resistor. In the case here, all resistance is contained on-chip. The driver output capacitance C_{dr} represents the capacitance formed by all NMOS
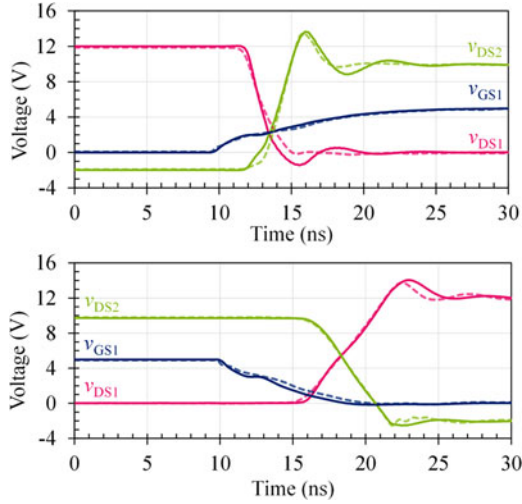
Fig. 7. Simulated (solid) and measured (dashed) switching waveforms for v_{GS1}, v_{DS1}, and v_{DS2} (Fig. 6). Top: turn-on transient with 4.5 Ω gate driving. Bottom: turn-off transient with 4 Ω gate driving.

Fig. 8. Representative switching waveforms of v_{GS1}, v_{DS1}, v_{DS2}, and i_{D1}, and the delineation of eight control phases.

and PMOS transistors in all output stages and is derived from post-layout simulation, the two resulting components being

$$C_{DS(NMOS)} = 10^{-10} - 10^{-11} \cdot V_{OUT} \quad (1)$$

and

$$C_{DS(PMOS)} = 10^{-10} - 10^{-11} \cdot (5 - V_{OUT}). \quad (2)$$

Based on these approximations, the sum of these capacitances is 150 pF and independent of voltage, which appears to be sufficiently accurate for the purpose of using in the model. This capacitance has a significant effect on the gate voltage waveforms prior to reaching the GaN FET's gate threshold. The parasitic inductances L_{dr1} and L_{dr2} of the driver package are extracted using Q3D Extractor and represent the bond-wire inductance. The remaining circuit components and layout-dependent parasitics of Fig. 6 are derived for the real circuit that is used to verify the simulations in Fig. 7 and to obtain the experimental results of Fig. 16 onward. The inductive load includes interturn capacitance, derived from the specified self-resonant frequency, and the dc-link capacitors are modeled with equivalent series inductance (ESL) and equivalent series resistance (ESR) as measured at 1 MHz with 10-V dc bias on a Wayne-Kerr 65120P impedance analyzer. A 0.5-Ω damping resistance is placed in series with the capacitance closest to the GaN devices. The GaN FETs are modeled using the EPC2015 Spice model available in [26]. The layout-dependent inductances of the power and gate loops are derived by creating a simplified geometric model of the circuit layout and device packages in Q3D Extractor. The model of Fig. 6 also shows nodes representing the Kelvin source connection (SS1) for the gate loop, and the source connection (S1) for the power loop. This separation reduces the effect of the parasitic source inductance, whose influence on switching losses is significant [19], [21].

The resulting model (see Fig. 6) is simulated in LTspice for load current flowing into the switch node. Fig. 7 shows the simulated switching waveforms compared to measured waveforms,
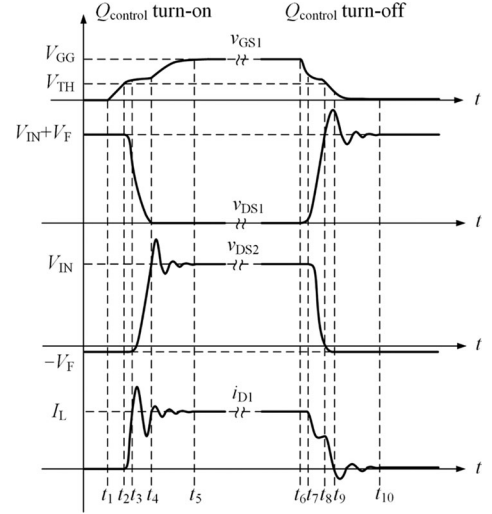
for constant-strength gate driving using a nominal 4.5 Ω for turn on and 4 Ω for turn off; it is worth recalling that constant nominal resistance settings do not provide a constant instantaneous resistance (see Section II-D).

It is apparent that delay times and overshoots are relatively accurate as are the trends and slopes; however, the damping and oscillation frequencies of the model appears to be slightly too low. This could be due to the omission of skin-effect models for the conductors. In the following, this model is used to illustrate the active gate driving strategy and find suitable resistance sequences.

B. Gate Driving Strategy

The aim of active gate driving here is to strike a better balance between power-circuit switching-waveform overshoot and the switching loss of the control device. Both the turn-on and turn-off of the synchronous device are soft-switched, generating negligible switching loss during the switching of the control device [21], and thus, the influence of active gate driving on losses in the synchronous devices is not considered in this paper.

A typical turn-on transition of $Q_{control}$ of Fig. 6 is shown in Fig. 8. It can be divided into four consecutive phases: turn-on delay time $(t_1 \ldots t_2)$, current rise time $(t_2 \ldots t_3)$, voltage fall time $(t_3 \ldots t_4)$, and oscillation time $(t_4 \ldots t_5)$. The overlap loss is roughly proportional to the duration of current rise time and voltage fall time [27]. In principle, a strong pull-up is needed for the duration of both intervals to reduce the switching loss; however, during the voltage fall, this increases the displacement current flowing through both devices, thereby exacerbating oscillation and switch-node overshoot in the final stage. A strong pull-up is also likely to incur gate voltage overshoot. This illustrates the limitations of a constant-strength driver. In contrast, active gate driving is able to choose the best driving strength in each of the phases. A general gate driving strategy for turn-on transitions is proposed.

Turn-on delay time ($t_1 \dots t_2$): The gate voltage is below the gate threshold voltage, Q_{control} remains off, and the gate driving strength affects primarily the duration of this phase. A strong pull-up is applied to reduce the delay time.

Current rise time ($t_2 \dots t_3$): The gate voltage controls the commutation of current from Q_{sync} to Q_{control}. As the drain current slew rate determines the current overshoot and oscillation in the next two phases, the pull-up strength is reduced slightly to slow down the rate of change of current while keeping the overlap loss low. Short durations of deviations from this average strength can be used to counteract ringing.

Voltage fall time ($t_3 \dots t_4$): The pull-up strength is further decreased at the beginning of this phase to reduce the voltage slew rate and the resultant displacement current flowing through Q_{control}. In order not to greatly increase the overlap loss, the pull-up strength is increased as v_{DS1} approaches zero.

Oscillation time ($t_4 \dots t_5$): After v_{DS1} reaches steady state, the gate driving strength does not affect the oscillation and overshoot in i_{D1} and v_{DS2}. If necessary, the pull-up strength is briefly reduced to prevent gate overshoot. Afterwards, the pull-up strength is increased to hold the device on.

Likewise, a general gate driving strategy for turn-off transitions is proposed.

Turn-off delay time ($t_6 \dots t_7$): The gate voltage is still above the value where Q_{control} would exit the ohmic region, and the gate driving strength affects mainly the duration of this phase. A strong pull-down strength is applied to reduce the delay time.

Voltage rise time ($t_7 \dots t_8$): The device exits the ohmic region, and the gate voltage controls the voltage slew rate of v_{DS1} as long as the channel remains on. A strong pull-down would turn the channel off quickly, leaving the voltage slew rate to be determined by the load current and nonlinear parasitic capacitance at the switch node. Load current is shed into Q_{sync} to discharge its output capacitance, which reduces overlap loss. Therefore, a driving strength is sought that is strong enough to reduce loss but that does not turn off the channel and thereby lose control of the switching. If this does occur, control can be regained by weakening the pull-down or by momentarily pulling up.

Current fall time ($t_8 \dots t_9$): A weak pull-down is applied at the beginning of this phase to reduce the current slew rate and the resultant voltage overshoot in v_{DS1}. In order not to greatly increase the overlap loss, the gate driving strength is increased as v_{DS1} approaches the peak.

Oscillation time ($t_9 \dots t_{10}$): After v_{GS1} falls below the threshold voltage V_{TH}, gate driving strength does not affect the oscillation or overshoot in i_{D1} and v_{DS1}. If necessary, the pull-down strength is briefly reduced to prevent gate undershoot. Afterwards, a strong pull-down is applied to hold the device off.

C. Simulated Application of the Active Gate Driving Strategy

Fig. 9 shows turn-on switching waveforms for two constant-strength and one active gate-driving scenarios. The turn-on switching loss [27]

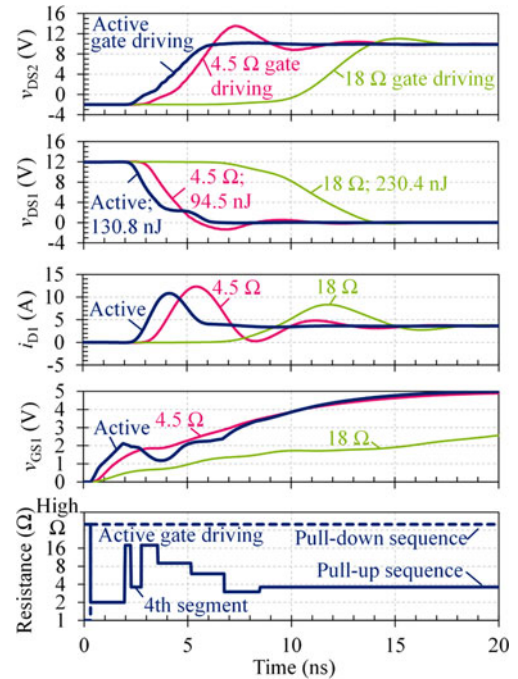$$E_{\text{sw\_on}} = \int (i_{D1} \times v_{\text{DS1}}) \, dt + E_{C_{\text{oss}}} \qquad (3)$$

Fig. 9. Simulated turn-on waveforms, with constant-strength gate driving (4.5 and 18 Ω), and active gate driving (nominal resistance sequence plots at bottom) to eliminate the overshoot.
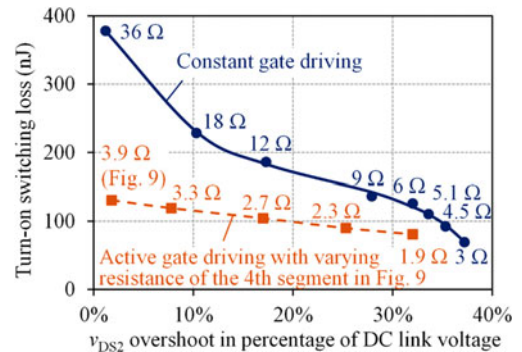

Fig. 10. Simulated v_{DS2} overshoot versus turn-on switching loss with constant and active gate driving.

of each scenario is calculated, and provided in the line labels of the v_{DS1} graph in Fig. 9. The energy $E_{C_{\text{oss}}}$ that is stored in the output capacitance of the device in its off state can be derived through simulation or using the datasheet [20]. Driving the lower control GaN FET with 4.5 Ω gate drive resistance results in 35.3% voltage (v_{DS2}) overshoot on the upper synchronous device. Increasing the drive resistance to 18 Ω increases switching loss by 143.8% but only reduces the overshoot to 10.3% of the rated voltage. The active gate driving strategy is shown at the bottom of Fig. 9. A low nominal resistance is applied for the first 1.6 ns of the switching transition to reduce the turn-on delay time and current rise time. An increase of the resistance in the subsequent 1.6 ns suppresses v_{DS2} overshoot, with momentary application of a lower value to optimize the switching waveform by activating fine driver pull-up in the
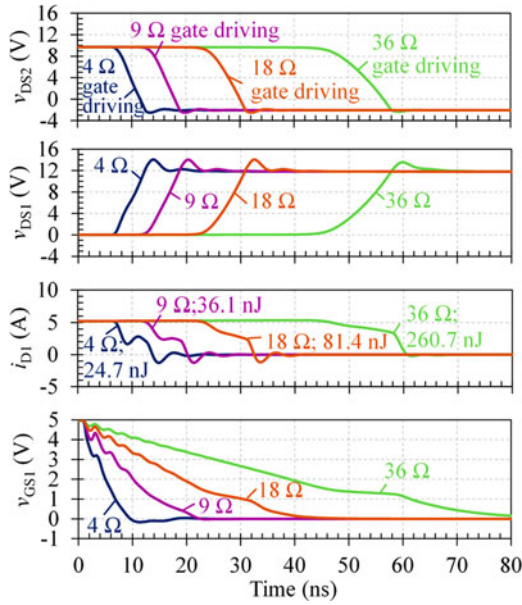
Fig. 11. Simulated turn-off switching waveforms with different constant gate driving strengths.

fourth segment. The final gradual decrease of drive resistance prevents in-circuit oscillation while providing a strong pull-up for the remaining on state. This strategy is seen to eliminate the overshoot, however, with an increase in switching loss by only 38.4%. This is a significantly better trade-off of overshoot against switching loss than 18 Ω constant driving. It is also observed that active gate driving has eliminated the oscillation in the displacement current, see the graph of i_{D1} in Fig. 9, at the expense of additional spectral content in the shaped gate voltage waveform v_{GS1}.

Fig. 10 plots v_{DS2} overshoot against turn-on switching loss, for both constant and active gate driving. The constant gate driving strength is swept from 36 to 3 Ω, and the active gate driving results are obtained by sweeping the value of the fourth segment of the sequence (starting at 2.3 ns in Fig. 9) from 3.9 to 1.9 Ω, where 3.9 Ω provides the waveforms of Fig. 9 and the lowest overshoot. It is apparent that active gate driving is the more efficient way of reducing overshoot.

Fig. 11 shows turn-off switching waveforms for 4, 9, 18, and 36 Ω constant driving, and their respective turn-off switching loss [27]

$$E_{sw\_off} = \int i_{D1} \times v_{DS1} dt - E_{C_{oss}} \qquad (4)$$

which is provided in the line labels in the i_{D1} graph.

Slowing the turn-off of $Q_{Control}$ using the 9 or 18 Ω settings has little effect on its voltage overshoot v_{DS1}. This is because the channel is turned off before the overshoot begins, as seen by the absence of a gate-voltage Miller plateau. From this point onward, the voltage gradient dv_{DS1}/dt is determined solely by the load current charging the nonlinear GaN FET output capacitances. The weakest gate drive strength (36 Ω) reduces the overshoot by 24.3%, as here the channel remains on until the overshoot; however, the switching loss has increased tenfold
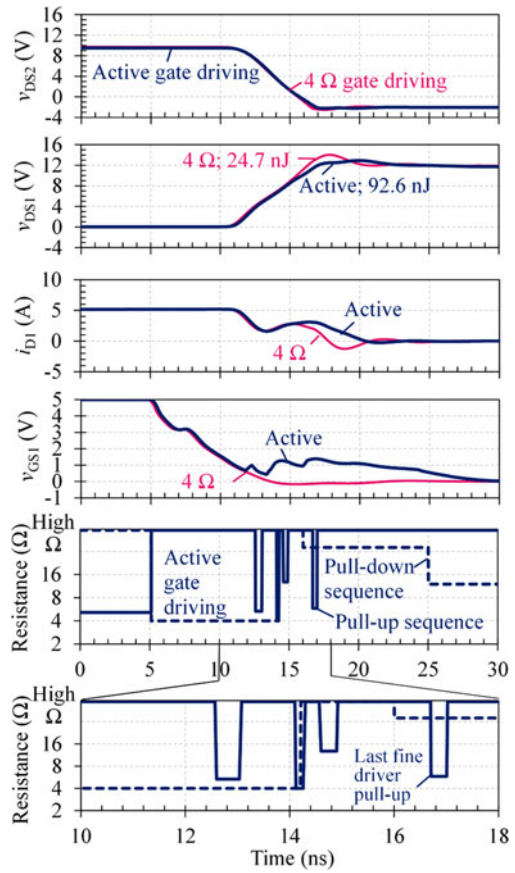

Fig. 12. Simulated shaping of turn-off waveforms using active gate driving compared to constant gate driving.

with respect to the 4 Ω switching. It follows that increasing the gate resistance is an unsuitable means of reducing turn-off voltage overshoot in this scenario.

Fig. 12 shows turn-off shaped by active gate driving, against the 4 Ω constant driving waveforms. The active gate driver loses control over turn-off at around 10 ns when the gate signal passes through the threshold voltage, and the v_{DS} transients begin. The driver regains control of the device at around 15 ns after the driver has been in a high-impedance state for 1.8 ns and Miller current has raised the gate voltage. The v_{DS1} overshoot is reduced by 54.6%, with no apparent slowing of the switching, and a 2.7 times increase in switching loss. This is a marked improvement over the constant drives of Fig. 11. The fact that the delay time does not increase using this method means that short dead times can be maintained, minimizing the time during which significant reverse conduction loss is incurred in the synchronous GaN FET [19], [21].

Fig. 13 shows turn-off loss of the control device against v_{DS1} voltage overshoot, for both active and constant gate driving. The active gate driving points are obtained by varying the driving strength of the last fine driver pull-up in the resistance sequence in Fig. 12 from 5.8 to 32 Ω, where 5.8 Ω provides the waveforms of Fig. 12 and the lowest overshoot. It is apparent that the active gate driving strikes a better balance between v_{DS1} overshoot and turn-off switching loss.
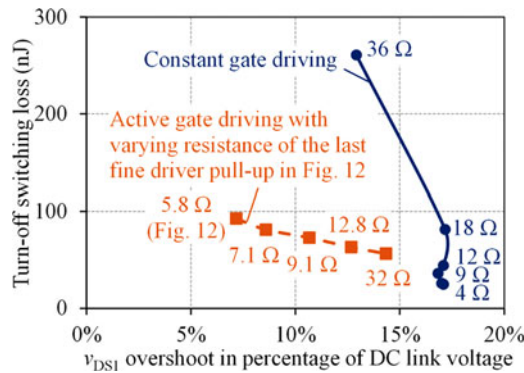
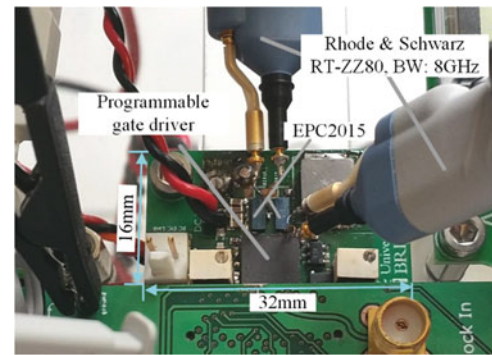Fig. 13.   Simulated turn-off switching loss versus v_{DS1} overshoot.

Fig. 14.   Detailed view of the test circuit and measurement probes. Not shown is the 2-GHz RT-ZD30 probe connected to the underside of the power board to measure v_{DS2}.

IV. SYSTEM IMPLEMENTATION FOR ACTIVE GATE DRIVING OF GAN FETS

To test active gate driving in GaN-based converters, a bridge leg of two EPC2015 GaN enhancement-mode FETs is used (see Fig. 2). This circuit replicates the device interaction and hard-switching transitions of a synchronous buck converter.

In contrast to the classic clamped-inductor circuit used for double-pulse testing, the load here contains R_o and C_o to facilitate continuous operation where the duty cycle of the PWM signal determines the test current level. This allows the accurate measurement of total circuit loss via the dc input and output values. In addition, the load is referenced to the high side, which places $Q_{control}$ on the low side; and therefore, measurements of gate and device voltages do not have common-mode components. This also permits a ground-referenced gate drive interface. For simplicity, the gate and source terminals of the top GaN FET Q_{sync} are shorted, since the driving of $Q_{control}$ actually determines the current and voltage commutations of both devices. Note that v_{DS2} is equivalent to the switch-node voltage of a synchronous buck converter.

Near-constant dc-link and gate-drive supply voltages are provided by carefully designed bypass networks incorporating high-frequency damping. The PCB design is optimized following recommendations in [17] to minimize loop inductance. The circuit board is composed of four layers with 2-ounce copper thickness. The overall board thickness is 0.5 mm. The distance between the top copper layer and the first inner layer is 95 μm. The simulated in-circuit power loop inductance is 0.57 nH. Such a low parasitic inductance is required to fully utilize the switching capability of the GaN devices [17]. A higher inductance would worsen the switching waveforms, but would not affect the feasibility of active gate driving.

Fig. 14 shows the power board under test. This test circuit is switched continuously at 1 MHz in order to obtain periodic switching waveforms for frequency-domain analysis. It also allows the circuit to reach thermal equilibrium before performing data capture, which is verified using a Fluke E30 thermal camera.

The test facility is shown in Fig. 15. The PC sends the desired gate drive sequences to a Digilent Zedboard FPGA development board, which programs the gate driver IC. Once programmed, the gate driver is fully autonomous. The programmer uses its
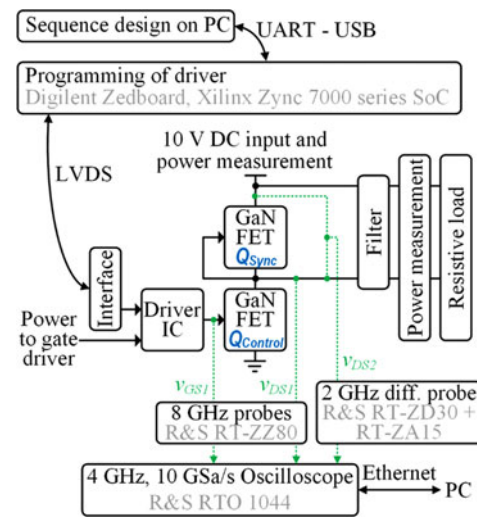

Fig. 15.   Test facility with driver programming, and power and signal measurement.

ARM CPU on the Xilinx SoC to communicate with the host PC, to allow the user to change resistance sequences. When a new sequence is sent to the programmer, the PWM signal is interrupted, the gate driver output disabled, new sequences programmed to the driver, the driver re-enabled, and the PWM signal resumed. This control sequence takes place in a few hundred milliseconds.

A pair of 8 GHz Rhode & Schwarz RT-ZZ80 transmission-line probes measure v_{GS1} and v_{DS1}, while a 2 GHz Rhode & Schwarz RT-ZD30 active differential probe with RT-ZA15 attenuator captures v_{DS2}. MATLAB, running on the host PC, configures the 4 GHz, 10 GSa/s Rhode & Schwarz RTO1044 oscilloscope to trigger on v_{DS2} rising edges, and to capture and average 8,192 consecutive waveforms in order to lower the measurement noise floor [8]. The process is repeated for v_{DS2} falling edges. A complete pulse train is reconstructed in MATLAB for analysis.

The overall power circuit loss is calculated by subtracting the measured output power from input power. Input power is calculated from dc input voltage and current, measured using TTi 1604 and Fluke 8845A multimeters. Output power is calculated from dc output voltage and current, respectively mea-
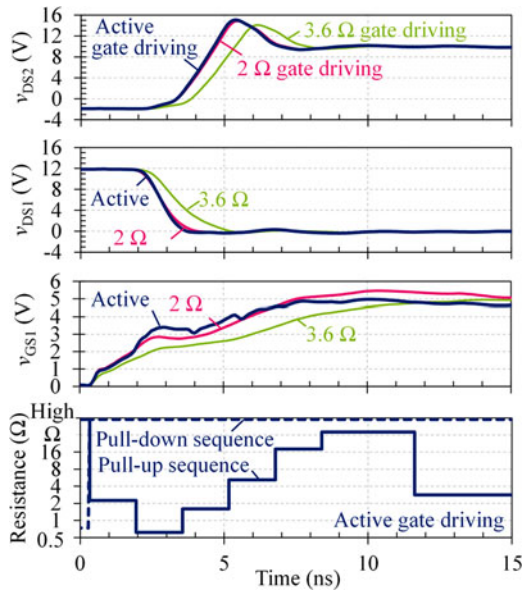
Fig. 16. Measured turn-on switching waveforms showing reduction of gate overshoot by active gate driving.

Fig. 17. Measured v_{DS1} 97%–3% fall time versus gate overshoot for the control GaN FET under constant-strength and active gate-driving scenarios.

Fig. 18. Measured turn-on switching waveforms and power-circuit losses, showing elimination of v_{DS2} overshoot without increased loss, by means of active gate driving.

sured using Keysight U1273A and Fluke 8845A multimeters. The nominal absolute accuracy of the input and output power measurements are each of the order of 100 mW; however, the majority of this is due to temperature dependency of the equipment. Therefore, groups of measurements that are compared in Section V are carried out in quick succession at the same temperature. It has been verified that the relative changes in loss as a function of gate driving strategy are repeatable and consistent.

V. EXPERIMENTAL RESULTS

A. Experiment 1: Speeding Up Turn On

The aim of this experiment is to demonstrate that active gate driving can suppress gate voltage overshoot and, therefore, allow faster driving than is possible with constant-strength driving. Fig. 16 shows the measured turn-on switching waveforms for three gate-driving scenarios: constant 3.6 and 2 Ω driving and active gate driving, whose nominal resistance sequences are shown in the bottom graph of Fig. 16.

3.6 Ω driving provides the fastest turn-on speed of the control GaN FET with no visible overshoot at the gate. 2 Ω driving is seen to not only speed up the switching but also lead to a gate-voltage overshoot to within 0.5 V of the GaN FET's absolute-maximum gate-source voltage of 6 V. The active driving strategy eliminates the gate voltage overshoot while maintaining the speed of 2 Ω driving. The active gate driving strategy of Fig. 16 shows the driver resistance being changed at the frequency of the internal clock using the main drivers only. The maximum time during which changes can be made is eight clock cycles, and in this case, seven changes are made. It is apparent that no subclock changes are made; the fine drivers are inactive. The transition starts with a low resistance, to switch the control device as fast as possible. The resistance is then increased to introduce damping
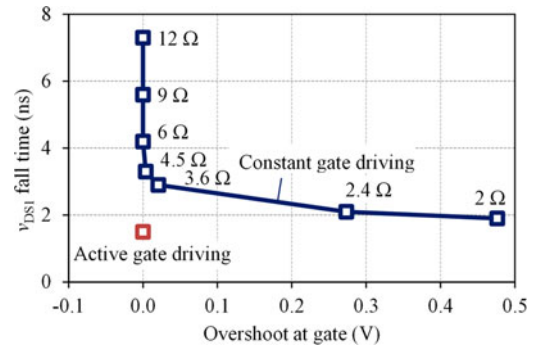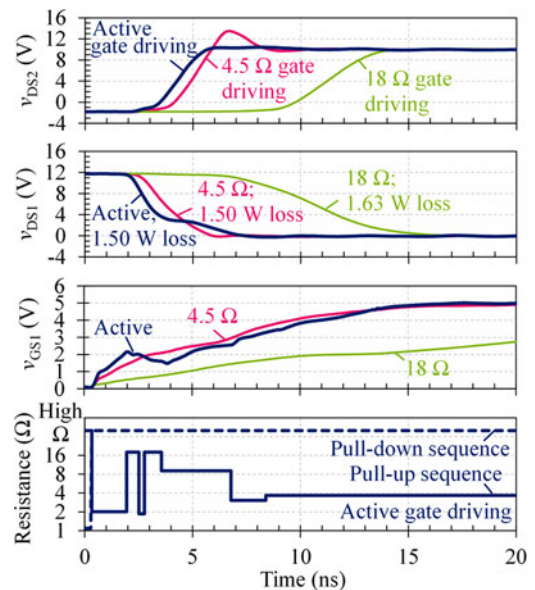
into the gate-drive loop. The result is that active gate driving has allowed the speed of 2 Ω driving to be combined with the gate voltage overshoot of 3.6 Ω driving. This is also shown in Fig. 17, where the measured 97%–3% fall time of v_{DS1} is plotted against voltage overshoot at the gate, for a range of constant driving strengths, and the active gate driving sequence of Fig. 16. Active gate driving achieves a power device switching edge that is faster than constant drive resistances down to 2 Ω while avoiding the overshoot that the lower resistances incur.

B. Experiment 2: Elimination of Switch-Node Voltage Overshoot

The aim of this experiment is to demonstrate how turn-on of the low-side control device can be shaped to eliminate device voltage v_{DS2} overshoot on the high-side synchronous device, which is the equivalent of the switch-node waveform of a synchronous buck converter. Fig. 18 shows measured turn-on switching waveforms for three gate-driving scenarios: constant 4.5 and 18 Ω driving and active gate driving. The line labels in
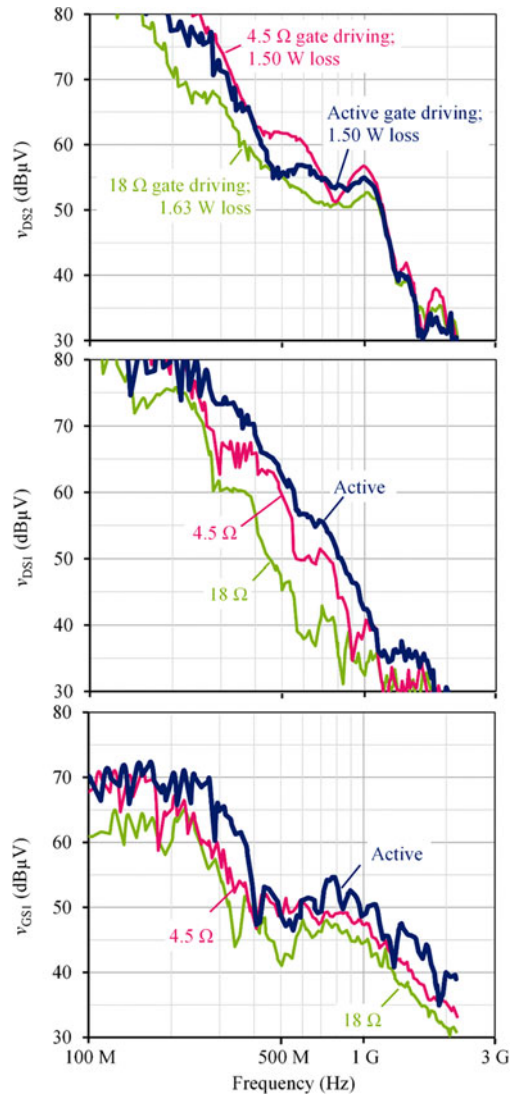
Fig. 19.   Spectral envelopes, calculated from the measured time-domain data of complete switching cycles, for the three gate-driving scenarios in Fig. 18.

the v_{DS1} graph also include the measured power-circuit loss for the respective operating condition. Constant-strength driving is used for the turn-off edge (not shown), with a value of 4 Ω in all three scenarios.

18 Ω constant gate driving incurs no v_{DS2} overshoot. Any lower resistances show overshoot, with the 4.5 Ω driving producing a significant overshoot of 4 V, with a reduction in delay by 5 ns, however. The increased speed reduces switching loss, as evidenced by the total circuit loss dropping by 8% from 1.63 to 1.50 W. The net reduction in turn-on switching loss is more than 8% as these power values include other constant losses, such as those incurred at the turn-off edge and the conduction loss of Q_{sync} with a shorted gate. It is also worth noting that for 1 MHz switching, approximately 0.12 W of loss is due to the C_{oss} of the GaN FETs, which is independent of the speed of the transients and which therefore puts a lower bound on switching loss. In this experiment, faster switching is possible but does not noticeably reduce total loss.

In contrast to Experiment 1, the active gate driving sequence now uses one fine driver activation at 2.5 ns, when the resistance is seen to change for 300 ps within a 1.6 ns clock period. The turn-on sequence starts at 2 Ω, to reach the threshold voltage quickly, which is the reason that the switching delay is reduced by 1 ns relative to constant 4.5 Ω driving. The drive resistance is then increased to slow the switching transition, with the fine drivers briefly adjusting the drive strength in order to optimize the shape of the switching waveform. The drive resistance is then reduced, to ensure the switching transition is completed fast enough to not incur excessive loss but slow enough not to excite any power-circuit resonances. The result is a control-device switching transient as fast as the 4.5 Ω constant-strength case but with no v_{DS2} overshoot, 20% lower delay, and no increase in total measured loss.

Frequency transformations of the time-domain data of Fig. 18 are shown in Fig. 19. The high-frequency spectral content of the v_{DS2} signal has a special significance in terms of the potential EMI generation. This is because the v_{DS2} signal is equivalent to the switch-node voltage of a buck converter, which would be connected to an output filter and load. At high frequencies, output filters can have reduced effectiveness due to parasitic circuit elements, especially the parasitic capacitance of the choke [28]. The output filter, load, and their interconnection can therefore form a structure which may radiate the high-frequency content that the output filter fails to attenuate. Consequently, a reduction in the high-frequency content of this signal can be beneficial from an EMI perspective.

The inverse relationship between loss and high-frequency spectral content of the v_{DS2} is apparent for constant-strength driving. Active gate driving alters this relationship by having the same loss as the faster constant-strength driving, but with reduced spectral content of v_{DS2} on visual inspection, over most of the spectrum, but in particular in the regions of 400 to 700 MHz and 900 MHz to 1.1 GHz. It is worth considering that these spectra include the contribution of turn off, which reduces the visible net influence of active gate driving on a single edge. It is also worth noting that the simulation results of Fig. 9 indicate that overshoot and subsequent ringing in the device current i_{D1} are reduced as well.

This improvement comes at the expense of increased spectral content in the v_{GS1} and v_{DS1} signals. As these signals are internal to the circuit, their associated trace lengths can be kept short relative to the electrical wavelength, and therefore, these signals are unlikely to be radiated efficiently. It is beyond the scope of this paper; however, a valuable area of future research could be to explore the transfer of high-frequency content between internal signals and the switch-node voltage and how this would affect EMC compliance, dependent upon the specific hardware layout and resultant parasitic radiative and conductive structures of particular converters.

Fig. 20 illustrates the influence of the fine driver by showing the results of Fig. 18 against a strategy where the fine driver is not activated. The fine driver is seen to bring the shape of v_{DS2} closer to the optimum smooth S-shape [9]. The high time resolution of the fine driver is instrumental in achieving this.
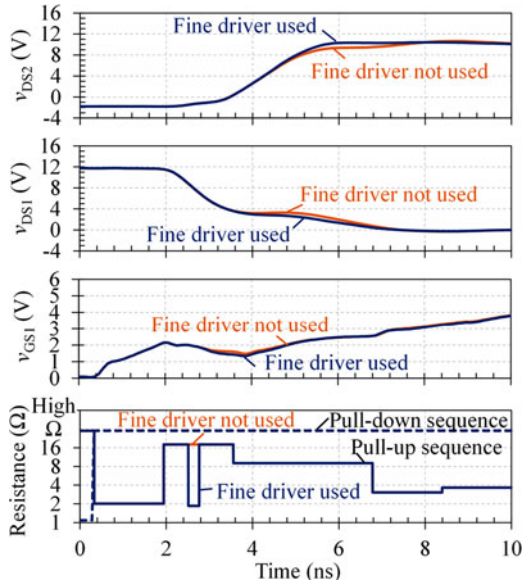
Fig. 20.   Comparison of waveform shaping with and without use of the fine driver.
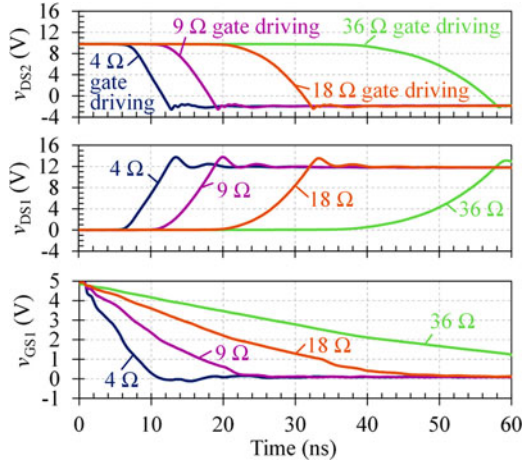

Fig. 21.   Measured turn-off switching waveforms for a variety of constant gate-driving strengths.
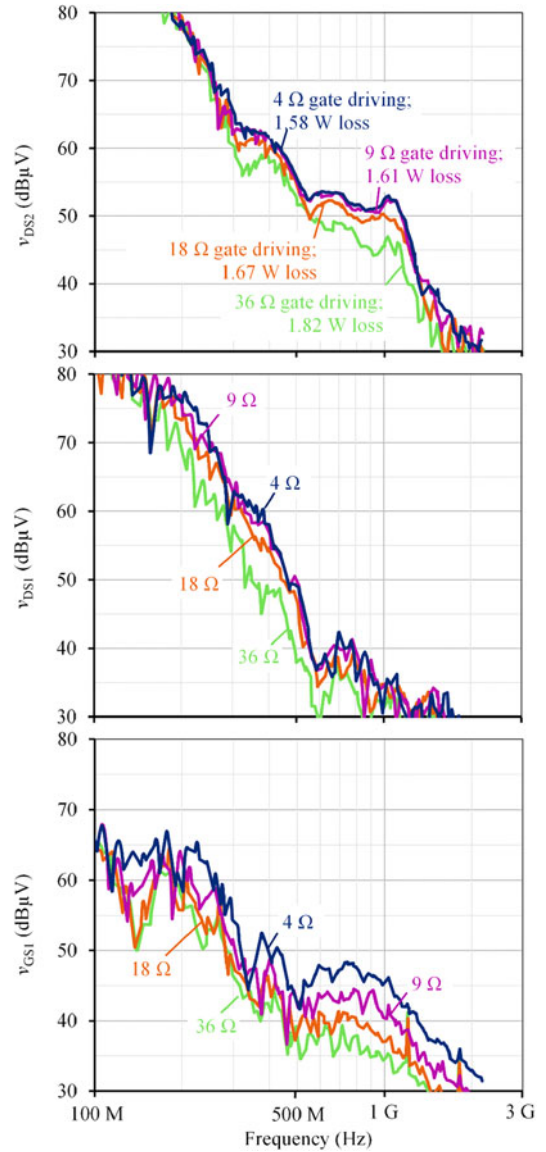

Fig. 22.   Spectral envelopes, calculated from the measured time-domain data of complete switching cycles, for the four gate-driving scenarios in Fig. 21.

C. Experiment 3: Reduction of the High-Frequency Spectrum of the Switch-Node Voltage

The aim of Experiment 3 is to shape the turn-off edge to reduce high-frequency spectral components of the switch-node waveform v_{DS2}. Fig. 21 shows the measured turn-off switching waveforms for four situations: 4, 9, 18, and 36 Ω constant driving.

4 Ω driving shows a turn-off voltage overshoot on v_{DS1} and a sharp undershoot on v_{DS2}. It is apparent that the gate voltage has dropped below the gate threshold voltage of around 1.5 V, turning the channel off, prior to the rise in device voltage. Therefore, the gate driver is not in control of the device voltage transients. These are instead set by the load current charging the GaN devices' voltage-dependent output capacitances. With increasing gate resistance, the point where loss of control occurs moves to later in the device voltage transients, leading to the gradi-

ent of v_{DS1} being reduced until this point. At 9 Ω and below, the gradient and voltage overshoot on v_{DS1} are independent of gate resistance. With 36 Ω driving, control is maintained until half way into the v_{DS1} rising edge, and therefore, a reduction in the gradient of the entire voltage rise and a slight reduction in overshoot are obtained. As drive resistance increases from 4 to 36 Ω, a significant increase in switching delay is observed. This is due to an increase in the time taken to discharge the control device's gate capacitance to the voltage required to exit the ohmic operating region.

Frequency transformations of the time-domain data of complete switching cycles are shown in Fig. 22. Constant-strength driving has been used for the turn-on edges (not shown in Fig. 21), with a value of 12 Ω in all four cases. The line labels in the v_{DS2} graph also include the measured power-circuit loss for the respective operating condition.
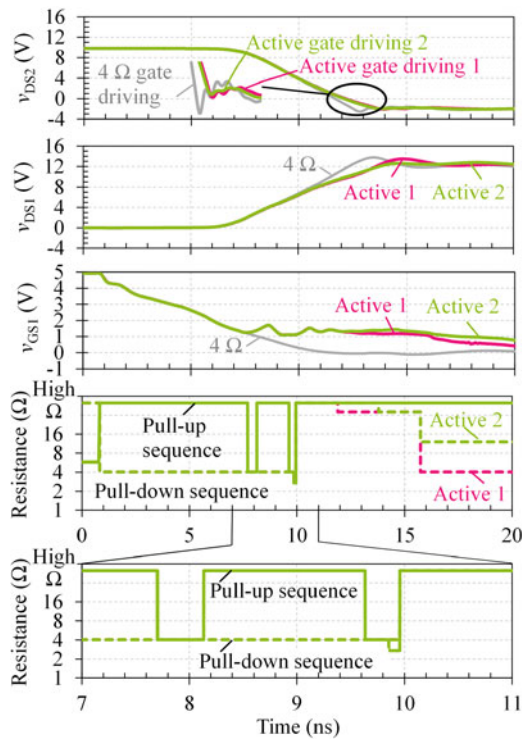
Fig. 23. Measured turn-off switching waveforms under constant-strength and two active gate-driving sequences. The inset in the top graph shows the detail of the end of the switching transition. The bottom trace shows a horizontal zoom of the active gate-driving strength sequence.

The results demonstrate the inextricable inverse relationship, when constant-strength gate driving is used, between circuit loss and high-frequency content of the switch-node voltage. To reduce the EMI generating potential of the circuit, an increase in circuit loss must be accepted.

The 4 Ω transition in the time domain v_{DS2} waveform starts smoothly but has an abrupt end, accompanied by high-frequency ringing, both of which are now targeted by active gate driving as follows: In order for the control device to have influence over the final part of the switching trajectory, it is momentarily turned back on. Fig. 23 shows the measured time-domain waveforms for the turn-off transition under fixed 4 Ω driving (identical to Fig. 21) and for two active gate driving sequences.

The sharpness and ringing in the v_{DS2} waveform and the overshoot in v_{DS1} have been visibly reduced. In order to be able to reactivate the control device at the end of the transient, the gate driver's internal clock period is 2.1 ns. Both active gate-driving sequences contain two fine driver activations which pull up, that is, in opposition to the polarity indicated by the PWM signal. This is seen to reverse the gradient of the control device's gate-source voltage. Just prior to the 10 ns time point, the main drivers are switched into a high-impedance state in order to maintain the gate-source voltage. The two active gate-driving scenarios differ only in the main driver strengths used from 12 ns onward. The zoomed inset in the top graph shows how these active gate drives significantly reduce both the amplitude of the initial undershoot and the high-frequency oscillations in v_{DS2}. The benefits of active gate driving are clearly observable in the frequency domain,
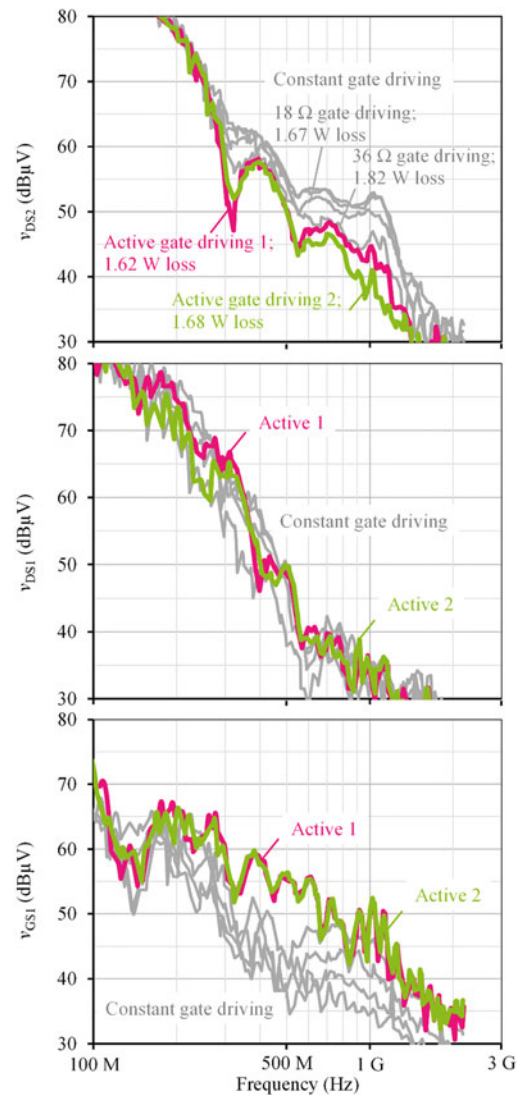

Fig. 24. Spectral envelopes, calculated from the measured time-domain data of complete switching cycles, for the four gate-driving scenarios in Fig. 21 and the two active gate-driving scenarios in Fig. 23.

as shown in Fig. 24. Also shown here are the power-circuit losses under each gate-drive scenario. As before, the turn-on edges are driven with a constant 12 Ω in all three cases.

Active gate driving is seen to reduce the spectral content of the switch-node-equivalent waveform v_{DS2} by up to 15 dB over a significant proportion of the spectrum. Most notably, the spike around 1 GHz has been lowered by 8–13 dB with respect to the 4 Ω driving, depending on which of the two active gate-driving sequences is used. Active gate driving 1 incurs high-frequency content equal to or better than that achieved with fixed 36 Ω driving but with additional loss of 40 mW—an increase of 2.5% of the total circuit loss. Active gate driving 2 results in high-frequency content well below that of 36 Ω driving, and loss has increased by 100 mW or 6%. Both active gate driving sequences maintain the switching delay of 4 Ω driving. Therefore, active gate driving is able to reduce high-frequency spectral content occurring at turn-off where an increase in constant gate driving would have little effect, without additional

delay or significant losses. It should be noted that as with the turn-on transition, there is an increase in spectral content on the gate signal v_{GS1}. This method also requires a gate driver with sufficient active duration to target the end of a transient, and the ability to pull in both directions during a transient.

VI. CONCLUSION

Active gate driving of a 40 V, 3.2 mΩ GaN FET has been demonstrated for both turn-on and turn-off transitions, using a silicon integrated active gate driver, whose output resistance and direction of pull can be programmed to change up to 88 times and with a 150 ps resolution, during each switching transition. A SPICE modeling method that takes into account circuit layout and component and device parasitics is shown to behave with sufficient high-bandwidth accuracy to analyze the impact of 150 ps resolution active gate driving sequences. An active gate driving strategy is proposed and tested with this model. Experimental results show that gate voltage overshoot can be eliminated. This allows the switching speed to be increased without running the risk of damaging GaN gates that have a limited voltage margin. Drain-source voltage overshoots at turn-on and turn-off are also eliminated or reduced, without an increase in switching loss. The high-frequency content of the switching waveforms that correspond to the switch-node of a synchronous buck converter has been reduced at both turn on and turn off. This has brought about a smaller increase in switching loss (2.5%) than if the fixed gate resistance is increased. The high-frequency content of the complimentary v_{DS} and gate signal has increased; however, this is a worthwhile trade-off, as these two signals are internal and less prone to causing radiation. Simulations show that active gate driving can also reduce the overshoot and ringing in current waveforms.

Generally, it has been shown that, with respect to constant-strength gate driving, active gate driving for 40 V GaN FETs provides favorable trade-offs between overshoots, oscillations, circuit losses, switching delay, and high-frequency spectral content of both voltage and current. The gate driver can be implemented as a separate silicon driver, rather than integrating the driver onto the GaN FET.

Further work will include the application of algorithms such as those in [28] to optimize and adapt drive resistance sequences in real time and the application of the driver to 650 V GaN FETs.

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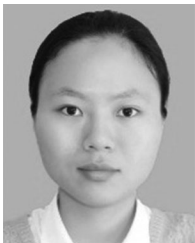
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