Lifetime-Based Power Routing of a Quadruple Active Bridge DC/DC Converter

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***Abstract*—Medium-voltage dc/dc converters have recently acquired importance in the smart grid and dc distribution framework. However, several open issues remain with regard to the reliability of such systems. This paper proposes a modular isolated dc/dc converter with multiple quadruple active bridge building blocks. This design, in combination with a virtual resistor-based control, weights the paths depending on the components wear-out and can balance the stress of the semiconductors in the attempt of extending overall system lifetime. The effectiveness of the approach is demonstrated in simulations and supported with measurements on a small-scale demonstrator with open modules, built in order to verify in real time the capability of controlling the thermal stress of the semiconductors.**

***Index Terms*—DC-DC power converters, power transformers, smart grids.**

I. Introduction

THE increase of decentralized energy production challenges the actual distribution grid [1], [2]. In many countries, the generation and the consumption are spatially separated and the energy, often produced by stochastic sources, needs to be transferred over a long distance [3]. This calls for new concepts to transfer the power without overloading the grid feeders, allowing the integration of storage and new loads, such as electric vehicles charging stations [4].

In the current configuration, the transformers are passive devices, which do not enable active grid management and the integration of storage. To address the current and the future system level challenges, there is a trend to install more intelligent devices in the grid to enable new grid services [5]. In this framework, dc/dc converters with high step-up ratio represent the key for the implementation of solid-state transformers (SST), which can regulate reactive power, active power (to a certain extent) for the optimization of grid feeders, integrate storage, and interact with the distributed energy sources [6]. The most adopted way in the literature to solve this task is to realize series/parallel structures based on single-input single-output dc/dc converters with high-frequency transformers [7], such as the dual active bridge (DAB) [8].

Also, resonant converters, such as the series-resonant converter (SRC) or the *LLC* converter, can be adopted to this aim. In particular, given the open-loop voltage stability of the SRC, this solution has been adopted in SST concepts [9].

Recently, the development of modular multilevel converters (MMC) has pushed researchers to extend their use even to the dc/dc realm, where an MMC leg can be used as a quasi-two-level cells operating with high voltage [10]. Push–pull configurations of the MMC operating as a dc/dc converter are reported too [11].

This paper presents a modular dc/dc converter based on multiport cells that are connected in series and in parallel, in order to have multiple paths through which the power can be routed. A power sharing technique between the cells is then proposed, with the aim of relieving the stress from the most deteriorated cells. In fact, while modular structures can be made fault tolerant either at system or at cell level [12], the novelty of this approach is that the control tries to delay the time of the failure by shifting the thermal stress to the healthier part of the converter. The proposed solution is described, analyzed, and simulated at system level, where the iteration among multiple building blocks is shown. A simulation showing the long-term effects on a single building block is carried out, and an experimental setup is built to confirm the latter result.

This paper is organized as shown in Fig. 1. Section II describes a possible application of the dc/dc converter to an SST. Sections III and IV deal with the control. Section V investigates the operation of the dc/dc stage in the medium voltage (MV) structure and, Sections VI and VII demonstrate the approach on a system level as well as for a building block for the proof of the concept. Finally, Section VIII draws the conclusion.

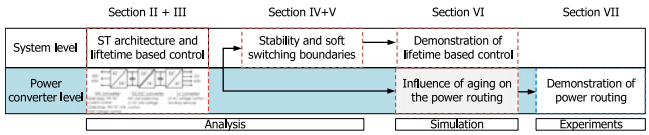

Fig. 1. Structure of the proposed work from analysis to simulations and experimental results.

II. SST Architecture and Basic Control

For this paper, a three-stage SST [6] is chosen, and a basic drawing is reported in Fig. 2. The availability of dc-links in both

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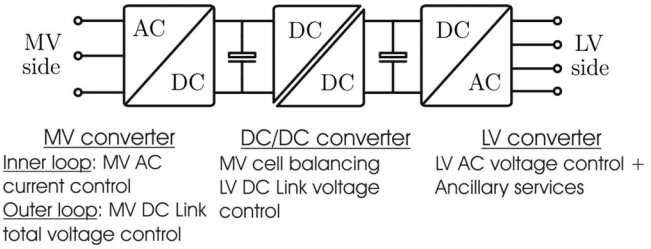

Fig. 2. Schematic architecture of the three-stage SST with the control objectives of each stage.

MV and low voltage (LV) side allows us to provide services to both MV and LV grid. Each converter controls a specific variable: The LV converter implements a voltage closed-loop control to ensure optimal voltage waveforms with low THD. The dc/dc converter controls the LV dc-link voltage, ensuring a stable supply for the LV converter. It also performs the balancing of the MV cells. Finally, the MV converter implements the MV ac closed-loop current control in order to regulate the total MV dc-Link voltage. For MV converter topologies that do not feature a common dc-link, the sum of the MV dc-link can be controlled instead of the total voltage.

This paper is focused on a specific modular architecture of the high-frequency dc/dc stage, that is based on multiple quadruple active bridge (QAB) converters [13], [14]. The concept can be extended to an arbitrary number of ports [15]. For increased flexibility, the separate control of the phases in the MV and LV is considered, and cascaded H-bridge (CHB) are considered in the MV. The dc/dc stage is composed of multiple QABs connected to a LV full bridge (FB) and to the CHB cells. A detailed example of the interconnections between the QABs and the CHB is reported (for one phase only) in Fig. 3. The LV ac inverter is omitted in the drawing, since it is not the focus of this paper. The two LV dc-links can be connected to separate three-phase converters or together to constitute the dc-link of a monolithic three-phase converter. In the figure, different colors describe different connections to the LV dc-links, highlighting the specific connections between the MV and LV dc-links. A change in V_2^{MV} can directly affect V_1^{LV} (direct connection), while a change in V_1^{MV} will affect both V_1^{LV} and V_2^{LV}. This basically means that the power from V_2^{MV} can be directly routed only to V_1^{LV}; in the case power from V_2^{MV} needs to be routed to V_1^{LV}, an intermediate step is needed, where the MV ports of the QAB exchange power among themselves. Many degrees of freedom for the connections are present, depending on physical constraints (insulation voltage of the secondary windings) or the degree of imbalance that is expected from the LV dc-links, to optimize a specific operating point. The optimization of the connections of the dc-links is object of future research.

The QAB schematic is shown in Fig. 4(a), along with the idealized waveforms in (b). In this figure, the conditions $V_b^{\mathrm{DC}} = V_c^{\mathrm{DC}} = V_d^{\mathrm{DC}}$ and equal phase shift are assumed; the QAB behaves exactly like a DAB and i_a results from the equal contribution of the other ports. The phase-shift modulation represents the simplest choice and a good solution if wide voltage variations do not happen in normal operating condition. One of

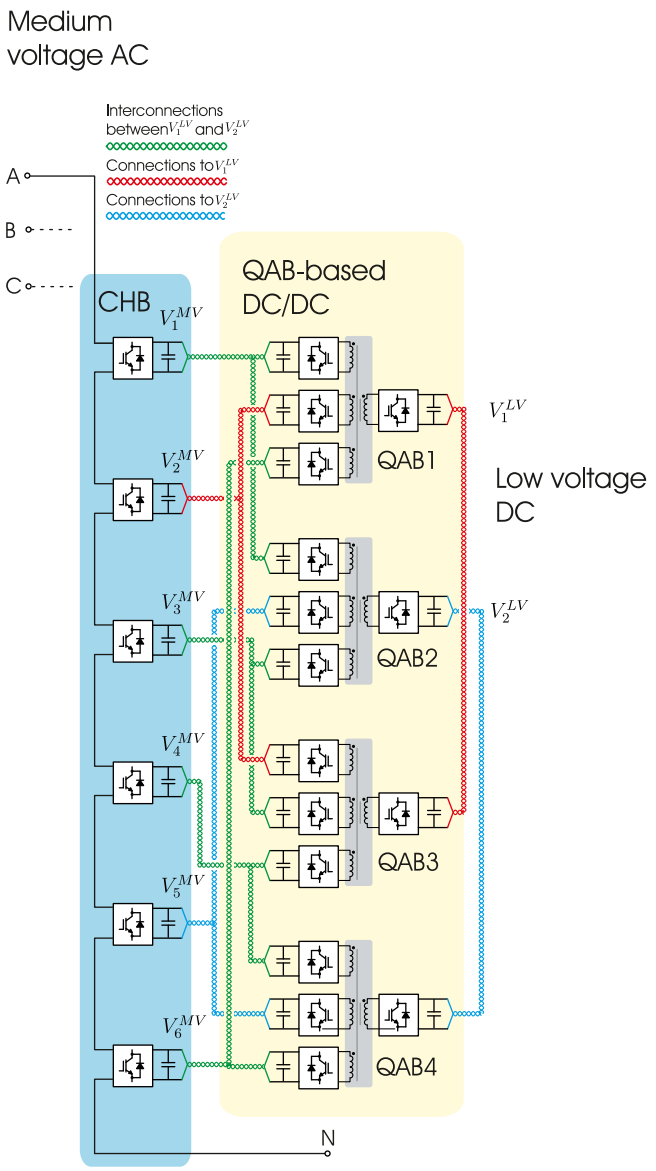

Fig. 3. Proposed architecture of smart transformer. The power paths between MV and LV are highlighted depending on the target LV dc-link.

the issues of the phase-shift modulation is the reactive power that each port is processing. Reactive power is defined when the current and the voltage at one port do not have the same sign and is visualized in Fig. 4(b). Therefore, the reactive power can be defined as $Q = f_{\mathrm{sw}} V_a^{\mathrm{DC}} \int_{t_1}^{t_2} i_a(t)dt$, where t_1 is the zero crossing instant of the current at port a, t_2 is the switching time of port a, and f_{sw} is the switching frequency. As it will be shown in the following, this fact is limiting the operation to small phase shifts, in order to limit the losses. The choice of the modulation and its thorough optimization is, however, not the core of this paper and has been investigated in [8], [16].

Multiple QABs will be connected to the LV and MV side, in order to obtain the desired medium-voltage level and ensure redundancy. The MV side controls the sum of the MV dc-link voltages, while the dc/dc ensures the balance between the CHB dc-links and regulates the LV dc-link voltage.

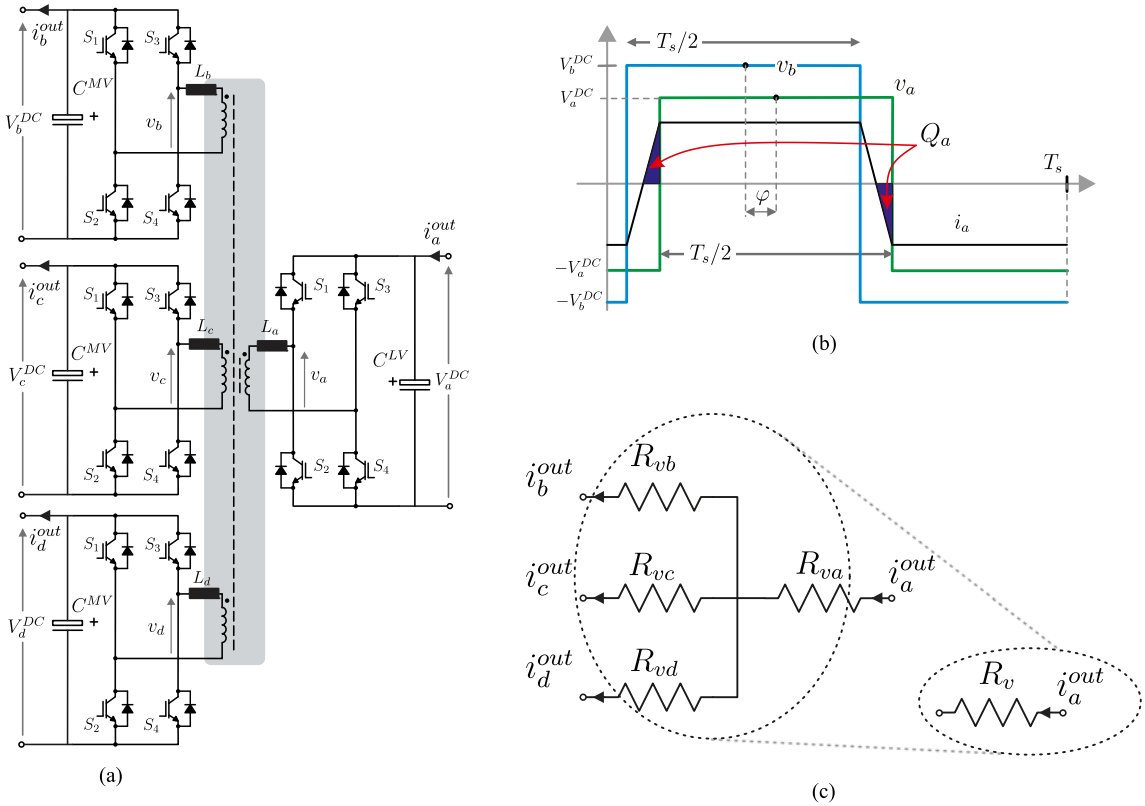

Fig. 4. QAB: (a) Circuit, (b) idealized phase-shift waveforms, and (c) equivalent virtual resistor schematic.

III. Lifetime-Based Control of the SST

In order to enable the power sharing, a droop control based on virtual resistors is implemented [17]. The concept is based on the fact that the parallel connection of ideal voltage sources is not possible, while if they were coupled through an impedance, the modulus of this impedance could be used for the power sharing (with the source having the higher output impedance giving less power). Since a physical impedance would add components and unacceptable losses, a resistance is mathematically emulated in the controller in order to have the same behavior of a resistor connected in series to a voltage source. Consequently, when the current provided by the source increases, the voltage decreases.

Virtual resistors are used both in the LV and MV sides of the dc/dc converter, as depicted in Figs. 4(c) and 5(a). A low-frequency equivalent circuit of the QAB is reported in Fig. 5(b). Controlled current sources represent the power transfer due to the phase-shift modulation. The virtual resistors R_{va}–R_{vd} are introduced only in the control and do not correspond to any physical component in Fig. 5(a). In this paper, it is assumed that each cell of the CHB processes the same amount of power (as the most usual application case). It is exactly by changing the value of the virtual resistor that the power routing will take place, as it will be explained in the following.

The control of the SST is based on a lifetime model. Each FB of the QAB has a consumed lifetime $A \in (0, 1)$, whereby $A = 0$ describes unstressed power semiconductors and $A = 1$ determines the end of life for the power semiconductors. A possible model to determine A is the linear Palmgren Miners rule, which is based on Rainflow counting of the power semiconductors junction temperature and damage accumulation [18].

In the configuration chosen for this paper (see Fig. 3), two LV dc-links and six MV dc-links are considered. The repetition of three of these structures would allow a complete three-phase to three-phase converters to be made, with at least two LV converters for LV phase.

In the following, the notation is divided so that the letters a, b, c, d denote the single QAB ports, with port a being the LV one [see Fig. 4(c)], while the numbers $1, 2, 3, 4$ refer to the QAB.

Equation (1) represents the total age of QAB1 that can be conceptually visualized as the series connection between the "age" of the LV port A_{a1} and the equivalent parallel of the three MV ports A_{b1}, A_{c1}, A_{d1}. It is important to note that A_1 now represents an aggregate lifetime so a direct relation to the Palmgren–Miner rule is not possible anymore. In fact, the total age is used only for the virtual resistance calculation and not for the lifetime estimation, so its physical meaning is not important.

Since in this example QAB1 and QAB3 (as defined in Fig. 3) are connected to LV dc1, the power request by this dc-link will be shared in an inversely proportional way [see (2)] and the resulting virtual resistor for QAB1 is expressed in (3). The term R_0 constitutes the proportionality between the age and the resistance, and represents a degree of freedom. However, a higher virtual resistance implies a higher steady-state error in the voltage control. The QAB can, therefore, be represented as an equivalent virtual resistor R_v [see Fig. 4(c)], that is related to

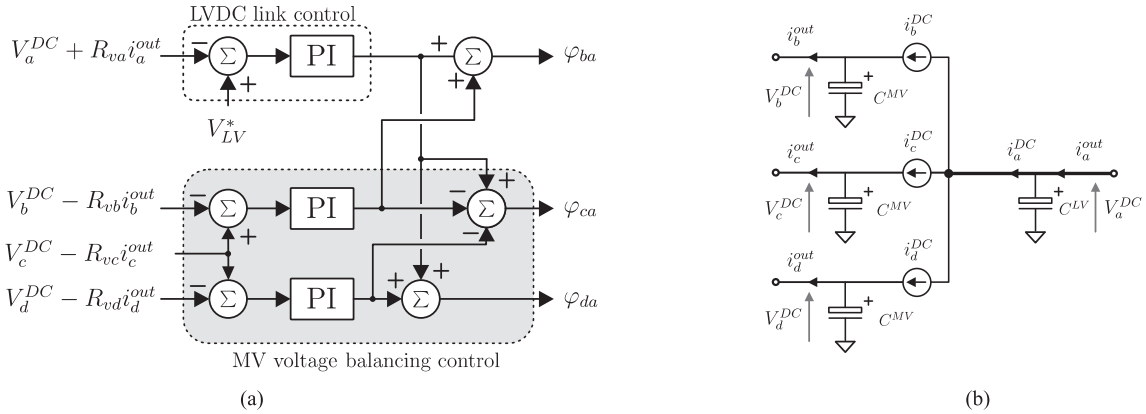

Fig. 5. QAB control. (a) Control structure with regulators and virtual resistors, (b) Low-frequency model of the QAB.

the total lifetime of the converter. In fact, if the LV side is aged or the three MV ports are aged, the idea is to set R_v to a high value to reduce the power transferred by this QAB.

This first control allows us to select how much power is processed by each QAB through its LV side, whereby a bigger resistance would cause the current to be diverted to other QABs. The virtual resistances of the MV ports of the QAB are proportional to their single lifetime (4); this allows rerouting the power in the MV side in the case of a healthy LV module and a deterioration of a single MV cell. The coefficient $9/2R_{v1}$ is added so that when all the H-bridges of the complete structure have the same age, the QAB presents a resistance $R_{v1}/2$ in the LV side and three parallel resistances of value $3R_{v1}/2$ in the MV side. Overall, the total virtual resistance of a QAB seen from the three MV ports in parallel and the LV one is equal to R_{v1}

$$A_1 = \frac{A_{a1}}{2} + \frac{3A_{b1}\cdot A_{c1}\cdot A_{d1}}{2\left(A_{b1}\cdot A_{c1} + A_{b1}\cdot A_{d1} + A_{c1}\cdot A_{d1}\right)} \quad (1)$$

$$\frac{P_1}{P_3} = \frac{A_3}{A_1} \quad (2)$$

$$R_{v1} = R_0 \frac{A_1}{A_1 + A_3} \quad (3)$$

$$R_{va1} = \frac{R_{v1}}{2}$$

$$R_{vb1} = \frac{9}{2} R_{v1} \frac{A_{b1}}{A_{b1} + A_{c1} + A_{d1}}. \quad (4)$$

It is worth noting that the imbalance happens only in the dc/dc side, and the power processed by the cells of the ac side is equally shared. If the ac cells were to process different powers, since they are series connected, a different ac voltage would result for each cell. However, the possibility of increasing the ac voltage is limited by the dc-link voltage. For this reason, in order to not modify the principle of operation of the CHB converter, it is assumed that the ac cell, and the MV dc-link as a consequence, process the same amount of power.

It is true that the maximum power limits of a dc path could be reached, preventing this condition to be fulfilled. In this case, the power routing control would be disabled because higher priority is given for supplying the load. The proposed power routing is to be applied only in partial load condition.

IV. Stability Analysis

In order to assess the stability margin and the performance of the virtual resistor-based power routing shown in Fig. 5(a), the simplified model of Fig. 5(b) is adopted, and the phase-shift modulation is represented by the currents $i_a^{\mathrm{DC}} - i_d^{\mathrm{DC}}$. For the control of the QAB in its presented configuration, the power transfer between the LV side and the MV side needs to be controlled by the PI controller of the "LV dc-link control." This controller determines the phase shift between the primary and all secondary-side ports. Furthermore, the MV dc-links need to be balanced and this is performed with two additional PI controllers in the "MV balancing control."

The intrinsic cross-coupled nature of the QAB causes interactions between the different ports during the transients because the modification of a phase shift would alter the power transfer of the other modules. While it does not constitute a stability problem, feedforward compensation can be realized. The nonlinear characteristic of the power transfer does not need to be taken into account if the system is designed to transfer the maximum power with a phase shift smaller than $\pi/8$.

C^{LV} and C^{MV} are the dc-link capacitances in the low- and medium-voltage sides. V_a^{DC} represents the generic LV port and $V_b^{\mathrm{DC}}, V_c^{\mathrm{DC}}, V_d^{\mathrm{DC}}$ the generic MV ports. The currents with the "out" superscript represent the output currents, which are used for the virtual resistance implementation, and are considered as disturbances.

Equations (5)–(8) represent the current balance at the capacitors, (9) represents the PI controller used to control the LV side, and (10)–(12) show the implementation of the PI balancing controllers.

In order to evaluate the positions of the poles, also the MV outer voltage loop must be considered, and this is represented by an additional PI regulator with parameters K_P^{CHB} and K_I^{CHB}. In this case, the measured value for the outer voltage controller is the sum of the individual MV dc-link voltages, since the CHB converter does not feature a common dc-link. The balancing of the CHB cells is performed by the proposed dc/dc converter. The

TABLE I
SIMULATION PARAMETERS

$f_{\rm sw}$	40 kHz·s	$\mathrm{BW}^{\rm LV}$	150 Hz
R	6.6 s	$\mathrm{BW}^{\rm CHB}$	300 Hz
T_s	1e−4 s	$L_{\rm lk}$	0.035 mH
$C^{\rm LV}$	0.33 mF	$C^{\rm MV}$	0.33 mF
$K_I^{\rm LV}$	0.2029	$K_P^{\rm LV}$	0.0014
$K_I^{\rm MV}$	0.2029	$K_P^{\rm MV}$	0.0014
$K_I^{\rm CHB}$	673	$K_P^{\rm CHB}$	1.19
$V_x^{\rm ref}$	400 V	$V_{\rm avg}^{\rm MV*}$	2400 V

delays of the pulse width modulation and of the discretization are neglected, since the control dynamics are set well below the Nyquist frequency

$$V_a^{\rm DC} = \frac{1}{C^{\rm LV}} \int -\left(i_b^{\rm DC} + i_c^{\rm DC} + i_d^{\rm DC} - i_a^{\rm out}\right) dt \tag{5}$$

$$V_b^{\rm DC} = \frac{1}{C^{\rm MV}} \int \left(i_b^{\rm DC} - i_b^{\rm out}\right) dt \tag{6}$$

$$V_c^{\rm DC} = \frac{1}{C^{\rm MV}} \int \left(i_c^{\rm DC} - i_c^{\rm out}\right) dt \tag{7}$$

$$V_d^{\rm DC} = \frac{1}{C^{\rm MV}} \int \left(i_d^{\rm DC} - i_d^{\rm out}\right) dt \tag{8}$$

$$i_a^{\rm DC} = -K_P^{\rm LV}\left(V_{\rm LV}^* - V_a^{\rm DC} + R_v i_a^{\rm out}\right) - K_I^{\rm LV} \int \left(V_{\rm LV}^* - V_a^{\rm DC} + R_v i_a^{\rm out}\right) dt \tag{9}$$

$$i_b^{\rm DC} = \frac{i_a^{\rm DC}}{3} - K_P^{\rm MV}\left(V_b^{\rm DC} - R_v i_b^{\rm out} - V_c^{\rm DC} + R_v i_c^{\rm out}\right) - K_I^{\rm MV} \int \left(V_b^{\rm DC} - R_v i_b^{\rm out} - V_c^{\rm DC} + R_v i_c^{\rm out}\right) dt \tag{10}$$

$$i_c^{\rm DC} = \frac{i_a^{\rm DC}}{3} + K_P^{\rm MV}\left(V_b^{\rm DC} - R_v i_b^{\rm out} - V_c^{\rm DC} + R_v i_c^{\rm out}\right) + K_I^{\rm MV} \int \left(V_b^{\rm DC} - R_v i_b^{\rm out} - V_c^{\rm DC} + R_v i_c^{\rm out}\right) dt + K_P^{\rm MV}\left(V_d^{\rm DC} - R_v i_d^{\rm out} - V_c^{\rm DC} + R_v i_c^{\rm out}\right) + K_I^{\rm MV} \int \left(V_d^{\rm DC} - R_v i_d^{\rm out} - V_c + R_v i_c^{\rm out}\right) dt \tag{11}$$

$$i_d^{\rm DC} = \frac{i_a^{\rm DC}}{3} - K_P^{\rm MV}\left(V_d^{\rm DC} - R_v i_d^{\rm out} - V_c^{\rm DC} + R_v i_c^{\rm out}\right) - K_I^{\rm MV} \int \left(V_d^{\rm DC} - R_v i_d^{\rm out} - V_c^{\rm DC} + R_v i_c^{\rm out}\right) dt. \tag{12}$$

The parameters of the simulations are reported in Table I, where also the sampling time T_s of the control and the leakage inductance of the four-phase transformer are reported.

Due to the high complexity and high number of inputs/outputs, a simplified design procedure is proposed. The procedure is based on the technical optimum criterion that allows us to maximize the phase margin in the case of system with a pole in the origin (such as in the case of dc voltage controls).

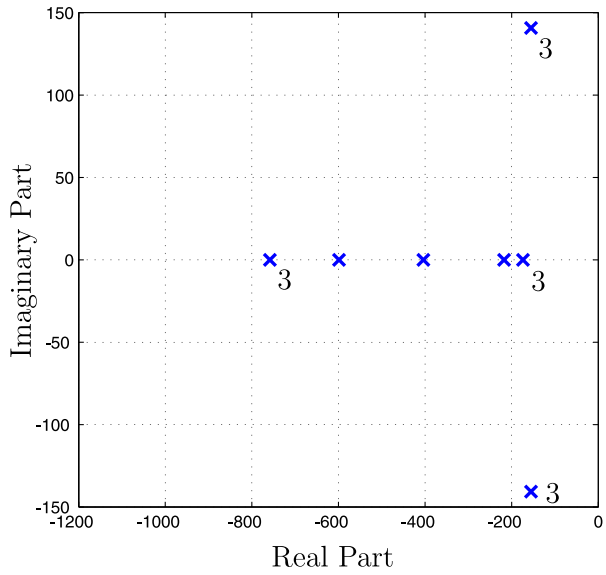

Fig. 6. Pole map of the closed-loop control system of one leg of the SST.

The system to be controlled, when all the MV ports are given the same phase shift φ, is represented by (13), so the gain G of the plant can be calculated by linearizing the system around the point $\varphi = 0$ [see (14)]. This approximation is valid if the converter is designed to operate with small phase shift. It is to be noted that due to the interactions between the active bridges, at the denominator, the equivalent leakage inductance is $4L_{\rm lk}$ instead of $L_{\rm lk}$, as may be expected from the DAB equation

$$i_a^{\rm DC} = \frac{V_b^{\rm DC} + V_c^{\rm DC} + V_d^{\rm DC}}{8\pi L_{\rm lk} f_{\rm sw}} \varphi \left(1 - \frac{\varphi}{\pi}\right) \tag{13}$$

$$G = \frac{di_a^{\rm DC}}{d\varphi} = \frac{V_b^{\rm DC} + V_c^{\rm DC} + V_d^{\rm DC}}{8\pi L_{\rm lk} f_{\rm sw}} \left(1 - 2\frac{\varphi}{\pi}\right). \tag{14}$$

In this way, the PI controller can be tuned with a specific bandwidth $\mathrm{BW}^{\rm LV}$. Due to the presence of one pole in the origin, the time constant of the PI regulator $\tau^{\rm LV} = \frac{K_p^{\rm LV}}{K_i^{\rm LV}}$ must be chosen to be bigger than the desired one for the closed-loop system. The ratio $R = \tau^{\rm LV}\mathrm{BW}^{\rm LV}$ basically selects the phase margin. The gain of the regulator can, therefore, be calculated as $K_p^{\rm LV} = \frac{C^{\rm LV}\mathrm{BW}^{\rm LV}}{G\sqrt{1+\frac{1}{R^2}}}$ and by choosing $R = 6.6$ a phase margin of 80° is obtained.

The same parameters are chosen for simplicity for the balancing regulators. Regarding the tuning of the outer voltage loop, the same procedure with $\mathrm{BW}^{\rm CHB}$ is performed. As a design rule, the bandwidth of the outer voltage control should be wider than the one for the QAB.

In order to verify that this simple design procedure allows us to realize a stable system, the pole map of the overall state-space model is calculated and is shown in Fig. 6. The system shows multiple complex conjugated poles, but is stable. The validity of the state-space model has been confirmed by comparing its

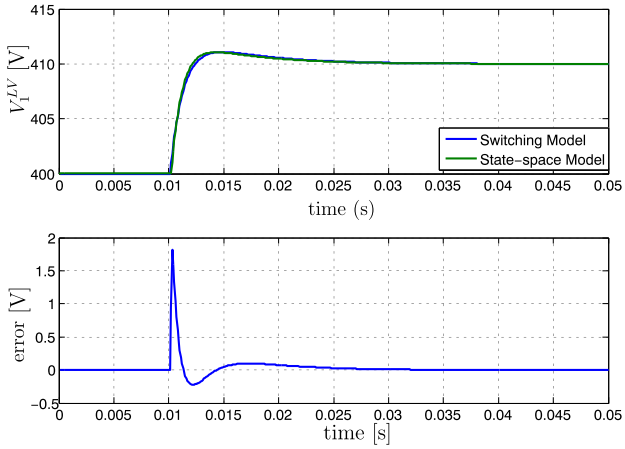

Fig. 7. Comparison between the state-space model and the switching model during a step change of the reference in the LV side.

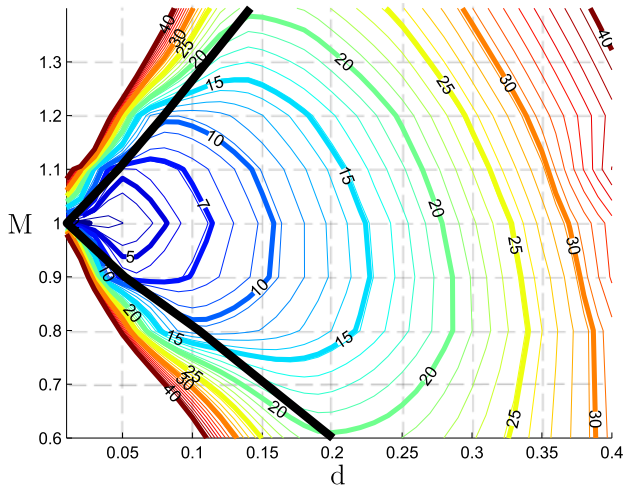

Fig. 8. ZVS at turn-on range of the QAB for symmetrical power transfer operation. The black line shows the ZVS border and the numbers on the contour lines depict the reactive current in percent of the load current.

output with the complete phase-shift model with the switches, and the agreement is excellent, as demonstrated in Fig. 7, where the outputs of the two models are compared for a step change in the reference for the low voltage side. The authors are confident that despite the assumption made, the pole map of Fig. 6 represents a good approximation of the complete system dynamics.

V. Analysis of the QAB Operation

In this section, the operation of the QAB will be analyzed, in particular, the soft-switching boundaries and the operation with power imbalance.

A. Zero Voltage Switching (ZVS) Range

In order to achieve ZVS turn-on of the devices, at the switching instant, the current must flow in the antiparallel diode. The soft-switching of the QAB can be calculated in a similar fashion to the DAB [16], extending the condition to all bridges. Fig. 8 depicts the simulation results for the ZVS range of the QAB, for symmetrical power transfer operation. $M = \frac{V^{\mathrm{MV}}}{V^{\mathrm{LV}}}$ is the voltage

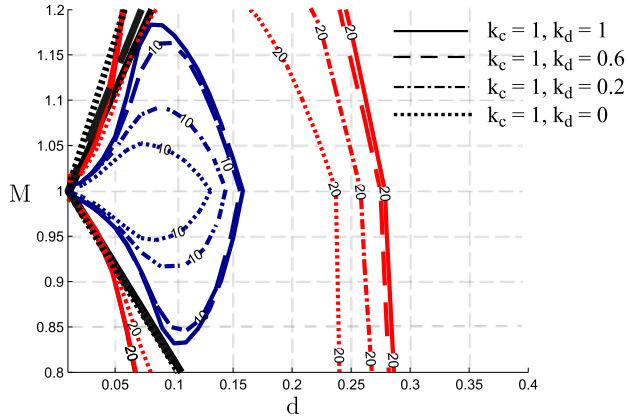

Fig. 9. Contour plot for different power imbalance conditions introduced to one port. The black lines show the ZVS border and the numbers on the contour lines depict the reactive current in percent of the load current.

transfer ratio and $d = \frac{\varphi}{\pi}$ is the normalized phase shift. The contour lines depict the reactive current at port a, defined above, in percent of the average load current and the thick black line depicts the ZVS border. When the QAB is operated in the area left of the black line, ZVS is lost. As a result, these bridges are hard switched at turn-on. In addition, the reactive current is increasing rapidly when operating in these regions as can be seen in Fig. 8.

If the voltages on the primary side and on the secondary side are equal ($M = 1$), ZVS at turn-on is achieved for the full power range of the QAB. For $M \neq 1$, ZVS at turn-on is lost for light loads (small phase shifts). As a conclusion, the ZVS at turn-on range of the QAB is decreasing with increasing voltage imbalance.

B. Power Imbalance

The core proposal of this paper is that an unbalanced power transfer can be realized to improve the lifetime of the converter. However, the cost of this procedure in terms of efficiency reduction should be evaluated in order to find the optimal tradeoff between thermal control and efficiency [19].

Fig. 9 depicts how the reactive current and the ZVS border are changing with different power imbalances, defined as $k_c = \frac{P_c}{P_b}$ and $k_d = \frac{P_d}{P_b}$. The power distribution of the secondary-side ports is being changed so that one of the input ports is transferring power while the overall power transfer remains constant. The following four power transfer situations are depicted in Fig. 9:

1) symmetrical power transfer operation ($k_c = 1$, $k_d = 1$): secondary-side ports power distribution 33.3%: 33.3%: 33.3%;
2) asymmetrical power transfer operation ($k_c = 1$, $k_d = 0.6$): secondary-side ports power distribution 38.5%: 38.5%: 23%;
3) asymmetrical power transfer operation ($k_c = 1$, $k_d = 0.2$): secondary-side ports power distribution 45%: 45%: 10%;
4) asymmetrical power transfer operation ($k_c = 1$, $k_d = 0$): secondary-side ports power distribution 50%: 50%: 0%.

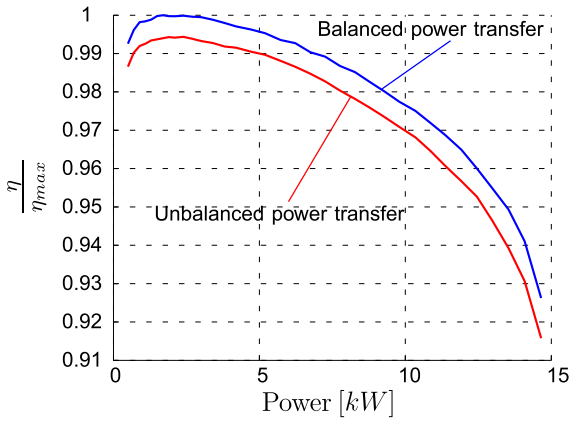

Fig. 10. Efficiency of the QAB normalized to the maximum efficiency (symmetrical power transfer operation) as a function of the transferred power. The power distribution of the unbalanced power transfer is $50\% : 25\% : 25\%$ for the three secondary-side ports.

It can be observed that with increasing power imbalance, the contour lines (constant reactive power) are moving to lower phase shifts.

C. Efficiency and Losses Distribution

Power losses calculations were done in order to assess the efficiency decrease in the case of unbalanced operation. The model of the insulated gate bipolar transistor (IGBT) SIGC32T120R3E was used in PLECS. In order to characterize the device's thermal model, a double-pulse test stand was used to evaluate the switching and conduction losses, and the results are published in [20]. As long as the converter is operating in soft-switching condition, the turn-on losses and the reverse-recovery losses do not happen. Fig. 10 depicts the efficiency in the simulation of the QAB normalized to the maximum efficiency $\eta_{\max}$, for symmetrical and asymmetrical power transfer operation (power distribution of the three secondary-side ports $50\% : 25\% : 25\%$). The voltages are equal at the primary and the secondary sides of the converter ($V_{\mathrm{DC}} = 400\,\mathrm{V},\ M = 1$). The efficiency shows a maximum for low power, compatible with the characteristic of an IGBT converter that has a constant component of the voltage drop, then starts decreasing when the resistive losses become dominant. The simulation also shows a nonlinear decrease in efficiency for power higher than 10 kW that can be attributed to the nonlinear increase in reactive current for higher phase shifts. Based on the simulation, the efficiency with unbalanced power transfer is in average 0.63% lower than for balanced power transfer.

The study of the overall efficiency depending on the dc voltage and of the switching frequency is outside the actual scope of this paper, that is to show that only a little decrease of efficiency takes place during unbalanced operation. The efficiency optimization happens in the design phase, and can be performed by using standard optimization techniques reported in the literature. This constitutes the starting point of the analysis, and is the reason why the efficiency is normalized to the maximum value. The price of the power routing capability is a decrease of the efficiency, but it has been shown that this decrease is limited in extent.

VI. Simulation Results

Simulations are carried out considering the structure in Fig. 3, where each dc-link reference is set to 400 V, the switching frequency is 40 kHz with phase-shift modulation, and the dc capacitors are 330 μF. The transformers have unity turn ratio. The age of the modules is assumed to be different in the modular structure for different possible reasons, such as thermal imbalances, parameter tolerances, or because of the choice of a repairable system, where all cells have different age, as explained in [21].

The simulations are carried out with MATLAB/Simulink and the PLECS toolbox. First, a variation in the aging indicator of a secondary-side bridge A_{d3} and the primary bridge A_{a4} is demonstrated in Fig. 11. In particular, for each QAB, the lifetime parameters (age and virtual resistance) as well as the power processed by each QAB port are reported.

Initially, all primary and secondary bridges have the same aging indicator, and constant power of 2 kW is processed by each QAB. All bridges are processing the same power, until at $t = 0.5\,\mathrm{s}$, the aging indicator of one secondary bridge in QAB 3 is increased. This results in an increase of the virtual resistor and the power for the according cell is reduced. Due to the modular interconnection of the cells, the power P_{b4} in QAB 4 is increased. At $t = 1.5\,\mathrm{s}$, the primary aging indicator A_{a4} of QAB 4 is increasing and further unbalances the power transfer. As a result, the power in all bridges of QAB 4 is decreased, while the parallel structure of QAB 2 has to process higher power.

The second simulation in Fig. 12 is showing the influence of the virtual resistances on a power cycle. It is assumed that all secondary bridges have equal aging indicator. Instead, on the primary side, the aging indicator of QAB1, QAB2, and QAB3 is assumed to be equal, i.e., $A_1 = A_2 = A_3$, while QAB 4 shows a higher aging indicator $A_4 > A_1$. The power is already unequally shared during constant power operation and a sinusoidal half-wave-shaped power cycle of $\Delta P = 4$ kW is applied to show the power sharing among the QABs. Similar to the constant power operation, the power cycle is unequally shared, resulting in different magnitudes of the power cycle for the QABs, which are quantified in Fig. 12. Particularly, the load in all bridges of QAB4 is significantly reduced, while the power cycle in QAB 2 is increased in all bridges. The power cycle in the primary bridge of QAB2 is approximately 2.4 times higher than the power cycle in the primary bridge of QAB 4.

The aim of these simulations is to prove that the power can be routed depending on an indicator of the consumed lifetime of the basic cells, leading to different power cycles within the system. Similar to the reduction of power cycles, the cycles of the power semiconductor's junction temperatures, which are causing wear out, can be controlled. If the age increases, the control reduces the stress on those semiconductors, and the distributed droop control keeps the correct dc-link voltages across the whole converter to delay the time of the next maintenance.

How the age of the semiconductor is determined is outside the scope of this paper, which demonstrates the power routing principle. However, to demonstrate the effect of the power routing on the lifetime, a system consisting of a single QAB is chosen, as shown in Fig. 13(a), with the QAB parameters as in

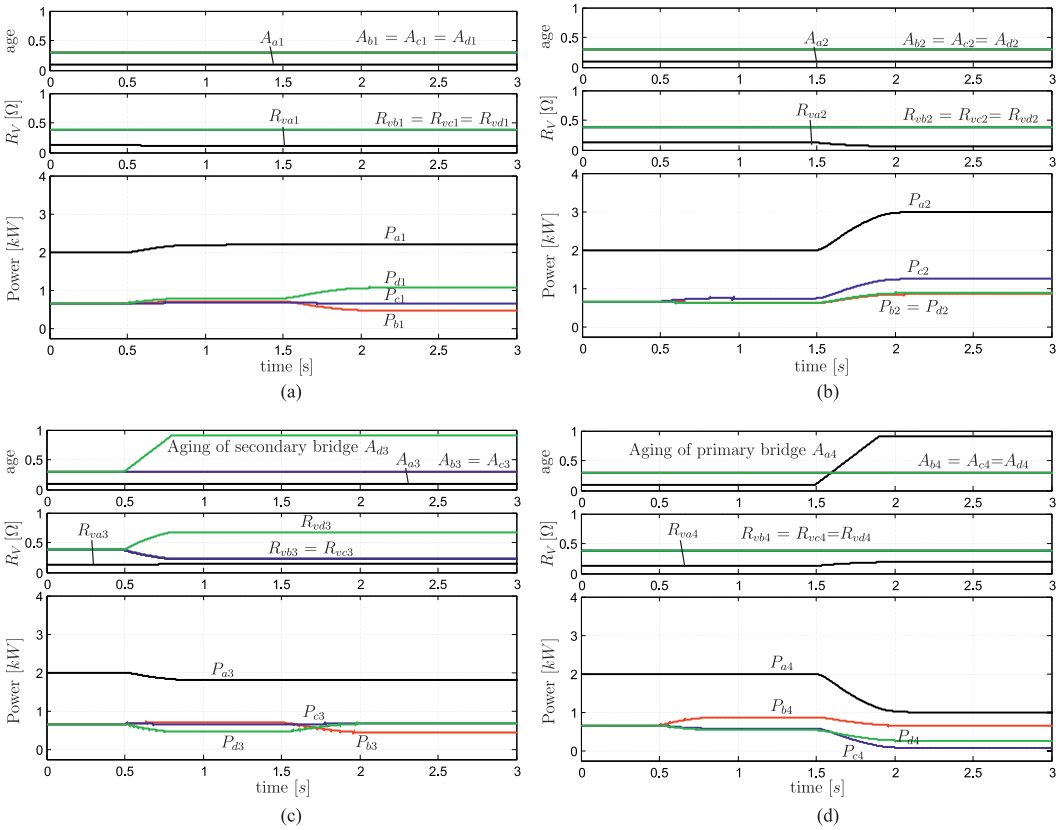

Fig. 11. Simulation: Power routing by the SST assuming change of the component lifetime. Constant power case. (a) QAB1. (b) QAB2. (c) QAB3. (d) QAB4.

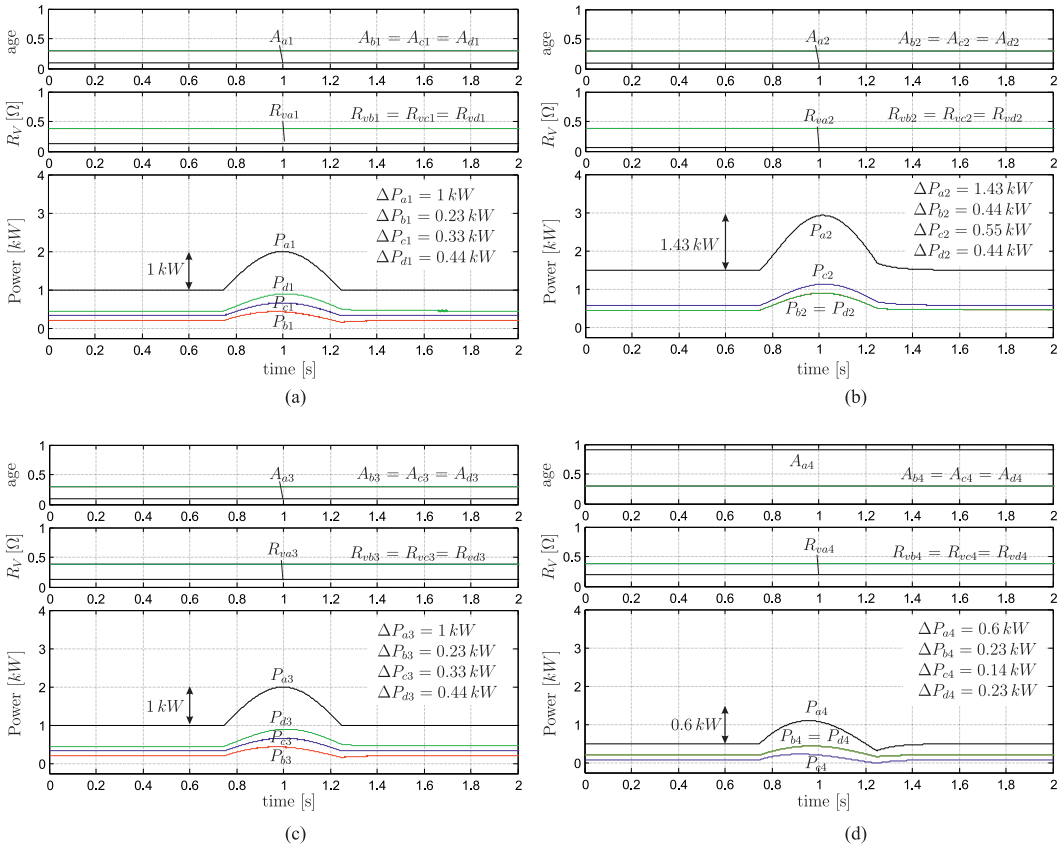

Fig. 12. Simulation: Power routing by the SST assuming change of the component lifetime. Power cycle case. (a) QAB1. (b) QAB2. (c) QAB3. (d) QAB4.

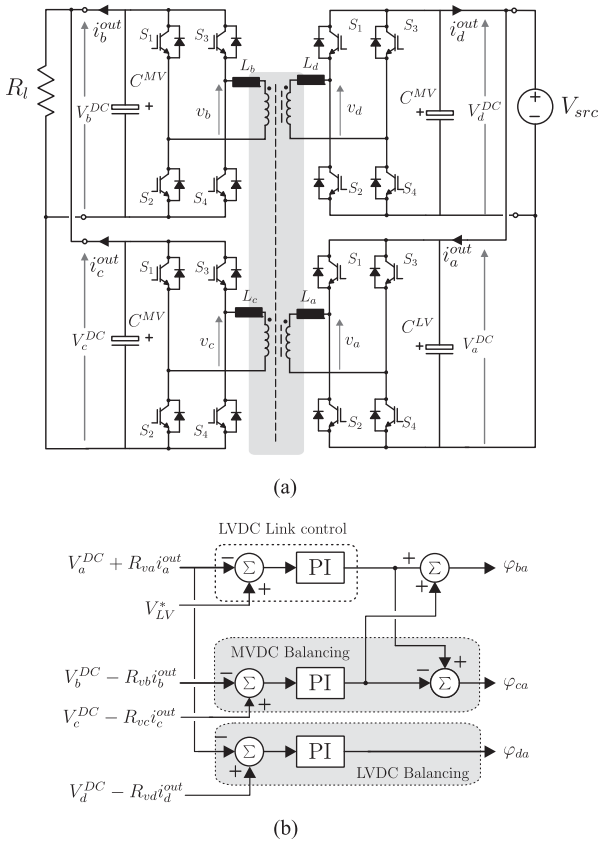

Fig. 13. QAB configuration for the virtual resistance test: (a) circuit connection (b) control.

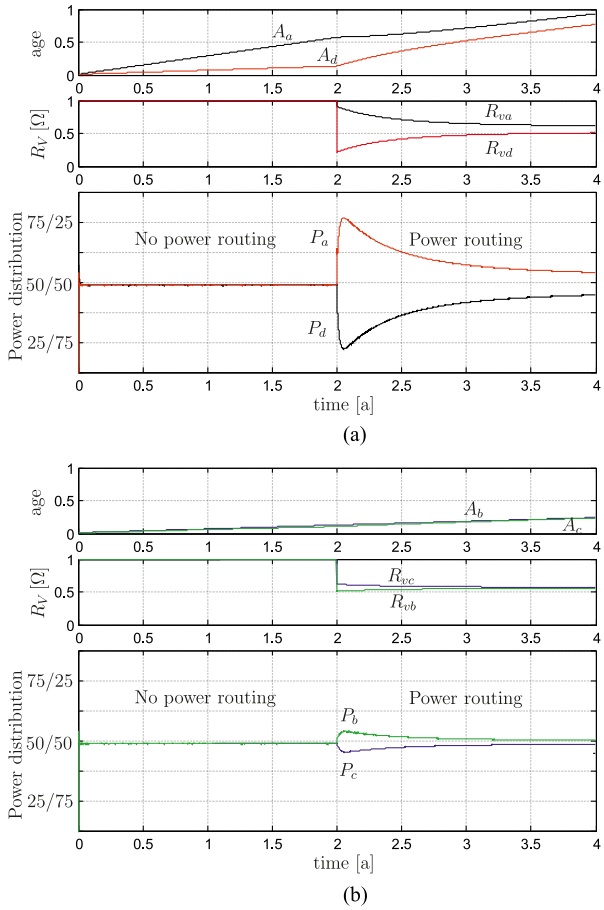

Fig. 14. Simulation: Power routing in one QAB with two primary and two secondary ports. (a) Primary side. (b) Secondary side.

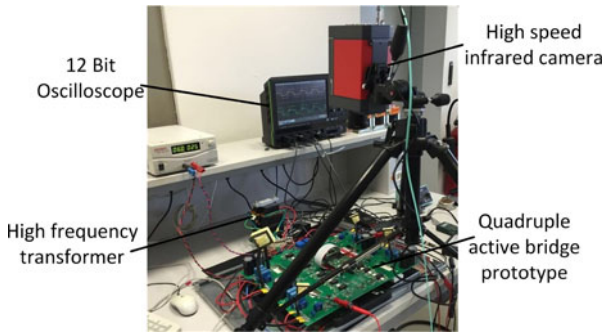

Fig. 15. Picture of the laboratory setup with a QAB prototype and a high-speed infrared camera for junction temperature measurement in one open IGBT module.

Table I. The values of the virtual resistors are variable, because they are used to route the power in the system. As a difference to the case studied before, this QAB has two parallel connected ports on the primary and two parallel ports on the secondary side. This requires to change the control diagram of the QAB as presented in Fig. 13(b). A regulator outputs the phase shift between the primary and the secondary sides, while the virtual resistors allow controlling the power distribution of the overall power in the parallel ports. The resulting power flow paths are two redundant paths on the primary and two redundant paths on the secondary side.

For this system, the long-time effect of the power routing is demonstrated. As pointed out before, different lifetime consumption is assumed for the different power converter cells. Moreover, in this case, the long-time increase of the age in all cells is assumed to be different, whereby the aging of cell *a* is happening faster than that of cell *d*. On the secondary side, the aging of the cell *c* is slower than the aging of cell *b*. For demonstration, the lifetime is modeled by setting the age A_a, A_b, A_c, and A_d proportional to the integral of the losses of the power semiconductors. From this age, the virtual resistors are derived, whereby the cells on the primary and secondary sides are modeled as parallel resistors as exemplary shown as follows for the virtual resistance of cell *a*:

$$R_{va} = \frac{A_a}{A_a + A_d}. \tag{15}$$

The power routing for the primary side is shown in Fig. 14(a) and the aging of the secondary side is shown in (b). For the first two years, this is presented without the power routing showing that on both sides one cell is going faster toward its end of life than the other one. By activating the power routing, the aging of the cell with higher wear-out is slowing down, while the aging of the other cell is accelerating. Affected by the activation of the power routing, the virtual resistors change and then converge to each other as expected for decreasing difference in the age. The power of the most aged cell is reduced as intended.

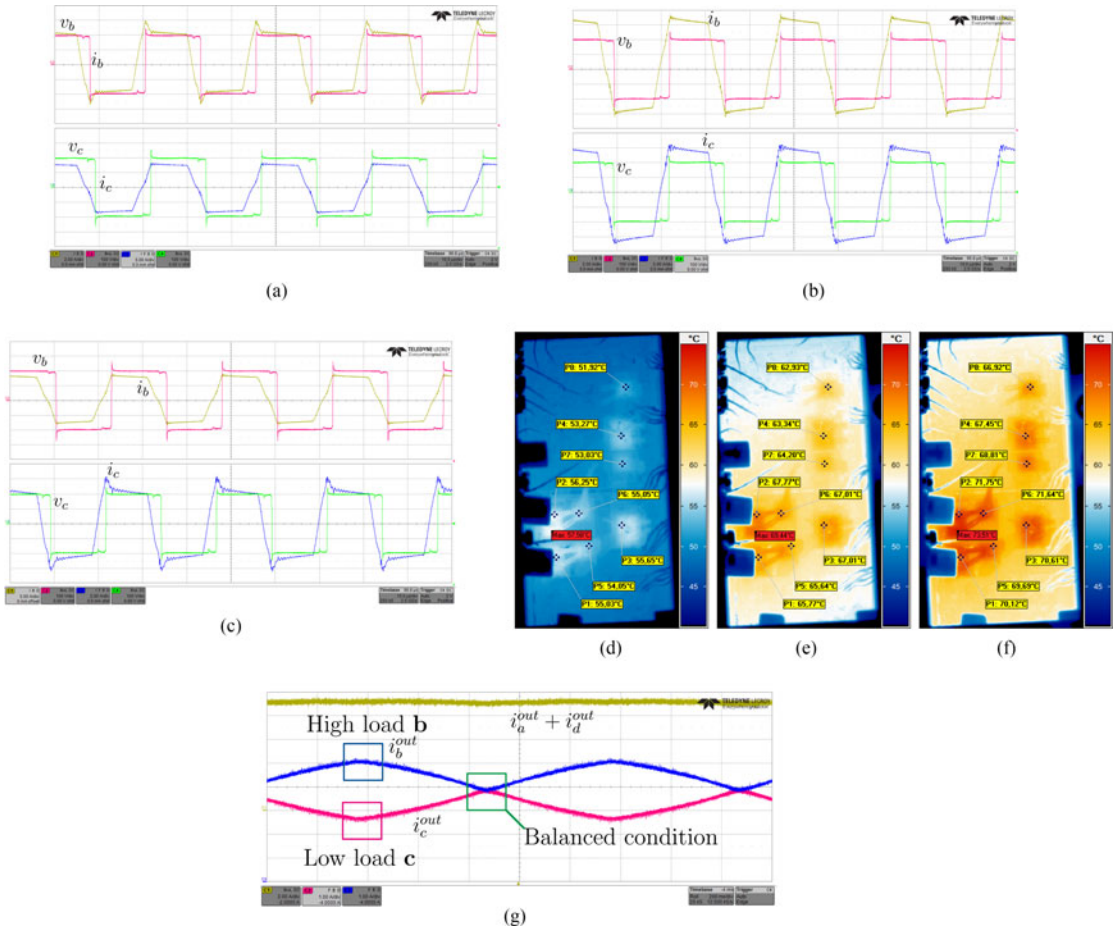

Fig. 16. Measurement: Power routing by the SST assuming different component lifetime: Voltage and current waveform of one QAB for different load sharing and thermal images of the used open IGBT module. (a) Reduced load for recorded FB. v_b, v_c 100 V/div, i_b 2 A/div, i_c 5 A/div, time step 10 μs/div. (b) Equal load sharing for the FBs. v_b, v_c 100 V/div, i_b 2 A/div, i_c 2 A/div, time step 10 μs/div. (c) Increased load for the recorded FB. v_b, v_c 100 V/div, i_b 5 A/div, i_c 2 A/div, time step 10 μs/div. (d) Reduced load for the recorded FB. (e) Equal load sharing for the FBs. (f) Increased load for the recorded FB. (g) Variation of the virtual resistors for a variation in the power routing. i_b^{out} 1 A/div, i_c^{out} 1 A/div, time step 200 ms/div.

VII. Experimental Results

A prototype of the QAB for reliability investigation was built based on a 25 A IGBT open module. This kind of module is not typically used for dc/dc converters; however, it was provided by the manufacturer without gel, allowing to track directly the temperature variations. Due to the absence of the gel, the prototype has to be operated at lower voltage due to insulation issues. The goal of the test bed is to prove, in simplified conditions, that a control based on variable virtual resistance can affect the thermal distribution inside the power module. Fig. 13(a) shows the configuration of the experimental setup, where port a and d are connected in parallel to a power supply at $V_{\mathrm{src}} = 200$ V and port b and c to a load resistor of $R_l = 25\,\Omega$. The other parameters are the same as in the simulations.

Fig. 15 shows a picture of the experimental setup, along with the oscilloscope and the infrared camera.

To prove the thermal stress variation, the low-load condition is are emulated by increasing the virtual resistance of the module under test to twice its value (initially $10\,\Omega$) and the high-load condition is emulated by increasing the virtual resistance of the other module in parallel.

An IR camera was used to monitor the chip temperature of the open module (that implements an H-bridge cell) used for the tests, and the temperature was measured in the steady state after 5 min. Fig. 16(d) shows the measured temperature and (a) shows the actual waveform of the converter. In the same fashion, equal load and high load are shown in Fig. 16(e), (b) and Fig. 16(f), (c).

This virtual resistance variation can be performed dynamically, as shown in Fig. 16(g), where the resistance of module **c** performs a square wave between 10 and 20 Ω with a period of 1 s. The output current is shared proportionally. Such fast variations of the virtual resistors only represent a proof-of-concept of the proposed method, while it is expected that the variations are much slower in operating conditions due to their correlation with the aging.

VIII. Conclusion

The paper is focused on using a QAB as a building block of a modular dc/dc converter for medium-voltage application. The use of this topology in conjunction with the proposed control algorithm enables power routing within the system. The algorithm is based on a virtual resistor voltage control, where

$$A = \begin{bmatrix}
0 & 1 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 \\
-\frac{K_I^{\mathrm{LV}}}{C^{\mathrm{LV}}} & -\frac{K_P^{\mathrm{LV}}}{C^{\mathrm{LV}}} & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 \\
0 & 0 & 0 & 1 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 \\
0 & 0 & -\frac{K_I^{\mathrm{LV}}}{C^{\mathrm{LV}}} & -\frac{K_P^{\mathrm{LV}}}{C^{\mathrm{LV}}} & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 \\
0 & 0 & 0 & 0 & 0 & 1 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 \\
\frac{K_I^{\mathrm{LV}}}{6C^{\mathrm{LV}}} & \frac{K_P^{\mathrm{LV}}}{6C^{\mathrm{LV}}} & \frac{K_I^{\mathrm{LV}}}{6C^{\mathrm{LV}}} & \frac{K_P^{\mathrm{LV}}}{6C^{\mathrm{LV}}} & -\frac{K_I^{\mathrm{MV}}}{C^{\mathrm{MV}}} & -\frac{K_P^{\mathrm{MV}}}{C^{\mathrm{MV}}} & \frac{K_I^{\mathrm{MV}}}{2C^{\mathrm{MV}}} & \frac{K_P^{\mathrm{MV}}}{2C^{\mathrm{MV}}} & 0 & 0 & 0 & 0 & \frac{K_I^{\mathrm{MV}}}{2C^{\mathrm{MV}}} & \frac{K_P^{\mathrm{MV}}}{2C^{\mathrm{MV}}} & 0 & 0 \\
0 & 0 & 0 & 0 & 0 & 0 & 0 & 1 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 \\
\frac{K_I^{\mathrm{LV}}}{3C^{\mathrm{LV}}} & \frac{K_P^{\mathrm{LV}}}{3C^{\mathrm{LV}}} & 0 & 0 & \frac{K_I^{\mathrm{MV}}}{2C^{\mathrm{MV}}} & \frac{K_P^{\mathrm{MV}}}{2C^{\mathrm{MV}}} & -2\frac{K_I^{\mathrm{MV}}}{C^{\mathrm{MV}}} & -2\frac{K_P^{\mathrm{MV}}}{C^{\mathrm{MV}}} & \frac{K_I^{\mathrm{MV}}}{2C^{\mathrm{MV}}} & \frac{K_P^{\mathrm{MV}}}{2C^{\mathrm{MV}}} & \frac{K_I^{\mathrm{MV}}}{2C^{\mathrm{MV}}} & \frac{K_P^{\mathrm{MV}}}{2C^{\mathrm{MV}}} & 0 & 0 & \frac{K_I^{\mathrm{MV}}}{2C^{\mathrm{MV}}} & \frac{K_P^{\mathrm{MV}}}{2C^{\mathrm{MV}}} \\
0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 1 & 0 & 0 & 0 & 0 & 0 & 0 \\
\frac{K_I^{\mathrm{LV}}}{6C^{\mathrm{LV}}} & \frac{K_P^{\mathrm{LV}}}{6C^{\mathrm{LV}}} & \frac{K_I^{\mathrm{LV}}}{6C^{\mathrm{LV}}} & \frac{K_P^{\mathrm{LV}}}{6C^{\mathrm{LV}}} & 0 & 0 & \frac{K_I^{\mathrm{MV}}}{2C^{\mathrm{MV}}} & \frac{K_P^{\mathrm{MV}}}{2C^{\mathrm{MV}}} & -\frac{K_I^{\mathrm{MV}}}{C^{\mathrm{MV}}} & -\frac{K_P^{\mathrm{MV}}}{C^{\mathrm{MV}}} & 0 & 0 & \frac{K_I^{\mathrm{MV}}}{2C^{\mathrm{MV}}} & \frac{K_P^{\mathrm{MV}}}{2C^{\mathrm{MV}}} & 0 & 0 \\
0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 1 & 0 & 0 & 0 & 0 & 0 \\
\frac{K_I^{\mathrm{LV}}}{6C^{\mathrm{LV}}} & \frac{K_P^{\mathrm{LV}}}{6C^{\mathrm{LV}}} & \frac{K_I^{\mathrm{LV}}}{6C^{\mathrm{LV}}} & \frac{K_P^{\mathrm{LV}}}{6C^{\mathrm{LV}}} & 0 & 0 & \frac{K_I^{\mathrm{MV}}}{2C^{\mathrm{MV}}} & \frac{K_P^{\mathrm{MV}}}{2C^{\mathrm{MV}}} & 0 & 0 & -\frac{K_I^{\mathrm{MV}}}{C^{\mathrm{MV}}} & -\frac{K_P^{\mathrm{MV}}}{C^{\mathrm{MV}}} & \frac{K_I^{\mathrm{MV}}}{2C^{\mathrm{MV}}} & \frac{K_P^{\mathrm{MV}}}{2C^{\mathrm{MV}}} & 0 & 0 \\
0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 1 & 0 & 0 & 0 \\
0 & 0 & \frac{K_I^{\mathrm{LV}}}{3C^{\mathrm{LV}}} & \frac{K_P^{\mathrm{LV}}}{3C^{\mathrm{LV}}} & \frac{K_I^{\mathrm{MV}}}{2C^{\mathrm{MV}}} & \frac{K_P^{\mathrm{MV}}}{2C^{\mathrm{MV}}} & 0 & 0 & \frac{K_I^{\mathrm{MV}}}{2C^{\mathrm{MV}}} & \frac{K_P^{\mathrm{MV}}}{2C^{\mathrm{MV}}} & \frac{K_I^{\mathrm{MV}}}{2C^{\mathrm{MV}}} & \frac{K_P^{\mathrm{MV}}}{2C^{\mathrm{MV}}} & -2\frac{K_I^{\mathrm{MV}}}{C^{\mathrm{MV}}} & -2\frac{K_P^{\mathrm{MV}}}{C^{\mathrm{MV}}} & \frac{K_I^{\mathrm{MV}}}{2C^{\mathrm{MV}}} & \frac{K_P^{\mathrm{MV}}}{2C^{\mathrm{MV}}} \\
0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 1 \\
\frac{K_I^{\mathrm{LV}}}{6C^{\mathrm{LV}}} & \frac{K_P^{\mathrm{LV}}}{6C^{\mathrm{LV}}} & \frac{K_I^{\mathrm{LV}}}{6C^{\mathrm{LV}}} & \frac{K_P^{\mathrm{LV}}}{6C^{\mathrm{LV}}} & 0 & 0 & \frac{K_I^{\mathrm{MV}}}{2C^{\mathrm{MV}}} & \frac{K_P^{\mathrm{MV}}}{2C^{\mathrm{MV}}} & 0 & 0 & 0 & 0 & \frac{K_I^{\mathrm{MV}}}{2C^{\mathrm{MV}}} & \frac{K_P^{\mathrm{MV}}}{2C^{\mathrm{MV}}} & -\frac{K_I^{\mathrm{MV}}}{C^{\mathrm{MV}}} & -\frac{K_P^{\mathrm{MV}}}{C^{\mathrm{MV}}}
\end{bmatrix}. \tag{18}$$

the virtual resistor is related to the accumulated damage of the power converter cells. The obtained capability of rerouting the power internally can be used in case of faults or, as it is proposed in this paper, to balance the consumed lifetimes of the different basic cells. Cells that have been more stressed (i.e., they have the lowest remaining lifetime) will see a reduction of their processed power, and healthier cells will share the load. Consequently, the power cycles of the stressed cells are reduced for prevention of a failure and maximization of the time to the next maintenance.

The theoretical analysis proved the stability of the proposed control. The state-space model was validated with a comparison with a complete switching model, featuring the parasitic elements. Extensive simulations showed the ability of the proposed concept to reroute the power depending on the remaining lifetime of the cells in the system. A QAB prototype was built to allow monitoring the junction temperature with an *IR* camera, proving that the virtual resistor voltage control can dynamically affect the thermal stress of the power modules.

Appendix
State-Space Model of the Adopted System

For the stability analysis purpose, (5)–(12) are converted into a state-space model. The state vector V is defined as (16), and the state derivative is calculate as (17). The actual state depends also on external stimuli, such as the current drained from the LV dc-links and the reference signals. These matrices, since they do not intervene in the stability analysis, are omitted for simplicity. Matrix A is reported in (18) as shown top of the page, the components relative the MV controller are omitted for simplicity, since they are common for all the MV dc-links. In particular, the value $-\frac{K_I^{\mathrm{CHB}}}{2C^{\mathrm{MV}}}$ should be added to the elements $A_{\{5,7,9,11,13,15\}\{5,7,9,11,13,15\}}$, and the value $-\frac{K_P^{\mathrm{CHB}}}{2C^{\mathrm{MV}}}$ to elements $A_{\{5,7,9,11,13,15\},\{6,8,10,12,14,16\}}$.

$$V = \Big[V_1^{\mathrm{LV}}, V_1^{\dot{\mathrm{LV}}}, V_2^{\mathrm{LV}}, V_2^{\dot{\mathrm{LV}}}, V_1^{\mathrm{MV}}, V_1^{\dot{\mathrm{MV}}}, V_2^{\mathrm{MV}}, V_2^{\dot{\mathrm{MV}}}, V_3^{\mathrm{MV}}, V_3^{\dot{\mathrm{MV}}}, V_4^{\mathrm{MV}}, V_4^{\dot{\mathrm{MV}}}, V_5^{\mathrm{MV}}, V_5^{\dot{\mathrm{MV}}}, V_6^{\mathrm{MV}}, V_6^{\dot{\mathrm{MV}}},\Big]^T \tag{16}$$

$$\dot{V} = AV. \tag{17}$$

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