Class-E Half-Wave Zero *dv/dt* Rectifiers for Inductive Power Transfer

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***Abstract*—This paper analyses and compares candidate zero *dv/dt* half-wave Class-E rectifier topologies for integration into multi-MHz inductive power transfer (IPT) systems. Furthermore, a hybrid Class-E topology comprising advantageous properties from all existing Class-E half-wave zero *dv/dt* rectifiers is analyzed for the first time. From the analysis, it is shown that the hybrid Class-E rectifier provides an extra degree of design freedom that enables optimal IPT operation over a wider range of operating conditions. Furthermore, it is shown that by designing both the hybrid and the current-driven rectifiers to operate below resonance provides a low deviation input reactance and inherent output voltage regulation with duty cycle allowing efficient IPT operation over wider dc load range than would otherwise be achieved. A set of case studies demonstrated the following performances: First, for a constant dc load resistance, a receiving end efficiency of 95% was achieved when utilizing the hybrid rectifier, with a tolerance in required input resistance of 2.4% over the tested output power range (50–200 W). Second, for a variable dc load in the range of 100–10%, the hybrid and current-driven rectifiers presented an input reactance deviation less than 2% of the impedance of the magnetizing inductance of the inductive link respectively and receiving end efficiencies greater than 90%. Third, for a constant current in the receiving coil, both the hybrid and the current-driven rectifier achieve inherent output voltage regulation in the order of 3% and 8% of the nominal value, respectively, for a variable dc load range from 100% to 10%.**

***Index Terms*—Class-E rectifiers, inductive power transfer, multi-MHz power electronics.**

I. Introduction

WEAKLY coupled inductive links, Fig. 1, tend to operate in the low MHz region in order to increase their link efficiency (η_{link}) [1]–[3]. The optimal link efficiency ($\eta_{\text{link,opt}}$) of a particular inductive link geometry occurs when the receiving coil (L_{rx}) is tuned at the frequency of the generated magnetic field and the ratio of the ac load resistance (R_{ac}) to the reactance of the tuning capacitor (C_{rx}) satisfies a specific value (α_{opt}) [1].

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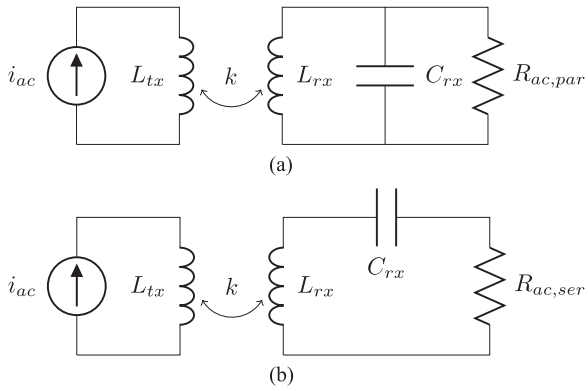


Fig. 1. Inductive link circuit configurations. (a) Parallel tuned receiving coil—compatible with voltage-driven rectifiers. (b) Series tuned receiving coil—compatible with current-driven rectifiers.

The α_{opt} value depends upon the coupling factor (k) between the transmitting coil (L_{tx}) and L_{rx}, the unloaded quality factors of the two coils, and the tuning method of L_{rx}, parallel [see Fig. 1(a)] or series [see Fig. 1(b)] [1]. When a rectifier is added to an inductive link, its input resistance will be the ac load and must therefore be evaluated according to maximum link efficiency requirements. Furthermore, the rectifier topology should be efficient at the frequency of operation, be compatible with the output type of the tuned receiving coil, voltage output for parallel tuned receiving coil [see Fig. 1(a)] or current output for series tuned coil [see Fig. 1(b)], and its input reactance should be absorbed by C_{rx} such that the tuning of L_{rx} will be unaffected.

Class-E rectifiers [4], [5] are very popular in multi-MHz resonant converters [6]–[13] due to their efficient soft switching capability and low electromagnetic footprint. Due to their success in resonant converters, the utilization of Class-E rectifiers is gaining popularity in weakly coupled multi-MHz inductive power transfer (IPT) systems [14]–[16]. This section provides a general description of the operation of Class-E rectifiers. It then examines and presents the various developments of the topologies presented in the literature. Fig. 2 summarizes the circuit configurations of the reviewed Class-E rectifiers. Fig. 3 classifies the reported Class-E designs according to their operating frequency and maximum output power and Table I provides further details about the operation, performance, and targeted application of the topologies shown in Fig. 3.

Class-E zero *dv/dt* rectifiers use a capacitor (C), or a capacitive network of total capacitance C in the case of the hybrid

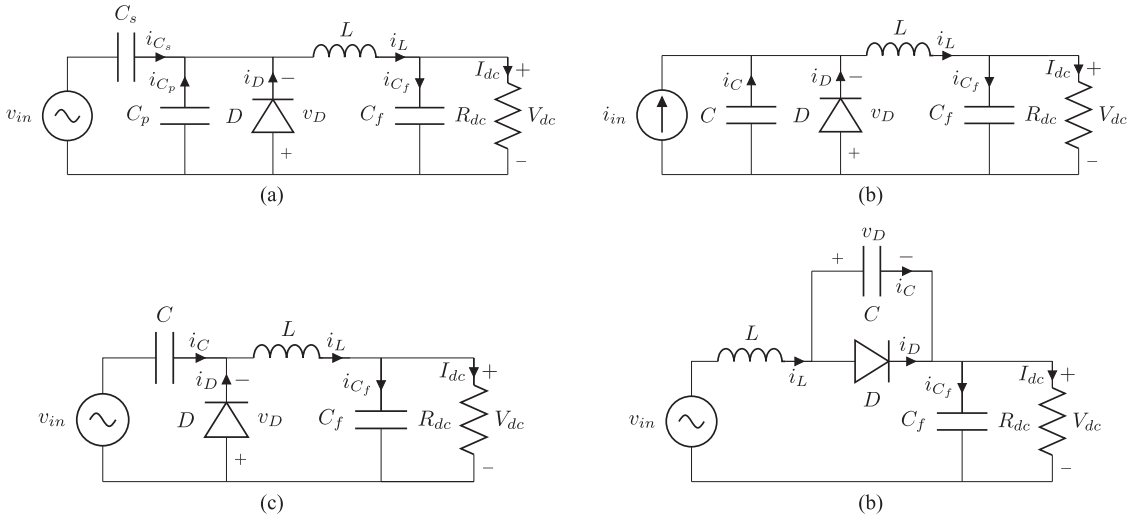


Fig. 2. Hybrid and conventional Class-E half-wave zero *dv/dt* rectifiers. (a) Hybrid rectifier (HVDR). (b) Current-driven rectifier (CDR). (c) Voltage-driven rectifier with series capacitor (series-C VDR). (d) Voltage-driven rectifier with series inductor (series-L VDR).

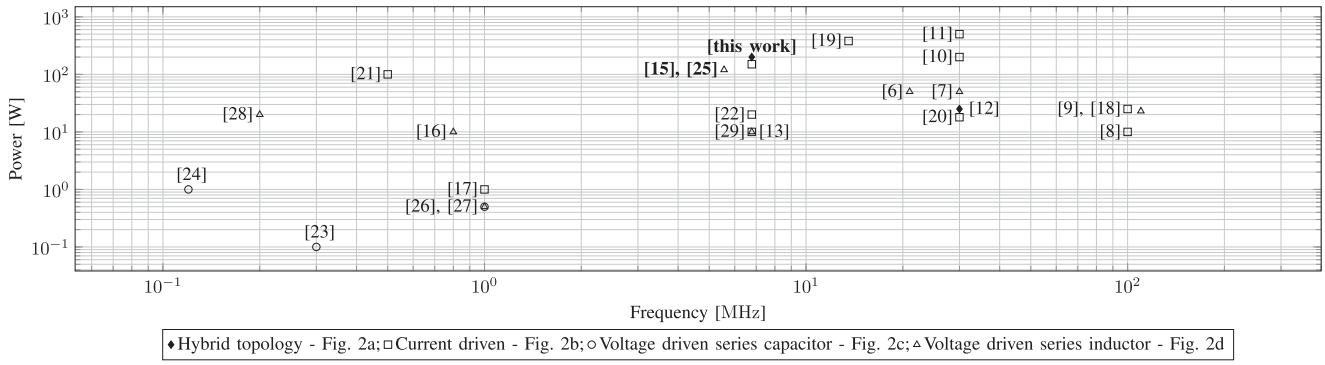


Fig. 3. Power versus frequency map for reported half-wave Class-E rectifiers.

topology [see Fig. 2(a)], to achieve zero rate of change of the voltage across the diode when it is reverse biased. An inductor (L) is used for the circulation of the dc load current when the diode is forward biased. A filter capacitor (C_f) is used to stabilize the output voltage. The operation of Class-E zero *dv/dt* rectifiers can be classified in three modes based on a variable A_r, defined as the ratio of the resonance frequency of the LC network (ω_r) to the operating frequency (ω). The first mode is at the point where ω_r equals to ω, A_r is equal to unity, and the rectifier is therefore operating at resonance. In the other two modes, the rectifier is operating away from resonance and A_r is either smaller than unity, for operation above resonance, or greater than unity, for operation below resonance. The functionality of L varies between the different Class-E topologies. In the hybrid topology shown in Fig. 2 (HVDR), the current-driven topology shown in Fig. 2(b) (CDR), and the voltage-driven topology with series capacitor shown in Fig. 2(c) (series-C VDR), L functions as a filter inductor and has a large harmonic distortion in the current through it (i_L). When the diode is forward biased, one end of the inductor is clamped to ground causing a constant rate of discharge of C_f through L. When the diode is reverse biased, i_L has a sinusoidal component superimposed to the output dc current. The magnitude of the ac component of i_L increases with A_r. When A_r approaches zero in operation above resonance, the current through L can be assumed to be dc. In the voltage-driven rectifier with a series inductor shown in Fig. 2(d) (series-L VDR), the presence of L decreases the harmonic content of the current drawn from the voltage source, and hence, the ac component of the current through L can be assumed sinusoidal in all operating modes. The sinusoidal current component is superimposed to the output dc current.

The HVDR [see Fig. 2(a)] was introduced in the case study of [23], where it was compared with the series-C VDR [see Fig. 2(c)]. Furthermore, the HVDR was empirically designed for operation at resonance and implemented in an SEPIC converter in [12]. Although not discussed in the aforementioned references, the HVDR is an improved design of the series-C VDR. Unlike the other rectifier topologies, the series-C VDR does not absorb the p-n junction capacitance of the diode (C_{pn}) in its LC network. The nonconstant behavior of C_{pn} with voltage makes the operation of the series-C VDR nonrobust when C is in the same order of magnitude as C_{pn}. In the HVDR, C is split into C_s and C_p. Since an external capacitor is now put across the diode, C_{pn} can be physically absorbed by C_p. In this paper, the HVDR

TABLE I
FURTHER CHARACTERISTICS OF REPORTED CLASS-E RECTIFIERS IN THE LITERATURE

Rectifier	Ref.	Full Load	Diode Technology	Application	η [%]	Comments on Developed Rectifiers
Fig. 2(a)	[This work]	77 V; 2.6 A	SiC Schottky	IPT[1]	95**	Most efficient design from the case studies. Rectifier developed to provide optimal loading to the IPT of [2].
Fig. 2(a)	[12]	28 V; 0.89 A	Schottky	RPC[2]	82.5*	Rectifier developed in an SEPIC converter as the dual circuit of Fig. 2(d).
Fig. 2(b)	[8]	12 V; 0.83 A	Si Schottky	RPC	75*	Designed to present a resistive input impedance by using a finite impedance inductor.
Fig. 2(b)	[9]	12 V; 2 A	Si Schottky	RPC	75*	Two circuits with resistive input impedances, as in [8], added in a resistance compression configuration.
Fig. 2(b)	[11]	65 V; 7.69 A	SiC Schottky	RPC	81.6*	Resistive input impedance design in a push–pull configuration.
Fig. 2(b)	[10]	33 V; 6 A	SiC Schottky	RPC	82.5*	Same design as in [8] but L was replaced with an autotransformer.
Fig. 2(b)	[13]	5 V; 2 A	Silicon Schottky	RPC	N/A	Analysis assuming a finite impedance inductor (L) and development to present a resistive input impedance.
Fig. 2(b)	[17]	5V; 0.2A;	Si Schottky	RPC	N/A	Analysis of the topology at any duty cycle assuming an infinite impedance inductor (L).
Fig. 2(b)	[19]	28 V; 13.57 A;	SiC Schottky	RPC	74*	Same concept as in [10] with increased output power capability.
Fig. 2(b)	[20]	12 V; 1.5 A	Si Schottky	RPC	N/A	Topology developed to present low deviation in input phase as the dc load varies between 100% and 10%.
Fig. 2(b)	[21]	100 V; 1 A	Ultrafast Recovery	IPT	90*	Topology developed for a contactless IPT system based on numerical analysis.
Fig. 2(b)	[22]	24.5 V; 0.82 A	Silicon Schottky	IPT	84*	Analysis based on [17] but including component losses. Case study based on a short-range IPT system.
Fig. 2(b)	**[25]**	60 V; 2.5 A	SiC Schottky	IPT	90**	Design of the topology with an infinite impedance inductor (L), for presenting optimal loading to the IPT of [2].
Fig. 2(c)	[27]	5 V; 0.1 A	Si Schottky	RPC	91**	Analysis at any duty cycle of operation with the LC network resonating at the frequency of operation.
Fig. 2(c)	[23]	2.6 V; 0.05 A	N/A	RPC	N/A	First implementation of the circuit with an infinite impedance inductor (L).
Fig. 2(c)	[24]	5 V; 0.2 A	Fast Recovery	RPC	N/A	Analysis at any duty cycle of operation with an infinite impedance inductor (L).
Fig. 2(d)	[6]	5 V; 10 A	N/A	RPC	87*	First developed zero *dv*/*dt* Class-E rectifier. Developed from an isolated voltage-driven Class-D rectifier.
Fig. 2(d)	[7]	24 V; 2.08 A	Si Schottky	RPC	81.6*	Integration of the topology in an isolated converter.
Fig. 2(d)	**[15]**	140 V; 0.85 A	SiC Schottky	IPT	90**	Design for operation below resonance to minimise the inductor size required by optimal IPT efficiency.
Fig. 2(d)	[16]	27 V; 0.36 A	Si Schottky	IPT	94**	State space analysis of the topology and integration in a short-range IPT system.
Fig. 2(d)	[26]	5 V; 0.1 A	Si Schottky	RPC	88.67**	Topology was analyzed at any duty cycle for operation at the resonant frequency of the LC network.
Fig. 2(d)	[18]	33 V; 0.7 A	Si Schottky	RPC	87**	Topology developed for a VHF boost converter. Maximum reported frequency of operation.
Fig. 2(d)	[28]	11.57 V; 1.16 A	MOSFET IRF540	IPT	80*	Synchronous rectification. Absorption of L in the receiving coil of a short-range IPT system.
Fig. 2(d)	[29]	18 V; 0.56 A	Si Schottky	IPT	92**	Absorption of L in the receiving coil of a contactless IPT system.

[1] Inductive power transfer; [2] Resonant power converters; * System efficiency; ** Rectifier efficiency.

is analyzed for the first time in all Class-E rectifier operating modes, at all duty cycles, for any ratio of C_p to C_s.

In resonant power converter applications, the most widely used Class-E rectifier is the CDR [see Fig. 2(b)]. The topology was introduced in [17], where it was analyzed at all duty cycles with an inductor (L) assumed to be of infinite impedance (A_r is zero). In [8]–[11], [13], and [20], more properties of the topology were exploited by utilizing an inductor (L) of finite impedance. For a specific duty cycle and A_r, the topology can exhibit a resistive input impedance at the frequency operation [8]–[11], [13], as otherwise appears resistive and either capacitive [17] or inductive [20]. Over a dc load range between 100% and 10%, and hence a varying duty cycle, the CDR can have a low input phase deviation by selecting the appropriate A_r, [20]. The series-L VDR [see Fig. 2(d)] was introduced in [6], where it was developed from an isolated voltage-driven Class-D half-wave rectifier. The analysis of this topology at all duty cycles was reported in [26] for operation at resonance and in [30] for an ω varying around resonance. In [23], the first implementation of the series-C VDR [see Fig. 2(c)] is reported. Its analysis at all duty cycles is reported in [24] with an L of infinite impedance and in [27] for operation at resonance.

Both the CDR [see Fig. 2(b)] and the series-L VDR [see Fig. 2(d)] were developed for IPT applications [15], [16], [21], [22], [25], [28], [29]. Our work in [15] reports the first Class-E rectifier integrated in a midrange multi-MHz IPT system. The circuit used was the series-L VDR. In [15], the implementation challenges of L, due to the large required inductance value at high frequency, were highlighted when the circuit is designed to emulate optimal link efficiency conditions for the inductive link in [2]. L is easier to fabricate when designing the topology at an A_r smaller than unity since the required inductance decreases. Another improvement was introduced in the short-range IPT system of [28] for sub-MHz operation and in the contactless IPT of [29] for multi-MHz operation, by including L in the tuned receiving coil. While this method solves the implementation problem, the receiving coil is never exactly at resonance. Therefore, the link efficiency drops significantly when the coils operate at midrange distances due to increased losses in the transmitting coil caused by the reduced reflected resistance as a result of the uncompensated reactance of the receiving coil.

The implementation of L in the other rectifiers shown in Fig. 2 does not impose such a great challenge as in the series-L VDR [see Fig. 2(d)]. Our work in [25] presented the design and implementation of the CDR [see Fig. 2(b)] for the inductive link

in [2] as an improvement on [15]. However, since the CDR is a current-driven topology it will experience higher conduction losses than the voltage-driven rectifiers when designed to present optimal loading for the same set of coils [1]. The CDR achieved the same efficiency as the series-L VDR but is more robust to the diode parasitic capacitance [15], [25]. Our study in [31] showed potential for improvement in the performance of the receiving end when the HVDR [see Fig. 2(a)] is utilized instead of the conventional Class-E rectifiers of Fig. 2.

As can be seen, much work has been reported in the Class-E rectifiers in a range of applications which has highlighted some advantages and disadvantages of the topologies. However, there exists no formal analysis for structured comparison of these topologies over a range of operating scenarios. This paper provides a design framework for Class-E half-wave zero *dv/dt* rectifier topologies which allows the designer to select the optimal topology based on power levels, frequency of operation, and inductive link properties. It will also be shown that rectifiers can be designed to present a low input reactance deviation and inherent output voltage regulation over a range of output load values. While the discussions focus on IPT applications, the rectifier analysis results are applicable for other applications. Section II discusses the design of Class-E rectifiers that provides optimal link efficiency conditions and Section III presents the behavior of rectifier design variables under several operating conditions. Section IV discusses the case studies that took place after the analysis results of Section III, and finally, Section V presents the conclusions.

II. Design for Integration in IPT Systems

For a successful Class-E rectifier integration in an IPT system, the input resistance of the topology must be set to an optimal value based on the configuration of the inductive link. It is mathematically convenient to represent the input impedance of the voltage-driven Class-E rectifiers as the parallel connection of a reactive component, $X_{\mathrm{in,p}}$, and the input resistance $R_{\mathrm{in,p}}$. On the other hand, in the current-driven topology it is more convenient to present the input impedance by a series combination between $X_{\mathrm{in,s}}$ and $R_{\mathrm{in,s}}$ [32].

When Class-E rectifiers are designed to provide optimal link efficiency conditions, designers can select the duty cycle d_r at full load and variable A_r

$$A_r = \frac{\omega_r}{\omega}. \tag{1}$$

In the case of the HVDR [see Fig. 2(a)], another degree of freedom is introduced in the selection of variable B defined as

$$B = \frac{C_p}{C_s} \tag{2}$$

where the sum of the two capacitances is given as

$$C = C_s + C_p. \tag{3}$$

The passive components in the circuit are then evaluated such that the specified conditions are met. The duty cycle depends on the loaded quality factor (Q_r) of the rectifier, defined as

$$Q_r = \frac{R_{\mathrm{dc}}}{X} \tag{4}$$

where R_{dc} is the rectifier's dc load and X is the reactance of the series component in the voltage-driven topologies (L or C) or in the current-driven topology. The relationship between the dc resistance with the input resistance in the voltage-driven rectifiers (assuming 100% efficiency) is given by

$$R_{\mathrm{dc}} = 2{M_V}^2 R_{\mathrm{in,p}} = 2{M_V}^2 R_{\mathrm{ac,par}} \tag{5}$$

where M_V is the ratio of output voltage to the peak of the ac input voltage (ac to dc voltage gain). In the current-driven topology, R_{dc} is given by

$$R_{\mathrm{dc}} = \frac{R_{\mathrm{in,s}}}{2{M_I}^2} = \frac{R_{\mathrm{ac,ser}}}{2{M_I}^2} \tag{6}$$

where M_I is the ratio of output current to the peak of the ac input current (ac to dc current gain). In order to directly relate the input ac resistance to the required X value, (5) and (6) are substituted into (4) and the variables are rearranged such that an expression is formed relating the ratio of the ac resistance to the required X value. This ratio will be called input loaded quality factor Q_{in} and is given by the following expressions:

$$Q_{\mathrm{in}} = \frac{Q_r}{2{M_V}^2} = \frac{R_{\mathrm{in,p}}}{X} \tag{7}$$

for the voltage-driven topologies and

$$Q_{\mathrm{in}} = 2{M_I}^2 Q_r = \frac{R_{\mathrm{in,s}}}{X} \tag{8}$$

for the current-driven topology. Using the definition of variable A_r, the relationship between the reactances forming the LC network is given by

$${A_r}^2 = \frac{X_C}{X_L}. \tag{9}$$

In the case of the HVDR, C_s and C_p are evaluated from (2), (3), and (9). Finally, the ratio of input reactance to X is given by

$$N_{\mathrm{in}} = \frac{X_{\mathrm{in}}}{X}. \tag{10}$$

The Class-E topologies shown in Fig. 2 were analyzed for operation at any duty cycle d_r and an A_r range between 0 and 2, while the analysis of the hybrid Class-E rectifier, Fig. 2(a), was also performed as a function of variable B. In the mathematical analysis of each rectifier, the diode and passive components were assumed ideal and lossless. The derivation of the design variables follows the same method as presented in [24], [32]–[34] which is summarized in Appendix A along with the equations of the design variables of the rectifiers that are shown in Fig. 2.

The choice of 50% duty cycle at full load is considered to be optimum by the authors because it provides maximum power output capability ($c_{P_{\mathrm{dc}}}$) in Class-E rectifiers and hence fully utilizes the device [32]. From this starting point (100% dc load), the duty cycle can only decrease as R_{dc} increases. Hence, the analysis of this paper has not been applied to duty cycles greater than 50%.

TABLE II
CHARACTERISTICS OF THE INDUCTIVE LINK IN [2]

Parameter	Value	Optimal Conditions	Value
f [MHz]	6.78	$\alpha_{\mathrm{opt,ser}}\left(\frac{R_{\mathrm{ac,ser}}}{X_{rx}}\right)$	0.044
k^* [%]	3.5	$\alpha_{\mathrm{opt,par}}\left(\frac{R_{\mathrm{ac,par}}}{X_{rx}}\right)$	22.77
L_{tx} [μH]	4	$\eta_{\mathrm{link,opt}}$ [%]	95
L_{rx} [μH]	5.67	$R_{\mathrm{ac,ser}}[\Omega]$	10.6
X_{tx} [jΩ]	170.4	$R_{\mathrm{ac,par}}[\Omega]$	5500
X_{rx} [jΩ]	241.54	$R_{\mathrm{ref}}[\Omega]$	6
Q_{tx}	1300		
Q_{rx}	1000		

* At a center to center coil separation equal to one diameter of the transmitting coil.

III. DISCUSSION OF RECTIFIER FEATURES

The design variables in (4)–(8) and (10) for the conventional Class-E topologies are presented in Fig. 4 as functions of A_r for duty cycle values from 50% to 10%, in steps of 10%. In Fig. 5, the design variables are illustrated as functions of A_r for several values of B at 50% duty cycle for the HVDR. The loaded quality factor (Q_r) is independent of variable B and is therefore the same for the HVDR [see Fig. 2(a)] and the series-C VDR [see Fig. 2(c)]. Also, Q_r in the CDR [see Fig. 2(d)] is the same as in the HVDR and in the series-C VDR since CDR forms the Norton equivalent circuit of the series-C VDR. Fig. 6 presents the diode stresses in half-wave Class-E rectifiers, and along with Figs. 4 and 5, maps out the entire state space of rectifier designs and can be utilized to discuss in detail the performance and tradeoffs of different rectifier designs operating across a range of conditions.

Positive and negative features of the candidate rectifier topologies when operating at duty cycles from 50% and below will now be discussed using Figs. 4–6. These discussions are based on the configuration of the inductive link mentioned in [2], the parameters of which are summarized in Table II (the optimal condition parameters were calculated using [1]).

A. Current-Driven Class-E Rectifier (CDR)

As given in Table I, the CDR [see Fig. 2(b)] is the most commonly implemented topology of the conventional half-wave Class-E rectifiers presented in the literature. It has previously been designed for values of A_r in the range of 0–1.42 [8]–[11], [13], [17]. However, a crucial property of the topology has been missed because as can be seen for N_{in} in Fig. 4(a), an A_r between 1.75 and 2 has the additional advantage of compressing the input reactance of the topology, $X_{\mathrm{in,s}}$, as the duty cycle decreases below 50% (as a result of increasing R_{dc}). The maximum deviation in $X_{\mathrm{in,s}}$ is 13% from its initial value at an A_r equal to 1.75 when the duty cycle changes from 50% to 43%. When the duty cycle decreases below 43%, the deviation of input reactance reduces and approaches the input reactance value for 50% duty cycle. As A_r increases above 1.75, the maximum deviation in $X_{\mathrm{in,s}}$ decreases. The effect of the $X_{\mathrm{in,s}}$ deviation on the receiving resonant tank depends on the absolute value of the input reactance, which depends on X_C and, thus from (8), on Q_{in} and the required emulated input resistance ($R_{\mathrm{ac,ser}}$ for the CDR). By evaluating $X_{\mathrm{in,s}}$ using $\alpha_{\mathrm{opt,ser}}$ from Table II and Q_{in} and N_{in} from Fig. 4(a), it can be seen that a deviation in $X_{\mathrm{in,s}}$ by 13% will result in a residual reactance at the receiving end smaller than 1% of the reactance of L_{rx}. Therefore, when the CDR is designed for values of A_r in the range of 1.75–2, its effect on the tuning of the receiving coil will be negligible when R_{dc} increases.

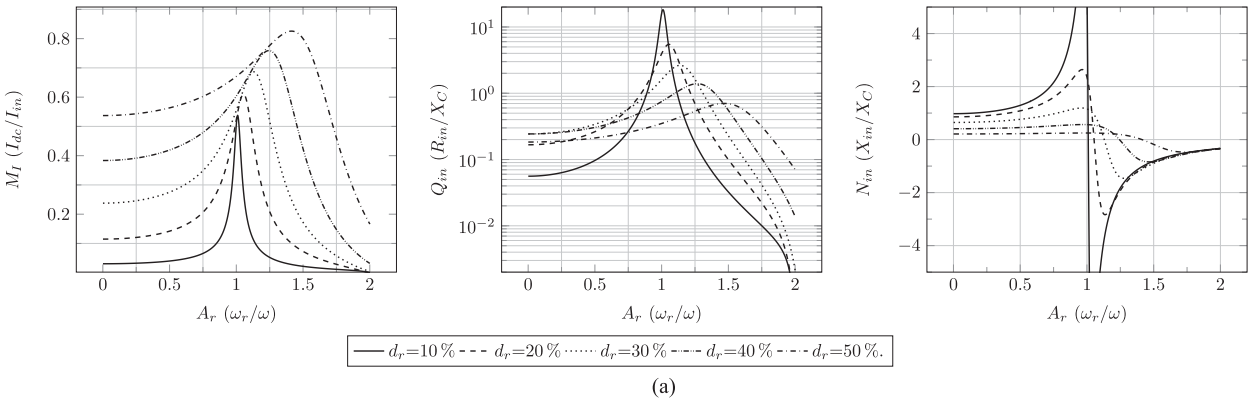
In the same A_r range (1.75–2), unlike $X_{\mathrm{in,s}}$ the input resistance ($R_{\mathrm{in,s}}$) of the topology will change significantly with duty cycle. From the definition of Q_{in} and by considering the behavior of duty cycle with R_{dc}, the input resistance of the topology decreases as R_{dc} increases. In fact, in the aforementioned A_r range, the input resistance of the circuit will be halved when R_{dc} is doubled. This behavior of $R_{\mathrm{in,s}}$ provides an inherent output voltage regulation assuming a constant input current. The inherent output voltage regulation can be observed by multiplying M_I and Q_r. From the definitions of the two variables, their product gives a direct relationship between the input current and the output voltage: $V_{\mathrm{dc}}/(X_C \,.\, i_{\mathrm{in}})$. By evaluating the product of the curves in Fig. 4(a) (left) with the curves in Fig. 4(d) (right), it can be observed that there is an insignificant deviation from the initial value of this product as the duty cycle decreases below 50%. When A_r is 1.75, for an output dc load variation from 100% to 10% the factor $V_{\mathrm{dc}}/(X_C \,.\, i_{\mathrm{in}})$ deviates by less than 10% of its initial value. In fact, the inherent voltage regulation actually occurs over a range of A_r from 1.6 to 2.

In resonant operation (A_r is one), a monotonic behavior of the input resistance of the topology can be observed in Q_{in} of Fig. 4(a). $R_{\mathrm{in,s}}$ increases with R_{dc}. Inherent output voltage regulation can exist in resonant operation by keeping the induced electromotive force (emf) in the receiving coil constant. However, the error in output voltage regulation is more difficult to find in this case without considering the value of the external capacitor added for the tuning of the receiving coil. Also, in this operating mode, the system is not as well regulated as in operation at an A_r between 1.6 and 2.

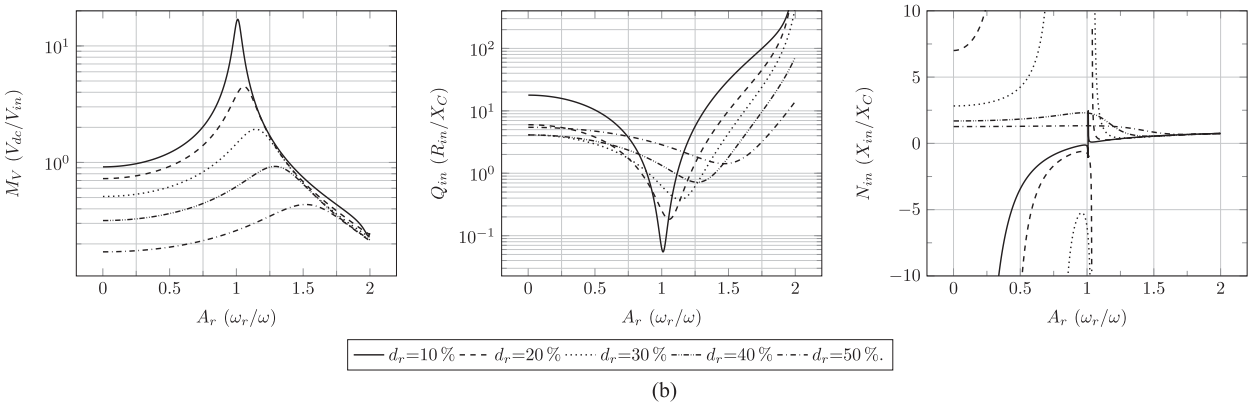
Finally, when the topology is designed at an A_r that tends to zero the resultant inductance value (L) is large. This can be deduced from Q_{in} of Fig. 4(a) and (9). A high inductance results in an inductor current (i_L) with a small ac component. This small ac component eases the implementation of the output filter capacitor (C_f).

B. Voltage-Driven Class-E Rectifier With Series Inductor (Series-L VDR)

The series-L VDR [see Fig. 2(d)] will generally introduce implementation challenges because the required inductance L will need to be in the μH range for most practical inductive links. Using the data from Table II and the definition of Q_{in} in the series-L VDR [see Fig. 4(c)], it can be shown that the ratio of L to L_{rx} will be greater than unity when A_r is greater than 0.5. Realizing these values of inductance requires a magnetic core which will be prohibitively lossy at MHz frequencies [15] and therefore we will not consider this topology any further here.



(a)



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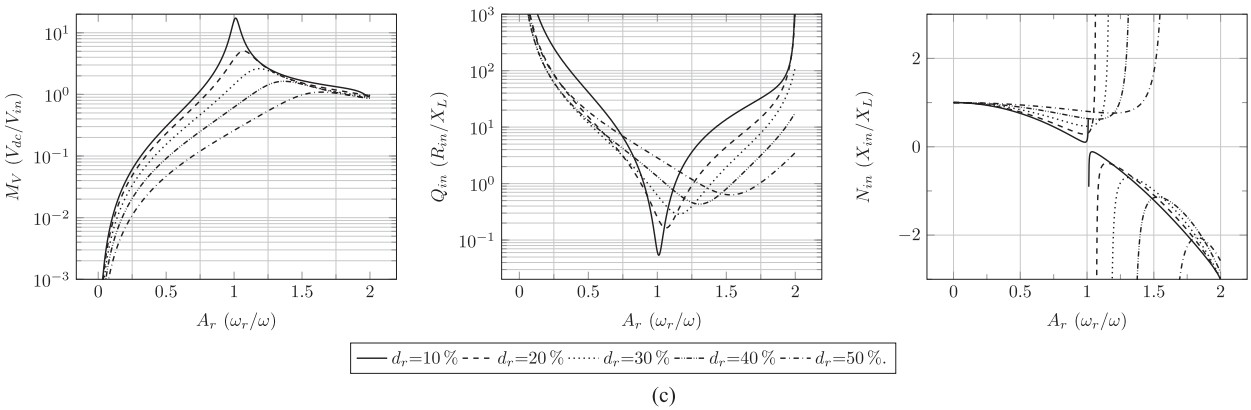

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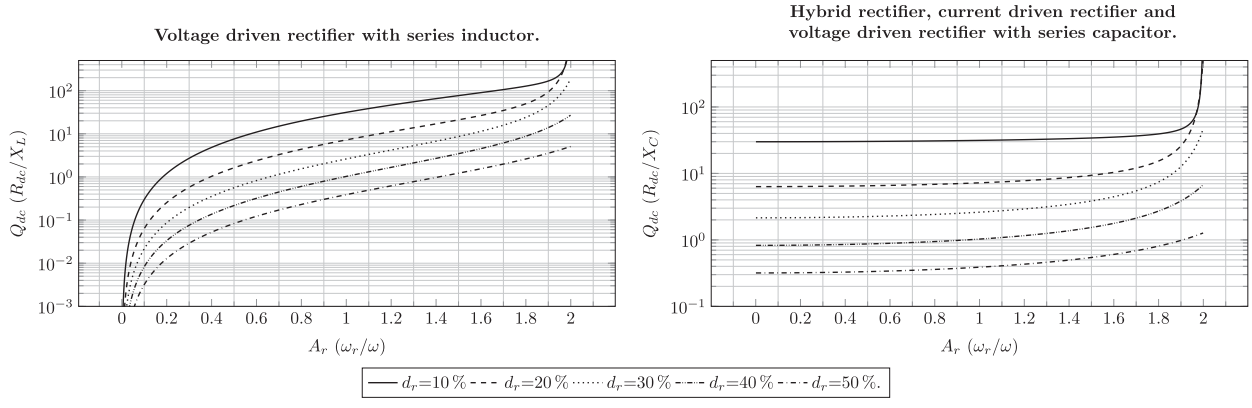

(d)

Fig. 4. Design variables of Class-E half-wave zero *dv/dt* rectifiers. (a) Current-driven rectifier [see Fig. 2(b)]. (b) Voltage-driven rectifier with series capacitor [see Fig. 2(c)]. (c) Voltage-driven rectifier with series inductor [see Fig. 2(d)]. (d) Loaded quality factors of rectifiers of Fig. 2.

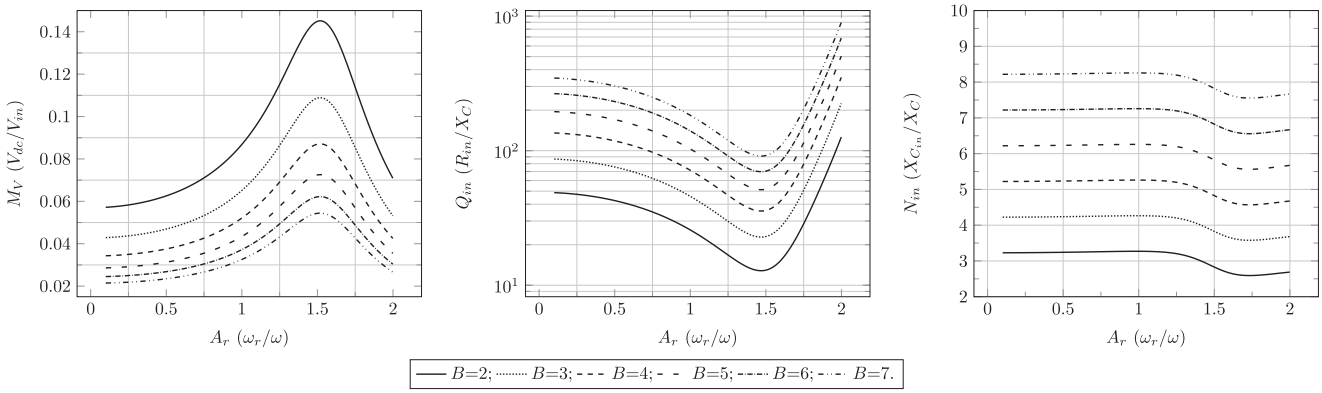

Fig. 5. Design variables of hybrid Class-E rectifier [see Fig. 2(a)] for 50% duty cycle.

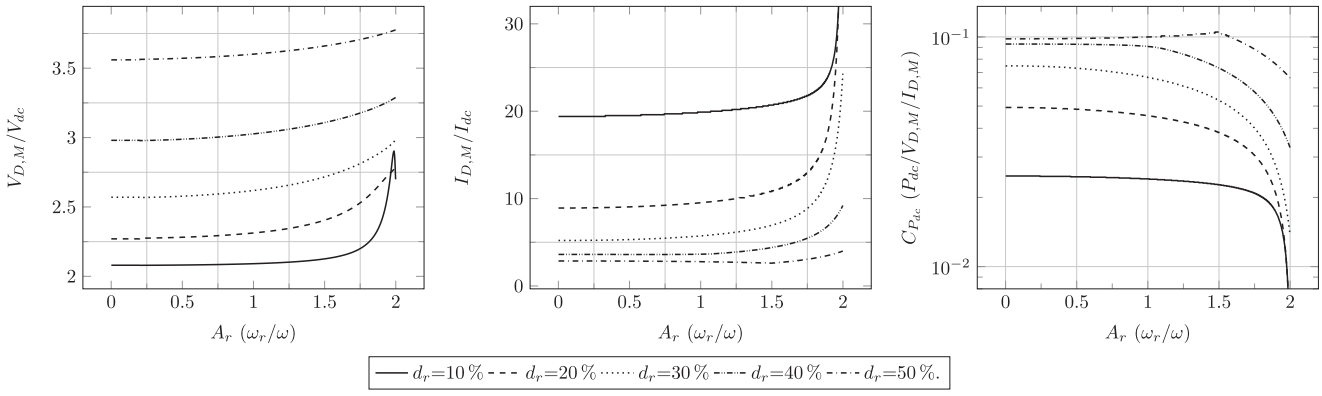

Fig. 6. Diode stresses for all examined Class-E half-wave topologies.

C. Voltage-Driven Class-E Rectifier With Series Capacitor (Series-C VDR)

This topology [see Fig. 2(c)] can be thought as the voltage-driven equivalent of the CDR [see Fig. 2(b)], and therefore, it exhibits the same input impedance behavior with A_r. As A_r tents to zero, a large L results from the design variables which eases the implementation of C_f. In resonant operation, a monotonic behavior of the input resistance of the topology ($R_{\mathrm{in,p}}$) can be observed in Q_{in} of Fig. 4(b) (center). $R_{\mathrm{in,p}}$ decreases as R_{dc} increases and hence, as observed in the CDR [see Fig. 2(b)], the equivalent series resistance seen by L_{Rx} increases with R_{dc} resulting in inherent output voltage regulation when the induced emf is constant.

From N_{in} in Fig. 4(b), it can be shown that the property of low input reactance ($X_{\mathrm{in,p}}$) deviation with increasing R_{dc} occurs over the same A_r range as the CDR (from 1.75 to 2). In this topology, however, the deviation of $X_{\mathrm{in,p}}$ is smaller than the deviation of $X_{\mathrm{in,s}}$ in the CDR. When A_r is 1.75, the input reactance of series-C VDR deviates less than 5% from its initial value as the duty cycle decreases below 50% due to the increase of R_{dc}. Furthermore, the inherent output voltage regulation at the aforementioned A_r range can be observed in M_V of Fig. 4(b). In the A_r range from 1.75 to 2, M_V changes insignificantly (less than 10%) from its initial value as R_{dc} increases up to ten times its initial value. Hence, by keeping constant the voltage across the input terminals of the rectifier the output voltage will be regulated. In an IPT scenario the input voltage of the rectifier is the voltage across the tuning capacitor and will be kept constant by keeping constant the current in the receiving coil (as in the CDR). $R_{\mathrm{in,p}}$ is an order of magnitude greater than $X_{\mathrm{in,p}}$ to satisfy the optimal link efficiency conditions [1]; therefore the magnitude of the voltage at the input terminals of the rectifier is primarily dependent on $X_{\mathrm{in,p}}$. As $X_{\mathrm{in,p}}$ remains within 5% of its initial value at this A_r range, at a constant $i_{L_{rx}}$ the voltage across the input terminals of the rectifier remains constant.

In contrast to the other rectifier topologies, the operation of the series-C VDR is highly dependent on the output power level because the nonconstant diode junction capacitance (C_{pn}) is not absorbed into a large fixed capacitor. Therefore, the HVDR [see Fig. 2(a)] can be seen as an improvement to the series-C VDR because C_{pn} can be absorbed into C_p. Hence, the HVDR is more robust to changes in output voltage than the series-C VDR and introduces an additional degree of design freedom in the selection of variable B, which allows the provision of optimal load for a desirable A_r [31].

D. Hybrid Class-E Rectifier (HVDR)

The behavior of M_V, Q_{in}, and X_{in} variables over A_r and d_r in both the HVDR [see Fig. 2(a)] and the series-C VDR [see

TABLE III
SUMMARY OF CLASS-E RECTIFIER PROPERTIES BASED ON DESIGN VARIABLE PLOTS

Property	HVDR	CDR	Series-C VDR	Series-L VDR
Low current ripple in C_f	$A_r \leq 0.5$	$A_r \leq 0.5$	$A_r \leq 0.5$	$\times$
Low loss inductor (L) realization	✓	✓	✓	$A_r \leq 0.5$
Matching of $R_{\rm dc}$ for any A_r	✓	$\times$	$\times$	$\times$
Resistive input impedance	$A_r \leq 1$	$A_r \geq 1$	$A_r \leq 1$	$A_r \geq 1$
Low deviation in $X_{\rm in}$	$1.75 \leq A_r \leq 2$	$1.75 \leq A_r \leq 2$	$1.75 \leq A_r \leq 2$	A_r tends to 0
Inherent output voltage regulation	$A_r = 1$ and $1.6 \leq A_r \leq 2$	$A_r = 1$ and $1.6 \leq A_r \leq 2$	$A_r = 1$ and $1.6 \leq A_r \leq 2$	$A_r = 1$ and $1.6 \leq A_r \leq 2$
Power robust operation	✓	✓	$\times$	A_r tends to 0

TABLE IV
DESIGN VARIABLES AND EXPERIMENTAL EVALUATION OF COMPONENTS OF IMPLEMENTED CLASS-E RECTIFIERS

	Design #1 Hybrid Rectifier			*Design #2* Hybrid Rectifier			*Design #3* Hybrid Rectifier			*Design #4* Hybrid Rectifier			*Design #5* Current-Driven Rectifier		
Property	*DC current output*			*Operation at resonance*			*Max power output capability*			*Low deviation* $\mathbf{X}_{\rm in,p}$			*Low deviation* $\mathbf{X}_{\rm in,s}$		
A_r	0.35			1			1.52			1.75			1.8		
B	2.5			4			7.5			4			N/A		
$M_V\,/M_I$	0.05			0.05			0.05			0.0683			0.3862		
$Q_{\rm in}$	62.1			71.53			105.6			79.49			0.2403		
$N_{\rm in}$	3.73			5.26			8.28			4.601			-0.4573		
	Theory	Exp.	Error [%]	Theory	Exp.	Error [%]	Theory	Exp.	Error [%]	Theory	Exp.	Error [%]	Theory	Exp.	Error [%]
$R_{\rm dc}$ [Ω]	29	30.58	-5.45	29	29.1	-0.34	29	29.51	-1.76	50	50.51	-1.02	33.5	30	10.45
L [μH]	16	16.31	-1.94	1.8	1.82	-1.11	0.529	0.596	-12.67	0.53	0.5	5.66	0.302	0.278	7.95
C [pF]	265	261	1.51	305	303	0.66	451	400	11.31	339	360	-6.19	564	575	-1.95
C_s [pF]	76	74	0.72	61	61	0.00	53	47	11.32	68	72	-5.88	N/A	N/A	N/A
C_p [pF]	189	186	1.59	244	242	0.82	398	353	11.31	271	280	-3.32	N/A	N/A	N/A
f [MHz]	6.78	6.78	0	6.78	6.84	-0.88	6.78	6.905	-1.84	6.78	6.741	0.58	6.78	6.76	0.29

Fig. 2(c)] is the same, and hence, these two topologies share the advantageous properties discussed in the previous section. However, an additional important property of the HVDR [see Fig. 2(a)] can be observed by considering the ac to dc gain (M_V) in Fig. 5. In this topology, M_V depends on two variables, A_r and B. The series-C VDR does not have this property because it does not split C into two components. By selecting the appropriate A_r and B combination, the topology can be used to match the optimal ac load of an inductive link to any given value of $R_{\rm dc}$ to be powered by the IPT system. Furthermore, different HVDR topologies can present the same ac load while having the same $R_{\rm dc}$ but with different values of the other passive components. It should be noted that for A_r greater than 1.7, the input capacitance of the HVDR can become greater than C_{rx}. From the $N_{\rm in}$ in Fig. 5, it can be seen that by decreasing the value of B the value of the input capacitance also decreases. This comes at the expense of increasing the value of M_V at the same time. Hence, for an A_r greater than 1.7, the range of $R_{\rm in,p}$ that can be matched to an $R_{\rm dc}$ is smaller than for any other A_r value.

E. Summary of Derived Properties

Two properties appear in all Class-E rectifiers of Fig. 2. For all the rectifiers shown in Fig. 2, the maximum possible power output capability can be achieved by designing the rectifier at 50% duty cycle at an A_r equal to 1.52 according to Fig. 6. Moreover from Fig. 4, for different A_r and d_r combinations every topology can appear with a resistive input impedance at the frequency of operation. A summary of the properties of the candidate rectifiers is presented in Table III.

Given the disadvantages of the series-C VDR and series-L VDR, it can be concluded that the HVDR [see Fig. 2(a)] and CDR [see Fig. 2(b)] topologies are the leading candidate solutions for the IPT system described in [2] and these will now be explored using several case studies that include practical implementations.

IV. CASE STUDIES

A. Rectifier Designs

The properties discussed in the previous section form the basis of the case studies. Five different rectifiers were implemented with five different A_r values and have the following properties.

1) *Design #1:* HVDR operating at an A_r smaller than one providing a low ac current ripple through the output filter capacitor.
2) *Design #2:* HVDR operating at resonance ($A_r = 1$) and exhibiting a monotonic behavior in its input resistance with varying $R_{\rm dc}$.
3) *Design #3:* HVDR operating at the maximum power output capability ($c_{P_{\rm dc}}$) point of Fig. 6 ($A_r = 1.52$).
4) *Design #4:* HVDR operating at an A_r equals to 1.75, exhibiting a low deviation input reactance and a monotonic behavior in input resistance with varying $R_{\rm dc}$.
5) *Design #5:* CDR with the same input impedance properties as Design #4 ($A_r = 1.8$).

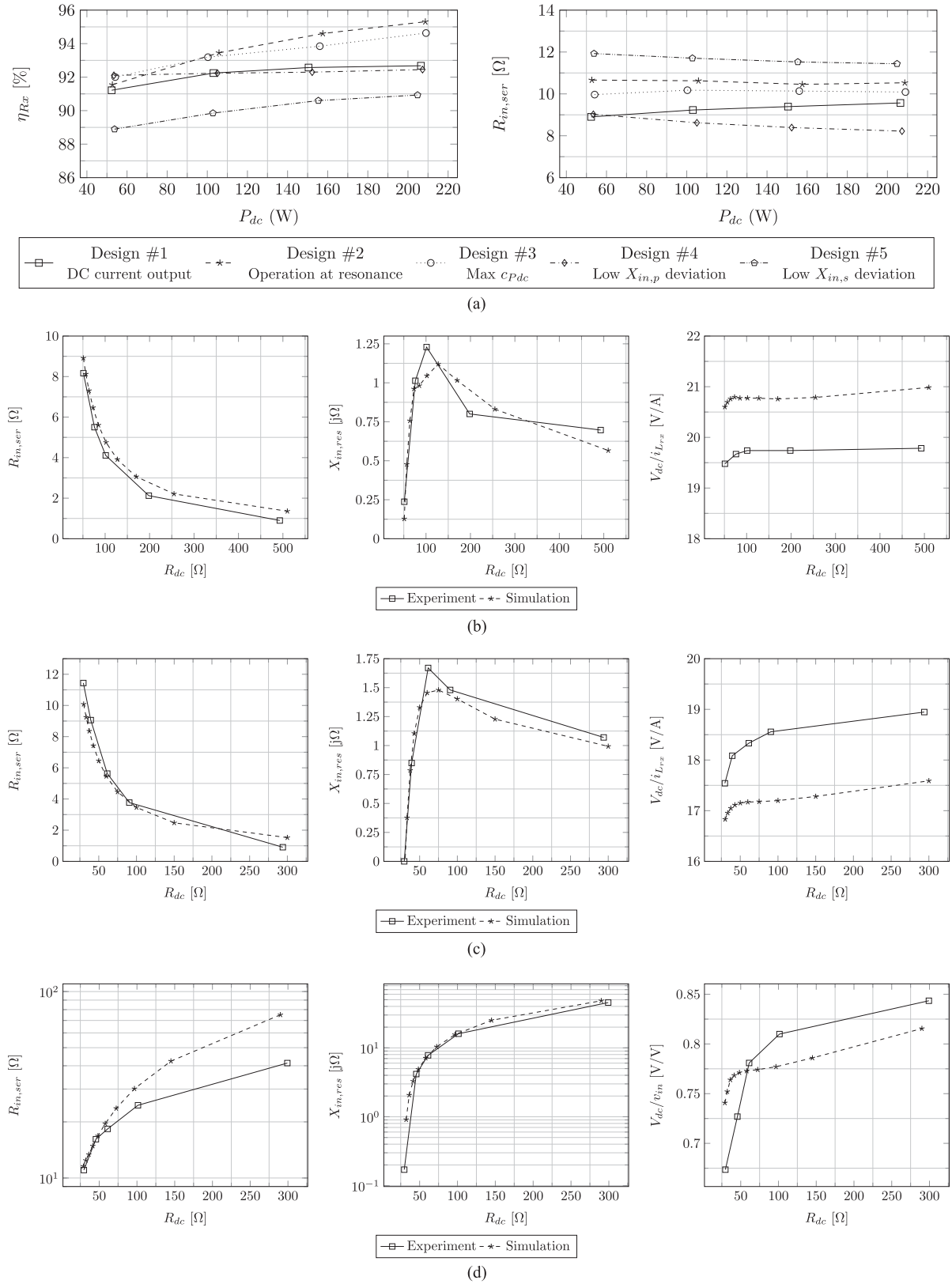

Fig. 7. Case studies experimental results. (a) Performance of all rectifier designs at a constant dc load resistance. (b) Series input resistance and reactance of Design #4 (HVDR: Low $X_{\mathrm{in,p}}$ deviation) at variable dc load. Output voltage was inherently regulated within 2.1% of its initial value by keeping constant the current in the receiving coil. (c) Series input resistance and reactance of Design #5 (CDR: Low $X_{\mathrm{in,s}}$ deviation) at variable dc load. Output voltage was inherently regulated within 8% of its initial value by keeping constant the current in the receiving coil. (d) Series input resistance and reactance of Design #2 (HVDR: Operation at resonance) at variable dc load. Output voltage was inherently regulated within 25.3% of its initial value by keeping constant the amplitude of the emulated induced emf in the receiving end.

The design values of the components in each design are presented in Table IV along with the actual values used in the experiments. The design variables of (5)–(8) were evaluated using the equations in Appendix A.

The four HVDR designs were implemented with a different combination of A_r and B to investigate which combination of LC network components will deliver the best efficiency and the required input resistance for the same $R_{\rm dc}$. All the HVDR designs had the same M_V, except Design #4, since as discussed in Section III-D, B had to be evaluated to yield an input capacitance smaller than the tuning capacitance of L_{rx}. A_r in the CDR (Design #5) was selected to also result in a circuit with $R_{\rm dc}$ equal to the value for the other rectifiers.

For each design, the inductor (L) was implemented first. Based on its measured value the other passive components were chosen such that the initial selection of A_r and B, or just A_r for the CDR, was satisfied. In Table IV, the experimental values of the capacitor in parallel with the diode, C_p for Designs #1–#4 and C for Design #5, do not include the p-n junction capacitance of the diode ($C_{\rm pn}$) and are hence the capacitance of the physical capacitors added to the circuit which is equal to the design value. All inductors were implemented with micrometals iron powder cores for RF applications. Specifically, in Design #1, a T106-3 core was used, and in Designs #2–#5, T106-2 cores were used. All capacitors were from the AVX high Q range. Component impedance measurements were made with a Keysight Technologies impedance analyzer. All rectifiers utilized a single Wolfspeed SiC Schottky diode, the C3D10065A, which has 10A forward current capability and 650V blocking voltage capability.

B. Experimental Test Rig

To allow careful characterization of rectifiers and to avoid the need of an inductive link and its associated instrumentation for testing the rectifier, a test rig was developed that reproduces IPT conditions in the tuned Rx coil when a rectifier is added at the receiver. With this test rig, calculation of the efficiency of the receiver (η_{Rx}) and the input resistance of the rectifier under test (RUT) as seen from the output of the inverter is possible without affecting any other part of the IPT system. More information about the test rig and the calculation of the worst case error in the experimental measurements can be found in Appendix B. Further implementation details for the test rig can be found from our work in [35].

C. Experimental Results and Discussion

The five implemented rectifiers will now be compared with respect to their efficiency and their effect on the inductive link. To ensure repeatability of results, a power sweep was performed in each experiment and measurements were recorded twice, when the output power was increasing from minimum to maximum and when the output power was decreasing from maximum to minimum. The results presented are the average.

The test rig enables measurement of the combined impedance of the receiving coil, external tuning capacitor, and the RUT. At resonance, this impedance is equal to the equivalent series input resistance of the rectifier, $R_{\rm in,ser}$. In the current-driven case, $R_{\rm in,ser}$ is equal to $R_{\rm in,s}$, and in the voltage-driven case, $R_{\rm in,ser}$ is equal to the series transformation of $R_{\rm in,p}$. When the rectifier is designed to reflect the optimal load this $R_{\rm in,ser}$ value is equal to $R_{\rm ac,ser}$ independent of series or parallel tuning (which is equal to 10.6Ω in this case study).

Fig. 7(a) presents the measured η_{Rx} and $R_{\rm in,ser}$ for varying power (50–200W). Fig. 7(b)–(d) shows the results of the variable $R_{\rm dc}$ experiments for Designs #2, #4, and #5 over a dc load range between 10% and 100%. At every dc load step, the $R_{\rm in,ser}$ of the topology and the residual reactance at the resonant tank ($X_{\rm in,res}$) were calculated. $X_{\rm in,res}$ is the uncompensated reactance between the reactances of the Rx coil, the external tuning capacitor, and the input reactance of the rectifier. To examine the inherent voltage regulation feature, the ratio between the output dc voltage to the current in the receiving coil ($V_{\rm dc}/i_{\rm in}$) was calculated in Designs #4 and #5, and in Design #2, the ratio between the output dc voltage to the amplitude of the presented emf ($V_{\rm dc}/v_{\rm in}$) was calculated. The experimental results are compared with time-domain SPICE simulations. The simulations used the measured component values from the experimental work (see Table IV).

According to the plots in Fig. 7(a), all designs showed low deviation in efficiency over the entire output power range. The worst case deviation in efficiency over $P_{\rm dc}$ was in Design #2 and was 4%. Designs #2, #3, and #5 exhibited deviations in $R_{\rm in,ser}$ lower than 3% from the nominal value, whereas Designs #1 and #4 exhibited deviations of 7.2% and 9.4%, respectively. Design #1 had the lowest capacitance across the diode amongst the implemented rectifiers and is therefore more sensitive to the variation of p-n junction capacitance. Design #4 on the other hand, although having a significantly higher C_p, is more sensitive to variations in X_C than Design #1 due to the selection of A_r. Based on the $Q_{\rm in}$ profile in Fig. 5, it can be seen that a small variation in A_r, when it is greater than 1.6, will result in a large variation of $Q_{\rm in}$ and therefore in $R_{\rm in,p}$. While Design #5, the current-driven topology, operates in the same A_r region as Design #4, its $R_{\rm in,ser}$ profile over output power has a much lower deviation than $R_{\rm in,ser}$ of Design #4. This is because the capacitance across the diode in Design #5 is twice the magnitude of the respective capacitance in Design #4.

Design #5 (the CDR) has the lowest η_{Rx} because the losses in its L are the highest amongst the five designs. Since all the designs, apart from Design #4, have the same $R_{\rm dc}$, the inductors (L) in Designs #1–#3 and #5 experience identical voltage waveforms over a cycle. Thus, the highest inductor current amongst the designs occurs in Design #5 causing the highest losses. Comparing the HVDR circuits, Designs #1–#4, the higher the presented $R_{\rm in,ser}$, the higher the receiving end efficiency was achieved. In general, all the developed rectifiers presented an error in their $R_{\rm in,ser}$ proportional to the error between theoretical and experimental values of $R_{\rm dc}$. Error in the experiment is larger for solutions where the diode parasitic capacitance is significant compared to the external capacitance across the diode and where the sensitivity of $Q_{\rm in}$ to A_r is large. Hence, the greatest error was observed in Designs #4 and #5.

Figs. 7(b)–(d) shows good agreement between simulation and experimental results. In simulations, the passive components were set equal to the measurements of the impedance analyzer. Designs #2, #4, and #5 performed as expected, in which in Designs #4 and #5, $R_{\mathrm{in,ser}}$ decreased with R_{dc}, and in Design #2, $R_{\mathrm{in,ser}}$ increased with R_{dc}. In terms of input reactance variation, Designs #4 and #5 presented residual reactances at the receiving end with magnitude smaller than 1% of the impedance of the receiving coil, X_{rx}. Furthermore, in these two designs, the output voltage was inherently regulated when the current in the receiving coil was kept constant. The output voltage was regulated within 3% and 8% of its initial value in Design #4 and in Design #5, respectively. Design #2 also exhibits some inherent output voltage regulation with a deviation of 25% for constant input voltage.

To investigate further how the implemented rectifiers affect the efficiency of the inductive link and the reflected impedance at the transmitting coil, the measured values of Fig. 7(b) and (d) were mapped on the contour plots of Fig. 8. Fig. 8(a)–(c) shows the contours of the inductive link efficiency (η_{link}), the reflected resistance at the transmitting coil (R_{ref}), and the reflected reactance at the transmitting coil (X_{ref}), respectively. All contours of Fig. 8 are plotted as functions of the normalized resistance seen by the receiving coil, $R_{\mathrm{in,ser}}/R_{\mathrm{ac,ser}}$, and the normalized residual reactance at the resonant receiving tank, $X_{\mathrm{in,res}}/X_M$. Note that $R_{\mathrm{ac,ser}}$ is the ac resistance at the receiving end that provides the optimal link efficiency and X_M is the impedance of the magnetizing inductance between the coils forming the inductive link (which is 7.11Ω at the frequency of operation). The data of the contours were derived from the parameters of the inductive link in [2] and the IPT expressions in [1]. Moreover, the contours of η_{link} and R_{ref} are normalized to their respective optimal values (given in Table II). Finally, the contours of X_{ref} are normalized to X_M.

The trajectories of the normalized values of $R_{\mathrm{in,ser}}$ and $X_{\mathrm{in,res}}$ have been added to the contours plots of Fig. 8. Specifically, the experimental data of Designs #2 and #4 have been used as they both exhibit the desirable property of inherent voltage regulation for variable dc load and Design #4 also exhibits low deviation in input reactance with variation in dc load. As Design #5 behaves in the same way as Design #4 with regards to these parameters, only the data from Design #4 have been plotted in Fig. 8.

As shown in Fig. 8(a), at 100% dc load, all tested designs are within the $\eta_{\mathrm{link,opt}}$ contour. As the load decreases down to 50%, all designs fall into lower efficiency contours but they are within 97% of the $\eta_{\mathrm{link,opt}}$. Although Design #2 is detuning the receiving coil at dc loads lower than 100%, the resultant link efficiency is actually slightly higher than that for Design #4 for the same load value. This occurs because $R_{\mathrm{in,ser}}$ of Design #2 increases from its initial value, rather than decreases as in the case of Design #4, where the link efficiency is more tolerant to the presence of residual reactance, as shown in the contours of Fig. 8(a). At dc loads lower than 20%, the link efficiency in both designs falls below 90% of $\eta_{\mathrm{link,opt}}$; however, the losses in the inductive link would be smaller in magnitude than the losses when maximum power is transferred at $\eta_{\mathrm{link,opt}}$.

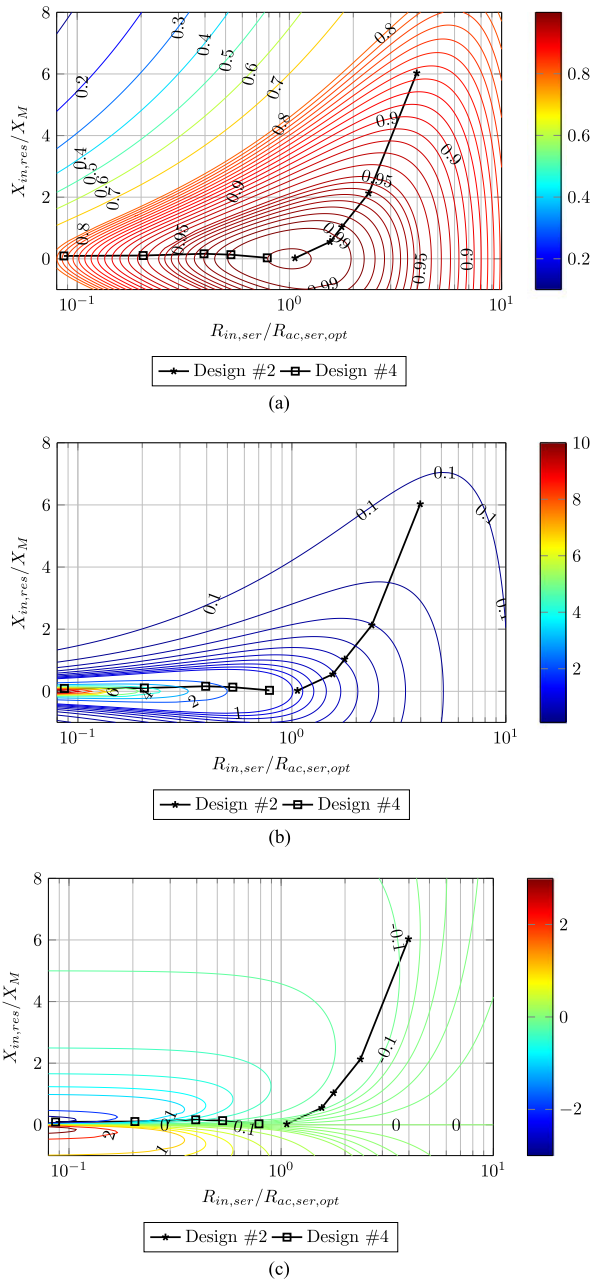

Fig. 8. Effect of implemented rectifiers on inductive link efficiency and loading on the transmitting coil. (a) Contours of link efficiency (η_{link}) normalized to the optimal link efficiency ($\eta_{\mathrm{link,opt}}$). From 80% to 95% the contours appear in steps of 1% and from 95% to 99% in steps of 0.5%. (b) Contours of reflected resistance (R_{ref}) to the transmitting coil (L_{tx}) normalized to the reflected resistance at optimal link efficiency conditions ($R_{\mathrm{ref,opt}}$). From 0.1 to 1 the contours appear in steps of 0.1 and then in steps of 1. (c) Contours of reflected reactance (X_{ref}) to the transmitting coil (L_{tx}) normalized to the impedance of the magnetizing inductance of the coils forming the inductive link (X_M). From 0 to 0.1 the contours appear in steps of 0.02, then from 0.1 to 0.2 in steps of 0.1 and then in steps of 0.2.

In Fig. 8(b) and (c), the reflected impedance at the transmitting coil behaves inversely to the input impedance of the utilized rectifier. This is a basic property of inductive links. In Design #2, R_{ref} decreases linearly as R_{dc} increases. On the other hand, in Design #4, R_{ref} increases linearly as R_{dc} increases. In terms of reflected reactance (X_{ref}), in Design #2, the

reflected reactance does not increase beyond 0.15 times X_M, despite the residual reactance at the receiving coil reaching six times X_M. Comparing the magnitude of $X_{\rm ref}$ for Design #2 to the impedance of the transmitting coil (X_{Tx}), $X_{\rm ref}$ is always lower than 1% of X_{Tx} and will not affect the tuning of the Tx coil. On the contrary, while Design #4 does not introduce a $X_{\rm in,res}$ greater than 25% of X_M, the $X_{\rm ref}$ for this design increases with $R_{\rm dc}$ and can reach almost three times the magnitude of X_M.

The inherent output voltage regulation feature can be achieved in both Design #2 and Design #4. For Design #2, a constant output current at the Tx will result in a constant induced voltage in the Rx coil, thus providing the condition for the output voltage regulation feature. In Design #2, the transmitting resonant tank will not be affected by the variation of $R_{\rm dc}$. Hence, since $R_{\rm ref}$ decreases with $R_{\rm dc}$, a constant output current Class-EF inverter such as the one presented in [36] will be compatible. In Design #4, inherent output voltage regulation occurs with a constant current in the Rx coil. This requires the variation of the magnitude of the induced voltage in the Rx coil and, hence, the variation in the current in the Tx coil. Since the reflected impedance increases with $R_{\rm dc}$, a Class-D ZVS constant output voltage inverter such as the one presented in [37] will be capable to provide the conditions for inherent output voltage regulation and compensate for the variation in reflected reactance at the Tx coil.

V. Conclusion

In this paper, conventional and hybrid Class-E half-wave zero *dv/dt* rectifiers were analyzed in terms of the parameter A_r, defined as the ratio of the resonant frequency of the utilized LC network to the operating frequency. The results of this analysis were illustrated in a way that designers are able to observe the variations in rectifier behavior over A_r and choose the best suited topology based on the requirements of the application. Based on the analytical results the following conclusions can be made about half-wave Class-E rectifiers operating with a duty cycle equal or lower than 50% when designed for IPT.

1) The voltage-driven Class-E rectifier with a series inductor will always require an inductor of larger impedance than the impedance of the receiving coil to allow the input resistance required by optimal link efficiency conditions to be presented. Therefore, the implementation of the series inductor will always be a challenge when high Q, high impedance coils are forming the link.
2) The voltage-driven Class-E rectifier with a series capacitor does not absorb the parasitic capacitance of the diode in its LC network and its operation will be heavily affected when the p-n junction capacitance is in the same order of magnitude as the series capacitor.
3) There are specific regions of A_r where the behavior of the input resistance of the rectifiers is consistent with duty cycle variations. When A_r is unity the series input resistance of the rectifiers, whether being voltage or current driven, increases as the output dc resistance increases. On the other hand, when A_r is greater than 1.5, the series input resistance of the rectifiers decreases as the dc resistance increases.
4) The current-driven topology, the voltage-driven topology with a series capacitor, and the hybrid topology exhibit a low deviation in their input reactance as the output dc resistance increases, when designed with an A_r between 1.75 and 2. In particular, a deviation of less than 13% is observed in the input reactance of the current-driven topology and a deviation of less than 5% is observed in the input reactance of the latter two rectifier topologies.

The case studies in this paper were focused on making the use of Class-E rectifiers feasible and effective in IPT systems. Furthermore, the experiments aimed to investigate the effect of passives on the performances of the hybrid rectifier and to evaluate the behavior of input resistance and input reactance of the hybrid and current-driven rectifiers. A test rig was developed that emulates IPT conditions and properly characterizes rectifiers without the need of an inductive link. Based on the experimental results, the following conclusions can be made.

1) The best efficiency was recorded in the hybrid topology when designed to operate at a unity A_r.
2) The sensitivity of the implemented rectifiers on the diode's p-n junction capacitance becomes higher when A_r is smaller than 0.4 and greater than 1.6. In the former region, the external capacitor across the diode is lower than the resultant capacitance in any other A_r region when the rectifier is designed to present the same input resistance while having the same dc load. In the latter region, a small variation in A_r will result in a much larger variation in the input resistance of the topology.
3) The hybrid and current-driven Class-E rectifiers, when designed at A_r between 1.75 and 2, can provide inherent output voltage regulation as their dc load decreases from 100% to 10%. This feature is feasible by keeping the current in the receiving coil constant. The achieved regulation was within 3% and 8% of the nominal output voltage for the hybrid and the current-driven rectifier, respectively.

In summary, the hybrid rectifier has been shown to be a good choice for weakly coupled inductive links as it can have a power robust operation and match any dc load to the desirable ac resistance while exhibiting any of the properties of the conventional Class-E half-wave zero *dv/dt* rectifiers. This includes low loss inductor realization, low deviation in input reactance, and inherent output voltage regulation.

Appendix A
Equations and General Derivation Method of Class-E Rectifier Design Variables

The input sources were assumed sinusoidal and were expressed by

$$v_{\rm in}(\theta) = \frac{V_{\rm dc}}{M_V}\sin(\theta+\phi) \tag{11}$$

in the voltage-driven topologies and

$$i_{\rm in}(\theta) = \frac{I_{\rm dc}}{M_I}\sin(\theta+\phi) \tag{12}$$

TABLE V
DESIGN VARIABLES OF CURRENT-DRIVEN RECTIFIER [SEE FIG. 2(B)]

Operating away from resonance, $A_r \neq 1$,	
$\tan\phi = -Ar\,[(\cos(Ar\,\psi)-\cos\psi)\,(\sin(Ar\,\psi)+Ar\,(2\,\pi-\psi))-(\sin(Ar\,\psi)-Ar\,\sin\psi)\,(\cos(Ar\,\psi)-1)]/\,\{(\cos(Ar\,\psi)-1)\,(Ar^2\,(\cos\psi-1)+2\,\sin((Ar\,\psi)/2)^2)-(\sin(Ar\,\psi)-Ar\,\sin\psi)\,[\sin(Ar\,\psi)+Ar\,(2\,\pi-\psi)]\}.$	(24)
$Q_r = -4\,\pi\,[\sin(Ar\,\psi)\,\sin\phi+Ar\,\cos(\phi+\psi)-Ar\,\cos(Ar\,\psi)\,\cos\phi]/\{-Ar^3\,[2\,\cos(\phi+\psi)\,(1-\cos(Ar\,\psi))+\cos\phi\,(2\,(\cos(Ar\,\psi)-1)+\cos\psi\,(2\,\pi-\psi)^2-\cos(Ar\,\psi)\,(\psi-2\,\pi)^2)+\sin\phi\,(2\,\pi-\psi)\,((\psi-2\,\pi)\,\sin\psi+2\,(\cos(Ar\,\psi)-1))]-2\,Ar\,(\cos(Ar\,\psi)-1)\,(\cos(\phi+\psi)-\cos\phi-2\,\pi\,\sin\phi+\psi\,\sin\phi)-Ar^2\,\sin(Ar\,\psi)\,\sin\phi\,(2\,\pi-\psi)^2\}.$	(25)
$M_I = [\sin(Ar\,\psi)\,\sin\phi+Ar\,\cos(\phi+\psi)-Ar\,\cos(Ar\,\psi)\,\cos\phi]/[Ar\,Q\,(Ar^2-1)\,(\cos(Ar\,\psi)-1)].$	(26)
$N_{\rm in} = -\psi/[2\,\pi\,(Ar^2-1)]-\{[(2\,\sin(Ar\,\psi)\,(1-Ar^2))\,(\cos\phi)^2+\sin\psi\,(2\,Ar\,(1-Ar^2))\,(\sin\phi)^2-2\,\sin(Ar\,\psi)]\,\cos\psi+[Ar\,\sin(2\,\phi)(1-Ar^2)]\,(\sin\psi)^2+[Ar\,\sin(2\,\psi)\,(Ar^2-1)]/2+\sin\psi\,[2\,Ar\,\cos(Ar\,\psi)-\sin(2\,\phi)\,\sin(Ar\,\psi)\,(1-Ar^2)]\}/[2\,Ar\,\pi\,(Ar^2-1)^2]-K\,Q\,\{2\,\cos(Ar\,\psi)\,\sin(\phi+\psi)-2\,Ar\,\sin(Ar\,\psi)\,\cos(\phi+\psi)+2\,\sin(\phi+\psi)\,(Ar^2-1)-2\,Ar^2\,\sin\phi\}/[2\,\pi\,(Ar^2-1)].$	(27)
Operating at resonance, $A_r = 1$.	
$\tan\phi = -[\psi\,\sin\psi\,(\psi-2\,\pi)+(\cos\psi-1)\,(\psi+\sin\psi)]/[(\cos\psi)^2+(\psi^2-2\,\pi\,\psi-4)\,\cos\psi+(2\,\pi-2\,\psi)\,\sin\psi+3].$	(28)
$Q_r = 4\,\pi\,[\psi\,\sin(\phi+\psi)-\sin\phi\,\sin\psi]/\{4\,\cos(\phi+\psi)+\cos\phi\,(4\,(\cos\psi-1)+\psi\,\sin\psi\,(\psi-2\,\pi)^2)-4\,\cos(\phi+\psi)\,\cos\psi+\sin\phi\,(2\,\pi-\psi)\,[4\,(\cos\psi-1)+(2\,\pi-\psi)\,(\psi\,\cos\psi-\sin\psi)]\}.$	(29)
$M_I = [\psi\,\sin(\phi+\psi)-\sin\phi\,\sin\psi]/[2\,Q_r\,(\cos\psi-1)].$	(30)
$N_{\rm in} = [2\,\psi+2\,\sin(2\,\phi)+\sin(2\,\psi)-2\,\sin(2\,(\phi+\psi))-4\,\psi\,(\sin\phi)^2-4\,\psi\,\sin(\phi+\psi)^2]/[16\,\pi]+[M_I\,Q_r\,(\sin(\phi+2\,\psi)/2-2\,\sin(\phi+\psi)+(3\,\sin\phi)/2+\psi\,\cos\phi)]/[2\,\pi].$	(31)

in the current-driven topology. In both (11) and (12), θ is the product of ω and time t and ϕ is the phase of the input source when the diode turns OFF. The following definitions were also used:

$$i_C(\theta) = \left(\frac{1}{X_C}\right)\frac{d}{d\theta}\left[v_D(\theta)\right] \tag{13}$$

$$v_L(\theta) = X_L\,\frac{d}{d\theta}\left[i_L(\theta)\right] \tag{14}$$

$$-V_{\rm dc} = \frac{1}{2\pi}\int_0^{\psi} v_D(\theta)d\theta \tag{15}$$

$$I_{\rm dc} = \frac{1}{2\pi}\int_{\psi}^{2\pi} i_D(\theta)d\theta \tag{16}$$

where (15) and (16) are derived by applying Kirchoff's voltage and current laws, respectively. Variable ψ is the interval in which the diode is reverse biased and is given as

$$\psi = 2\pi(1-d_r). \tag{17}$$

From (15) and (16), the loaded quality factor as a function of ψ, and hence duty cycle, is given by

$$Q_r = -\left(\frac{\int_0^{\psi} v_D(\theta)d\theta}{\int_{\psi}^{2\pi} i_D(\theta)d\theta}\right)\left(\frac{1}{X}\right). \tag{18}$$

In order for the topologies to achieve low dv_D/dt at turn off the following conditions must also be met

$$v_D(0) = v_D(\psi) = \frac{d}{d\theta}\left[v_D(0)\right] = 0 \tag{19}$$

$$i_D(2\pi) = 0 \tag{20}$$

$$i_C(\psi^-) = i_D(\psi^+). \tag{21}$$

Finally, the following expressions have to be used for deriving the input reactance of the rectifiers at the frequency of operation:

$$i_{\rm in,1} = \frac{1}{\pi}\int_0^{2\pi} i_{v_{\rm in}}(\theta)\,\cos(\theta+\phi)d\theta \tag{22}$$

$$v_{\rm in,1} = \frac{1}{\pi}\int_0^{2\pi} v_{i_{\rm in}}(\theta)\,\cos(\theta+\phi)d\theta \tag{23}$$

where $i_{\rm in,1}$ is the first harmonic of the current $i_{v_{\rm in}}$, which is drawn from the input source in the voltage-driven rectifiers and $v_{\rm in,1}$ is the first harmonic of the voltage $v_{i_{\rm in}}$ across the input source in the CDR.

The equations of the design variables of the examined rectifiers are presented in Tables V–VIII. It should be noted that for the CDR [see Fig. 2(b)] and the series-C VDR [see Fig. 2(c), there are different equations describing variables ϕ and Q_r, although their profiles over duty cycle and ratio A_r have the same evaluation. Furthermore, in the HVDR [see Fig. 2(a), variables ϕ and Q_r are independent of variable B and are therefore expressed by the equations of the respective variables in the series-C VDR. The process of deriving the design variables as functions of duty cycle and ratio A_r can be found in [26] for operation at resonance and in [30] for operation around resonance.

APPENDIX B
DESCRIPTION OF TESTING APPARATUS

Characterizing a rectifier in terms of input resistance and efficiency while integrated in a multi-MHz IPT system is not a trivial task. Calculation of the input power to the rectifier will be required and therefore the voltage across the receiving coil, $v_{L_{rx}}$, and the current through it have to be measured. In this frequency range, the capacitance introduced by a voltage probe is not negligible and can affect the circuit under test. Therefore, measuring the voltage across L_{rx} while operating in a complete IPT system will detune the receiving end and lead to wrong assumptions about the effect of the rectifier on the inductive link. Furthermore, while instrumentation via capacitive division could make the presence of a voltage probe intrinsic capacitance

TABLE VI
DESIGN VARIABLES OF VOLTAGE-DRIVEN RECTIFIER WITH SERIES INDUCTOR [SEE FIG. 2(A)]

Operating away from resonance, $A_r \neq 1$.

$$\tan(\phi+\pi) = \{4\sin((Ar\,\psi)/2)^2\,(Ar^2\sin(\psi/2)^2-1)+Ar\sin\psi\,(\sin(Ar\,\psi)-Ar\,(2\pi-\psi))-Ar\sin(Ar\,\psi)\,(2\pi-\psi)\}/\{Ar\,[(1-\cos\psi)\sin(Ar\,\psi)+(Ar\,(2\pi-\psi+\sin\psi))\cos(Ar\,\psi)-Ar\,(\sin\psi+\cos\psi\,(2\pi-\psi))]\}. \quad (32)$$

$$M_V = \{Ar\,[\cos\phi\,(\sin(Ar\,\psi)-Ar\sin\psi)+Ar\sin\phi\,(\cos(Ar\,\psi)-\cos\psi)]\}/[(Ar^2-1)\,(\cos(Ar\,\psi)-1)]. \quad (33)$$

$$Q_r = 2\,\{(Ar^2-1)\,(Ar\,\psi-\sin(Ar\,\psi))\,M_V + Ar^2\,(\sin(Ar\,\psi)-Ar\sin\psi)\sin\phi + Ar\,(2\sin((Ar\,\psi)/2)^2+Ar^2\,(\cos\psi-1))\cos\phi\}/\{Ar\,(Ar^2-1)\,(2\sin(\phi+\psi)-2\sin\phi+2\cos\phi\,(2\pi-\psi)+M_V\,(\psi-2\pi)^2)\}. \quad (34)$$

$$N_{\text{in}} = [4\pi\,Ar\,(Ar^2-1)^2]/\{[4\pi-2\psi+2\sin(2\phi+\psi)-\sin(2\phi)-\sin(2\phi+2\psi)+2\sin\psi-4\,M_V\,(\cos(\phi+\psi)-\cos\phi-\sin(\phi+\psi)(2\pi-\psi))]\,Ar^5+[2\psi-8\pi+2\sin(2\phi+\psi)\,(\cos(Ar\,\psi)-2)+\sin(2\phi)+\sin(2\phi+2\psi)-2\sin\psi\,(\cos(Ar\,\psi)+2)-M_V\,(4\cos(\phi+\psi)\,(\cos(Ar\,\psi)-2)+4\cos\phi+8\sin(\phi+\psi)\,(2\pi-\psi))]\,Ar^3+4\sin(Ar\,\psi)\,[(\cos\psi-M_V\sin(\phi+\psi))\,Ar^2+M_V\sin(\phi+\psi)]+[2\,(2\pi-(\sin(2\phi+\psi)+\sin\psi)\,(\cos(Ar\,\psi)-1))+4\,M_V\,(\cos(\phi+\psi)\,(\cos(Ar\,\psi)-1)+\sin(\phi+\psi)\,(2\pi-\psi))]\,Ar\}. \quad (35)$$

Operating at resonance, $A_r = 1$ (Derived expressions same as in [26]).

$$\tan\phi = [2\cos\psi\,(\cos\psi+\psi\,(\psi-2\pi)-4)+4\sin\psi\,(\pi-\psi)+6]/[\sin(2\psi)+2\,((\psi-2\pi)\,\psi-1)\sin\psi+2\,\psi\,(\cos\psi-1)]. \quad (36)$$

$$M_V = [\psi\cos(\phi+\psi)-\cos\phi\sin\psi]/[2\,(\cos\psi-1)]. \quad (37)$$

$$Q_r = [\cos(\phi-\psi)+3\cos(\phi+\psi)-4\cos\phi+2\,\psi\sin(\phi+\psi)+4\,M_V\,(\psi-\sin\psi)]/[4\sin(\phi+\psi)-4\sin\phi+4\cos\phi\,(2\pi-\psi)+2\,M_V\,(\psi-2\pi)^2]. \quad (38)$$

$$N_{\text{in}} = -16\pi/[(4\cos(\phi+2\psi)+16\cos(\phi+\psi)-20\cos\phi+16\,(\psi-2\pi)\sin(\phi+\psi)+8\,\psi\sin\phi)\,M_V+6\psi-16\pi)-8\sin(2\phi+\psi+4\sin(2\phi)+\sin(2\psi)+4\sin(2\phi+2\psi)-8\sin\psi+2\psi\cos(2\phi)-2\psi\cos(2\phi+2\psi)]. \quad (39)$$

TABLE VII
DESIGN VARIABLES OF VOLTAGE-DRIVEN RECTIFIER WITH SERIES CAPACITOR [SEE FIG. 2(C)]

Operating away from resonance, $A_r \neq 1$.

$$\tan\phi = -[(\cos(A_r\,\psi)-1)\,(A_r{}^2\,(\cos\psi-1)+2\sin((A_r\,\psi)/2)^2)-(\sin(A_r\,\psi)-A_r\sin\psi)\,(\sin(A_r\,\psi)+A_r\,(2\pi-\psi))]/[A_r\,(\sin(A_r\,\psi)-A_r\sin\psi)\,(\cos(A_r\,\psi)-1)-A_r\,(\cos(A_r\,\psi)-\cos\psi)\,(\sin(A_r\,\psi)+A_r\,(2\pi-\psi))]. \quad (40)$$

$$M_V = (\sin(A_r\,\psi)\cos\phi-A_r\,(\sin(\phi+\psi)-\cos(A_r\,\psi)\sin\phi))/(A_r\,(A_r{}^2-1)\,(\cos(A_r\,\psi)-1)). \quad (41)$$

$$Q_r = [4\sin((A_r\,\psi)/2)^2\cos\phi+2\,A_r\sin(A_r\,\psi)\,(M_V+\sin\phi)-2\,A_r{}^2\,(\cos\phi-\cos(\phi+\psi)+M_V\,\psi)-2\,A_r{}^3\,M_V\,(\sin(A_r\,\psi)-A_r\,\psi)]/[A_r{}^4\,(2\sin(\phi+\psi)-2\sin\phi\,(\sin\psi\,(2\pi-\psi)+1)+M_V\,(2\pi-\psi)^2+2\cos\phi\cos\psi\,(2\pi-\psi))-A_r{}^2\,(2\sin(\phi+\psi)-2\sin\phi+2\cos(A_r\,\psi)\cos\phi\,(2\pi-\psi))-A_r{}^6\,M_V\,(2\pi-\psi)^2-2\,A_r{}^5\,M_V\sin(A_r\,\psi)\,(2\pi-\psi)+2\,A_r{}^3\sin(A_r\,\psi)\,(M_V+\sin\phi)\,(2\pi-\psi)]. \quad (42)$$

$$N_{\text{in}} = 4\pi\,(A_r{}^2-1)^2/\{[4\pi+M_V\,(4\,(\cos(A_r\,\psi)\cos(\phi+\psi)-\cos\phi))]\,A_r{}^4+M_V\,[4\sin(A_r\,\psi)\sin(\phi+\psi)]\,A_r{}^3+[2\psi-8\pi+\sin(2\phi)+2\cos(A_r\,\psi)\sin\psi+\sin(2\phi+2\psi)-M_V\,(4\,(\cos(A_r\,\psi)\cos(\phi+\psi)-\cos\phi))-2\sin(2\phi+\psi)\cos(A_r\,\psi)]\,A_r{}^2-[M_V\,(4\sin(A_r\,\psi)\sin(\phi+\psi))+4\sin(A_r\,\psi)\cos\psi]\,A_r+2\,(2\pi-\psi)-\sin(2\phi)+2\cos(A_r\,\psi)\sin\psi-\sin(2\phi+2\psi)+2\sin(2\phi+\psi)\cos(A_r\,\psi)\}. \quad (43)$$

Operating at resonance, $A_r = 1$ (Derived expressions same as in [33]).

$$\tan\phi = [2\,(\pi-\psi)\sin\psi+(\cos\psi)^2+((\psi-2\pi)\,\psi-4)\cos\psi+3]/[(\cos\psi-1+(\psi-2\pi)\,\psi)\sin\psi+\psi\,(\cos\psi-1)]. \quad (44)$$

$$M_V = -[\cos\phi\sin\psi-\psi\cos(\phi+\psi)]/(2\cos\psi-2). \quad (45)$$

$$Q_r = \{4\,[(\sin\psi-\psi)\,M_V+\cos\phi]-2\,[\cos(\phi+\psi)+\cos\phi\cos\psi+\psi\sin(\phi+\psi)]\}/\{(4\,(2\pi-\psi)\sin\psi+2\,(\psi-2\pi)^2)\,M_V+4\sin\phi+3\cos(\phi+\psi)\,(\psi-2\pi)+(\psi-2\pi)\cos(\phi-\psi)+2\sin(\phi+\psi)\,[(\psi-2\pi)\,\psi-2]\}. \quad (46)$$

$$N_{\text{in}} = (16\pi)/[4\,M_V\,(\cos(\phi+2\psi)-\cos\phi+2\psi\sin\phi)+16\pi+\sin(2\psi)+2\psi\,(\cos(2\phi)-\cos(2\phi+2\psi)-1)]. \quad (47)$$

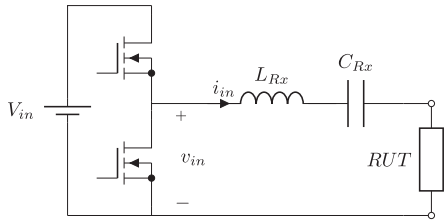

Fig. 9. Class-D inverter based test rig [25].

insignificant, the input power measurement will still be of great uncertainty because the phase between $v_{L_{rx}}$ and the current input to the rectifier will be nearly 90°. Therefore, small errors in phase will cause large errors in the ac power measurement. Hence, a test rig for rectifier characterization was developed that overcomes these challenges by taking the measurements separately from the inductive link.

The developed test rig, Fig. 9, is based on the voltage source Class-D inverter. The rig consists of a half-bridge, a resonant tank, and the RUT. The resonant tank is formed by the receiving coil, L_{rx}, and the tuning capacitor, C_{rx}. The half-bridge is driven by square wave gate drives to be able to generate voltages over a wide frequency band and it outputs a square wave voltage, v_{in}, which represents the voltage induced in a coil at the presence of an alternating magnetic field (IPT conditions). Due to the high quality factor of the resonant tank, which is essential for high link efficiencies at weakly coupled inductive links, only the fundamental harmonic of the square wave delivers power to the rectifier. Therefore, the current in L_{rx}, represented by i_{in} in Fig. 9, is sinusoidal. According to the tuning method of the receiving coil, the rig presents the appropriate ac source, voltage, or current for the RUT. As v_{in}, in Fig. 9, simulates the induced emf in the receiving coil it will be in phase with i_{in} when L_{rx} is properly tuned and small phase errors will be insignificant. Moreover, the presence of a voltage probe at the output of the half-bridge does not affect the tuning of the resonant tank. Hence, all the challenges from the presence of the inductive link are solved.

From Fig. 9, the average of the product of v_{in} and i_{in} at one period provides a measurement for the input power, P_{in}, which represents the power into the receiver (Rx) of an IPT system. Using the dc output power of the rectifier the efficiency of the

TABLE VIII
DESIGN VARIABLES OF HYBRID RECTIFIER [SEE FIG. 2(A)]

Operating away from resonance, $A_r \neq 1$		
$\tan\phi = eq(40)$	$M_V = eq(41)/[B+1]$	$Q_r = eq(42)$
$N_{\text{in}} = (4\,\pi\,(Ar^2-1)^2\,(B+1)^2)/\{[\cos\phi\,(4\,\cos\psi\,(1-Ar^2)\,(\cos(Ar\,\psi)-\cos\psi)) + 4\,Ar\,M_V\,(Ar^2-1)\,(\sin(Ar\,\psi)\,\cos\psi - Ar\,\cos(Ar\,\psi)\,\sin\psi)$		
$(B+1)]\,\sin\phi + 4\,\pi\,(B+1) - 2\,\psi + \sin(2\,\psi) + Ar^4\,(4\,\pi\,(B+1)) - [4\,\sin\psi\,(Ar^2-1)\,(\cos(Ar\,\psi)-\cos\psi)]\,\cos\phi^2 + \cos\phi\,[4\,Ar\,M_V\,(Ar^2-1)$		
$(B+1)\,(\sin(Ar\,\psi)\,\sin\psi + Ar\,(\cos(Ar\,\psi)\,\cos\psi - 1))] - Ar^2\,(8\,\pi\,(B+1) - 2\,\psi + \sin(2\,\psi) - 4\,\cos(Ar\,\psi)\,\sin\psi) - 4\,Ar\,\sin(Ar\,\psi)\,\cos\psi\}.$ (48)		
Operating at resonance, $A_r = 1$		
$\tan\phi = eq(44)$	$M_V = eq(45)/[B+1]$	$Q_r = eq(46)$
$N_{\text{in}} = 16\,\pi\,(B+1)^2/\{[8\,M_V\,\psi\,\sin\phi + 16\,\pi + 4\,M_V\,(\cos(\phi+2\,\psi) - \cos\phi)]\,(B+1) + \sin(2\,\psi) + 2\,\psi\,(\cos(2\,\phi) - \cos(2\,\phi+2\,\psi) - 1)\}.$ (49)		

TABLE IX
WORST CASE ERRORS IN TEST RIG MEASUREMENTS

Measured Quantity	Probe Part Number	Attenuation	Attenuation Error	Measurement Error
v_{in}	PPE 6kV	1000:1	2%	1.96%
i_{in}	6585 CM	1:1	N/A	1%*
V_{dc}	N2891A	100:1	2%	1.94%
I_{dc}	N2783A	10:1	1%	0.892%

* Error in current to voltage transformation.

TABLE X
WORST CASE ERRORS IN RECEIVING END RFFICIENCY (η_{Rx}) AND RECTIFIER INPUT SERIES RESISTANCE ($R_{\text{in,ser}}$)

Calculated Quantity	Positive Error	Negative Error
η_{Rx}	5.97%	5.63%
$R_{\text{in,ser}}$	2.99%	2.93%

receiver, η_{Rx}, can be calculated. Furthermore, using P_{in} and the rms of i_{in} the input resistance seen by the receiving coil, $R_{\text{in,ser}}$, can also be calculated. When a rectifier is added to the test rig, the amplitude of v_{in} is kept constant while its switching frequency is adjusted such that maximum dc output power is achieved. Maximum extracted dc power will be achieved only at the point where L_{rx} is at resonance.

Phase compensation for the instrumentation was performed to eliminate any time scale errors in the P_{in} measurement. First, the phase introduced by the transfer impedance of the current probe was accounted for using data provided by the manufacturing company (Pearson Electronics). Second, a comparison was made between the propagation delays in the BNC cable connecting the output of the current probe to the oscilloscope and the voltage probe used to monitor v_{in}. No difference was found between the propagation delays in the two cables. For zero skew, v_{in} and i_{in} will be in phase during rectifier characterization for a perfectly tuned circuit. Therefore, Fig. 7(a) shows the worst case efficiencies because any skew that is unaccounted for would result in the measured input power being lower than the actual input power and hence the actual efficiency would be higher than the recorded efficiency.

The instrumentation used to monitor each signal of the test rig is listed in Table IX, along with the maximum attenuation error and the worst case systematic error in the measurement of each signal. From the worst case error in each measurement, the worst case systematic error in parameters η_{Rx} and $R_{\text{in,ser}}$ were also calculated and are presented in Table X.

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