Stability Analysis and Controller Synthesis for Single-Loop Voltage-Controlled VSIs

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***Abstract*—This paper analyzes the stability of digitally voltage-controlled voltage-source inverters (VSIs) with the linear voltage regulators. It is revealed that the phase lags, caused by using the resonant controller and the time delay of a digital control system, can stabilize the single-loop voltage control without damping of the *LC*-filter resonance. The stability region for the digital single-loop resonant voltage control is then identified, considering the effects of different discretization methods for the resonant controller. An enhanced voltage control approach with a widened stability region is subsequently proposed, and a step-by-step design method of the proposed controller is developed based on the root contours in the discrete *z*-domain. Simulations and experimental tests of a 400-Hz VSI system validate the stability analysis and the performance of the proposed control approach.**

***Index Terms*—Stability, time delay, voltage control, voltage-source inverters (VSIs).**

I. Introduction

THE voltage-controlled voltage-source inverters (VSI) with an *LC*-filter have commonly been used for uninterruptible power supplies [1], [2], distributed generation systems [3], and other high-performance ac power sources, e.g., grid emulators [4] and power amplifiers in the hardware-in-the-loop tests [5]. A stable ac voltage with high waveform quality is demanded in these applications. To meet the requirements, a wide variety of voltage control schemes have thus been developed, which are, in general, categorized into two groups in respect to the control structure, i.e., the double-loop voltage–current control [6]–[8], [12], and the single-loop voltage control [9]–[11].

The double-loop control schemes are composed by an inner current loop based on feeding back the *LC*-filter inductor- or capacitor-current, and an outer voltage loop for controlling the filter capacitor voltage [6]. It has been shown that the inner loop can be equivalent to a virtual impedance, which is in series with the filter inductor or capacitor, corresponding to the feedback of filter inductor- or capacitor-current [7]. Besides the damping of the *LC*-filter resonance, the virtual impedance has also been used to decouple the resonant poles of the *LC*-filter in order to improve the dynamic performance of the voltage loop [12]. However, the virtual impedance only works well when the time delay of digital control has a negligible phase lag effect [11]. Considering the one sampling period (T_s) of digital computation delay and the zero-order hold (ZOH) effect of the digital pulsewidth modulation (PWM) [14]–[16], the virtual impedance exhibits a negative real part above the one-sixth of the sampling frequency ($f_s/6$). As a consequence, a negative damping is added into the system above $f_s/6$, which not only constrains the control bandwidth of the inner current loop [11], but may also degrade the voltage control performance [10].

For the VSIs with a high pulse ratio, namely, the ratio of the switching to fundamental frequency, the critical frequency $f_s/6$, is usually far above the fundamental frequency and low-order harmonic frequencies. The double-loop voltage control allows for a high-performance voltage regulation. However, for the VSIs with a low pulse ratio, either the very high power VSIs with 50-Hz outputs [4] or the 400-Hz ground power units [10], [11], the low-order harmonic frequencies may be close to or even above the critical frequency $f_s/6$. A negative damping will thus be synthesized by the inner loop at certain harmonic frequencies, which challenges the controller design of the outer voltage loop. Therefore, the double-loop control schemes can hardly fulfill the voltage waveform-quality requirement for the low-pulse-ratio VSIs [10], [11].

The single-loop voltage control schemes are thus preferred for low-pulse-ratio VSIs [9]–[11]. In order to mitigate the effect of the *LC*-filter resonance, the direct pole placement method based on the discrete z-domain model of VSIs has been reported in [9], [10]. It exhibits a better dynamic performance than the double-loop control schemes, but does also make the system sensitive to the variations of system parameters. To overcome this drawback, a single-loop resonant (R) control scheme was developed in [11]. Instead of the proportional + integral (PI) or P + R (PR) controllers, only the R controllers tuned at the fundamental frequency and low-order harmonic frequencies are adopted to regulate the output voltage with high waveform quality. However, the stabilization mechanism underlying this control approach is not explained. Moreover, the effects of the discretization methods for the R controller are also overlooked. Hence, the stability region of the single-loop R control is still not identified.

This paper thus presents first an in-depth stability analysis of the single-loop voltage control with the linear P or R regulators. The effects of digital computation and modulation delays on the system stability are analyzed. The critical frequency, above

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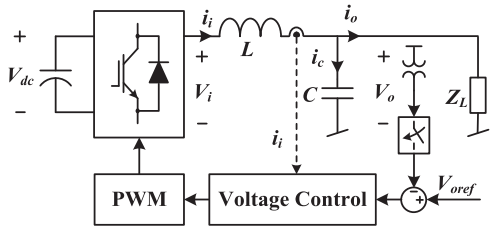

Fig. 1. Simplified single-line diagram of a three-phase voltage-controlled VSI with an *LC*-filter.

which the nonnegative phase margin (PM) can be preserved, is found in each case. The stability region for the single-loop R voltage control is identified, where the effects of discretization methods applied to the R controller is also considered. Moreover, it is found that the R controller gain is also affected by the output fundamental frequency, when the fundamental frequency approaches to the phase crossover frequency of the control loop, i.e., the frequency for the phase response crossing over $-\pi$. This effect complicates the tuning of the R controller gain.

Then, an enhanced single-loop voltage control scheme with the widened stability region is proposed in this paper. In this method, instead of using R controllers only, the basic integrator "1/*s*" is inserted in series with a PR controller. The R part of the PR controller is merely used for zero steady-state tracking error. The system dynamics are determined by the P controller, whose value is, unlike the single-loop R control scheme, independent on the fundamental frequency, and thus facilitates the parameter tuning. Moreover, a damping controller based on a negated low-pass filter is added in the capacitor voltage loop, which widens the stability region compared to that of the single-loop R control. A holistic design procedure for controller parameters is further developed based on the root contours in the discrete *z*-domain. Simulations and experimental tests of a 400-Hz VSI system are performed. The results confirm the effectiveness of the theoretical analysis and the performance of the proposed approach.

II. Stability of Voltage-Controlled VSIs

A. System Description

Fig. 1 illustrates a simplified single-line diagram of a three-phase voltage-controlled VSI with an *LC*-filter. The ac voltage across the filter capacitor is controlled with either the single- or double-loop control structure, and the filter inductor current is controlled as an inner loop in the double-loop control structure. The main circuit parameters of the VSI are provided in Table I. A constant dc-link voltage $V_{\rm dc}$ is assumed, and hence the *LC*-filtered VSI can be modeled as a linear time-invariant system in the stationary frame [13].

Fig. 2 shows the block diagrams of the digital single- and double-loop voltage control schemes, where the delay response of the digital PWM is modeled by the ZOH effect [14]–[16], and the one sampling period of computational delay (z^{-1}) is included [15]. The total time delay, in the continuous *s*-domain,

TABLE I
Main Circuit Parameters

Symbol	Electrical constant	Value
V_o	AC output voltage	400 V
f_1	AC output fundamental frequency	50 Hz
$f_{\rm sw}$	Inverter switching frequency	10 kHz
f_s	Control sampling frequency	10 kHz
V_{dc}	Inverter dc-link voltage	730 V
L	*LC*-filter—filter inductor	1.5 mH
C	*LC*-filter—filter capacitor	10 μF
Z_R	Resistive load	254 Ω
Z_{R-L}	Series *R-L* load—resistance (R_o)	134 Ω
	Series *R-L* load—inductance (L_o)	78 mH
$Z_{R//C}$	Parallel *R//C* load—resistance (R)	254 Ω
	Parallel *R//C* load—capacitance (C_o)	4.4 μF

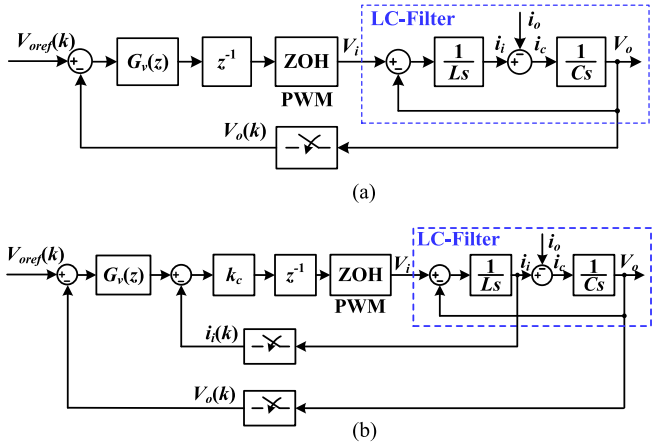

Fig. 2. Block diagrams of single- and double-loop voltage control schemes. (a) Single-loop voltage control. (b) Double-loop voltage control.

can thus be denoted by $G_d(s)$, which is given by

$$G_d(s) = e^{-1.5T_s s} \tag{1}$$

where T_s is the sampling period of the digital control system. In the double-loop voltage control scheme given in Fig. 2(b), the P controller k_c is used with the inner current loop, whereas the PR controller is used for the voltage regulation in the outer voltage loop.

B. Double-Loop Voltage Control

Fig. 3 depicts the block diagram of the double-loop voltage control scheme in the continuous *s*-domain and its equivalent diagram. By redrawing the inner current loop, the equivalent diagram given in Fig. 3(b) illustrates that the inner loop can be equivalent to a virtual impedance $Z_v(s)$ in series with the filter inductor. $Z_v(s)$ is given by

$$Z_v(s) = k_c e^{-1.5T_s s} \tag{2}$$

which is, by applying the Euler's formula, equivalent to

$$Z_v(j\omega) = k_c \left[\cos(1.5\omega T_s) - j\sin(1.5\omega T_s)\right]. \tag{3}$$

From (3), it is noted that the real part of the virtual impedance $Z_v(j\omega)$ is frequency dependent. It becomes negative between $f_s/6$ and the Nyquist frequency $f_s/2$. On the other hand, if

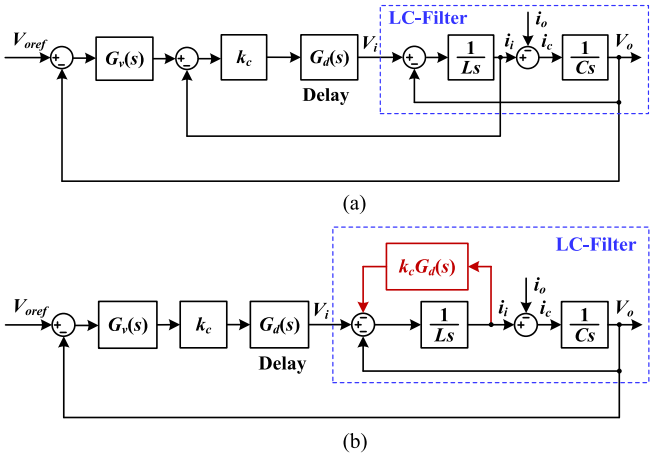

Fig. 3. Block diagram of the double-loop voltage control in the continuous s-domain and its equivalent diagram. (a) Double-loop voltage control in the continuous s-domain. (b) Equivalent diagram of double-loop voltage control.

the delay $G_d(s)$ is ignored, $Z_v(s)$ turns as a pure resistance $(Z_v(s) = k_c)$. The insertion of the negative damping resistance leads to an unstable open-loop gain and the consequent nonminimum closed-loop response of the outer voltage control loop [11].

Moreover, the addition of the integrator, i.e., $k_{\rm ic}/s$, in the inner current controller will aggravate the negative damping effect, due to the phase lag of $\pi/2$ brought by the integrator. This can also be explicitly elaborated by replacing the proportional gain k_c in (3) with the PI controller, i.e., $k_c + k_{\rm ic}/s$, which is given by

$$Z_v(j\omega) = \left(k_c + \frac{k_{\rm ci}}{j\omega}\right)\left[\cos(1.5\omega T_s) - j\sin(1.5\omega T_s)\right]. \quad (4)$$

The real part of the virtual impedance $Z_v(j\omega)$ is then changed as

$$\mathrm{Re}\left\{Z_v(j\omega)\right\} = k_c\cos(1.5\omega T_s) - \frac{k_{\rm ci}}{\omega}\sin(1.5\omega T_s) \quad (5)$$

where the term $\cos(1.5\omega T_s)$ becomes negative in the frequency region $(f_s/6,\ f_s/2)$, whereas the term $\sin(1.5\omega T_s)$ is kept positive in the region $(0,\ f_s/3)$. Hence, the negative damping effect will be aggravated in the region $(f_s/6,\ f_s/3)$ by using the PI controller. Above the frequency $f_s/3$, the coefficient $k_{\rm ci}/\omega$ tends to be much smaller than k_c, and thus the term $\sin(1.5\omega T_s)$ has minor effect on reducing the negative damping in the region $(f_s/3,\ f_s/2)$ [19].

C. Single-Loop Voltage Control

The single-loop voltage control in the continuous s-domain can then be drawn in Fig. 4, where $G_p(s)$ and $Z_o(s)$ characterize the dynamics of the *LC*-filter plant, which are transfer functions from the inverter voltage and load current to the output voltage, respectively

$$G_p(s) = \left.\frac{V_o}{V_{\rm pwm}}\right|_{i_o=0} = \frac{\omega_r^2}{s^2+\omega_r^2}, \quad \omega_r = \frac{1}{\sqrt{LC}} \quad (6)$$

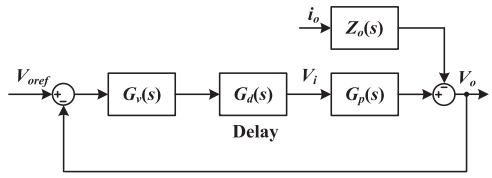

Fig. 4. Single-loop voltage control system in the continuous s-domain.

$$Z_o(s) = -\left.\frac{V_o}{i_o}\right|_{V_{\rm pwm}=0} = \frac{s}{C(s^2+\omega_r^2)} \quad (7)$$

where ω_r is the *LC*-filter resonance frequency.

From Fig. 4, the open-loop gain of the voltage loop can be derived as

$$T(s) = G_v(s)G_d(s)G_p(s). \quad (8)$$

Based on (8), the system stability with the P controller used for $G_v(s)$ is evaluated first in the following. Then, the stability of using the R controller only with $G_v(s)$, as reported in [11], is analyzed, and the stability region of the single-loop R voltage control scheme is identified.

1) P Controller: The phase and magnitude of $T(j\omega)$ with the P controller only, i.e., $G_v(s) = k_p$, can be given by

$$\angle T(j\omega) = \begin{cases} -1.5T_s\omega, & \omega < \omega_r \\ -\pi - 1.5T_s\omega, & \omega_r < \omega \end{cases} \quad (9)$$

$$|T(j\omega)| = \frac{k_p}{|1 - LC\omega^2|}. \quad (10)$$

For a stable voltage loop with the P controller, the following two conditions can be formulated based on the Nyquist stability criterion.

1) ω_r is above the phase crossover frequency ω_p for a positive PM. A critical value of ω_r, i.e., $\omega_c = \omega_s/3$, can thus be derived, which is illustrated by

$$-1.5T_s\omega_c = -\pi \Rightarrow \omega_c = \frac{\omega_s}{3}. \quad (11)$$

2) The magnitude of $T(j\omega)$ is below 0 dB at the phase crossover frequency for a positive gain margin (GM).

Fig. 5 plots the bode diagrams of $T(s)$ for $f_s = 5$ kHz with the different *LC*-filter resonance frequencies and k_p values. It can be seen that the system is stable (GM > 0, PM > 0) in the case of $C = 5\,\mu$F, $k_p = 0.1$, owing to $\omega_r > \omega_s/3$ and $|T(j\omega)| < 0$ dB at ω_p. However, a nontrivial steady-state error is inevitable at the fundamental frequency, and the increase of k_p will lead to a negative GM, as shown by the case of $C = 5\,\mu$F, $k_p = 1$. On the other hand, the decrease of ω_r below ω_c will result in a negative PM, which is shown in the case of $C = 10\,\mu$F.

2) R Controller: Next is to consider the R controller only for $G_v(s)$ [11], whose basic form is given by

$$G_v(s) = k_i R(s), \quad R(s) = \frac{s}{s^2+\omega_1^2} \quad (12)$$

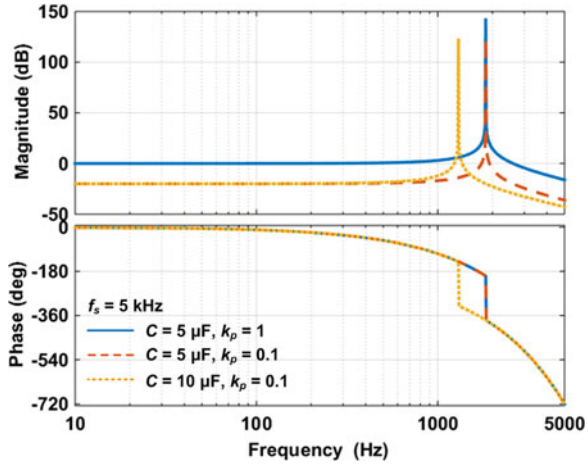

Fig. 5. Bode diagrams of $T(s)$ with the P controller at $f_s = 5$ kHz.

where $\omega_1 = 2\pi f_1$ is the output fundamental frequency. The phase and magnitude of $T(j\omega)$ in this case can be given by

$$\angle T(j\omega) = \begin{cases} \dfrac{\pi}{2} - 1.5T_s\omega, & \omega < \omega_1 \\ -\dfrac{\pi}{2} - 1.5T_s\omega, & \omega_1 < \omega < \omega_r \\ -\dfrac{3\pi}{2} - 1.5T_s\omega, & \omega_r < \omega \end{cases} \tag{13}$$

$$|T(j\omega)| = \left| \frac{k_i\omega}{\omega_1^2 - \omega^2} \cdot \frac{1}{1 - LC\omega^2} \right|. \tag{14}$$

From (13), it is noted that a phase lag of $\pi/2$ is added by the R controller above the fundamental frequency ω_1. Consequently, the critical frequency ω_c is reduced to $\omega_s/6$, which is illustrated by

$$-1.5T_s\omega_c - \frac{\pi}{2} = -\pi \Rightarrow \omega_c = \frac{\omega_s}{6}. \tag{15}$$

Also, the controller gain at the phase crossover frequency is changed as

$$\left| \frac{k_i\omega_p}{\omega_1^2 - \omega_p^2} \right| \approx \frac{k_i}{\omega_p}, \text{ if } \omega_p >> \omega_1 \tag{16}$$

which allows GM > 0 to be more readily obtained than using the P controller given in (10), provided that $\omega_p >> \omega_1$. However, when ω_1 approaches to ω_p, the choice of k_i will also be affected by ω_1, and the system tends to become unstable.

Fig. 6 shows the Bode diagrams of $T(s)$ with the $R(s)$ only for $G_v(s)$. Two cases with the different sampling and fundamental frequencies are plotted. In the case of $f_s = 5$ kHz in Fig. 6(a), the *LC*-filter resonance frequencies ω_r for both $C = 5\,\mu$F and $C = 10\,\mu$F are above $\omega_s/6$, and $|T(j\omega)|$ is below 0 dB except at the frequencies ω_1 and ω_r. The voltage loop can hence be designed with PM > 0 and GM > 0, and the phase lag of the R controller plays a critical role in stabilizing the system. In contrast, adding the P controller can only reduce the phase lag of the R controller and worsen the system stability. Fig. 6(b) shows the frequency responses at $f_s = 10$ kHz, where $\omega_r < \omega_s/6$ for

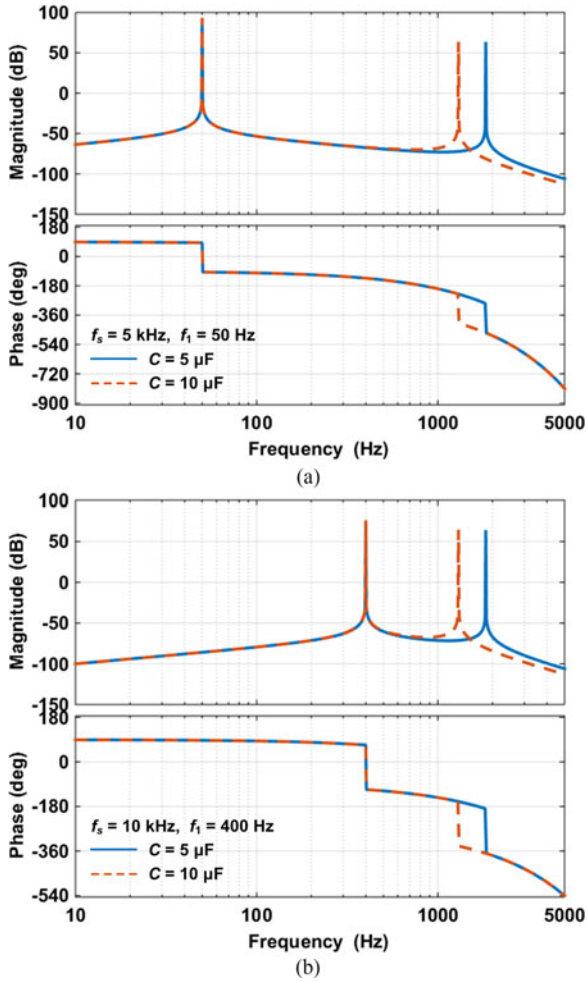

Fig. 6. Bode diagrams of $T(s)$ with the unity-gain-R controller, i.e., $R(s)$. (a) $f_s = 5$ kHz, $f_1 = 50$ Hz. (b) $f_s = 10$ kHz, $f_1 = 400$ Hz.

$C = 10\,\mu$F and the voltage loop cannot be designed as stable (PM < 0). This agrees with the critical frequency predicted by (15).

Besides the phase lag of the continuous form of the R controller, the discretized R controller may bring in additional time delay affecting the stability region of the voltage loop. Fig. 7 plots the frequency responses of the R controller discretized with three different methods, which are as follows:

1) the Tustin transformation with the prewarping at ω_1, i.e., $R_{t-p}(z)$;
2) the two-integrator-based scheme with the forward and backward Euler integrators, which is denoted by $R_{f-b}(z)$ [17];
3) the ZOH transformation, i.e., $R_{\text{zoh}}(z)$, which is used in [11].

Their specific discrete forms are, respectively, given as

$$R_{t-p}(z) = \frac{\sin(\omega_1 T_s)}{2\omega_1} \frac{1 - z^{-2}}{1 - 2z^{-1}\cos(\omega_1 T_s) + z^{-2}} \tag{17}$$

$$R_{f-b}(z) = \frac{T_s\left(z^{-1} - z^{-2}\right)}{1 + z^{-1}\left(\omega_1^2 T_s^2 - 2\right) + z^{-2}} \tag{18}$$

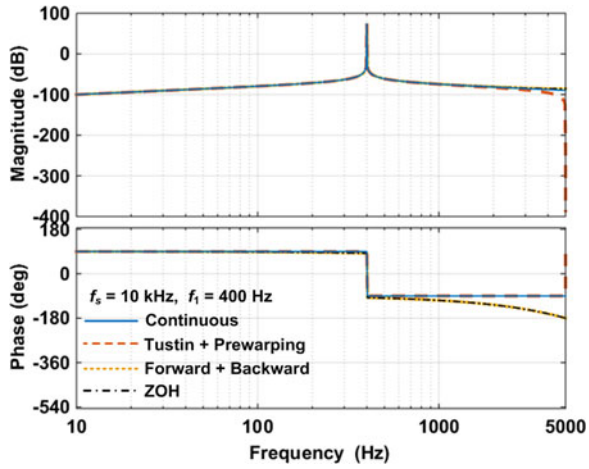

Fig. 7. Frequency responses of the $R(s)$ with different discretization methods.

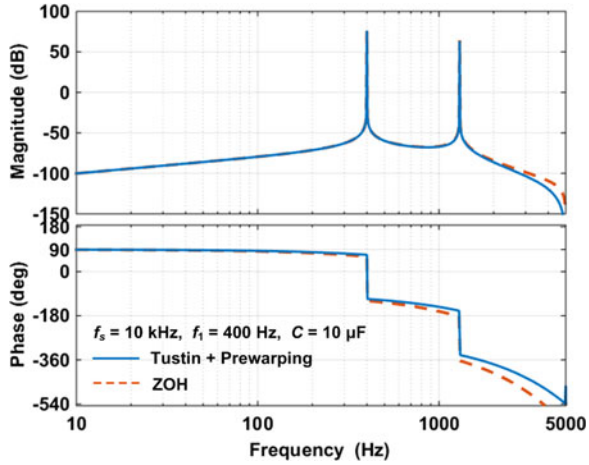

Fig. 8. Bode diagrams of $T(z)$ with two different discretized R controllers $R(z)$.

$$R_{\text{zoh}}(z) = \frac{\sin(\omega_1 T_s)}{\omega_1} \frac{z^{-1} - z^{-2}}{1 - 2z^{-1}\cos(\omega_1 T_s) + z^{-2}}. \quad (19)$$

It can be seen that the Tustin with prewarping has no additional phase lag introduced, whereas the latter two methods add an additional $0.5T_s$ delay, which consequently leads to a critical frequency $\omega_c = \omega_s/8$, corresponding to the $2T_s$ delay.

Fig. 8 shows the Bode diagrams of $T(z)$ for the R controller discretized with two different methods. $T(z)$ is derived from Fig. 2(a), which is given by

$$\begin{aligned} T(z) &= R(z)z^{-1}Z_{\text{zoh}}\left[G_p(s)\right] \\ &= R(z)z^{-1}\frac{(1+z^{-1})\left[1-\cos(\omega_r T_s)\right]}{1-2z^{-1}\cos(\omega_r T_s)+z^{-2}} \end{aligned} \quad (20)$$

where the ZOH transformation is applied to $G_p(s)$ at $f_s = 10$ kHz, $R_{t-p}(z)$ and $R_{f-b}(z)$ are considered for the R controller $R(z)$. It is seen that the unstable case in Fig. 6(b) is stabilized when the R controller is discretized with the two-integrator-based method. This explains why the voltage loop is stable in [11] even though ω_r is below $\omega_s/6$ therein.

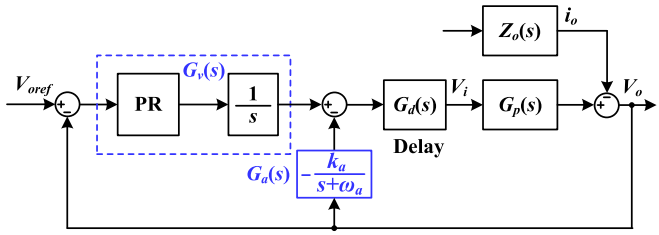

Fig. 9. Block diagram of the proposed single-loop voltage control scheme.

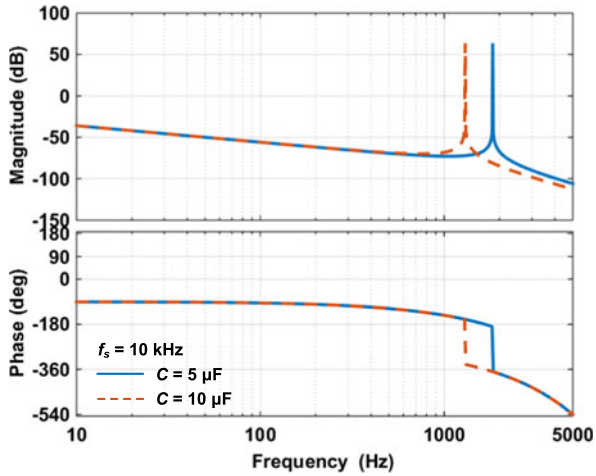

Fig. 10. Bode diagrams of $T(s)$ with the unity-gain I controller, i.e., $1/s$.

III. Proposed Control Approach

In this section, a single-loop voltage control approach with the widened stability region is proposed, and a holistic design of controller parameters based on the z-domain root contours is presented.

A. Operation Principle

Fig. 9 illustrates the block diagram of the proposed control scheme, which is composed by the voltage controller $G_v(s)$ for the output voltage regulation and a damping controller $G_a(s)$ for active stabilization when the filter resonance frequency ω_r is below the critical frequency $\omega_s/6$. For the voltage controller $G_v(s)$, instead of using the R controller, the basic I controller is inserted in the forward path for obtaining the phase lag of $\pi/2$. The conventional PR controller can then be adopted, where the R controller gain is merely designed for zero steady-state error, yet with little phase effect at the phase crossover frequency ω_p, which is given by [18], [19]

$$\frac{k_{\text{ci}}}{\omega_p} \approx \frac{k_p}{20} \quad (21)$$

where k_{ci} is the gain of the R controller used with the proposed scheme. In contrast, the P controller is designed for the system stability, whose value is not affected by ω_1 as that using the R controller only in (12).

Fig. 10 shows the Bode diagrams for $T(s)$ with the basic I controller ($1/s$) only at $f_s = 10$ kHz. The same stability

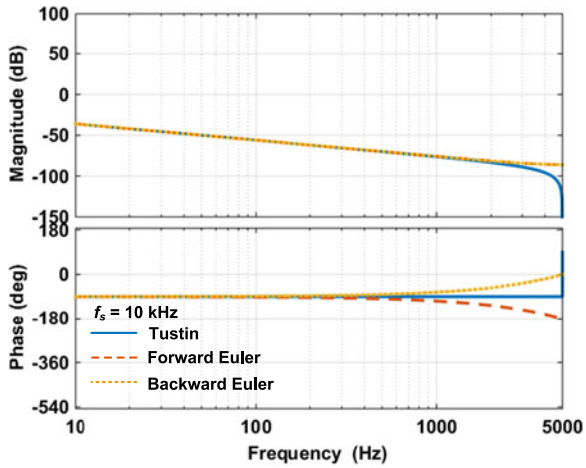

Fig. 11. Frequency responses of the different discretized I controllers.

characteristics as that using the R controller in Fig. 6(b) can be observed. However, it is noted that the phase response in Fig. 9 starts from $-\pi/2$, rather than $\pi/2$ as shown in Fig. 6(b). This implies the phase compensation is needed for the R controller and particularly when the fundamental frequency is increased. The R controller with the phase compensation is given by

$$R_c(s) = \frac{s\cos(\theta_c) - \omega_1 \sin(\theta_c)}{s^2 + \omega_1^2} \tag{22}$$

where θ_c is the phase lead, which can be derived as [17]

$$\theta_c = \frac{\pi}{2} + 1.5\omega_1 T_s. \tag{23}$$

Fig. 11 plots the Bode diagrams of the discretized I controller with different methods. Similar to Fig. 7, the Tustin method has no additional phase lag, which leads to $\omega_c = \omega_s/6$. Yet, the forward Euler adds $0.5T_s$ delay, which shifts ω_c to $\omega_s/8$ ($2T_s$ delay), yet the backward Euler reduces $0.5T_s$ delay, and thus ω_c is increased to $\omega_s/4$ (T_s delay).

To further widen the stability region, a damping controller $G_a(s)$ (see Fig. 9) is equipped with the voltage feedback loop, which is based on a negated first-order low-pass filter, as given in the following:

$$G_a(s) = \frac{-k_a}{s + \omega_a}. \tag{24}$$

The closed-loop response of the voltage loop including $G_v(s)$ and $G_a(s)$ can then be derived as

$$V_o = \frac{G_v(s)G_d(s)G_p(s)}{1 + [G_v(s) + G_a(s)]\, G_d(s)G_p(s)} V_{\text{oref}} - \frac{Z_o(s)}{1 + [G_v(s) + G_a(s)]\, G_d(s)G_p(s)} i_o \tag{25}$$

where the open-loop gain with $G_a(s)$ is changed as

$$T_a(s) = [G_v(s) + G_a(s)]\, G_d(s)G_p(s). \tag{26}$$

As $G_v(s)$ can be simplified to k_p/s for the stability analysis, $T_a(s)$ can be equivalent as (27) showing that $G_a(s)$ and $G_v(s)$ essentially synthesize a lead-lag filter in cascade with the I controller

$$T_a(s) = \left[\frac{k_p}{s} - \frac{k_a}{s + \omega_a}\right] G_d(s)G_p(s) = \frac{(k_p - k_a)s + k_p\omega_a}{s + \omega_a} \frac{1}{s} G_d(s)G_p(s). \tag{27}$$

It is worth noting that $G_a(s)$ can also be used with the single-loop R control, where the R controller in (12) is approximated as k_i/s, which, together with the damping controller $G_a(s)$, also forms a lead-lag filter together.

To see the stabilization effect of $G_a(s)$, the phase of the lead-lag filter can be derived as

$$\angle\left\{(k_p - k_a)\frac{j\omega + \frac{\omega_a}{1 - k_a/k_p}}{j\omega + \omega_a}\right\} = \begin{cases} [-\frac{\pi}{2},\ 0], & k_a < k_p \\ [-\frac{\pi}{2},\ 0], & k_a = k_p \\ [-\pi,\ 0], & k_a > k_p \end{cases} \tag{28}$$

It is seen that this lead-lag filter adds an additional phase lag and therefore widens the stability region of the voltage loop. The case of $k_a > k_p$ leads to a wider range of phase lag than the other cases, yet it also adds a right half-plane zero into the open-loop gain, leading to the nonminimum phase response of the system.

B. Codesign of Active Damping and Voltage Controller

From (24) to (27), it is noted that three controller parameters mainly affect the system stability: k_a, ω_a, and k_p. A codesign procedure for these parameters is thus formulated below based on the root contours in the discrete z-domain. For discretization, the Tustin transformation is applied to $G_a(s)$ and the I controller, which are given by

$$G_a(z) = -\frac{k_a}{\frac{2}{T_s}\frac{1 - z^{-1}}{1 + z^{-1}} + \omega_a}, \quad \frac{1}{s} = \frac{T_s}{2}\frac{1 + z^{-1}}{1 - z^{-1}} \tag{29}$$

such that no additional time delay is added by the discretized I controller. The discretized form of the open-loop gain with the damping controller $G_a(z)$ can then be expressed as

$$T_a(z) = \left[\frac{k_p T_s(1 + z^{-1})}{2(1 - z^{-1})} - \frac{k_a T_s(1 + z^{-1})}{2(1 - z^{-1}) + \omega_a T_s(1 + z^{-1})}\right] \cdot z^{-1} \cdot \frac{(1 + z^{-1})\,[1 - \cos(\omega_r T_s)]}{1 - 2z^{-1}\cos(\omega_r T_s) + z^{-2}}. \tag{30}$$

The sampling frequency f_s is 10 kHz, since in this case $C = 10\,\mu$F leads to $\omega_r < \omega_s/6$, which necessitates the use of $G_a(s)$.

The overall objective of the codesign is to shift the root loci to equate the natural frequencies of the conjugate pole pairs [9], [20].

1) The root locus of $T(z)$ without $G_a(z)$ is plotted first to see the effect of varying k_p on the closed-loop poles of the system.
2) A few typical k_p values are then chosen based on step 1), and the root contours of $T_a(z)$ with the changes of k_a and ω_a are plotted. Each root locus depicts the movement of

closed-loop poles with the increase of k_a for a given k_p. A sweep of ω_a from $0.1\omega_s$ to $0.5\omega_s$ at the step of $0.1\omega_s$ is performed to identify the range of controller parameters.

3) Finally, the parameters are chosen by sweeping ω_a at a smaller step and slightly tuning the k_p value.

For illustration, Fig. 12 plots the root contours for the case of $C = 10\ \mu$F. First, the root locus for $T(z)$ (dashed line) is plotted, which clearly shows that the system is unstable without $G_a(z)$. This agrees with the stability region predicted in Fig. 10. Then, three values of k_p are chosen for plotting the root contours (solid lines) with a sweep of ω_a. Each root locus (solid line) indicates the movement of poles along with the increase of k_a. It can be seen that two conjugate pole pairs will appear if the controller parameters are not properly chosen. Their natural frequencies affect the system response [9]. Moreover, simply increasing the cutoff frequency ω_a can hardly equate the conjugate pole pairs. Hence, the tuning of k_p is needed. By taking a closer look at Fig. 12(c), it can be found that the possible range of ω_a is $0.2\omega_s < \omega_a < 0.3\omega_s$. With a sweep at a smaller step, $0.02\omega_s$ for example, the controller parameters for the single conjugate pole pair can be found, which is shown in Fig. 13.

Fig. 14 then shows the frequency response of the open-loop gain of the proposed control scheme, $T_{\rm ad}(z)$, which is based on the controller parameters identified in Fig. 13. It is seen that the phase crossover frequency is reduced to 780 Hz, which implies that the control loop is kept stable, since the *LC*-filter resonance frequency is above that frequency. A positive GM (3.12 dB) at the phase crossover frequency can also be observed. The R controller gain $k_{\rm ci}$ can be identified according to (19). Table II summarizes the codesigned controller parameters.

IV. Simulation and Experimental Results

For validating theoretical analysis, time-domain simulations using the MATLAB/Simulink and PLECS Blockset are carried out, and the experimental tests for a 400-Hz three-phase, three-wire VSI system with the 10 kHz sampling frequency are also performed. The main circuit and controller parameters provided in Tables I and II are used in simulations and experiments. All voltage waveforms shown below are line-to-line voltages and current waveforms are phase currents. *LC*-filter parameters, $C = 10\,\mu$F, $L = 1.5$ mH, result in $\omega_s/8 < \omega_r < \omega_s/6$, which enables to see the effects of the discretization methods used with the R controller in the single-loop R voltage control scheme.

A. Simulation Results

First, the single-loop R voltage control scheme is evaluated at the zero-load condition, which is the worst case with no damping provided by the load. The simulated capacitor-voltage waveform is shown in Fig. 15, where the discretization method applied to the R controller is changed, from the two-integrator-based method to the Tustin transformation with prewarping, at the time instant of 0.4 s. It is clear that the system is destabilized after 0.4 s, which confirms the stabilizing effect of the additional time delay ($0.5T_s$) with the two-integrator-based discretization method. In this case, the R controller gain (see Table II) is

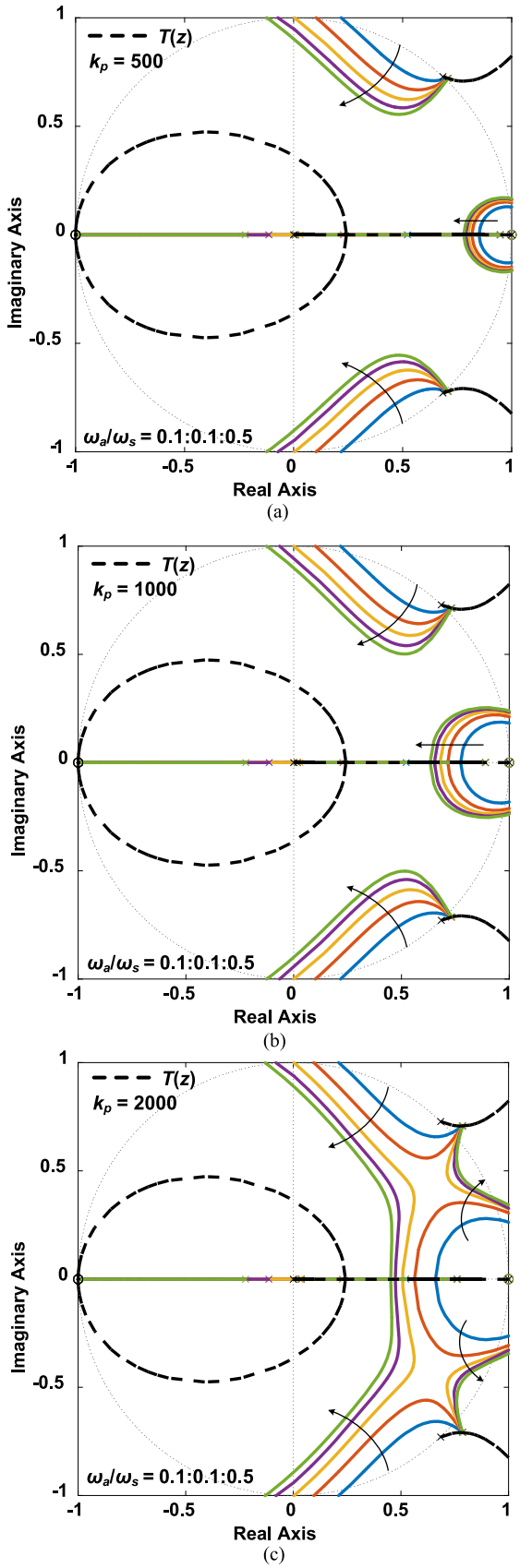

Fig. 12. Root contours for designing the proposed controller parameters with $C = 10\ \mu$F and $f_s = 10$ kHz. (a) $k_p = 500$. (b) $k_p = 1000$. (c) $k_p = 2000$.

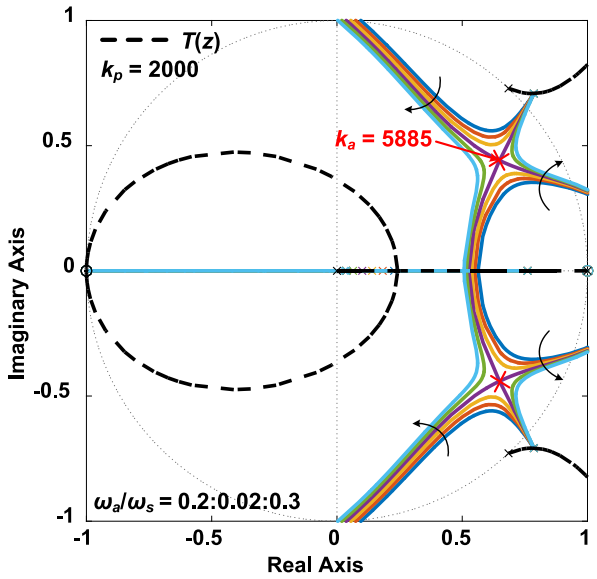

Fig. 13. Root contours for identifying the proposed controller parameters ($k_p = 2000$, $k_a = 5885$, $\omega_a = 0.26\omega_s$) with $C = 10\ \mu$F and $f_s = 10$ kHz.

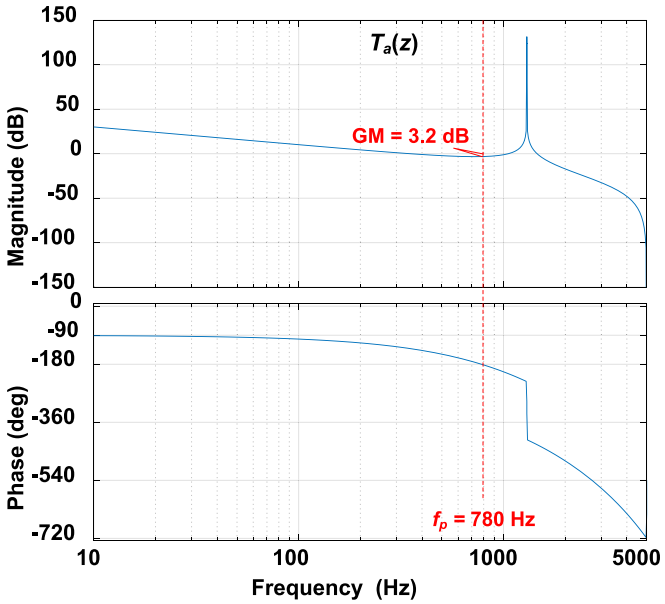

Fig. 14. Frequency response of the open-loop gain $T_a(z)$ with the controller parameters identified in Fig. 13.

TABLE II
CONTROLLER PARAMETERS

Symbol	Controller parameter	Value
k_i	Gain for using the *R* controller only	200
k_p	P controller gain of PR-I controller	2000
k_{ic}	*R* controller gain of PR-I controller	490 000
k_a	Gain of damping controller $G_a(s)$	5885
ω_a	Cutoff frequency of controller $G_a(s)$	$0.26\omega_s$

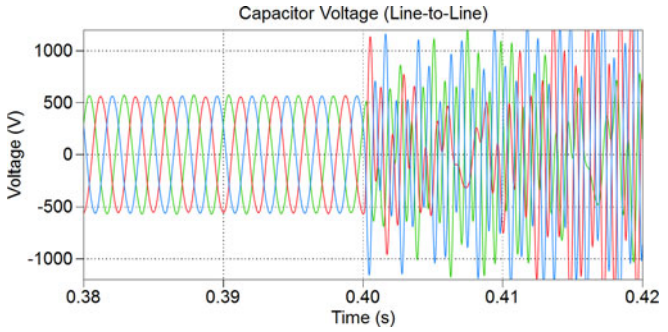

Fig. 15. Simulated ac capacitor (line-to-line) voltage for the single-loop R control scheme at the zero-load condition, where the discretization method for the R controller is changed from the two-integrator-based scheme to the Tustin transform with prewarping at the time instant of 0.4 s.

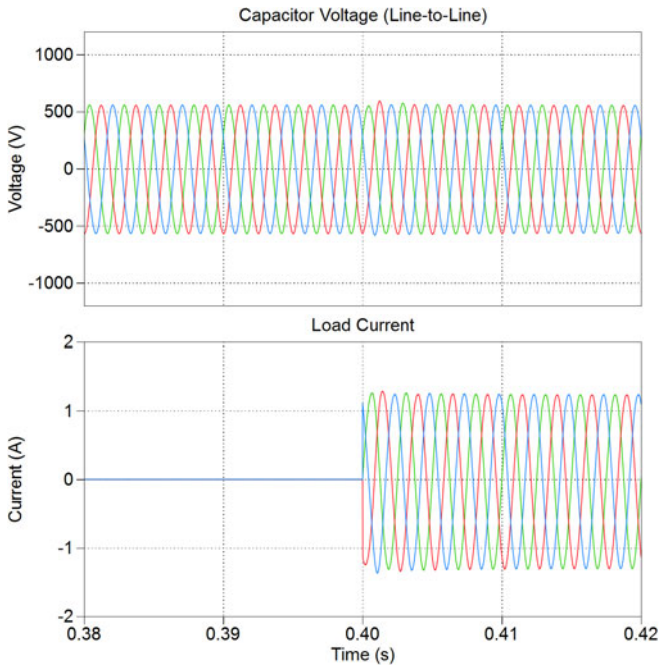

Fig. 16. Simulated ac capacitor (line-to-line) voltage and load current for the proposed control scheme, where a step response of a resistive load (254 Ω) is tested at the time instant of 0.4 s.

designed based on the frequency response of $T(z)$ shown in Fig. 8. No phase compensation as in the case of the R controller in (22) is needed.

Fig. 16 then shows the simulated capacitor voltage and load current with the proposed control scheme. Both the I controller of $G_v(s)$ and $G_a(s)$ are discretized by the Tustin transformation, which implies that no additional time delay ($0.5T_s$) is added into the system. The R controller of $G_v(s)$, which is given by (22), is discretized with the Tustin transformation with prewarping at the fundamental frequency. The controller parameters, which are codesigned based on Figs. 12 and 13, are evaluated with a step change of a resistive load (254 Ω). A stable operation with a good dynamic response is observed. The stable operation under the zero-load condition also confirms that the proposed control scheme exhibits a widened stability region even without adding additional time delay by the discretization of the I controller.

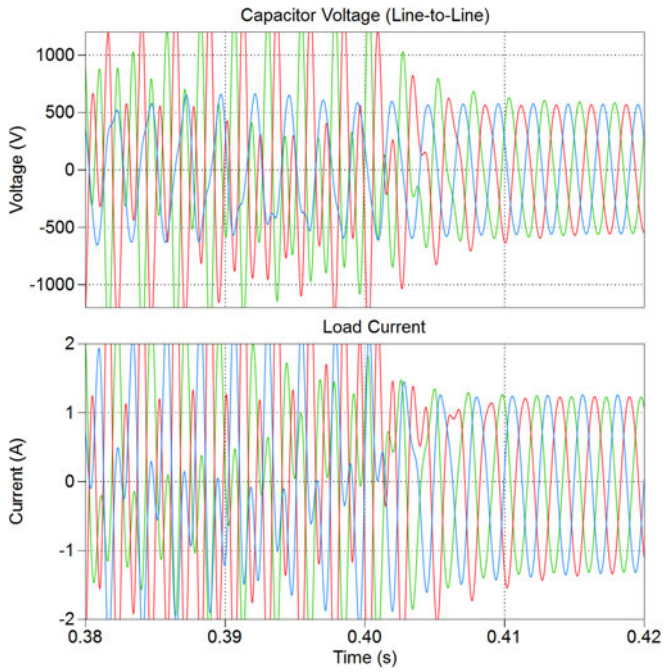

Fig. 17. Simulated ac capacitor (line-to-line) voltage and the R-load current for the proposed control scheme with the parallel R//C load, where the P controller gain is reduced from 2000 to 1500 at the time instant of 0.4 s.

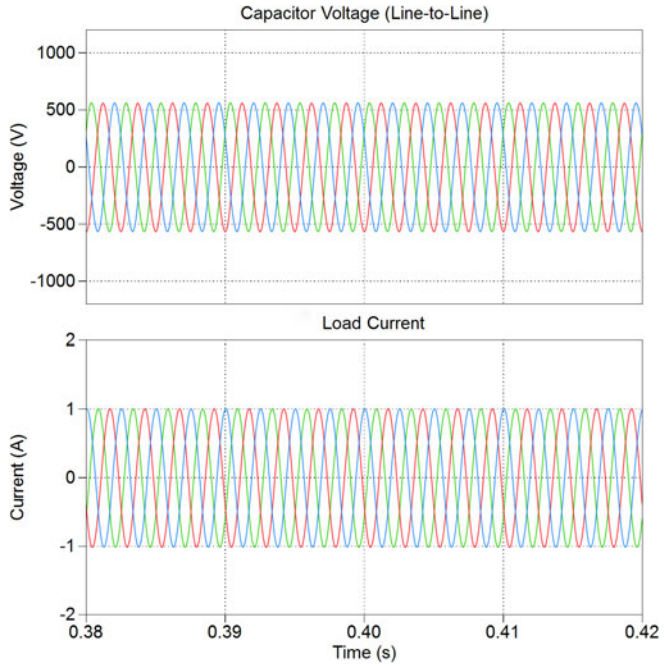

Fig. 18. Simulated ac capacitor (line-to-line) voltage and the R-load current for the proposed control scheme with the series R-L load.

Subsequently, Fig. 17 shows the simulation results for the proposed control scheme with a parallel R//C load. Since the switching current ripples flow through the load capacitance, only the current flowing through the resistance is provided. In this case, the P controller gain of $G_v(z)$ is reduced from 2000 to 1500 at the time instant of 0.4 s. It is clear that the presence of load capacitance destabilizes the control system, and a reduced P controller gain is needed to preserve stability. This is due to the fact that the load capacitance shifts the resonance frequency to a lower value, which tends to cause a negative GM of the open-loop gain. In contrast, the series R-L load is tested in Fig. 18, where a stable response can be observed.

Fig. 19 further shows the simulation results considering the *LC*-filter parameter variations, where the zero-load condition is simulated. The filter capacitance is reduced to 9 μF for three phases, whereas the filter inductances of the phases A and C are increased to 1.8 mH and of the phase B is increased to 2.3 mH. The stable response of the capacitor voltage demonstrates the effectiveness of the proposed control scheme even under the variations of system parameters.

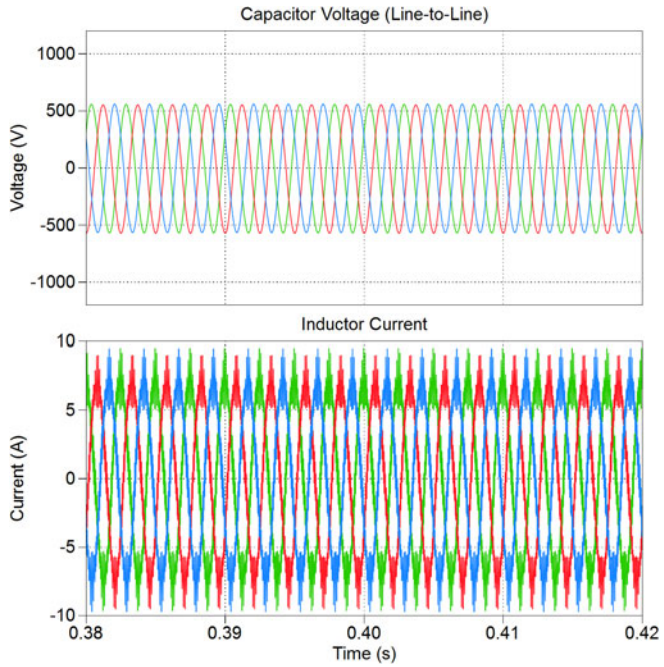

Fig. 19. Simulated ac capacitor (line-to-line) voltage and the filter inductor current for the proposed control scheme under the variation of the *LC*-filter parameters.

B. Experimental Results

In the experiments, the single-loop voltage control schemes are implemented in the DS1007 dSPACE system, which integrates the DS2004 high-speed (800 ns) 16-b A/D sampling board and the DS5101 digital waveform output board for the generation of switching pulses. The single-update mode of the PWM generation is adopted, which causes one sampling period of computational delay plus half sampling period delay of the digital PWM. A constant-voltage (730 V) dc power supply is used to power the dc-link of the VSI. Due to the limited number of (four) channels of the oscilloscope, two line-to-line voltages ($V_{\rm AB}$ and $V_{\rm BC}$) and two phase currents ($i_{\rm A}$ and $i_{\rm B}$) are shown in the measured results.

To verify the simulation case studies, Fig. 20 shows the measured ac voltage waveform with the single-loop R control scheme at the zero-load condition. The discretization for the R

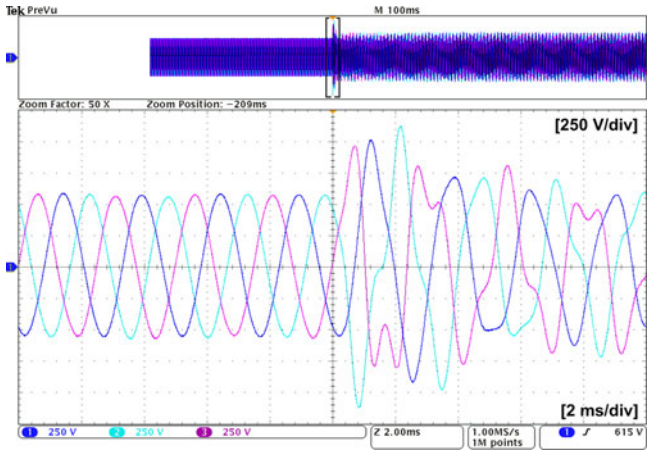

Fig. 20. Measured ac capacitor (line-to-line) voltage for the single-loop R control scheme at the zero-load condition, where the discretization of R controller is changed from the two-integrator-based method to Tustin with prewarping method.

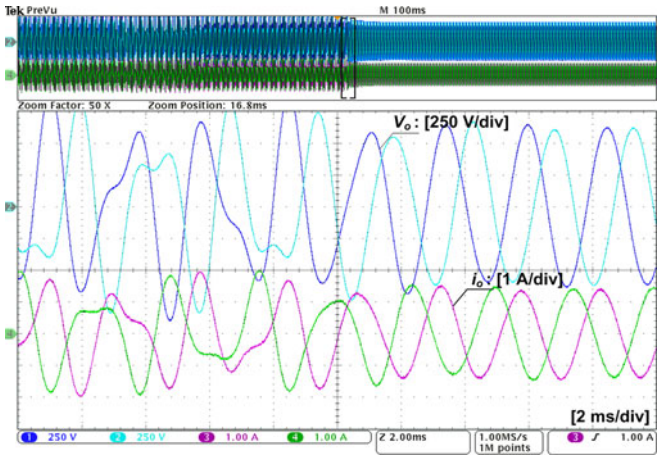

Fig. 22. Measured ac capacitor (line-to-line) voltage and the R-load current for the proposed control scheme with the parallel R//C load, where the P controller gain k_p is reduced from 2000 to 1500 for system stabilization.

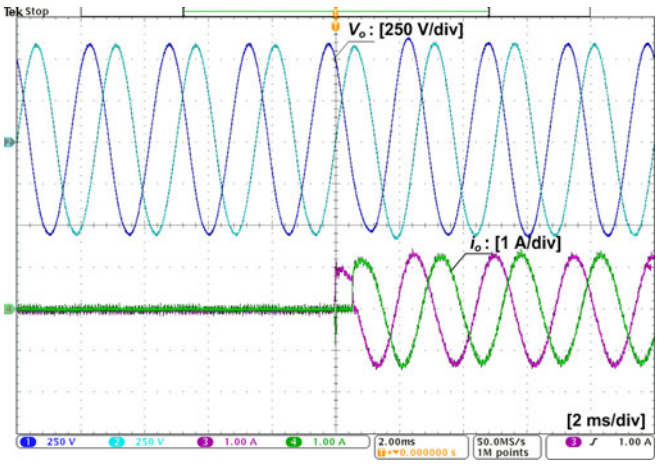

Fig. 21. Measured ac capacitor (line-to-line) voltage and load current for the proposed control scheme with a step response of a resistive load (254 Ω).

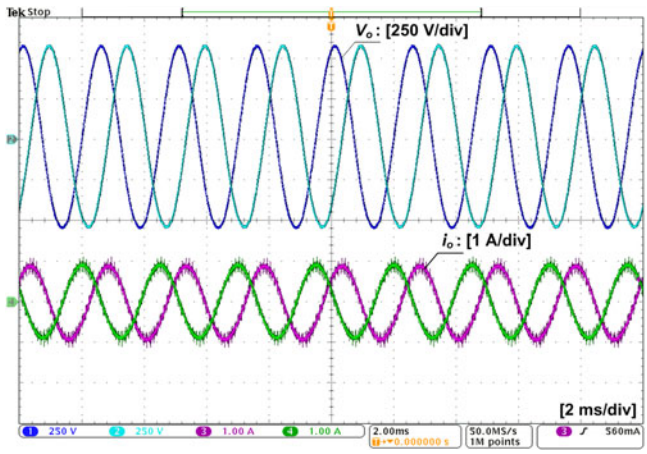

Fig. 23. Measured ac capacitor (line-to-line) voltage and load current for the proposed control scheme with the series R-L load.

controller is changed from the two-integrator-based method to the Tustin transformation with prewarping at the fundamental frequency. The unstable response matches with the simulation result in Fig. 15. Fig. 21 then shows the measured voltages and currents for the proposed control scheme with a step change of a resistive load (254 Ω). It agrees with the simulation study in Fig. 16 and further confirms the stabilizing performance of the control approach.

Fig. 22 provides the measured results for the proposed control scheme with a paralleled R//C load. The current flowing through the R load is shown. Similar to the simulation result shown in Fig. 17, the system is destabilized by the capacitive load, and it subsequently turns into stable operation when the P controller is reduced to $k_p = 1500$.

Fig. 23 shows the measured voltage and current waveforms with the series R-L load, where a stable response is observed. The measured results under the same variations of the *LC*-filter parameters as the simulation study are given in Fig. 24. A close

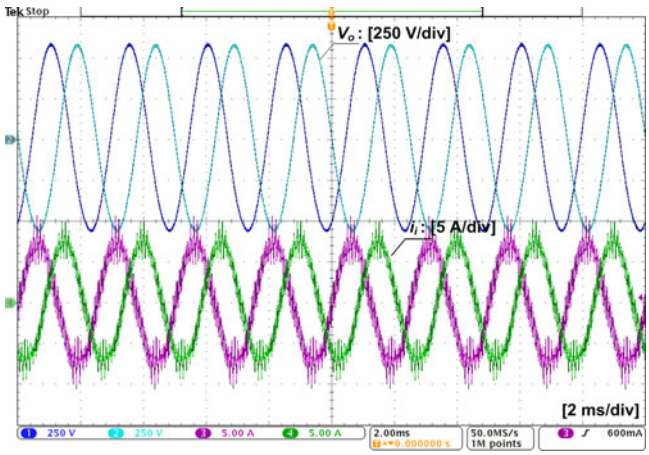

Fig. 24. Measured ac capacitor (line-to-line) voltage and the filter inductor current for the proposed control scheme under the variation of filter parameters ($C = 9$ μF).

correlation with the simulation results shown in Figs. 18 and 19 can be observed in both cases. Hence, the test results verify the effectiveness of the proposed control approach.

V. Conclusion

This paper discussed the stability of digital single-loop voltage control schemes for *LC*-filtered VSIs. The influences of the discretized R or I controllers on the system stability have been systematically identified with frequency-domain analysis, time-domain simulations, and experimental tests. It has been shown that the phase lag of the R or I controller can stabilize the control loop with a second-order *LC*-filter plant. A voltage feedback damping scheme has also been discussed with the root contours analysis in the discrete z-domain, and its stabilizing performance has been verified in simulations and experiments.

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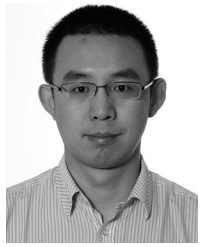

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