Analysis and Design of a Modular Multilevel Converter With Trapezoidal Modulation for Medium and High Voltage DC-DC Transformers

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***Abstract*—Conventional dual-active bridge topologies provide galvanic isolation and soft-switching over a reasonable operating range without dedicated resonant circuits. However, scaling the two-level dual-active bridge to higher dc voltage levels is impeded by several challenges among which the high *dv/dt* stress on the coupling transformer insulation. Gating and thermal characteristics of series switch arrays add to the limitations. To avoid the use of standard bulky modular multilevel bridges, this paper analyzes an alternative modulation technique, where staircase approximated trapezoidal voltage waveforms are produced; thus, alleviating developed *dv/dt* stresses. Modular design is realized by the utilization of half-bridge chopper cells. This way the analyzed dc-dc transformer employs modular multilevel converters operated in a new mode with minimal common-mode arm currents, as well as reduced capacitor size, hence reduced cell footprint. Suitable switching patterns are developed and various design and operation aspects are studied. Soft-switching characteristics will be shown to be comparable to those of the two-level dual-active bridge. Experimental results from a scaled test rig validate the presented concept.**

***Index Terms*—DC fault, dc/dc power conversion, dc transformer, dual-active bridge, modular multilevel converter (MMC).**

NOMENCLATURE

T_t	Voltage transit time between the two dc rails.
N	Number of cells per arm (or series IGBTs per valve).
N_s	Number of ac voltage steps.
T_d	Dwell time spent in each voltage level.
V_{dc}	DC-link voltage.
m	Modulation index.
f_s, ω_s	Fundamental frequency ($f_s = 1/T_s$).
$t_{d(\mathrm{off})}$	IGBT turn-off delay time.
t_f	IGBT fall time.
$t_{d(\mathrm{on})}$	IGBT turn-on delay time.
t_r	IGBT rise time.
t_{DB}	Dead time (underlap time) between two IGBTs.
Z^*	Set of nonnegative integers.
Z^+	Set of positive integers.

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I. INTRODUCTION

DC grids of various topologies, structures, and voltage levels are drawing increasing attention, a tendency driven by the rapidly advancing power electronics technology and the unprecedented growth of global energy demand. Migration from ac to dc systems is further promoted by the steadily rising dependence on renewable distributed generation, the economic challenges of long-distance bulk power transmission, and the nature of available energy storage technology. As high-voltage dc (HVDC) proves economical for, for instance, transporting large-scale wind power generated offshore, utilization of dc collector grids may spare the extra conversion stages needed when wind plants use ac collection networks. Moreover, most of energy storage devices considered for industrial, transportation, and power system applications are typically interfaced either by dc connections or through a dc conversion stage [2].

In power systems, the evolution of dc grids awaits a technical leap in dc protection and an efficient means of dc voltage level transformation [3]. For a high-power dc–dc converter to compete with the high efficiency standards set by ac power transformers, hard switching is not a viable option. Soft-switching, on the other hand, has long been investigated and can be achieved by, for instance, resonant converters [4]–[8]. However, significant challenges impede the scaling of most resonant designs to the high-power high-voltage range. That is, resonant stages experience high internal voltage stresses and, hence, require a special insulation design. Additionally, in practice inductance and capacitance values drift owing to aging and operating conditions. In transformerless resonant designs, lack of galvanic isolation may be an additional drawback [9], [10].

Dual active bridge (DAB) dc–dc converters, first proposed in [11] for an industrial application, classically employ two H-bridges or three-phase bridges connected via an ac transformer, in what can be termed a front-to-front connection [12]–[18]. Bidirectional power flow is possible and is controlled by the voltage across the transformer leakage inductance [13]. Typically, power flow direction and magnitude are dictated by the phase shift angle between the bridges, as well as their individual voltage output magnitudes [18]. Utilizing an ac transformer

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stage offers the galvanic isolation necessary for servicing, reliability, and grounding. Zero-voltage switching of both bridges is assured within a certain operating range, subject to the internal structure of each bridge [15]. DAB converters have been considered for solid-state ac transformers, which are expected to play a key role in a wide spectrum of applications including dc distribution [3].

On the downside, traditional DAB converters typically operate at a high-switching frequency in order to reduce ac transformer volume. This is not viable for higher power and voltage levels due to thermal and gating limitations of high-voltage power electronic device arrays. Furthermore, the impact of ac transformer parasitic components is more pronounced with higher voltage, rendering transformer design a challenging task. Therefore, potential high-power DAB converter designs must employ reasonably low-switching frequencies [19]. Another problem is *dv/dt* stress [20]. In a two-level mode, a high-voltage DAB converter will produce a potentially destructive *dv/dt* upon transformer insulation. This stress results in insulation degradation and eventually breakdown, and must be relieved to allow for voltage scalability.

One of the DAB prototypes developed for a 1-MW solid-state ac transformer was reported in [19]. The 12-kV/1200-V DAB employs a modular design in which six 2-kV/400-V DAB converter modules were series connected at the 12 kV side and series-parallel connected at the 1200 V side. A diode clamped topology was proposed for each 2-kV bridge. Though promising, it is not clear how challenges facing higher voltage/power versions of such a topology are to be addressed, with regard to the optimum choice of voltage ratings, number of modules, switching frequency, complexity of connections, number of components, and capacitor balancing issues [21].

Front-to-front connections of modular multilevel converters (MMC) or the so called alternate arm converters have been analyzed in [22] in attempt to build an efficient, low *dv/dt*, and relatively compact modular dc–dc converter. A similar connection is presented in [23], where each MMC contributes to the voltage stepping in addition to the ac transformer stage. Each MMC operates under either sinusoidal or two-level modulation, forming what can be termed an "electronic dc tap changer." Bipolar MMC cells are employed in the lower voltage-side MMC to boost the voltage. When the voltage gain of the lower voltage-side converter is higher than unity, each cell must be rated at the lower voltage dc-link voltage. It is therefore suited for medium and low-voltage applications.

Direct-connected high-power dc–dc converters have been reported in [24], [25]. They lack galvanic isolation which may limit their application scope.

An improved design of conventional two-level bridge converters has been proposed in [26] and [27] for HVDC applications. The voltage square wave slopes are reduced by introducing intermediary voltage steps, such that the bridge output voltage resembles a trapezoidal waveform. A capacitor in series with an IGBT/antiparallel diode pair shunts every IGBT in all arms of the conventional two-level converter. The added shunt components act as active soft-voltage clamps, as well as energy tanks for brief periods. Structure wise, the converter enjoys the same half-bridge cell-based modular structure as a conventional MMC, facilitating manufacturing, installation, and maintenance. The size of passive components, as well as conduction losses are lower than a typical MMC of same voltage and power ratings [26]. This paper extends the analysis presented in [26] for generic medium-/high-voltage DAB applications, focusing on bridge operation aspects. It will be shown that the operation of the considered converter is distinct from a conventional MMC.

The analyzed converter is denoted as a "quasi two-level converter (Q2LC)" for expedience. Switching patterns, harmonic content, and voltage modulation techniques of the Q2LC are discussed. Cell capacitance is quantified and the use of the Q2LC as the building block in a high-power high-voltage DAB dc–dc converter is analyzed. An insight on soft-switching capabilities is presented, and finally, experimental validation of the concept is provided.

In addition to serving as a high voltage dc-dc transformer, the proposed concept is expected to help extend the application of solid-state ac transformers to the medium and upper medium voltage ranges.

II. Structure and Operating Principle of the Q2LC

The single-leg Q2LC structure is outlined in Fig. 1(a). The bold lines represent the main power paths, traditionally, a series array of IGBTs in each bridge arm. A simple auxiliary circuit of a capacitor and an IGBT/diode pair is connected across each main path IGBT/diode pair. The added circuit provides an auxiliary path for power flow. Every time ac pole voltage polarity is reversed, an appropriate switching pattern permits the auxiliary circuit of each main IGBT to act as an energy buffer, where the load current flows through the capacitor, whose voltage acts upon the load. Simultaneously, the auxiliary circuit acts as a switched soft voltage clamp, resulting in equal dynamic and static voltage sharing between all the main IGBTs of an arm. The insertion of auxiliary shunting capacitors allows for sequential switching of the main IGBTs in each arm in brief time steps $T_{\rm d}$ (order of microseconds) summing to a total transition time T_t, where

$$T_t = (N-1)T_d. \tag{1}$$

T_d is the dwell time spent at each intermediary voltage level during ac pole level transitions. Being a few microseconds, choice of the dwell time must account for the turn-on and turn-off times of the IGBT modules and ensure an acceptable level of *dv/dt* stress. On the other hand, a large T_t implies higher energy buffering requirements; hence, relatively larger auxiliary capacitances.

The net result is a staircase approximation of a trapezoidal load voltage waveform, as shown in Fig. 1(c). The magnitude of each voltage step is determined by the voltage of a single-auxiliary capacitor. For equal steps, all the auxiliary capacitor voltages must remain near equal. Since each arm of a two-level converter must block the dc-link voltage, the required voltage level of each auxiliary capacitor is ideally $V_{\rm dc}/N$. The Q2LC

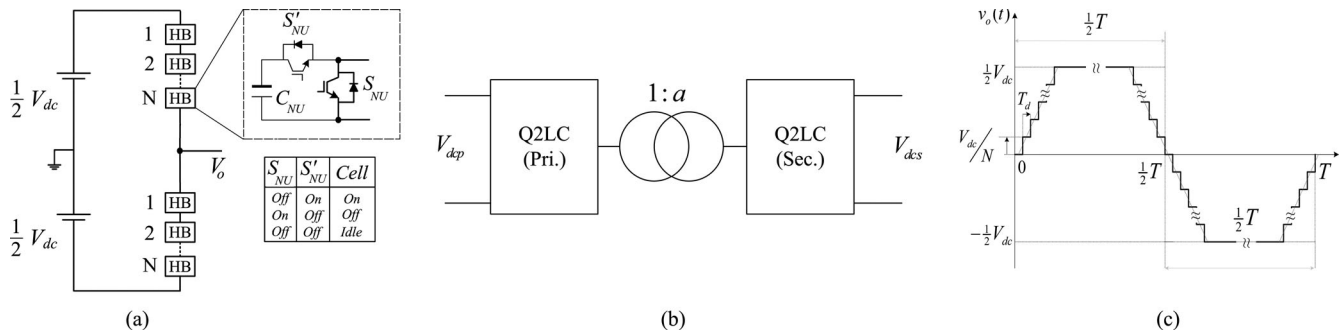

Fig. 1. (a) Single-leg Q2LC, (b) Generic structure of a Q2LC-based DAB, and (c) the output voltage waveform of the single-leg Q2LC.

controllers must ensure balanced capacitor voltages within an acceptable band around this set point.

A two-level converter where the main IGBTs are shunted by the said auxiliary circuits evolves to an MMC structure [26]–[37], where the trapezoidal modulation technique allows for reduced passive component values. Typical half-bridge chopper cell design can be utilized, with all the advantages of a modular structure.

With stepped voltage transitions introduced between $-1/2V_{\rm dc}$ and $1/2V_{\rm dc}$, the steady-state voltage seen by each arm in Fig. 1(a) is

$$v_X = V_{\rm dc}(1 - N_{Y\,\rm on}/N) \tag{2}$$

where subscripts $X \in \{U, L\}$ and $Y = \bar{X}$. Symbols U and L refer to the upper and lower arms, respectively. In (2), $N_{Y\,\rm on}$ is the number of inserted auxiliary capacitors in the complementary arm. The ac pole is tied to one of the dc rails when $N_{Y\,\rm on} \in \{0, N\}$. Stepped voltage transitions occur when $1 \leq N_{Y\,\rm on} < N$, in a staircase approximation of a trapezoid. Since the voltage across both arms of a pole at any instant equals the dc-link voltage, maintaining the capacitors voltages around the $V_{\rm dc}/N$ set point requires that the total number of inserted auxiliary capacitors in both arms at any instant satisfies (3), entailing a complementary switching (CS) patterns of both arms of the same phase leg [29],[30]

$$N_{U\,\rm on} + N_{L\,\rm on} = N. \tag{3}$$

However, the Q2LC operating mode permits the use of a third switching state—denoted idle state—where both the main and auxiliary IGBTs are in an off-state [see Fig. 1(a)]. Possible switching patterns employing this switching state, as will be shown in Section II-A, are able to achieve proper operation with $N_{U\,\rm on} + N_{L\,\rm on} < N$. The single-leg Q2LC output voltage expression is given in (4). Equation (4) holds for all switching patterns. Nonetheless, when the idle state is employed, the arm having idle cells is to be avoided while applying (4).

$$v_o(t) = V_{\rm dc}\left(\frac{1}{2} - \frac{N_{U\,\rm on}(t)}{N}\right) = V_{\rm dc}\left(\frac{N_{L\,\rm on}(t)}{N} - \frac{1}{2}\right). \tag{4}$$

In production of the quasi-two-level ac output, the Q2LC is not required to produce an $N+1$ voltage levels when N low-voltage cells are installed per arm. The main Q2LC design constraint can be set to the selection of voltage level counts, T_d, and ω_s values to alleviate the *dv/dt* stress at minimum drop in fundamental voltage magnitude and with minimum cell capacitance. This issue will be revisited several times along this paper. In order to achieve such a compromise especially at higher dc voltages, the number of output ac voltage levels may need to be reduced from $N+1$ to N_s+1, where

$$N_s = \lceil N/n \rceil \tag{5}$$

and n is the number of cells per cell subgroup. The minimum value of N_s, which corresponds to the upper value of n, is subject to the permissible *dv/dt* levels. In such a case, each subgroup will be composed of n MMC half-bridge cells effectively series connected, where equal static and dynamic voltage sharing is assured by the auxiliary capacitors. Gating delays may cause slight voltage imbalance between capacitors of the subgroup. To avoid complex gate drive/snubbering circuitry, the employed capacitor balancing technique will need to address individual cell capacitors of the arm rather than cell subgroups.

As an alternative to cell grouping, medium voltage half-bridge cells can be employed, where IGBT/diode modules are series connected to form the main and auxiliary cell switches, as in the cascaded two-level converter [38]. In this case, N becomes the total number of main path IGBTs per arm and n denotes the number of series IGBT/diode pairs per cell.

In either approach, a suitable redundancy margin in terms of cell numbers/ratings is mandatory for uninterrupted and balanced operation of the Q2LC with faulted cells.

A. Switching Sequences

Four possible switching patterns can be employed to achieve stepped two-level operation, and are termed "noncomplementary switching (NCS)," "CS," "shifted complementary switching (SCS)," and "shifted noncomplementary switching (SNCS)," modes.

1) Noncomplementary Switching: In this pattern, all three possible switch states of each cell [see Fig. 1(a)] are exploited. The switching sequence is shown in Fig. 2(a) for a four cell-per-arm, single-leg Q2LC. Starting with the load voltage at $1/2V_{\rm dc}$, all the upper arm cells are in an off-state, while the lower arm cells are in the on-state. The lower arm cells are then brought to an idle state a period T_i before the ac pole voltage transition commences. T_i may be chosen in the region of a few microseconds to ensure that cell voltages track (pro rata) any dc-link

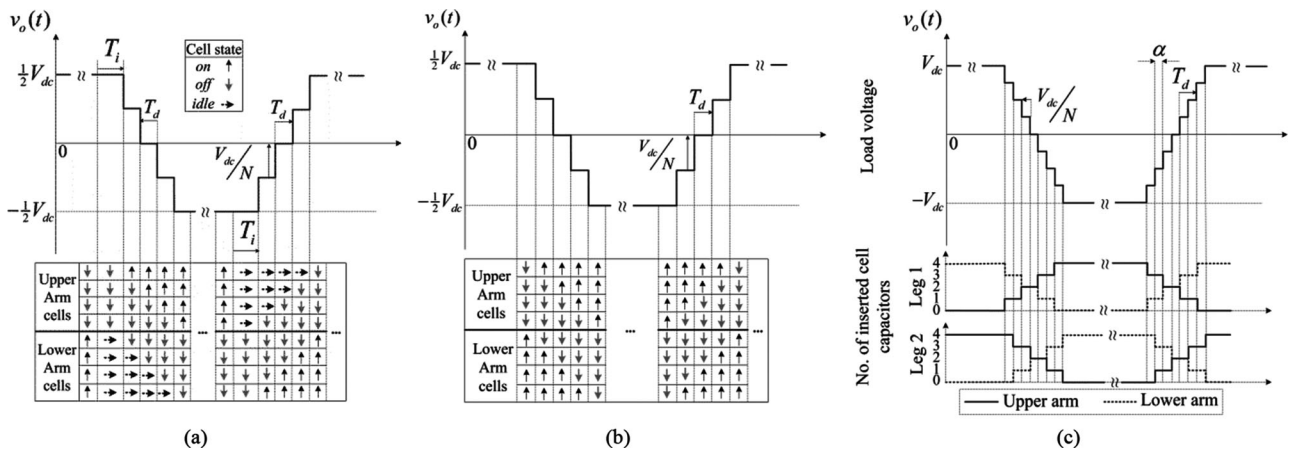

Fig. 2. Q2LC cell states with different switching sequences. (a) NCS sequence, (b) CS sequence, and (c) SCS sequence.

voltage variations occurring while the ac pole is clamped to either of the dc rails. For a stepped voltage transition from $1/2V_{\rm dc}$ to $-1/2V_{\rm dc}$ to occur, capacitors C_{1U} to C_{4U} are sequentially inserted by switching-on the corresponding cells with a dwell delay T_d. The load voltage transits to $-1/2V_{\rm dc}$ in four discrete steps, each being $1/4V_{\rm dc}$. During the transition, the lower arm voltage decreases in $1/4V_{\rm dc}$ steps, according to (2). For each step voltage drop, a lower arm cell is switched-off. With the last upper arm capacitor inserted into the circuit, the last lower arm cell turns off, and the pole load current commutates from the upper arm to the lower arm. A few microseconds (T_i) before the next load voltage polarity reversal, the upper arm cells are switched to an idle state, and a similar switching procedure is repeated for the voltage transit from $-1/2V_{\rm dc}$ to $1/2V_{\rm dc}$, as in Fig. 2(a). The idle cells of an arm could alternatively be switched-off simultaneously at the instant when the last capacitor of the complementary arm is inserted. However, this may bring about additional switching losses, depending on the loading conditions at the instant of switching.

2) Complementary Switching: In this switching sequence [see Fig. 2(b)], cells are utilized only in the ON or OFF states (no idle state). Cells of both arms switch in a complementary pattern. With $N_{L\rm on} = N - N_{U\rm on}$, the number of inserted capacitors in one arm always equals the number of off-state cells in the other arm of the same leg. This is a similar principle to conventional MMC switching [31]–[33]. Equation (3) holds for this switching mode. Therefore, according to (2) and (3), arm voltages are continuously complementary over the fundamental cycle.

3) Shifted Complementary Switching: The use of this switching pattern is preferred for single-phase H-bridge Q2LCs. The SCS sequence produces $2N_s + 1$ levels in the output voltage by introducing a time lag $0 < \alpha < T_d$ between the switching functions of the two phase legs, where the arms in each leg switch complementarily as in the CS sequence. This is shown in Fig. 2(c). The SCS sequence produces a further relieved *dv/dt* stress for the same value of T_t. A Q2LC of *N* cells per arm operating with the SCS sequence is functionally equivalent to a Q2LC structure of 2*N* cells per arm operating with the SC sequence and a smaller dwell time ($1/2T_d$ when $\alpha = 1/2T_d$), therefore has similar voltage and current dynamics as featured with the CS sequence.

The delay α can alternatively be inserted between the complementary switching functions of both arms of the same leg; thus, becoming valid for single-leg and three-phase Q2LCs as well. However, this may trigger extra common-mode currents. This applies to SNCS as well. A further study is needed.

4) Shifted Noncomplementary Switching: Similarly, a SNCS sequence can be produced by inserting a delay $0 < \alpha < T_d$ between the switching functions of the two phase legs of a single-phase H-bridge Q2LC, where the arms in each leg switch in a noncomplementary manner as in the NCS sequence. Again, operation is functionally equivalent to Q2LC with double the number of cells per arm operating under the NCS sequence with a smaller dwell time; thus, with alleviated *dv/dt* stress.

The analysis carried out in the rest of this paper will consider the CS and NCS sequences for the study of various operation aspects of Q2LCs. However, all conclusions are valid for operation with SCS and SNCS sequences—after accounting for the doubled number of levels and shorter T_d—as duals to CS and NCS, respectively, unless otherwise stated.

B. Q2LC Operation

A further investigation of the Q2LC operation aspects will be carried out in light of the proposed switching sequences. A case study is simulated using MATLAB/Simulink involving the three-phase Q2LC of Fig. 3 and Table I. The Q2LC is energized by a stiff dc source and applies a three-phase trapezoidal voltage waveform across the load. Although the Q2LC concept is not considered here for single-stage dc/ac conversion applications, the arrangement of Fig. 3 is useful for a simple demonstration of internal bridge dynamics under the said switching sequences.

The ±30-kV Q2LC of Fig. 3 uses the IHV FZ1500R33HL3 IGBT module from Infineon rated at 3300 V and 1500 A. Thirty three cells are connected in each arm to achieve redundant

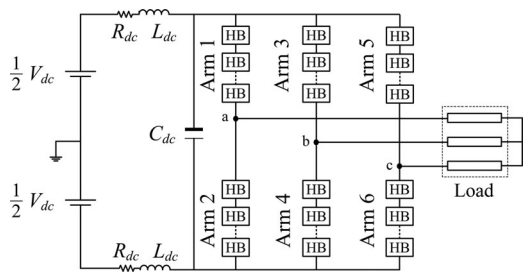

Fig. 3. Three-phase Q2LC.

TABLE I
PARAMETERS OF THE CONSIDERED THREE-PHASE Q2LC

V_{dc}	±30 kV	f_s	250 Hz
L_L (phase)	1.5 mH	L_{dc}	1 mH
R_L (phase)	40 Ω	R_{dc}	0.1 Ω
T_d	5 μs	C_{dc}	100 μF
C_{sm}	80 μF	R_{arm}	80 mΩ
N_s	10	L_{arm}	16.5 μH

operation with 1.8 kV per cell, or 2 kV per cell with three cells per arm bypassed (e.g., failure). The IGBT on-state and diode forward voltages are modeled as per the datasheet. A 0.5-μH stray inductance is modeled for each half-bridge cell. The cells of each arm are arranged in subgroups to produce $N_s = 10$ with 80-uF capacitance per subgroup. Individual cell voltages are balanced using the conventional sorting algorithm used for MMCs, where cell capacitors are continuously rotated based on measurements of their individual voltages and arm current polarities [34]–[36].

Fig. 4 depicts the output voltage, output current, arm currents, and cell voltages for both CS and NCS sequences. With a modulation index $m_f = 1$, the output voltage exhibits stepped behavior with a total of eleven $(N_s + 1)$ voltage levels independent of the switching sequence [see Fig. 4(g)]. Except during switching periods, only one arm per leg conducts the full load current, similar to a conventional two-level bridge. When ac pole voltage transition is realized by the CS sequence, load current flows simultaneously in both arms and nearly all cell capacitors in the leg experience current flow. With the connected load being inductive, this current will be charging for the capacitors of the switching-off arm (in which cells switch successively to the on-state) and discharging for the switching-on arm, where cells switch to the off state. The net result is that cell capacitors in each arm charge or discharge some of their energy once per half cycle of the fundamental frequency with voltage variation confined to a certain ripple band by action of the capacitor balancing technique. Fig. 4(b) and (e) shows that the ripple is about ±1.6% the nominal cell subgroup voltage.

Any ripple in the dc-side voltage will be exported (pro rata) to the on-state cells in each leg, since they must instantaneously balance with the dc-side voltage. This is the reason for the slight voltage variation observed in the on-state cells while load current fully flows in the complementary arm [see Fig. 4(b) and (e)]. A common-mode current is triggered in each leg during switching periods. This current, acting to regain voltage balance between each leg and the dc link, is limited by stray circuit impedance. As modeled, the individual cell stray arm inductances sum up to 16.5 μH per arm, while the equivalent device on-state resistance per arm is about 80 mΩ. Resonance between connected leg capacitance and the parasitic inductance triggers common-mode oscillations as seen in Fig. 4(a). It is observed that these oscillations are of insignificant magnitude and damp rapidly without dedicated arm resistance. These Q2LC internal current and voltage dynamics are not reflected on to the load side, as confirmed in Fig. 4(g).

The Q2LC exhibits slightly different internal voltage and current dynamics when the NCS sequence is employed. Nonetheless, the load side remains isolated from these dynamics as well. Each capacitor remains in conduction path for an average period of $1/2T_s - T_i$, where its voltage follows any dc-link ripple pro rata and, then, becomes bypassed for the rest of the fundamental period. Unlike the CS sequence, the full-load current flows through cell capacitors of the switching-off arm brought into the conduction path. In consequence, the cell subgroup voltage ripple becomes ±2% peak-to-peak for the same 80-μF cell subgroup capacitance. At the instant the last cell of the switching-on arm switches from idle to off, cell capacitors of the switching-off arm are all in conduction path and instantaneously balance with the dc-link voltage, triggering common-mode currents with slightly higher peak and oscillations as compared to CS sequence [see Fig. 4(a)]. It will be shown in section IV that NCS (SNCS) may offer better switching characteristics.

It can be seen in Fig. 4(d) that the current flow in the auxiliary circuit is significantly less than in the main path IGBT modules, apart from the adopted switching sequence. This allows the use of lower current rating devices in the auxiliary circuit. Furthermore, it extends the life time of cell capacitors. In this test the FZ400R33KL2C IGBT module from Infineon with 3300 V 400 A are used for the auxiliary circuit in each cell. Note that the peak auxiliary circuit "pulse" current depends on the instant the cell balancing controller brings the capacitor into conduction path. It is worth noting as well that the cell balancing controller succeeds to sustain such a low-voltage ripple while modeled to measure cell voltages only twice per half cycle. Nevertheless, cell voltages may need to be frequently polled for failure handling.

III. Q2LC Component Sizing

In a Q2LC-based dc/dc converter for dc-grid applications, capacitors briefly engage in power transfer with a small power factor range relative to an ac/dc conversion application, which facilitates capacitor size estimation. Investigation of current flow through the ac stage of the Q2LC-based DAB converter is mandatory for capacitance calculation.

The generic three-phase DAB dc transformer in Fig. 5(a) is considered, whereas the phase voltages and ac pole currents of two corresponding phase legs referred to primary side are plotted in Fig. 5(b). The primary and secondary Q2LCs phase voltages v_p and v_s, respectively, are phase shifted by the load angle φ applying a voltage v_{Ls} across the ac transformer leakage

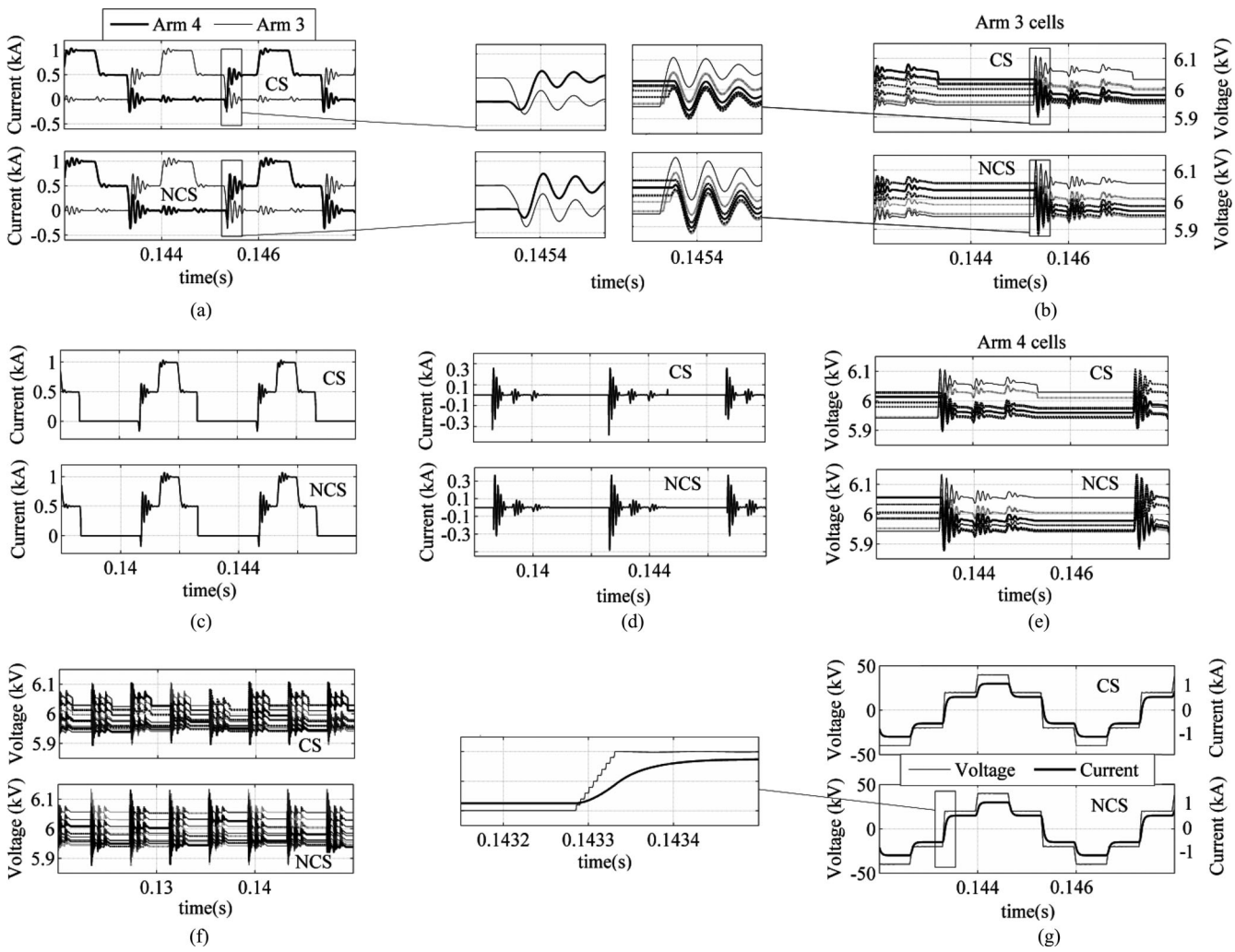

Fig. 4. Simulation results for the Q2LC of Fig. 3 and Table I. (a) Arm currents, (b) arm 3 cell voltages (six cells), (c) main path IGBT/diode current, (d) auxiliary IGBT/diode current, (e) arm 4 cell voltages (four cells), (f) time window of balanced arm four cell voltages, and (g) phase b output voltage and current.

inductance L_s. The ac transformer series resistance is neglected. Auxiliary capacitance size in a Q2LC cell is subject to the ac pole current profile during the switching period T_t. The cell subgroup capacitance of the primary and secondary sides ($C_{\rm gp}$ and $C_{\rm gs}$, respectively) can be expressed as

$$C_{\rm gp} = \gamma \frac{N_s}{\omega_s \ell V_{\rm dcp}} \int_{\theta_o}^{\omega_s T_t + \theta_o} \left(i(\theta_o) + \frac{1}{\omega_s L_s} \int_{\theta_o}^{\theta} v_{L_s}(\theta - \theta_o) d\theta \right) d\theta$$

$$C_{\rm gp} = \rho^2 a^2 C_{\rm gs} \tag{6}$$

where $i(\theta)$ is the ac pole current and γ is a factor of safety to account for the impact of Q2LC common-mode arm currents and the neglected series resistance ($\gamma \geq 1$). ℓ is the capacitor voltage ripple in per unit (e.g., $\ell = 0.1$ for 10% peak-to-peak capacitor voltage ripple). The dc ratio is $\rho = b/a$, where a is the ac transformer turns ratio and $V_{\rm dcs} = bV_{\rm dcp}$. Voltage transition periods are assumed equal for both bridges ($T_{tp} = T_{ts} = T_t$). Equation (6) is set to design the first subgroup capacitance of the switching-off arm to be brought into conduction path. Under inductive loading and NCS, this capacitor sustains full load current flow for a time T_t and undergoes the highest voltage variation. All cell subgroup capacitances need to be sized to this value since they circulate to the top rank of the switching sequence.

Starting at point 0 in Fig. 5(b), where $\theta = 0$, the formulae for $v_{Ls}(\theta)$ for each section of a half cycle can be developed and the primary phase current $i_p(\theta)$ can be calculated in terms of its initial value $i_p(\theta_o)$, where $\theta_o = 0$. Using the property $i_p(0) = -i_p(\pi)$, $i_p(0)$ and all half-cycle currents are calculated as given in the Appendix. From which all three-phase currents can be constructed. It is noteworthy that during the voltage transition period T_t of each phase leg in either bridge, the respective ac pole current is parabolic. The calculations carried out in this section and in the Appendix are valid for the range of load angles $\omega_s T_t \leq \varphi \leq \frac{1}{3}\pi - \omega_s T_t$. Similar calculations can be repeated for higher load angle ranges if the application requires so. In dc-grid applications, high-load angles are not typical. The current

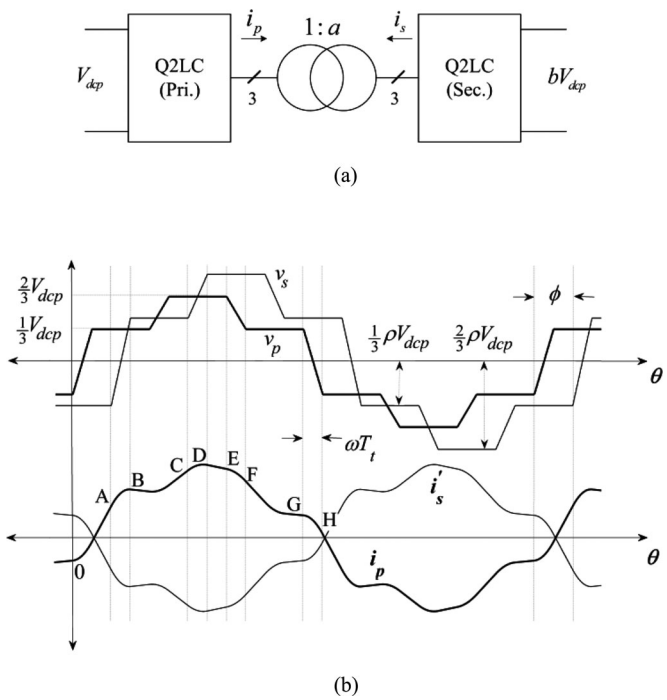

Fig. 5. (a) Block diagram of a generic three-phase Q2LC based DAB converter, and (b) ac voltages and currents of one transformer phase referred to the primary side [i_s' is the secondary-side phase current referred to primary].

profiles of segment CD, where $\frac{1}{3}\pi + \varphi \leq \theta \leq \frac{1}{3}\pi + \varphi + \omega_s T_t$, and segment EF, where $\frac{2}{3}\pi \leq \theta \leq \frac{2}{3}\pi + \omega_s T_t$, are important for switch rating selection. The current flow during T_t for $\varphi \leq \theta \leq \varphi + \omega_s T_t$ (segment AB) and $\pi \leq \theta \leq \pi + \omega_s T_t$ (segment GH) are of particular importance for cell capacitor sizing. Switching devices are to be rated at the peak arm current, which is the peak phase current, at rated power conditions. The peak of phase current at rated power flow (i.e., $\varphi = \varphi_{\max}$) is subject to the dc ratio. In dc-grid applications, the dc ratio in a DAB can vary within a limited range around unity depending on loading and by action of converter controllers. At $\varphi = \varphi_{\max}$, the local phase current peak value within segment CD is the maximum phase current magnitude when $\rho = \rho_{\max}, \rho_{\max} > 1$ and occurs at $v_{Ls}(\theta_{\mathrm{CD}}) = 0$. When $\rho = \rho_{\min}, \rho_{\min} < 1$, the phase current maximum magnitude (at $\varphi = \varphi_{\max}$) shifts to segment EF occurring at $v_{Ls}(\theta_{\mathrm{EF}}) = 0$. Using the Appendix, the maximum current values $i_p^{\mathrm{pk}}(\theta_{\mathrm{CD}}^{\mathrm{pk}})$, $i_p^{\mathrm{pk}}(\theta_{\mathrm{EF}}^{\mathrm{pk}})$, and the corresponding angles $\theta_{\mathrm{CD}}^{\mathrm{pk}}$ and $\theta_{\mathrm{EF}}^{\mathrm{pk}}$ are obtained as in (7) for $\rho_{\max} \geq 1$ and as in (8) for $\rho_{\min} \leq 1$

$$\theta_{\mathrm{CD}}^{\mathrm{pk}} = \frac{1}{\rho}\omega_s T_t(2 - \rho_{\max}) + \varphi_{\max} + \frac{1}{3}\pi \tag{7a}$$

$$i_p^{\mathrm{pk}}(\theta_{\mathrm{CD}}^{\mathrm{pk}}) = \frac{V_{\mathrm{dc}p}}{3\omega_s L_s}\left(\begin{array}{l}\left(\rho_{\max} - 3 + \dfrac{2}{\rho_{\max}}\right)\omega_s T_t \\ + 2\varphi_{\max} + (\rho_{\max} - 1)\dfrac{\pi}{3}\end{array}\right) \tag{7b}$$

$$\theta_{\mathrm{EF}}^{\mathrm{pk}} = 2(1 - \rho_{\min})\omega_s T_t + \frac{2}{3}\pi \tag{8a}$$

$$i_p^{\mathrm{pk}}(\theta_{\mathrm{EF}}^{\mathrm{pk}}) = \frac{V_{\mathrm{dc}p}}{3\omega_s L_s}\left(\begin{array}{l}(2\rho_{\min}^2 - 3\rho_{\min} + 1)\omega_s T_t \\ + 2\rho_{\min}\varphi_{\max} + (1 - \rho_{\min})\dfrac{\pi}{3}\end{array}\right). \tag{8b}$$

In case a DAB design requires $\rho_{\min} > 1$, then (7) defines the phase current maximum value. Similarly, if $\rho_{\max} < 1$, then (8) defines the phase current maximum magnitude. Equation (7) is also valid for partial loading for any $\rho > 1$ and $\omega_s T_t \leq \varphi \leq \frac{1}{3}\pi - \omega_s T_t$, whereas (8) is valid for partial loading as long as $\rho < 1$ and $\omega_s T_t \leq \varphi \leq \frac{1}{3}\pi - \omega_s T_t$. At $\rho_{\min} = \rho_{\max} = 1$, the peak currents in (7) and (8) will reduce to

$$i_p^{\mathrm{pk}}(\theta) = \frac{2V_{\mathrm{dc}p}\varphi_{\max}}{3\omega_s L_s}. \tag{9}$$

When rating switching devices current capacity, the higher of the current values produced by (7) and (8) is considered. A factor of safety may be introduced. Equations (7)–(9) represent currents of the primary side. The maximum current of the secondary side $i_s^{\mathrm{pk}}(\theta)$ can be described by (7)–(9) divided by the factor ρa.

In segments AB and GH, the formulae of $v_{Ls}(\theta)$ and $i_p(\theta)$ are given in (10)–(13). For $\varphi \leq \theta \leq \varphi + \omega_s T_t$

$$v_{L_s}(\theta_{\mathrm{AB}}) = \frac{V_{\mathrm{dc}p}}{3}\left((\rho + 1) - \frac{2\rho}{\omega_s T_t}(\theta - \varphi)\right) \tag{10}$$

$$i_p(\theta_{\mathrm{AB}}) = \frac{V_{\mathrm{dc}p}}{3\omega_s L_s}\left(\begin{array}{l}-\dfrac{\rho}{\omega_s T_t}(\theta - \varphi)^2 + (\rho + 1) \\ \times\ (\theta - \dfrac{1}{2}\omega_s T_t) + 2(\rho - 1)\dfrac{\pi}{3} - \rho\varphi\end{array}\right). \tag{11}$$

For $\pi \leq \theta \leq \pi + \omega_s T_t$

$$v_{L_s}(\theta_{\mathrm{GH}}) = \frac{V_{\mathrm{dc}p}}{3}\left((1 - \rho) - \frac{2}{\omega_s T_t}(\theta - \pi)\right) \tag{12}$$

$$i_p(\theta_{\mathrm{GH}}) = \frac{V_{\mathrm{dc}p}}{3\omega_s L_s}\left(\begin{array}{l}-\dfrac{1}{\omega_s T_t}(\theta - \pi)^2 + (1 - \rho) \\ \times\ (\theta - \dfrac{\pi}{3} - \dfrac{1}{2}\omega_s T_t) + \rho\varphi\end{array}\right). \tag{13}$$

The phase current has no dc offset and, consequently, $i_p(\theta) = -i_p(\theta + \pi)$. Also, current polarity is irrelevant for capacitor sizing; therefore, the currents of (11) and (13) at rated conditions are sufficient to quantify the maximum arm current flow during switching periods over the fundamental cycle.

For $\varphi > 0$, $i_p(\theta_{\mathrm{AB}})$ is higher than $i_p(\theta_{\mathrm{GH}})$ for $\rho > 1$ and is lower than $i_p(\theta_{\mathrm{GH}})$ for $\rho < 1$. Equations (11) and (13) confirm this for $\omega_s T_t \leq \varphi \leq \frac{1}{3}\pi - \omega_s T_t$. Also, they show that $i_p(\theta_{\mathrm{A}}) = i_p(\theta_{\mathrm{H}})$ and $i_p(\theta_{\mathrm{B}}) = i_p(\theta_{\mathrm{G}})$ for $\rho = 1$. At rated conditions where $\varphi = \varphi_{\max}$ and for $\rho = \rho_{\max}, \rho_{\max} > 1$, (6), (10), and (11) are used to calculate the primary-side capacitance requirement C_{gp} at rated power, given as

$$C_{\mathrm{gp}} = \gamma\frac{N_s T_t}{3\ell\omega_s L_s}\left(\varphi_{\max} + 2(\rho_{\max} - 1)\frac{\pi}{3} - \frac{\rho_{\max}}{3}\omega_s T_t\right). \tag{14}$$

TABLE II
PARAMETERS OF THE SIMULATED THREE-PHASE Q2LC-BASED DAB

	Primary side	Secondary side
DC voltage ($V_{\rm dc}$)	±30 kV	±60 kV
Arm impedance	16.5 μH/80 mΩ	30 μH/150 mΩ
Subgroup capacitance (C_g)	20 μF	10 μF
Subgroups per arm (N_s)	10	
Dwell time (T_d)	5 μs	
DC side inductance ($L_{\rm dc}$)	1 mH	
DC side resistance ($R_{\rm dc}$)	0.1 Ω	
DC link capacitor ($C_{\rm dc}$)	25 μF	
Operating frequency (f_s)	250 Hz	
Coupling transformer	55 kV/110 kV—power: 63 MVA series inductance: 10%—series resistance: 0.3%—Base impedance: 48.2 Ω at the 55 kV side	

For $\rho = \rho_{\min}, \rho_{\min} < 1$, (6), (12), and (13) are used to calculate $C_{\rm gp}$ at rated power as

$$C_{\rm gp} = \gamma \frac{N_s T_t}{3\ell\omega_s L_s}\left(\rho_{\min}\varphi_{\max} + 2(1-\rho_{\min})\frac{\pi}{3} - \frac{1}{3}\omega_s T_t\right). \tag{15}$$

Equation (14) gives the design value of $C_{\rm gp}$ when the dc ratio ultimate values $\rho_{\min}$ and $\rho_{\max}$ are both above unity. Otherwise, if $\rho_{\min}$ and $\rho_{\max}$ are both designed to be less than unity, the required capacitance $C_{\rm gp}$ is given by (15). If the system is designed such that $\rho_{\min} \le 1$ and $\rho_{\max} > 1$, the required capacitance size is given by (14) when the condition in (16) is true, otherwise the capacitance is designed by (15)

$$\rho_{\max} \ge \frac{4\pi - 3\varphi_{\max} - \omega_s T_t + \rho_{\min}\left(3\varphi_{\max} - 2\pi\right)}{2\pi - \omega_s T_t}. \tag{16}$$

When $\rho_{\max} = \rho_{\min} = 1$, (14) and (15) reduce to

$$C_{\rm gp} = \gamma \frac{N_s T_t}{3\ell\omega_s L_s}\left(\varphi_{\max} - \frac{1}{3}\omega_s T_t\right). \tag{17}$$

Switch rating and capacitance design carried above considers bidirectional rated power flow. A similar derivation when $\varphi_{\max} < \omega_s T_t$ can be done. Nonetheless, calculations using the given equations at $\varphi_{\max} = \omega_s T_t$ are expected to produce practically insignificant errors. The switch rating and capacitance design methods can be acceptably simplified by using (9) and (17) with appropriate safety factors to account for dc ratio range as well as other operation aspects (see section VII).

A simulation case study will be used to assess the proposed design method for device ratings and cell capacitances. The ±30-kV three-phase Q2LC described in Section II is connected to another ±60-kV three-phase Q2LC through an ac transformer to form a DAB converter. The ±60-kV side is considered the secondary side. Both converters are connected to stiff dc sources through impedance as per Table II. The ac transformation stage is modeled as a three-phase linear transformer with 10% leakage inductance, 0.3% series resistance, and 1:2 primary to secondary turns ratio. Each cell of the ±60-kV Q2LC model employs Infineon's IHV FZ800R33KL2C IGBT module with 3300 V and 800 A for the main power path, and the IHV FZ400R33KL2C IGBT module with 3300 V and 400 A for the auxiliary path. The modeled values of IGBT on-state and diode forward voltages are taken from datasheets. A 0.5-μH stray inductance is modeled for each half-bridge cell. Sixty cells per arm are connected in series for operation at 2 kV per cell for redundancy. This way, the equivalent device on-state resistance modeled per arm is 150 mΩ and the arm stray inductance is 30 μH (60 μH × 0.5 μH). Cells are grouped in subgroups with $N_s = 10$ (i.e., $n = 6$). Both Q2LCs employ NCS sequence. A load angle $\varphi = 7.2°$ is modeled such that 60 MW flows from primary to secondary. The secondary dc voltage is set to ±60.6 kV to produce a dc ratio $\rho = 1.01$. Other system parameters are summarized in Table II.

Fig. 6 shows results obtained mainly from the primary side with 2% dc voltage ripple. Fig. 6(f) shows that $\varphi > \omega_s T_t$ and $\rho > 1$; hence, (7) is used to calculate the peak of the primary-phase current (arm current) yielding 1080 A. This is in close agreement with the simulated value given in Fig. 6(b). Also, at the instant phase b ac pole becomes tied to the negative dc rail through arm 4, the arm current is found to reach over 800 A although (36) or (37) at $\theta = \varphi + \omega_s T_t$ in the Appendix expect an arm current value of 605 A. This mismatch is due to the superimposed common-mode current component seen in Fig. 6(b). Note that the maximum arm currents of the primary and secondary converters are well below the selected device current ratings.

If the said power flow and load angle represent rated conditions (i.e., $\varphi_{\max} = 7.2°$, $\rho_{\max} = \rho_{\min} = 1.01$), the previously calculated peak phase current can be used to design device ratings to the values detailed above while allowing for a factor of safety. At the same rated conditions, the cell subgroup capacitance can be designed using (14). With $\gamma = 1$ and for ±10% cell voltage ripple, (14) produces $C_{\rm gp} = 20$ μF. This value accounts for reverse power flow as well. As seen in Fig. 6, extra voltage ripple results from common mode current. The ripple was found to be confined to ±10% in primary and secondary sides irrespective of power flow direction when $C_{\rm gp} = 25\mu$F (i.e. $\rm Y = 1.25$).

When medium voltage half-bridge cells are employed like in a cascaded two-level converter (refer to Section II), the capacitance $C_{\rm gp}$ represents the individual cell capacitance. Alternatively, when $C_{\rm gp}$ is the aggregate capacitance of a subgroup of cells, the cell capacitance is $C_{\rm cell} = nC_{\rm gp}$. For the current example, where $n = 3$, $C_{\rm cell} = 75$ μF is required. In the secondary side, where $C_{\rm gs} = 6$ μF for ±10% voltage ripple and $n = 6$, $C_{\rm cell}$ is nearly 36 μF. For comparison, a regular MMC in sinusoidal mode with the same number of cells per arm and power flow will need a 7.3-mF cell capacitance at ±30-kV dc voltage level assuming 80 MVA apparent power capability. This estimation is based on 30 kJ/MVA cell specific energy [37], [39]. Therefore, a significant reduction of cell footprint is expected.

IV. ANALYSIS OF THE Q2LC OPERATION

A. Output Trapezoidal Voltage Analysis

In a Q2LC design, the number of cells per arm, the dwell time, and the operating frequency have direct impact on the

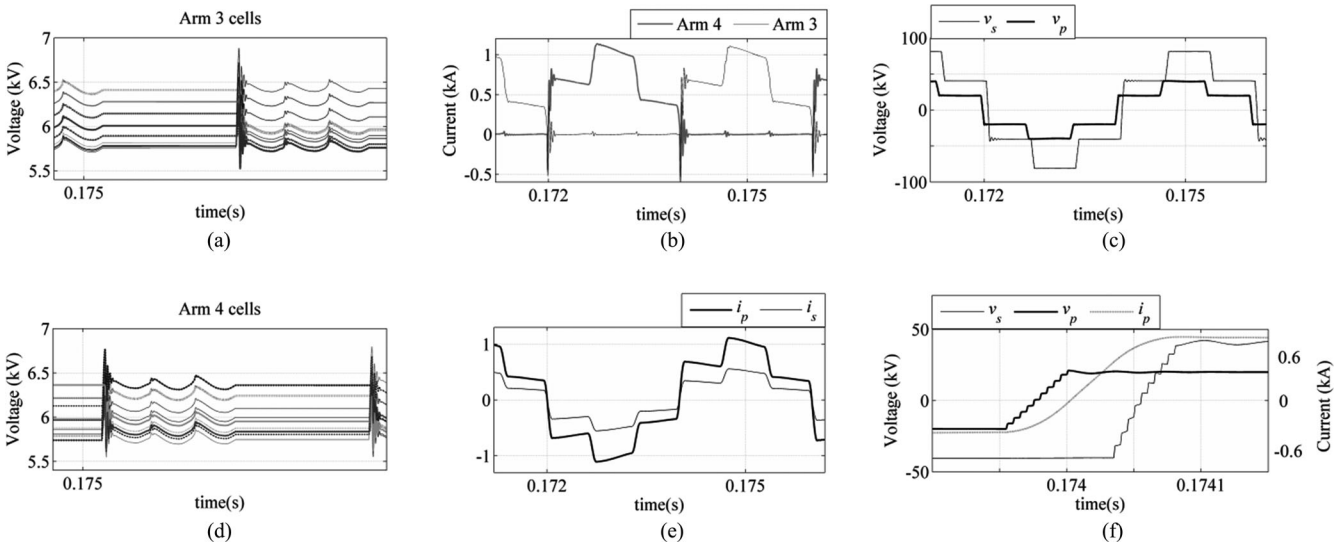

Fig. 6. Plotted waveforms from the DAB case study. (a) Arm 3 Cell subgroup voltages of primary Q2LC, (b) arm 3 and arm 4 of primary Q2LC currents (phase b), (c) the primary and secondary phase b voltages, (d) arm 4 Cell subgroup voltages of primary Q2LC (phase b), (e) the primary and secondary phase b currents, and (f) a zoomed section of subplot (c) with primary current of phase b included.

bridge output voltage v_o. The magnitude of the *k*th harmonic component of v_o can be calculated for a stepped trapezoidal waveform by decomposing it into square wave components as

$$\begin{aligned} v_{o(k)} &= m_k \frac{4}{\pi k} \frac{V_{\rm dc}}{N_s} \sin\left(\frac{k\pi}{2}\right)\eta \quad \forall\, N_s \in 2Z^+ \\ v_{o(k)} &= m_k \frac{4}{\pi k} \frac{V_{\rm dc}}{N_s} \sin\left(\frac{k\pi}{2}\right)\lambda \quad \forall\, N_s \in 2Z^+ + 1 \end{aligned} \tag{18}$$

where

$$\begin{aligned} \eta &= \sum_{i\in 2Z^*+1}^{N_s-1} \sin\left(\frac{k}{2}\left(\pi - iT_d\omega_s\right)\right) \\ \lambda &= \frac{1}{2} + \sum_{i\in 2Z^+}^{N_s-1} \sin\left(\frac{k}{2}\left(\pi - iT_d\omega_s\right)\right) \end{aligned} \tag{19}$$

where m_k is the modulation index ($0 \le m_k \le 1$) of the *k*th harmonic component ($k \in 2Z^*+1$). Alternatively, using the Fourier expansion of a periodical trapezoidal function, the magnitude of the *k*th harmonic component Φ_k is expressed as

$$\Phi_k = 2A\delta \frac{\sin\left(k\pi\delta\right)}{k\pi\delta} \frac{\sin\left(k\pi f_s T_t\right)}{k\pi f_s T_t} \tag{20}$$

where *A* is the peak-to-peak magnitude, δ is the duty ratio. Using (2) and (20), the approximate fundamental magnitude of v_o for $\delta = 0.5$ [see Fig. 1(c)] can be expressed as

$$v_{of} = m_f \frac{2V_{\rm dc}}{\pi} \frac{\sin\left({}^1\!/_2\omega_s\left(N_s-1\right)T_d\right)}{{}^1\!/_2\omega_s\left(N_s-1\right)T_d} \tag{21}$$

where m_f is the fundamental modulation index. The magnitude of $v_{\rm of}$ has less than 0.1% error when calculated by (21) rather than (18) over the expected range of parameter values; therefore, both equations are suitable for studying the impact $N_{\rm s}$, ω_s and T_d have on $v_{\rm of}$.

The peak magnitude of $v_{\rm of}$ is $2V_{\rm dc}/\pi$ when T_d is small (using the identity $\lim_{x\to 0}(\sin(x)/x) = 1$), which is $4/\pi$ the peak of $v_o(t)$, resembling square wave operation. For a single-phase H-bridge Q2LC, the right-hand-sides of (18) and (21) must be multiplied by 2 since the output voltage of a H-bridge converter transits between $\pm V_{\rm dc}$. With $m_f = 1$, taking $2V_{\rm dc}/\pi$ as a base value, (21) can be expressed in per unit as

$$v_{\rm of}^{\rm pu} = \frac{\sin({}^1\!/_2\omega_s(N_s-1)T_d)}{{}^1\!/_2\omega_s(N_s-1)T_d}. \tag{22}$$

The per unit representation in (22) holds for all single- and three-phase configurations (phase-to-ground voltage). $v_{\rm of}^{\rm pu}$ is graphed in Fig. 7 for different values of N_s, f_s, and T_d. As expected, $v_{\rm of}^{\rm pu}$ decreases with an increase in any of the three parameters, with a minimum of $2/\pi$ p.u. when $(N_s-1)T_d = 1/2T_s$, which represents a triangular-shaped output voltage.

The lower the fundamental voltage magnitude, the higher the load current for a given amount of power transfer, with subsequent penalties in terms of efficiency, volume, and capital cost. Expectedly, the results show that the sacrifice in the fundamental modulation index with a quasi-two-level output is insignificant for an acceptable range of parameter values. This allows for a margin for various design objectives to be met. Proper design of each of the three parameters in (22) depends mainly on the operating voltage, control design, employed switches, and volume constraints.

The low-order harmonics are to contribute to power transfer; therefore, investigating their magnitudes is important for the ac transformer design, as will be further highlighted in Section VII. Fig. 8 depicts the per unit magnitudes of the main harmonic components of v_o plotted against N_s and T_d at a constant frequency ($f_s = 500$ Hz). With higher values of N_s and T_d, the harmonic magnitudes fall and may reverse polarity (half-cycle phase shift). The base value for each harmonic p.u.

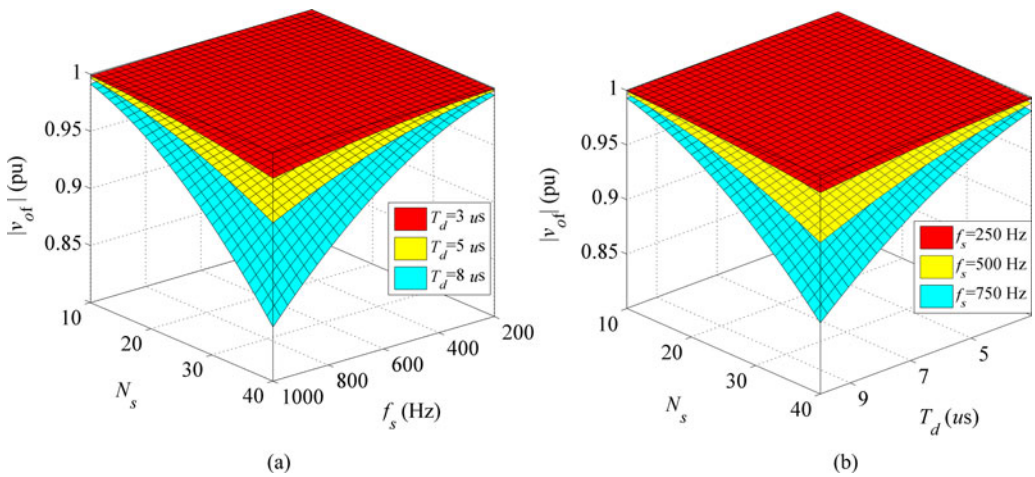

Fig. 7. Fundamental output voltage of the Q2LC in terms of N, ω_s, and T_d. (a) For discrete values of T_d and (b) discrete values of ω_s.

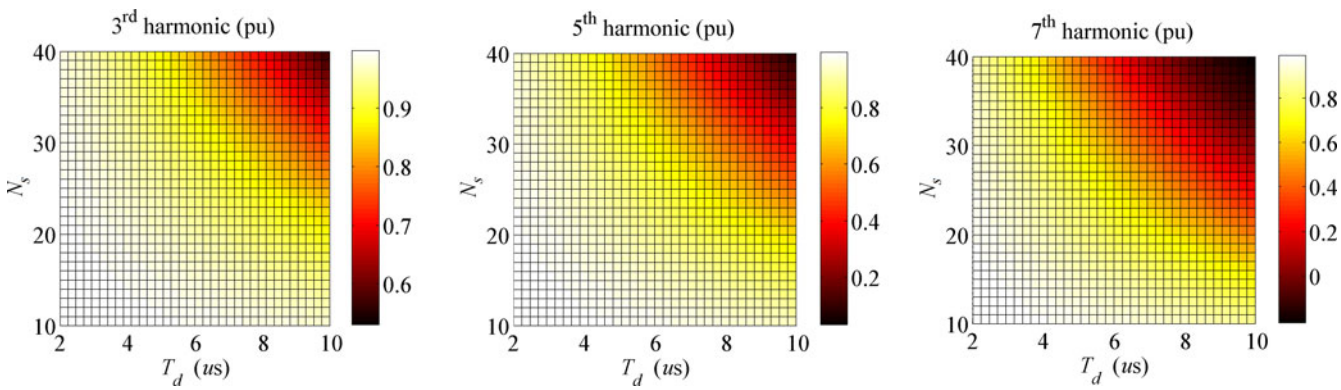

Fig. 8. Per unit magnitude of main harmonic components of the Q2LC output voltage, with $f_s = 500$ Hz.

magnitude is $2V_{\rm dc}/k\pi$ (4 $V_{\rm dc}/k\pi$ for a single-phase H-bridge) with k being the harmonic order.

B. Dwell Time Range

Selection of the dwell time T_d involves tradeoffs between *dv/dt* stress, cell capacitor size, and fundamental output voltage. The required dead time $T_{\rm DB}$ between the two IGBTs of each cell as well as other switching delays and transit times become significant considering the small value of T_d. The total switching time of one cell $T_{\rm sc}$ (IGBTs switch complementarily) can be defined as

$$T_{\rm sc} = t_{d(\rm off)} + t_f + t_{\rm DB} + t_{d(\rm on)} + t_r. \tag{24}$$

For instance, the Infineon FZ1500R33HL3 3.3-kV 1500-A IGBT module has a total turn-on time of $t_{d(\rm on)} + t_r = 1$ μs and turn-off time of $t_{d(\rm off)} + t_f = 5$ μs [40]. When a dead time of 0.5–1 μs is inserted, $T_{\rm sc}$ must be at least 6.5 μs. Consequently, the switching process of a cell must be initiated a time $t_{d(\rm off)} + t_f$ before the cell is actually meant to alter its state.

The dwell time, however, is not bounded by $T_{\rm sc}$, which is beneficial for applications where higher frequency is required. For a dwell time $T_d < T_{\rm sc}$, cell switching becomes naturally overlapped. Switching overlap in an arm means that the gating of the next cell to switch is initiated before the currently switching cell has actually changed state.

The overlapped switching sequence with positive (charging) arm current is shown in Fig. 9, where the cells per arm are numbered in ascending order for simplicity. The actual order is determined by the employed capacitor balancing method. With negative (discharging) arm current, a cell capacitor is inserted (a step in output voltage) only when the respective auxiliary IGBT fully turns on.

C. Soft-Switching Characteristics

With three states, a total of six different state transitions between on, off, and idle can take place in the half-bridge chopper cell of a Q2LC. During state transition, the voltage and current of each IGBT/diode pair in the cell depends on the direction of current flow through the cell terminals. The cell terminal current is considered positive if it flows so as to charge the capacitor. Fig. 10 shows all possible cell state transitions of a half-bridge chopper cell. An IGBT is soft switched when it turns on or off, while its antiparallel diode is conducting current [4]. With positive terminal current [see Fig. 10(a)], a cell state transition from off to on forces the main IGBT S to interrupt current flow (hard turn-off). The current forces the diode D' to conduct. Thus, the

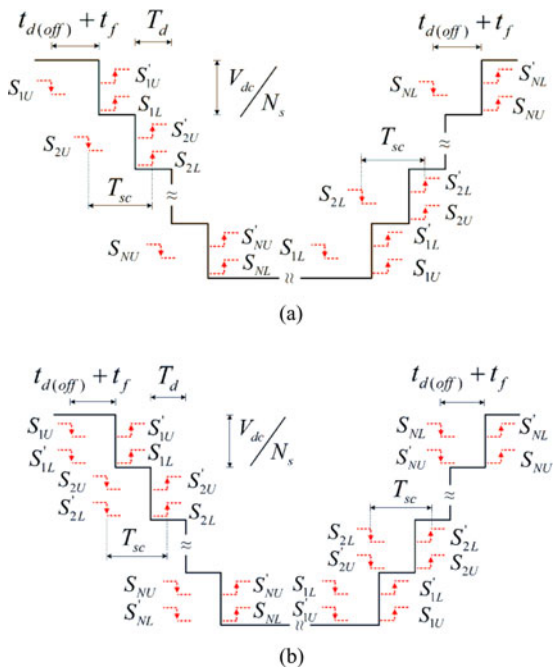

Fig. 9. Overlapped cell switching for dwell time $T_d < T_{\rm sc}$. (a) NCS (SNCS) sequence, and (b) CS (SCS) sequence.

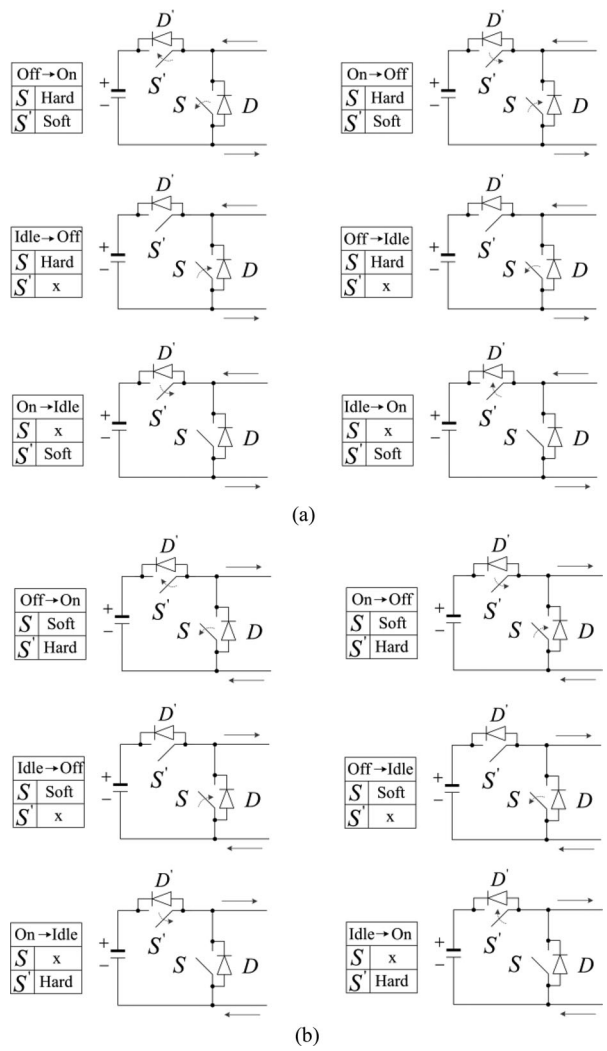

Fig. 10. All possible state transitions of a half-bridge Q2LC cell with (a) Positive (charging) current, and (b) Negative (discharging) current.

auxiliary IGBT S' turns on after the dead time $T_{\rm DB}$ with its antiparallel diode conducting (soft turn-on). For the same terminal current direction, when the cell state changes from on to off, S' undergoes soft turn-off, while S is hard switched. Once S turns on, D' becomes reverse-biased and a short reverse recovery time is necessary. Therefore D' must be a fast-recovery diode.

When the cell switches between on and off states under negative current, S turns on and off under zero voltage and current, while S' is hard switched. When S' turns on, D becomes reverse biased and must be a fast recovery device. When a cell transits between on and idle states, only the auxiliary IGBT S' is involved, and is hard switched under negative current and soft switched with positive current, as shown in Fig. 10. Similarly, when switching between idle and off states, only the main IGBT S is involved, and it undergoes soft switching under negative current and hard switching with positive current. Fast-recovery characteristics are required for both antiparallel diodes (D' for transit from idle to off state with positive current and D for transit from idle to on with negative current).

The soft turn-on capability is of pivotal importance for switching loss curtailment [14], [41]. Hard turn-off losses can be reduced using passive lossless snubbers, although any form of discrete snubbering should be avoided, when possible, in order to reduce complexity and costs. Therefore, an augmented soft-turn off feature is undoubtedly a plus.

In a Q2LC phase leg, the switching-off arm—where cells states transit sequentially from off to on—experiences positive current flow when the phase current zero-crossing instant lags that of the phase voltage by an angle $\upsilon \geq 1/2\omega_s T_t$ (inductive loading). Conversely, it experiences negative current flow when the phase current zero-crossing instant leads that of the phase voltage by an angle $\upsilon \geq 1/2\omega_s T_t$ (capacitive loading). Consequently, inductive loading will cause all auxiliary IGBTs of the switching-off arms to turn-on with zero voltage and current in a lossless manner. With capacitive loading, these IGBTs will hard turn-on, increasing switching losses.

The switching losses of the switching-on arm(s)—where cells switch sequentially to the off state—-depend on the switching sequence. With the CS sequence, the switching-on arm has all cells switching from on to off state. This state transition takes place with some current flow in the arm. In case of inductive loading with $\upsilon \geq 1/2\omega_s T_t$, this current flow is in the discharging direction. Thus the main path IGBTs of the switching-on arms experience soft turn-on, while the auxiliary IGBTs have a lossy turn-off, as displayed in Fig. 10. The direction of current flow in the switching-on arm(s) will be positive for capacitive loading with $\upsilon \geq 1/2\omega_s T_t$, resulting in hard turn-on of the main path IGBTs and soft turn-off of the auxiliary IGBTs.

With the NCS sequence, current flows in the IGBT/diode pairs of the switching-on arms only when the last cell (cell subgroup) transits from the idle to off state. This way, soft turn-on is ensured for at least $N_s - 1$ main path IGBTs in each switching-on arm,

TABLE III
COMPARISON OF SWITCHING CHARACTERISTICS UNDER DIFFERENT SWITCHING SEQUENCES [↓ = OFF, ↑ = ON]

Loading		Inductive $\upsilon \geq ½\omega_s T_t$		Capacitive $\upsilon \geq ½\omega_s T_t$		Inductive $\upsilon < ½\omega_s T_t$			
Switching sequence		CS (SCS)	NCS (SNCS)	CS (SCS)	NCS (SNCS)	CS (SCS)		NCS (NSCS)	
						Before i_{load} zero crossing	After i_{load} zero crossing	Before i_{load} zero crossing	After i_{load} zero crossing
Switching off arms (cells switching to on state)	Main IGBTs	Hard↓	Hard↓	Soft↓	Soft↓	Similar to CS (SCS) with inductive loading	Similar to CS (SCS) with capacitive loading	Similar to NCS (SNCS) with inductive loading	Similar to NCS (SNCS) with capacitive loading
	Aux. IGBTs	Soft↑	Soft↑	Hard↑	Hard↑				
Switching on arms (cells switching to off state)	Main IGBTs	Soft↑	Soft↑	Hard↑	Soft↑[2]				
	Aux. IGBTs	Hard↓[1]	No switching	Soft↓	No switching				

[1] Except first cell to switch, when dc side voltage is stable and with low ripple. [2] Except last cell to switch.

regardless of the loading conditions. Note that transition of cells states from on to idle in the same arm—a period T_i before the output voltage transition—occurs at zero current with all the load current flowing in the other arm of the phase leg. In Fig. 10, the state transitions from off to idle and from idle to on are irrelevant to Q2LCs employed in DAB applications and operating under the presented switching sequences.

Table III summarizes the switching characteristics explained above, with the improvements offered by NCS over CS shaded in gray. As Table III confirms, NCS sequence will generate lower switching losses under capacitive loading than with the CS sequence. Furthermore, the turn-off losses of the auxiliary IGBTs of the switching-on arm(s) under inductive loading are not present with the NCS sequence. A further study is needed to quantify the significance of the switching loss curtailment brought about by NCS sequence with regard to the extra common-mode oscillation and capacitor voltage ripple it triggers as compared to the CS sequence.

So far, one can conclude that regardless of the switching pattern, inductive loading is favored for a Q2LC in terms of switching losses. This characteristic is used to define the soft-switching region for a Q2LC-based DAB. It will be illustrated with the aid of the space vector representation of the fundamental components of ac quantities, referred to primary (see Fig. 11a). Both Q2LCs will be inductively loaded with $\boldsymbol{\upsilon} \geq 1/2\omega_s T_t$ (i.e., soft switched) as long as the ac current space vector lies within the shaded area representing an angular span $\varphi - \omega_s T_t$. So for both converters to operate soft switched, $\varphi > \omega_s T_t$ is an essential operation constraint. Additionally, the dc ratio for soft switching of both converters must lie within the boundary defined by

$$\rho_h = \frac{4\pi - 3\omega_s T_t}{4\pi + 3\omega_s T_t - 6\varphi} \tag{25a}$$

$$\rho_l = \frac{1}{\rho_h} \tag{25b}$$

where ρ_h and ρ_l are the highest and lowest values of the dc ratio, respectively, for soft-switched primary and secondary Q2LCs. Equation (25) can be derived by setting $i_p(\theta = \omega_s T_t) = 0$ and $i_p(\theta = \varphi) = 0$. The soft-switching boundary defined above is graphed in Fig. 11(b) and (c) for different values of load angle, dwell time, and fundamental frequency. The area bounded by each curve is the soft-switching region for the respective operating conditions.

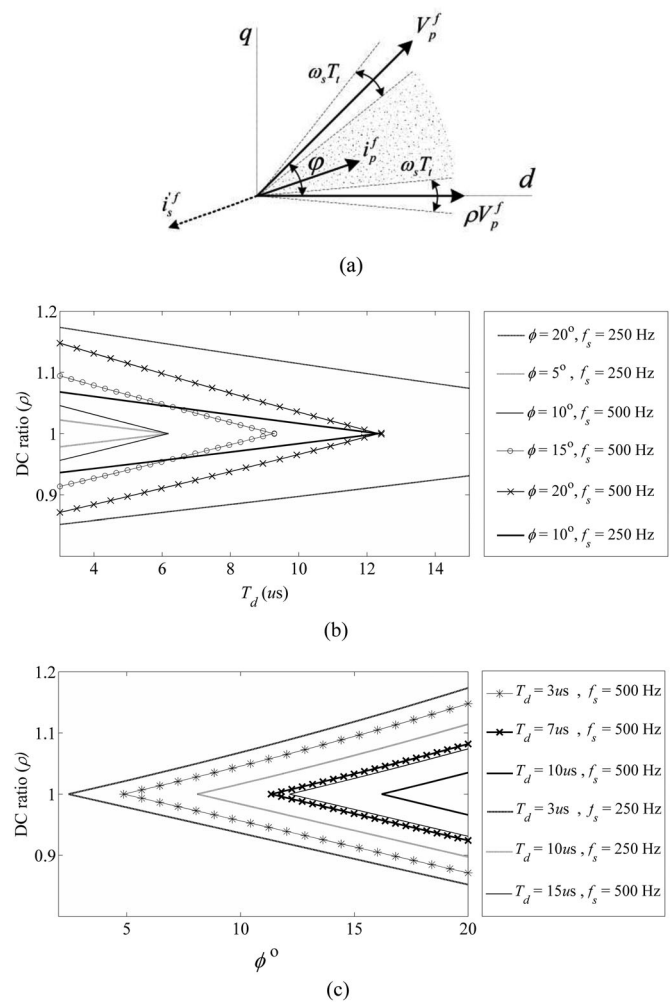

Fig. 11. (a) Phasor diagram representing ac voltages and currents of a Q2LC-based DAB. [Superscript *f* denotes fundamental component], (b) equation (25) plotted against dwell time, and (c) equation (25) plotted against load angle.

Alternatively, if the ac current vector lies within the angle $\omega_s T_t$ surrounding the voltage space vector of either converter, this converter will operate in partial soft switching, with one or more cells per arm switching under capacitive loading (i.e., $\boldsymbol{v} < 1/2\omega_s T_t$). In Fig. 11a, an extended region including the partial soft-switching areas (an angle span $\varphi + \omega_s T_t$) can also be defined. In this region a slightly higher range of dc ratio than that plotted in Fig. 11(b) and (c) is possible. This region is bounded by $\varphi = \omega_s T_t$, $i_p(0) = 0$ and $i_p(\theta = \varphi + \omega_s T_t) = 0$, yielding the dc ratio boundary values given by

$$\rho_h = \frac{4\pi - 3\omega_s T_t}{4\pi - 3\omega_s T_t - 6\varphi} \tag{26a}$$

$$\rho_l = \frac{1}{\rho_h}. \tag{26b}$$

V. Q2LC Operation With Modulation Index Control

Modulation index control in a DAB converter enhances the capability of voltage regulation and power flow control [15], [42]–[45]. In a Q2LC, the sequential switching nature allows the fundamental voltage magnitude produced by the Q2LC be varied by a number of techniques. However, in practice, the variation range will be limited relative to a standard MMC dc/ac converter. The main limiting factors are switching losses and harmonic content. Nevertheless, when utilized within a dc grid, the bridges of a front-to-front dc–dc transformer may not be required to operate at as wide range of modulation indices as a terminal dc/ac converter is expected to. Furthermore, the presence of an ac transformer stage with on-load tap changers may help reduce the modulation index control range required to account for steady state dc voltage variations. An exception to that is a faulty condition, where the nonfault-side Q2LC may have to operate in a current controlled mode to enable the healthy sections of the dc grid ride-through the fault/disturbance.

For a generic Q2LC design, (21) implies that the fundamental voltage magnitude $v_{\rm of}$ can be changed by varying the dwell time T_d (while $m_f = 1$). As has been shown in Fig. 7, this change is limited except for higher values of N_s and f_s. However, further reduction of $v_{\rm of}$ can be produced by sequencing some of the cells per arm at a dwell time T_{dm} higher than T_d [see Fig. 12(a)]. Equation (18) can be applied to each set of cells having the same dwell time then summing to produce the fundamental output voltage and harmonic magnitudes. Clearly, the multislope waveform requires sizing the cell capacitance to the highest dwell time. Double or triple slope waveform can be produced to extend the control range and eliminate high order harmonics; however; on the expense of larger cell capacitors. "Slope modulation" may be considered the primary modulation index control technique. Additional auxiliary techniques may be employed in conjunction with slope modulation for a wider control range, if needed.

A number of auxiliary techniques will be briefly analyzed. These are denoted "interswitching modulation," "clamp modulation," and the conventional "phase-shift modulation." Fig. 12(b) and (c) displays the modulated Q2LC output voltage (with $m_f < 1$) for two auxiliary modulation techniques. Note that only auxiliary techniques—not the slope modulation—are regarded to act upon the value of m_f in (18).

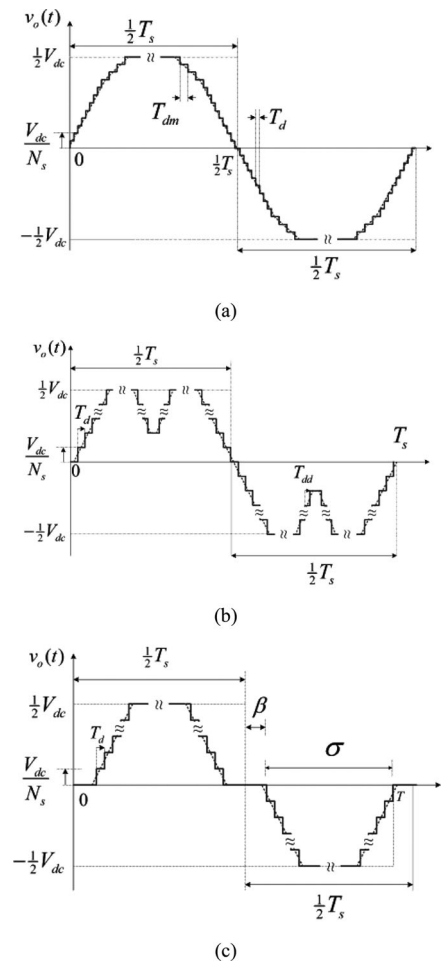

Fig. 12. Modulated Q2LC output voltage. (a) Multislope trapezoid, (b) interswitching modulation, and (c) phase-shift modulation.

A. Interswitching Modulation

In the interswitching modulation [see Fig. 12(b)], a controlled stepped dip is symmetrically introduced into the output voltage. The dip magnitude and time span are controlled to achieve the required modulation index. The dip magnitude is $N_m V_{\rm dc}/N_s$, where N_m is the number of dip steps ($N_m \leq 1/2N_s$). The dip time is $2N_m T_{dd}$, where T_{dd} is the step dwell time. Using (18), the p.u. magnitude of the *k*th odd harmonic component of the interswitching modulated output voltage $v_{o(k)}$ is given in (27). Equation (27) is valid for single-leg, H-bridge, and multi phase Q2LC topologies

$$V_{o(k)}^{\rm pu} = \begin{cases} \dfrac{2}{N_s}\sin\left(\dfrac{k\pi}{2}\right)(\eta - \chi), & N_s \in 2Z^+ \\ \dfrac{2}{N_s}\sin\left(\dfrac{k\pi}{2}\right)(\lambda - \chi), & N_s \in 2Z^+ + 1 \end{cases} \tag{27a}$$

where

$$\chi = \sum_{i}^{N_m - 1} \sin\left(kT_{dd}\omega_s\left(N_m - i\right)\right). \tag{27b}$$

The base value for each harmonic p.u. magnitude is $2V_{\rm dc}/k\pi$ ($4V_{\rm dc}/k\pi$ for the single-phase H-bridge). To achieve a certain m_f, the following condition must apply to (27):

$$\chi|_{k=1} = \begin{cases} (1-m_f)\,\eta|_{k=1}\,, & N_s \in 2Z^+ \\ (1-m_f)\,\lambda|_{k=1}\,, & N_s \in 2Z^+ + 1. \end{cases} \tag{28}$$

The condition in (28) can be realized by controllers. For example, with one of the two parameters N_m and T_{dd} held constant, a control loop can vary the other parameter within an intended range in order to follow the m_f command. Once the first control parameter reaches its limit with a nonzero m_f error, a second control loop activates to vary the other parameter. The m_f command itself can be the output of a current-control loop.

B. Clamp Modulation

The clamp modulation method is similar to conventional MMC modulation index control [46]–[48], where the output voltage peaks at $\pm m_f V_{op}$ where $V_{op} = 1/2V_{\rm dc}$ for a single-leg or a multi-phase Q2LC and $V_{op} = V_{\rm dc}$ for an H-bridge Q2LC. For the latter structure, number of cells per arm in on state required to achieve a certain m_f is given by (29), over a cycle. In (29), $||x||$ is the value of x rounded to the nearest integer. From (29) in conjunction with (2) one can note that at least one cell per arm must remain in on-state such that $m_f < 1$. This implies that load current always flows through the inserted capacitor(s); thus, a large cell capacitance is needed to retain acceptable voltage ripple. The required capacitance increase may be significant even if the inserted cells per arm are cycled during operation. Furthermore, the values the modulation index can take are discrete, thus reducing controllability.

C. Phase-Shift Modulation

In phase-shift modulation [see Fig. 12(c)], a phase shift $\beta > T_t$ is inserted between the switching functions $N_{Y\rm on}(t)$ of the two legs of the single-phase H-bridge Q2LC such that they are no longer complementary. This introduces zero-volt intervals in each output voltage half cycle [43]. Zero-volt intervals can be inserted in the ac pole voltage of single-leg or multi-phase Q2LCs by splitting the transit period T_t into two halves with a time delay angle 2β. This way ac pole voltage transits for $1/2T_t$ to zero, where it remains for an angle 2β (no cell state transition), then transits to the other dc rail voltage in $1/2T_t$. However, the range of β will be narrower than an H-bridge converter to avoid significant increase of cell capacitance. Using (18), for a phase shift of $\beta = 1/2(\pi - \sigma)$, $v_{o(k)}^{\rm pu}$ can be expressed as in (30), which holds for single-leg, H-bridge and multi-phase Q2LC designs

$$v_{o(k)}^{\rm pu} = \begin{cases} \dfrac{2}{N_s}\sin\left(\dfrac{k\pi}{2}\right)\varsigma, & N_s \in 2Z^+ \\ \dfrac{2}{N_s}\sin\left(\dfrac{k\pi}{2}\right)\psi, & N_s \in 2Z^+ + 1 \end{cases} \tag{30a}$$

where

$$\varsigma = \sum_{i\in 2Z^*+1}^{N_s-1} \sin\left(\tfrac{1}{2}k\left[\sigma - iT_d\omega_s\right]\right)$$

$$\psi = \frac{1}{2} + \sum_{i\in 2Z^+}^{N_s-1} \sin\left(\tfrac{1}{2}k\left[\sigma - iT_d\omega_s\right]\right). \tag{30b}$$

Using (18) and (30), the phase shift angle required to produce a certain m_f must satisfy the condition

$$\eta|_{k=1} = \begin{cases} \dfrac{1}{m_f}\,\varsigma|_{k=1}\,, & N_s \in 2Z^+ \\ \dfrac{1}{m_f}\,\psi|_{k=1}\,, & N_s \in 2Z^+ + 1. \end{cases} \tag{31}$$

$v_{o(k)}^{\rm pu}$ is graphed in Fig. 13 for interswitching modulation and phase-shift modulation. Both graphs are developed with a Q2LC design, where $T_d = 5$ μs, $N_s = 20$, and $\omega_s = 1000\pi$ rad/s. These values result in a 1.5% drop in fundamental output voltage before application of a further modulation technique (i.e., $m_f = 1$). For this design, interswitching modulation employed with $T_{dd} = 10$ μs and $N_m = 1/2N_s = 10$ achieves a fundamental modulation index of about $m_f = 0.7$. Increasing T_{dd} generates further reductions, but at the expense of larger cell capacitances and switching losses. A study of the output waveform harmonic content (particularly low order harmonics) is important for power flow and transformer loss analyses. In Fig. 13(a), the third and seventh harmonic voltages may rise above 1 p.u. over some range, whereas the fifth and ninth remain below their base values over the shown range.

As introduced previously, the base value of each harmonic voltage is its corresponding value in a square wave of the same frequency and magnitude. In Fig. 13(b), the fundamental voltage decreases while increasing β. The same occurs to the third harmonic, which reverses polarity for $\beta > 26°$. Other main harmonic components are less than their base values over the considered range. At $\beta = 0$ (i.e., no phase-shift modulation), the per unit values of harmonic voltages are also below 1 p.u. due to the trapezoidal shape.

Theoretically, all three auxiliary modulation techniques can concurrently control the output voltage in conjunction with slope modulation. Practically, in terms of cell capacitance

$$N_{Y\rm on}(t) = \begin{cases} \|N_s(1-m_f)\| + \sum_{i}^{\|N_s(2m_f-1)-1\|} u(t - iT_d), & 0 \le t < \|N_s(2m_f-1)-1\|\,T_d \\ \|m_f N_s\|\,, & \|N_s(2m_f-1)-1\|\,T_d \le t < \tfrac{1}{2}T_s \\ \|m_f N_s\| - \sum_{i}^{\|N_s(2m_f-1)-1\|} u(t - [\tfrac{1}{2}T_s + iT_d]), & \tfrac{1}{2}T_s \le t < \tfrac{1}{2}T_s + \|N_s(2m_f-1)-1\|\,T_d \\ \|N_s(1-m_f)\|\,, & \tfrac{1}{2}T_s + \|N_s(2m_f-1)-1\|\,T_d + \le t < T_s \end{cases} \tag{29}$$

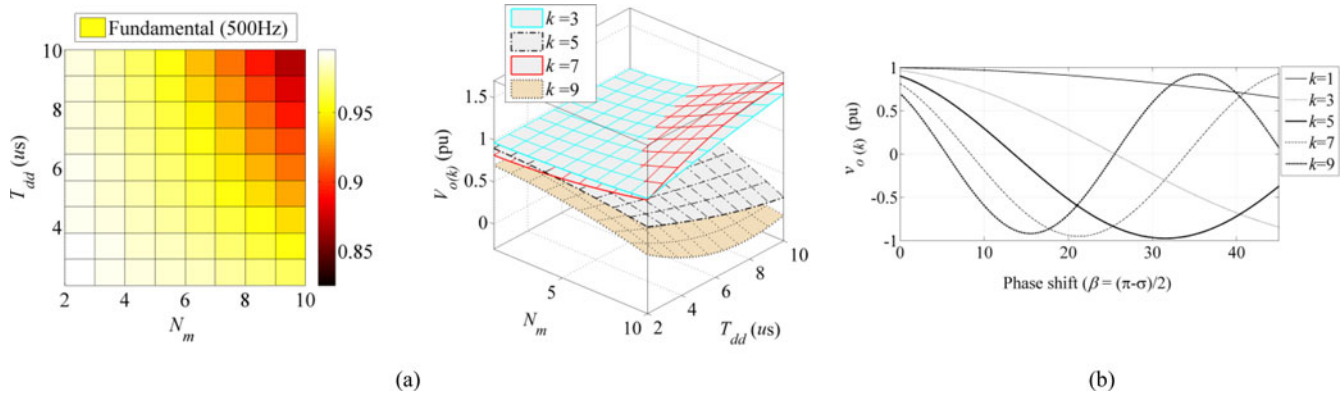

Fig. 13. Harmonic magnitudes of Q2LC output voltage at $T_d = 5\ \mu$s, $N_s = 20$, and $f_s = 500$ Hz, with (a) interswitching modulation, and (b) Phase-shift modulation.

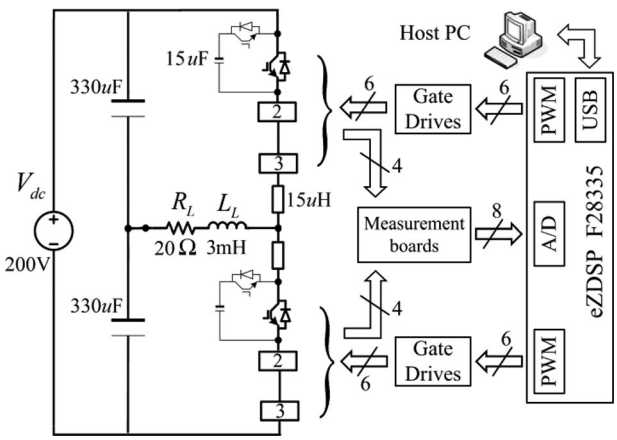

Fig. 14. Schematic for the reduced-scale single phase Q2LC.

requirement, interswitching, and phase-shift modulation techniques are favored over clamp modulation. When interswitching and phase-shift modulation techniques are merged with slope modulation, (27) and (28) evolve to (32) and (33), respectively

$$v_{o(k)}^{\mathrm{pu}} = \begin{cases} \dfrac{2}{N_s}\sin\left(\dfrac{k\pi}{2}\right)(\varsigma - \chi), & N_s \in 2Z^+ \\ \dfrac{2}{N_s}\sin\left(\dfrac{k\pi}{2}\right)(\psi - \chi), & N_s \in 2Z^+ + 1 \end{cases} \tag{32}$$

$$\chi|_{k=1} = \begin{cases} (1 - m_f)\,\varsigma|_{k=1}, & N_s \in 2Z^+ \\ (1 - m_f)\,\psi|_{k=1}, & N_s \in 2Z^+ + 1. \end{cases} \tag{33}$$

Equations (32) and (33) offer at least five degrees of freedom for output voltage modulation design, namely N_s, N_m, T_d, T_{dd}, and σ. An extra degree of freedom is implicitly present due to the variable dwell time of the slope modulation mode. Direct design constraints are cell capacitance size, switching losses, and ac transformer design and losses.

VI. Experimental Validation of Concept

Fig. 14 and Table IV summarize the layout and parameters of the utilized test-rig. With a 200-V dc source, a stepped output voltage of about ±100-V peak drives a 10-A peak-to-peak load current (see Fig. 15). In Fig. 15(c), the cell voltages are maintained within a ±12% peak-to-peak ripple band for a 5-A peak load current, with 15-μF cell capacitance. This band can be reduced with higher capacitance for the same loading, as per (6).

TABLE IV
Other Parameters of the Scaled Laboratory Setup

Dwell time (T_d)	25 μs
Operating frequency	250 Hz
Switching sequence	CS

The load voltage transits in three uniform steps (a four-level waveform). Common-mode inrush current peaks at around 1.4 p.u. of the load current and will be minimal with proper design of inductance/capacitance ratio. Circuit parasitic resistance rapidly damps common-mode oscillations, which quickly disappear after the voltage transition period. As predicted, the load current is decoupled from arm current oscillations. The results confirm that small cell capacitance and arm inductance is needed compared to conventional MMCs of similar power.

A power analyzer connected across the load and the dc supply showed 95% efficiency. The primary source of the incurred sizable losses is the on-state voltage of low voltage IGBTs. For the employed IRG4IBC30UDPBF 17 A 600 V devices, this voltage constitutes a significant percentage of the device voltage rating, particularly since the IGBTs are operated at a fraction of their rated voltage and well below their current rating. In a practical MV or HVDC application, the on-state voltage/resistance of high-power high-voltage IGBT modules are insignificant against their rating, reducing the percentage contribution in conduction losses despite the higher number of IGBTs employed. Also, optimal conductor sizing and circuit routing is a characteristic of manufactured systems where stray components are minimized.

VII. Discussion

Cell voltage ripple design involves trading off cell capacitance and common-mode current. Due to the small cell capacitance size, the energy required to balance the dc voltage with the sum of cell voltages in each phase leg is low. Under such condition, small arm inductance is needed and the circuit stray inductance

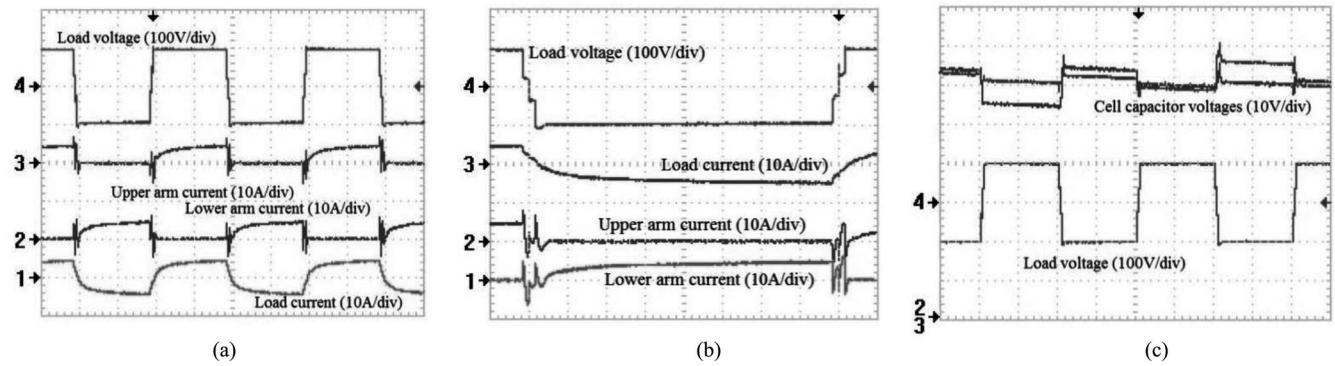

Fig. 15. Experimental results from the scaled test rig. (a) 1 ms/div, (b) 250 μs/div, (c) 1 ms/div.

may be sufficient. Also, stray resistance provides suitable damping. A further study needs to estimate the impact of fault current limiting, power reversal and start up requirements on cell capacitance and arm inductance sizes. A larger cell voltage ripple leads to larger common-mode current peaks, particularly with the NCS sequence. A larger common-mode current will in turn contribute to higher dc voltage ripple. Therefore, selection of cell voltage ripple band is strongly related to dc-side filtering.

Transformer design for medium and high voltages, even at the medium frequency range is challenging. Although the Q2LC provides acceptable *dv/dt* stress levels, issues like transformer core losses and the impact of parasitic components need to be addressed. Particularly, in upper medium and high voltage dc–dc converter designs, ac transformer efficiency will be of higher priority than its volume, which will allow designers to decrease the operating frequency towards lower ranges (< 500 Hz). This postulate is supported when considering the physical clearance and voltage creepage distance requirements at such high voltage levels, which is likely to contradict any volume reduction. Note that, at very high- power levels, the use of three single-phase ac transformers may be unavoidable. Alternatively, a high-voltage Q2LC DAB may be split to several medium voltage modules with series, parallel, or series parallel connections to facilitate transformer design. In traction and dc distribution applications, at medium voltage levels, the frequency could be relatively increased for a smaller ac transformer stage.

The Q2LC structure utilizes double the number of IGBTs as an equivalent series-switch-array two-level converter. Although the auxiliary IGBT/diode pair does not require the same continuous current rating as the main IGBT/diode pair, the capital cost of a Q2LC is expected to be higher as the silicon area has increased. Nevertheless, the operation of each Q2LC cell involves only one IGBT in on-state at any instant. Except for the brief voltage transition periods, the Q2LC is effectively a two-level converter. As a direct result, conduction losses are expected to be similar. The soft-switching characteristics, on the other hand, have been shown in Section IV to be comparable to a two-level bridge in a DAB configuration.

Measurements and control are more complex in a Q2LC than in a two-level bridge, but not more complex than in a conventional MMC, due to structural similarity.

In principle, a Q2LC structure offers scalability and can be extended to ultra-high dc voltages without encountering the gating or *dv/dt* problems impeding the extension of series-switch arrays. An ultra-high-voltage DAB-based dc transformer could be beneficial for dc fault isolation, which is one of the main obstacles impeding a multiterminal HVDC technology [9]. When the considered dc transformer is connected between two links of different dc voltages, dc fault at one side is not propagated to the other side [26]. Minimal current is fed into the dc fault and the dc fault appears as an ac fault to the non-faulted side of the dc transformer, where active power balance becomes the primary dc system stability concern.

VIII. Conclusion

The modular multilevel design of DAB converters was analyzed. The multilevel DAB structure is meant to serve medium and high voltage applications. The modular design facilitates scalability in terms of manufacturing and installation, and permits the generation of an output voltage with controllable *dv/dt*. The modular design is realized by connecting an auxiliary soft voltage clamping circuit across each IGBT of the series switch arrays in the conventional two-level DAB design. With auxiliary active circuits, series connected IGBTs effectively become series connection of half-bridge submodules (cells) in each arm, resembling a MMC structure. For each half-bridge cell, capacitance for quasi-square wave operation is significantly smaller than typical capacitance used in modular multilevel converters. Also, no bulky arm inductors are needed. Consequently, the footprint, volume, weight and cost of cells are lower. Four switching sequences were proposed and analyzed in terms of switching losses and operation aspects. A design method to size converter components was proposed and validated. Soft-switching characteristics of the analyzed DAB were found comparable to the case of a two-level DAB at the same ratings and conditions. Simulation and experimental results were presented to substantiate the concept.

The analyzed DAB converter provides additional flexibility for modulation index control, which enhances power flow controllability. Utilization of this control is beneficial in high voltage dc-dc transformers or solid-state ac transformers. For the former application, the DAB topology provides natural

TABLE V
PRIMARY-PHASE CURRENT WAVEFORM SECTIONS FOR $\omega T_t \leq \varphi \leq \frac{1}{3}\pi - \omega T_t$

$i_p(\theta)$	
For $0 \leq \theta \leq \omega_s T_t$	(34)
$\frac{V_{\mathrm{dc}p}}{3\omega_s L_s}\left(\frac{1}{\omega_s T_t}\theta^2 + (\rho-1)(\theta + \frac{2}{3}\pi - \frac{1}{2}\omega_s T_t) - \rho\varphi\right)$	
for $\omega_s T_t \leq \theta \leq \varphi$	
$\frac{V_{\mathrm{dc}p}}{3\omega_s L_s}\left((\rho+1)\left(\theta - \frac{1}{2}\omega_s T_t\right) + 2(\rho-1)\frac{\pi}{3} - \rho\varphi\right)$	(35)
for $\varphi \leq \theta \leq \varphi + \omega_s T_t$	
$i_p(\varphi) - \frac{\rho V_{\mathrm{dc}p}}{3\omega_s^2 L_s T_t}(\theta - \varphi)^2$	(36)
for $\varphi + \omega_s T_t \leq \theta \leq \frac{\pi}{3}$	
$\frac{V_{\mathrm{dc}p}}{3\omega_s L_s}\left((1-\rho)\left(\theta - \frac{2}{3}\pi - \frac{1}{2}\omega_s T_t\right) + \rho\varphi\right)$	(37)
for $\frac{\pi}{3} \leq \theta \leq \frac{\pi}{3} + \omega_s T_t$	
$i_p(\frac{\pi}{3}) + \frac{V_{\mathrm{dc}p}}{6\omega_s^2 L_s T_t}(\theta - \frac{\pi}{3})^2$	(38)
for $\frac{\pi}{3} + \omega_s T_t \leq \theta \leq \frac{\pi}{3} + \varphi$	
$\frac{V_{\mathrm{dc}p}}{3\omega_s L_s}\left((2-\rho)\theta + (2\rho-3)\frac{\pi}{3} + (\frac{1}{2}\rho - 1)\omega_s T_t + \rho\varphi\right)$	(39)
for $\frac{\pi}{3} + \varphi \leq \theta \leq \frac{\pi}{3} + \varphi + \omega_s T_t$	
$i_p(\frac{\pi}{3} + \varphi) - \frac{\rho V_{\mathrm{dc}p}}{6\omega_s^2 L_s T_t}\left(\theta - \varphi - \frac{\pi}{3}\right)^2$	(40)
for $\frac{\pi}{3} + \varphi + \omega_s T_t \leq \theta \leq \frac{2}{3}\pi$	
$\frac{V_{\mathrm{dc}p}}{3\omega_s L_s}\left((1-\rho)(2\theta - \pi - \omega_s T_t) + 2\rho\varphi\right)$	(41)
for $\frac{2}{3}\pi \leq \theta \leq \frac{2}{3}\pi + \omega_s T_t$	
$i_p(\frac{2}{3}\pi) - \frac{V_{\mathrm{dc}p}}{6\omega_s^2 L_s T_t}\left(\theta - \frac{2}{3}\pi\right)^2$	(42)
for $\frac{2\pi}{3} + \omega_s T_t \leq \theta \leq \frac{2\pi}{3} + \varphi$	
$\frac{V_{\mathrm{dc}p}}{3\omega_s L_s}\left((1-2\rho)\theta + (3\rho-1)\frac{\pi}{3} + \left(\rho - \frac{1}{2}\right)\omega_s T_t + 2\rho\varphi\right)$	(43)
for $\frac{2\pi}{3} + \varphi \leq \theta \leq \frac{2\pi}{3} + \varphi + \omega_s T_t$	
$i_p(\frac{2}{3}\pi + \varphi) + \frac{\rho V_{\mathrm{dc}p}}{6\omega_s^2 L_s T_t}\left(\theta - \varphi - \frac{2}{3}\pi\right)^2$	(44)
for $\frac{2}{3}\pi + \varphi + \omega_s T_t \leq \theta \leq \pi$	
$\frac{V_{\mathrm{dc}p}}{3\omega_s L_s}\left((1-\rho)\left(\theta - \frac{\pi}{3} - \frac{1}{2}\omega_s T_t\right) + \rho\varphi\right)$	(45)

dc fault isolation capability, which is mandatory for reliable multi-terminal HVDC networks. The enhanced modulation index control capabilities may facilitate design and control of three-port DAB converters for use in three-terminal solid-state ac transformers or three-port dc transformers.

The design of the ac transformer stage may be challenging, given harmonic energy is also transferred. For high power and high voltages, an acceptable compromise between power density and efficiency is needed.

APPENDIX

The primary-side phase current waveform sections for the Q2LC-based DAB for a half cycle are given as in Table V [Fig. 5(b)] for $\omega T_t \leq \varphi \leq \frac{1}{3}\pi - \omega T_t$.

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