A High-Power CMOS Class-D Amplifier for Inductive-Link Medical Transmitters

Virgilio Valente, *Member, IEEE*, Clemens Eder, *Member, IEEE*, Nick Donaldson, and Andreas Demosthenous, *Senior Member, IEEE*

***Abstract*—Powering of medical implants by inductive coupling is an effective technique, which avoids the use of bulky implanted batteries or transcutaneous wires. On the external unit side, class-D and class-E power amplifiers (PAs) are conventionally used, thanks to their high efficiency at high frequencies. The initial specifications driving this study require the use of multiple independent stimulators, which imposes serious constraints on the area and functionality of the external unit. An integrated circuit class-D PA has been designed to provide both small area and enhanced functionality, the latter achieved by the addition of an on-chip (PLL) a dead-time generator and a phase detector. The PA was designed in a 0.18-μm CMOS high-voltage process technology and occupies an area of 9.86 mm^2. It works at frequencies up to 14 MHz and 30-V supply and efficiencies higher than 80% are obtained at 14 MHz. The PA is intended for a closed-loop transmitter system that optimizes power delivery to medical implants.**

***Index Terms*—Class-D amplifier, dead time, high-power, inductive powering, integrated circuit, medical implant, power amplifier.**

I. Introduction

POWERING implanted biomedical devices via inductive coupling is an efficient and commercial technique, which avoids the use of transcutaneous leads that may cause infection and bulky implanted batteries that need regular surgical intervention for replacement [1]. Inductive powering requires the use of a power amplifier (PA) at the external unit to convert dc power, from a supply unit, into ac power that can be transferred across a weakly-coupled link to the internal unit. An illustration of an inductive power link for passive medical implants is shown in Fig. 1. The external unit consists of a modulator, which defines the stimulation parameters, an oscillator, which provides a carrier frequency, and a PA to drive the primary resonant network. On the implant side, the modulated high-frequency signal is picked up by a receiver resonant network and converted back to the original modulated signal via a rectifier and a voltage regulator. The power requirement of the implant dictates the power delivery capability of the external unit, with power specifications in the implant unit between tens of microwatts for pacemaker systems and up to 250 μW for more complex systems, which feature both stimulation and neural recording [1]. The overall efficiency of the power transmission depends on the efficiency of its individual components. The main contribution of losses in the power transmission is associated with the inductive link, which acts like a loosely-coupled transformer, where the coupling strongly depends on the distance between the coils [2], [3]. On the external unit side, class-D and class-E PAs are conventionally used thanks to their high efficiency at high frequencies [4]–[10].

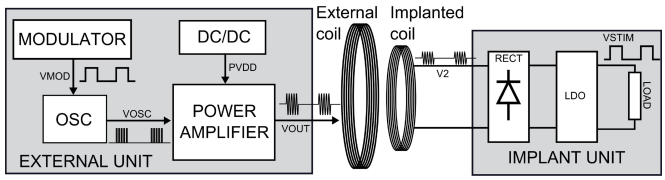

Fig. 1. Simplified architecture of a wireless power link for medical implants.

Class-D PAs offer more flexibility with respect to class-E counterparts. Wide frequency coverage can be achieved with class-D output stages without the need to optimize individual components for different frequencies as required in class-E PAs [11]. Additional features of class-D PAs include no strict 50% duty cycle, full-bridge operation (allowing for phase-controlled power stages [12]), and stagger tuning for bandwidth improvements [13]. The specific application of the study reported in this paper, requires efficient powering of a number of passive commercial stimulators (manufactured by Finetech Medical Ltd), with the aim of delivering independent stimulation patterns to different regions of the sacral and lumbar areas of the spinal cord of patients with partial or complete spinal cord injury. Table I summarizes the key specifications of the wireless powering system under development for multiple passive stimulators (see Fig. 1).

In order to provide constant voltage levels to the implant in a way that is independent of the coupling between the coils, supply voltage levels up to 30 V may be required for the transmitter unit under specific load conditions [14]. A feedback loop needs to be included in the external unit, in order to adjust the power delivered to the implant for different levels of coupling between the external and implanted coils [7], [14], [15] and adjust the carrier frequency to obtain optimal power transfer [16]. The application provides substantial challenges in terms of area and functionality of the external units. Most commercial

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TABLE I
SPECIFICATIONS OF THE SYSTEM FOR WIRELESS POWERING OF MULTIPLE PASSIVE RECEIVER UNITS

PARAMETER	nDMOS
Number of implant units	5
Carrier frequencies (MHz)	0.875–9
Implant voltage, VSTIM (V)	1–15
Implant coil size (mm)	25
External coil size (mm)	45–65
Implant power (W)*	200 μ–45 m
System efficiency	$>30\%$

*Estimated for each unit with a load impedance of 1 kΩ and a stimulation pulse duty cycle of 0.2.

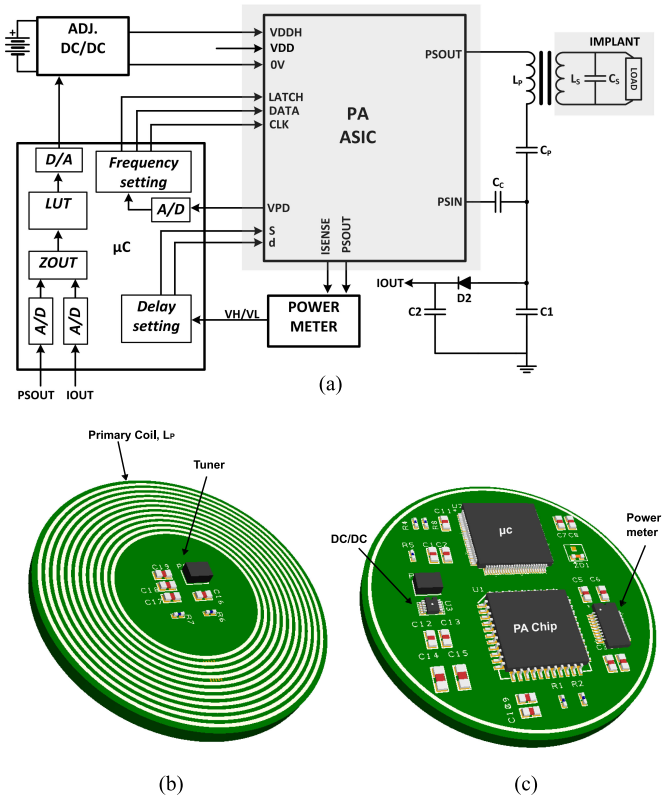

Fig. 2. Wireless closed-loop transmitter system with integrated PA. (a) System architecture. (b) Printed spiral primary coil and tuner. (c) PCB-coil-mounted transmitter system.

class-D fully integrated PAs or integrated drivers for half-bridge output stages are limited to frequencies up to a few hundreds of kilohertz and are not suitable for operation in the megahertz region. A custom integrated circuit class-D PA has, therefore, been designed to miniaturize the physical size of the external unit so that the complete circuit could be placed within the primary coil, without having to sacrifice functionality in addition to allowing easy interfacing with multiple passive implants. Fig. 2 shows the architecture and conceptual design of the wireless transmitter system, comprising of the PA, a power meter, a microcontroller, and a dc/dc converter [14], [17]. The full system will be mounted on the back of a printed spiral coil [see

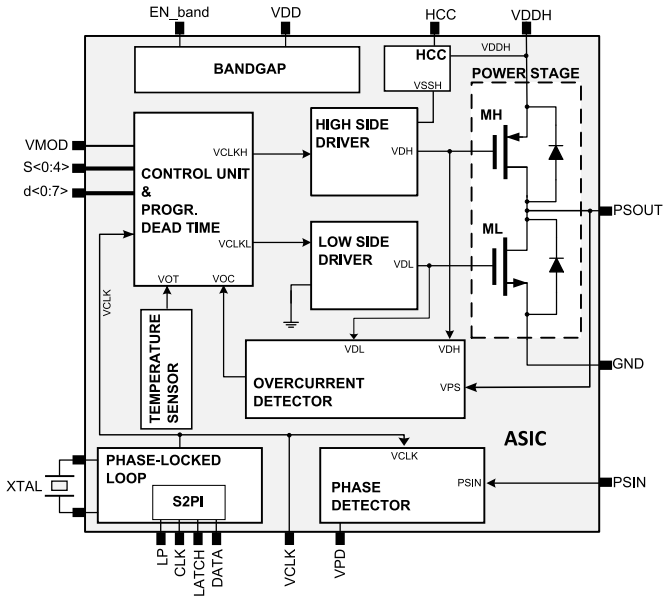

Fig. 3. Architecture of the integrated class-D PA.

Fig. 2(b)], whose size will dictate the overall dimensions of the system.

The focus of this paper is on the design of an integrated class-D PA, suitable for powering multiple passive implants for epidural stimulation. The application requires the PA to cover a range of operating frequencies between 0.9 MHz and 6 MHz. This range has been extended to 14 MHz, to cover the industrial-scientific and medical bands of 6.78 MHz and 13.56 MHz. The functionality of the PA has been greatly enhanced with respect to conventional commercial or discrete implementations by the addition of i) an on-chip nanosecond programmable delay line for accurate setting of the dead time, ii) a phase-locked loop (PLL) for the generation of a precise carrier frequency, and iii) a phase detector to assess the tuning between the carrier frequency of the PA and the resonant frequency of the tank network. This chip provides a unique and flexible platform for the design of miniaturize medical transmitter systems and the implementation of several feedback schemes that improve the efficiency of the inductive link. This paper is a development of [14] and presents the chip design and measured results from the fabricated samples.

The rest of this paper is organized as follows. Section II presents a detailed description of the circuit design of the PA building blocks. Section III reports on measured performance of the fabricated chip. Section IV concludes this paper by highlighting key results, comparison with equivalent developments, and future developments.

II. PA ASIC DESIGN AND SPECIFICATIONS

The architecture of the integrated class-D PA is shown in Fig. 3. Its core is the power stage consisting of a n-type low-side DMOS transistor, *ML,* and a p-type high-side DMOS transistor, *MH*, driven by a low-side and a high-side driver, respectively. The inputs to the drivers are two non-overlapping clock signals,

TABLE II
SPECIFICATIONS OF POWER STAGE DMOS TRANSISTORS. V_{T} IS THE TRANSISTOR THRESHOLD VOLTAGE, W IS THE DEVICE WIDTH, R_{on} IS THE ON-RESISTANCE, $V_{\mathrm{DS,max}}$ IS THE DRAIN-SOURCE BREAKDOWN VOLTAGE, C_{GG} IS THE GATE CAPACITANCE, AND A IS THE TRANSISTOR AREA.

PARAMETER	nDMOS	pDMOS
V_{T} (mV)	867	866
$V_{\mathrm{DS,max}}$ (V)	40	40
W (mm)	120	204
R_{on} (Ω)	0.2	0.2
C_{GG} (pF)	213	304
A (mm^2)	0.6	1

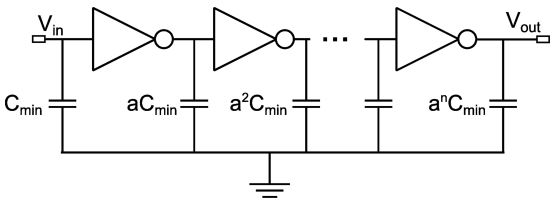

Fig. 4. Low-side driver consisting of a number of tapered buffer stages.

generated by an on-chip programmable delay line. This allows the dead-time to be accurately set and adjusted, which is conventionally either fixed [18] or adjustable via an external resistor [19], [20].

Protection circuits are included in order to detect excess voltage and current that could damage the DMOS devices and additionally monitor the operational temperature of the power stage. The signals generated by the protection circuits are managed by a control unit, which sets the normal operation of the power stage and adjusts the power stage operation in case of overcurrent or overtemperature events.

A. Power Stage and Drivers

The DMOS transistors of the power stage in a class-D PA are used as switches. In theory, therefore, the amplifier can reach an efficiency of 100%. In practice, however, the efficiency is reduced by the finite on-resistance of the switches and the finite switching transition time. In order to optimize efficiency, the transistors must be scaled so that the contribution to the losses due to their on-resistance and gate capacitance (which are inversely proportional) are minimized [21]. Table II summarizes the specifications of the DMOS transistor switches used in the design.

The current capability of the drivers must be large enough to satisfy the current requirements of the input capacitance of the power stage, as reported in Table II. Designs of DMOS drivers can be implemented with gate current injection drivers [22], [23] or high current capability voltage buffers. The former solution needs the use of protection diodes whose performance is not always satisfactory in integrated form. An architecture consisting of tapered buffers was, therefore, selected to increase the current drive of the last stage of the driver, by successive scaling of the transistor area of each stage [24]. Fig. 4 shows the architecture of the low-side driver, where C_{min} is the input capacitance of the first stage, a is the taper factor, and n is the number of stages.

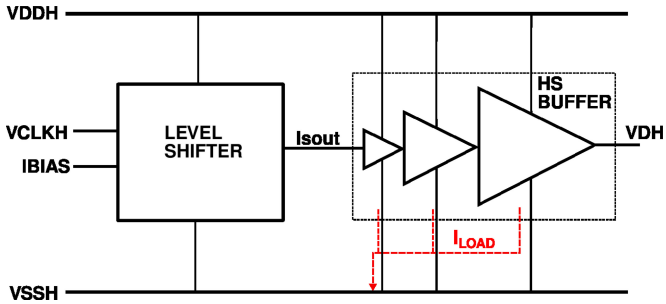

Fig. 5. Block diagram of the high-side driver.

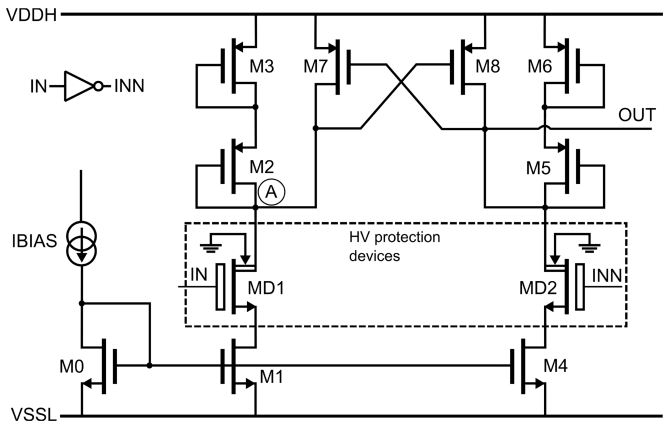

Fig. 6. Schematic of the level shifter.

The design approach of the tapered buffers can focus on minimization of the propagation delay or minimization of the number of stages [24]. The PMOS–NMOS ratio of the first inverter in the buffer, $W_{\mathrm{p}}/W_{\mathrm{n}}$, was set to 9 μm/2 μm, with $L_{\mathrm{n}} = L_{\mathrm{p}} = 0.5$ μm. This results in C_{min} equal to 31.8 fF. With a load capacitance, $a^{\mathrm{n}}C_{\mathrm{min}}$ equal to 220 pF (gate capacitance of *ML*), the capacitance ratio is $a^{\mathrm{n}} = 6700$. The low-side driver was designed to have a propagation delay (*tp*) of 5 ns and rise and fall times less than 3.5 ns (10% of pulse width at 14 MHz). This results in three stages with a tapering factor of 30. The high-side driver consists of a level shifter and a tapered buffer as illustrated in Fig. 5. The latter was designed following the same procedure used for the low-side driver. The function of the level shifter is to track the high-voltage supply, *VDDH*, which can swing to voltages up to 30 V and clamp the output voltage to 5 V below *VDDH*, which corresponds to the maximum gate-source voltage of the high-side DMOS transistor *MH*.

The level shifter consists of two complementary clamping branches, formed by transistors *M*1–*M*3 and *M*4–*M*6 and a latch (*M*7, *M*8) for fast switching, as shown in Fig. 6. The clamping sections are biased with a 270-μA current, *IBIAS*, and transistors *M*2–*M*3 and *M*5–*M*6 are scaled to provide a voltage drop of 2.5 V each. High-voltage transistors *MD*1 and *MD*2 are used to protect the low-voltage current-mirroring transistors *M*1 and *M*2, when the voltage at point *A* swings beyond 5 V.

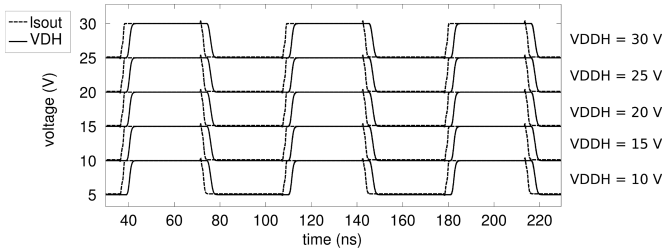

Fig. 7. Simulated transient performance of the high-side driver at 14 MHz and different values of the supply voltage, *VDDH*.

TABLE III
RESULTS OF 100 MONTE CARLO SIMULATIONS OF LOW-SIDE DRIVER (LSD) AND HIGH-SIDE DRIVER (HSD) PROPAGATION DELAYS (*tplh* AND *tphl*) AND RISE AND FALL TIMES (*tr* AND *tf*) AT 14 MHZ

PARAMETER	LSD	HSD
tplh (ns) $\pm$ std (ps)	2.4 ± 25.7	4.4 ± 54
tphl (ns) $\pm$ std (ps)	2.5 ± 26.6	4.8 ± 50
tr (ns) $\pm$ std (ps)	0.92 ± 10	1.7 ± 27
tf (ns) $\pm$ std (ps)	0.96 ± 10	2 ± 30

The delays of the HSD was not found to vary substantially with *VDDH*.

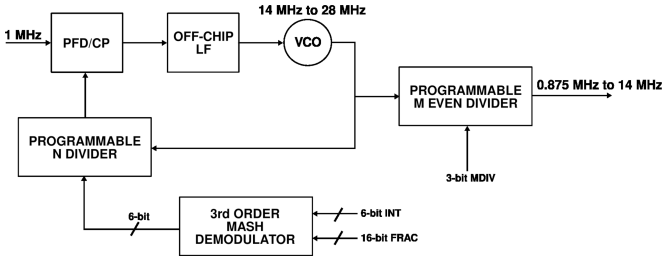

Fig. 8. Architecture of the *N*-fractional PLL.

The simulated transient performance of the high-side driver at 14 MHz for different values of the supply voltage, *VDDH*, is shown in Fig. 7. The simulated performance of the drivers is summarized in Table III.

B. PLL

The PA is equipped with an on-chip fractional-*N* PLL, to set the operational clock to a precise frequency with a 1-kHz resolution. The architecture of the PLL is shown in Fig. 8. The PLL frequency range is between 0.875 MHz and 14 MHz.

The PLL comprises a phase/frequency detector (PFD), a charge pump (CP), an off-chip loop filter (LP), and a voltage-controlled oscillator (VCO). The PFD compares the phase between the output of the VCO and a scaled version of the input reference frequency. The CP adjusts the tuning voltage of the VCO in order to minimize the frequency difference. The frequency resolution of the PLL is set by a 6-bit integer value and a 16-bit fractional value. The PLL is interfaced to a microcontroller via an on-chip serial peripheral interface (SPI). The PLL frequency is set by three inputs, *CLK*, *DATA*, and *LATCH*,

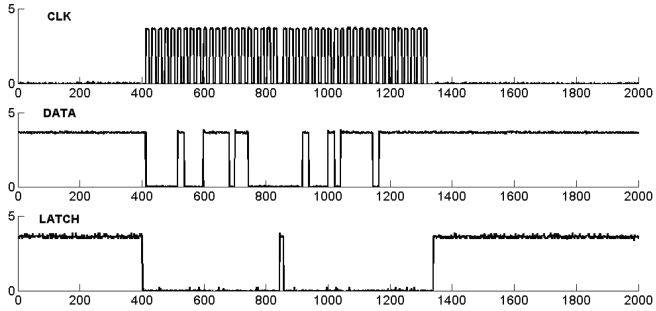

Fig. 9. Programming of the PLL for frequency setting.

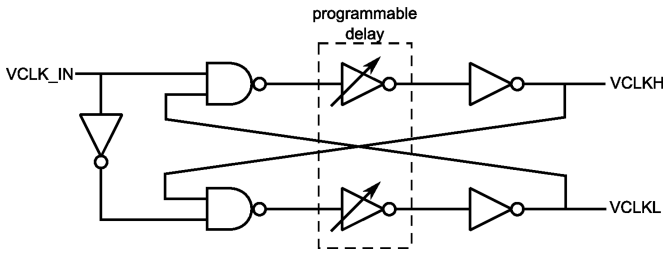

Fig. 10. Nonoverlapping clock generator with programmable delay line for accurate setting of dead-time.

generated by a microcontroller. An example of these digital signals is shown in Fig. 9.

The SPI comprises two 16-bit registers. At a high-low transition of the *LATCH* signal, the *DATA* is clocked into the first register (*R*0). At the second transition of the *LATCH* signal, *DATA* is written onto the second register. The first register comprises i) 1 bit used to enable/disable the PLL, ii) 3 bits to set the value of *MDIV* between divide-by-2 and divide-by-16, iii) 1 bit to enable the charge state machine controlling the CP, iv) 1 bit to enable the sigma–delta modulator for fractional operation, v) 6 bits to set the integer values *INT*, and vi) 4 unused bits. The second register consists of 16 bits, *FRAC*, which set the PLL fractional value.

The PLL frequency is set by the following equation:

$$f_{\mathrm{PLL}} = \frac{f_{\mathrm{REF}} \cdot (INT + \frac{FRAC}{2^{16}})}{MDIV} \tag{1}$$

where f_{REF} is the 1-MHz crystal (XTAL) reference frequency, *INT* is the 6-bit integer of the PLL, *FRAC* is the 16-bit fraction, and *MDIV* is the post-VCO divider. The VCO frequency is constrained between 14 MHz and 28 MHz and divided to obtain a PLL output frequency range between 0.875 MHz and 14 MHz. The PLL resolution is 1 MHz/$2^{16} = 15.258$ Hz.

C. Programmable Delay Line for Dead-Time Adjustment

The operation of the class-D PA relies on the synchronous switching of the low-side and high-side switches that form a half-bridge structure [21]. At high frequencies, the power loss during switching transitions contributes substantially to the total power loss [25]. In order to increase the efficiency of the class-D PA, a technique based on the use of a dead-time between the

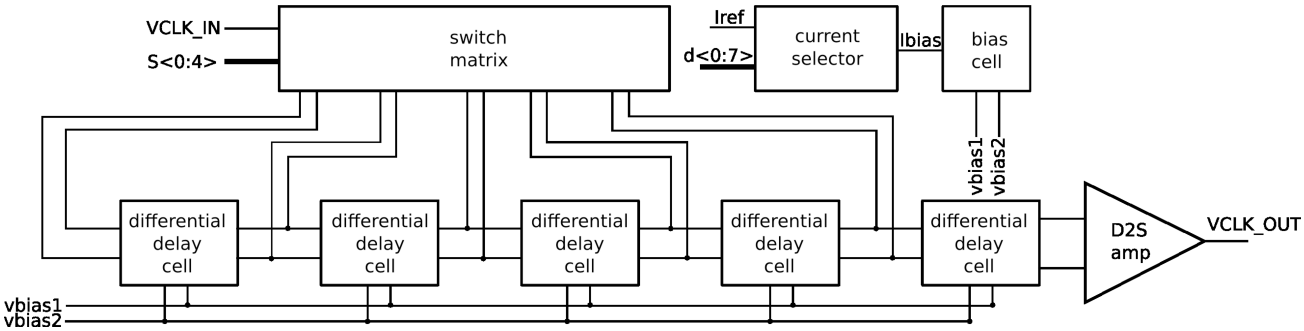

Fig. 11. Architecture of a 5-tap delay line.

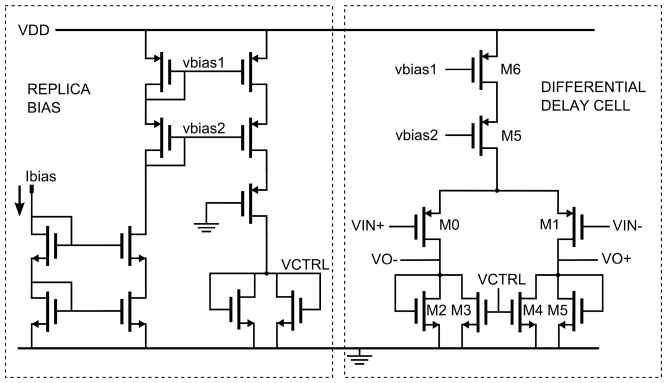

Fig. 12. Schematic of a differential delay cell with replica biasing circuit.

TABLE IV
SIMULATED DISCRETE BIAS CURRENTS, *Ibias*, AND DEAD-TIMES, *dt*, GENERATED BY THE PROGRAMMABLE DELAY LINE

	Ibias (μA)	**S0**	**S1**	**S2**	**S3**	**S4**
d7	93	9	12	15	17	21
d6	83	10	14	18	22	26
d5	60	11	16	21	26	31
d4	48	12	18	24	30	36
d3	39	13	20	27	34	41
d2	33	14	22	30	38	46
d1	27	15	24	33	42	51
d0	24	16	26	36	46	56

All delays are in *ns*.

switching of the low-side and high-side switches can be used [21]. A dead-time avoids both switches being on simultaneously causing large surge currents and potential damage. If the dead-time is too long, however, the intrinsic body diode of the switches turns on, resulting in larger losses than the switch conduction losses, due to the high diode reverse recovery charge. Conventional class-D PAs are designed with a fixed dead-time, which is set to be large enough to cover the whole operational range [22], [26]–[28]. At frequencies in the megahertz region, the dead-time has a substantial impact on the efficiency of the PA, and the optimum dead-time varies with frequency of operation and supply voltage [14]. The dead-time is generated by a non-overlapping clock generator with a programmable delay line, as shown in Fig. 10.

Each programmable delay is implemented with the architecture in Fig. 11. The programmable delay comprises five differential-delay cells in series. A 5-bit switch matrix circuit selects which delay cell *VCLKL_IN* is connected to by setting the control bit, $S<0{:}4>$. The delay of each cell is controlled by a bias current, *Ibias*, which is defined by an 8-bit current selector, $d<0{:}7>$.

Each delay cell is implemented as a differential amplifier with symmetric loads [29], as shown in Fig. 12. The symmetric loads combine two parallel NMOS transistors in order to linearize the current-to-voltage (*I–V*) relationship for different values of the bias current. The delay contribution of each cell is then given by an *RC* time constant, where *R* is the resistance of the symmetric loads (*M*2–*M*5) seen at the drains of *M*0 and *M*1, and *C* is the cell load capacitance, which equals the input capacitance of the following stage (i.e., the gate capacitance of transistors *M*0 and *M*1).

The resistance *R* is controlled by the bias voltage *VCTRL*. This voltage is generated by the replica bias cell of Fig. 12, by applying *Ibias* to a symmetric load via a cascode current mirror. By changing *Ibias*, *VCTRL* is changed and, hence, the *R* of the differential cell. The delay of each cell is proportional to *Ibias*. This is set by a current selector, which consists of a series of eight switched cascode current mirrors, which scale an input current *Iref* to a specific bias point, resulting in a specific delay for each differential cell, according to which control bit, $d<0{:}7>$, is selected. The differential signals are converted to a single-ended clock signal by a self-biased differential-to-single amplifier (D2S amp) and a logic buffer is used to clean the edges of the output signal. The nominal contribution of D2S amp to the overall delay of the delay line is about 6 ns. The simulated transient performance of the delay line is summarized in Table IV.

D. Control Unit and Protection Circuits

A state machine (control unit) manages the normal switching operation of the power stage and provides protection in case of detected overtemperature or overcurrent events. The state machine consists of seven states (*S*0–*S*6), as shown in the flow diagram in Fig. 13. During normal operation, the control circuit

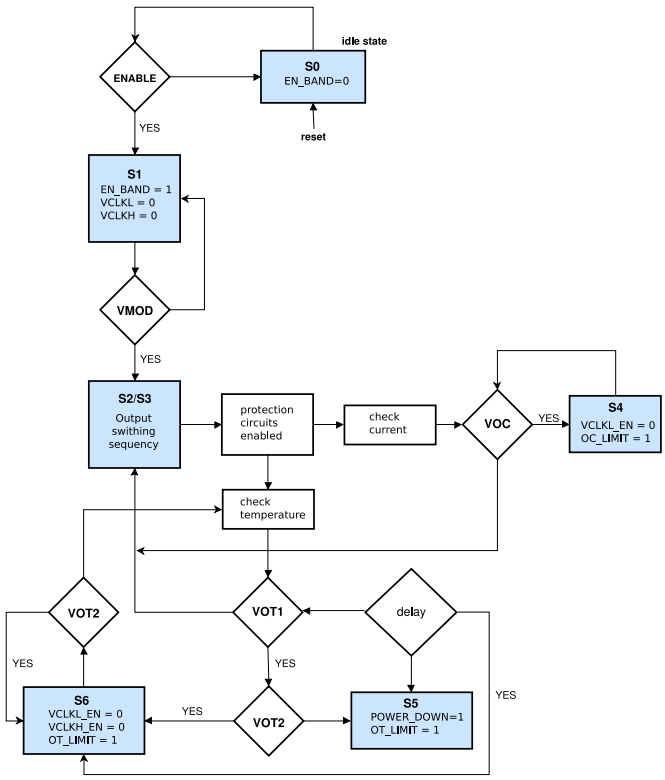

Fig. 13. Flowchart of the operation of the control unit.

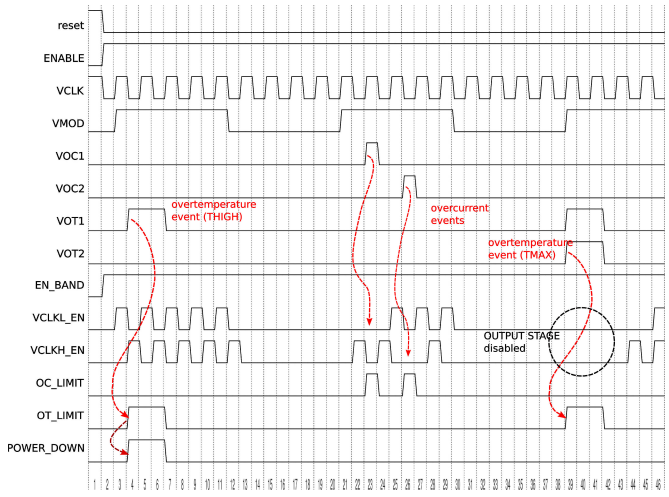

Fig. 14. Timing diagram of the operation of the control unit under normal, overcurrent detection, and overtemperature detection mode.

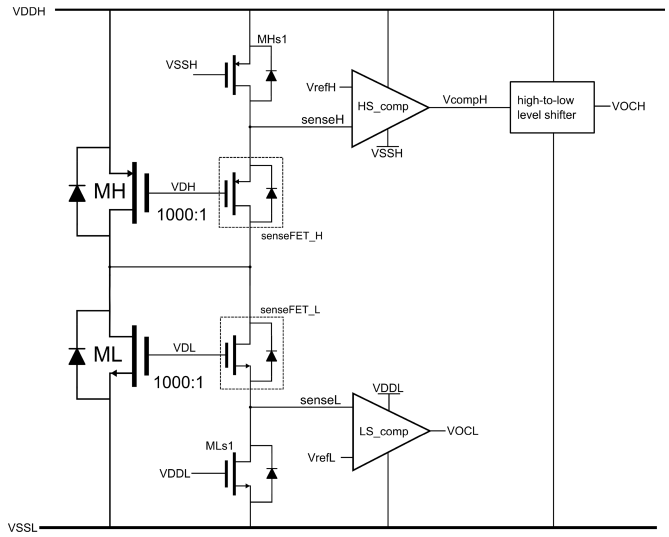

Fig. 15. Schematic of the overcurrent detection circuit.

operates between states *S*2 and *S*3 and provides two enable signals to the output stage: *VCLKL_EN* and *VCLKH_EN*.

If an overcurrent or overtemperature event is detected during the output switching sequence, the control unit exits states *S2* and *S3* in order to provide protection to the output stage. In the case of an overcurrent event, the control unit instantly disables the output device associated with the event occurrence. If an overtemperature event is detected, the control unit checks if the temperature has exceeded the warning threshold (*THIGH*). In this case, a *POWER_DOWN* flag is enabled and the power can be decreased for a fixed delay. If the maximum temperature threshold (*TMAX*) is also exceeded, the output stage is disabled for a short time until the temperature is below *TMAX*. Fig. 14 shows the control-unit timing diagram during normal operation, overcurrent, and overtemperature events.

One major cause of failure of the power stage is overcurrent. The power stage transistors must be operated within the safe operating region (SOA), given by the manufacturer's specifications [21]. The SOA describes an area on the drain current versus gate voltage (or drain voltage versus gate voltage). In case of failure due to short circuit or excessive power, the operation of the transistors will move outside the SOA and failure will occur within a time frame in the order of μs to ms. In order to prevent this occurrence, the chip is equipped with an overcurrent detection circuit. It is based on the use of one low-side and one-high side sensing transistors known as senseFETs [30], [31]. A senseFET is a single finger of the multifinger DMOS structure and is placed between the nDMOS and pDMOS transistors, in order to track variations due to temperature changes. Several senseFETs can also be distributed across the DMOS transistors to capture the average current of the transistor more accurately [32].

The architecture of the overcurrent protection circuit is shown in Fig. 15. When either power transistor (*ML* or *MH*) is conducting, a small amount of current, related to the current flowing through the power transistors by a ratio k (1000 in this implementation), flows through the senseFET. This current is then channeled to a sensing resistor (a transistor operating in the triode region, *MLs*1, and *MHs*1) to generate a sense voltage. By scaling the senseFETs and the sensing resistors equally, the sense voltage will be approximately half the voltage across the power transistor. This voltage can then be applied to a comparator, which compares this voltage to a reference voltage relating to the SOA of the power transistors. The output of the overcurrent detection circuit is two control signals: *VOCL* and *VOCH*. When either of these signals goes high (5 V), an overcurrent event has

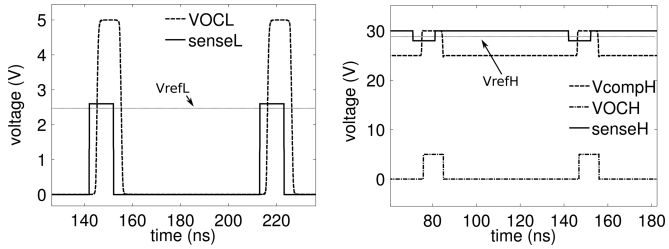

Fig. 16. Transient response of the LS_comp (left) and HS_comp (right) to 10-ns square pulse at a frequency of 14 MHz. *VrefL* and *VrefH* were set to 2.5 and 28.5 V, respectively.

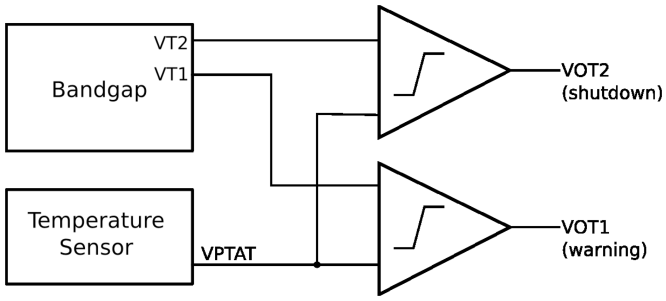

Fig. 17. Schematic of the overtemperature detection circuit.

been detected. The comparators comprise a preamplifier, a decision circuit, and an output buffer. The high-side comparator (HS_comp) is implemented using deep *N*-well isolated 5-V transistors. The output of HS_comp is referenced to *VDDH*, such that a logic "1" is represented by the voltage *VDDH*-5V and a logic "0" by the voltage *VDDH*. A high-to-low voltage shifter is used to translate these voltage levels to low voltages compatible with the control logic circuit [22]. The current limits for safe operation are set to $ILIML = 7.5$ A and $ILIMH = 7$ A for the low-side and high-side switches, respectively. This occurs when the gate-source voltage of the switches is 5 V and its drain-source voltage 2.5 V. The reference voltages of the low-side comparator (LS_comp) and HS_comp, *VrefL* and *VrefH*, are set to 2.5 V and 28.5 V, respectively.

Fig. 16 shows the transient simulated behavior of the LS_comp and HS_comp, in response to a 10-ns square pulse at a frequency of 14 MHz. The propagation delay, i.e., the time difference between the input crossing the reference voltage and the output changing state, of the LS_comp is estimated to be approximately 2.36 ns. The LS_comp time resolution is in the order of 1 ns, i.e., the comparator is able to detect overcurrent events lasting for a minimum of 1 ns. The propagation delay of the HS_comp is estimated to be 2.9 ns and its time resolution to be approximately 1 ns.

The operating temperature range of the power switches is $-40\,^{\circ}$C to 125 °C. Operation outside this range will result in device destruction. During operation, the temperature of the devices will increase, in proportion to the increase of power generated and frequency. The overtemperature detection circuit in Fig. 17 prevents the power stage from overheating by detecting when the temperature has reached a warning level and when the temperature has reached the maximum rating.

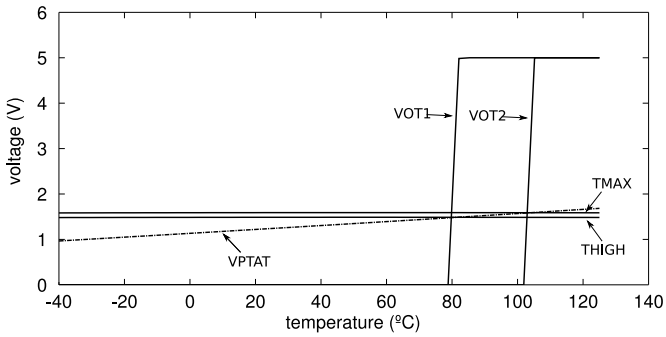

Fig. 18. Simulated dc performance of the temperature sensor.

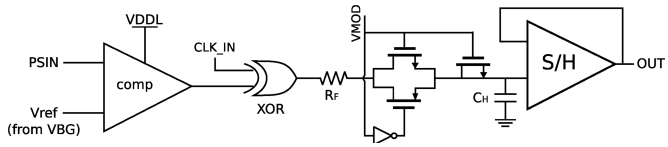

Fig. 19. Architecture of the XOR-based phase detector.

The circuit consists of a temperature sensor, implemented as a proportional to absolute temperature (PTAT) reference voltage generator, which generates a voltage *VPTAT* with a temperature coefficient of approximately 4 mV/°C, and a bandgap circuit, which generates two temperature-independent reference voltages, *VOT1* and *VOT2*, serving as threshold to detect a warning temperature ($T > 80$ °C) and a shutdown temperature ($T > 105$ °C). Two comparators are used to generate the control signals used by the control logic for overtemperature event management. The simulated dc performance of the overtemperature detector is reported in Fig. 18.

E. Phase Detector

The chip is equipped with a phase detector, which compares the phase of the output current, flowing through the tank circuit, with the phase of the clock signal. The architecture of the phase detector is shown in Fig. 19. *PS_IN* is converted to a square pulse by a fast latched comparator with a reference voltage equal to *VDDL*/2. The phase difference between the output of the comparator and the clock signal, *CLK_IN*, is obtained by an XOR gate, which returns a pulse whose width represents the phase difference between the two signals.

The output of the XOR gate is then filtered by $R_{\rm F}$ and $C_{\rm H}$ and converted to a dc signal proportional to the phase difference. The dc voltage is stored in $C_{\rm H}$ by a sample and hold circuit controlled by the modulation signal *VMOD*. This allows the output of the phase detector to be available, even when the power stage is OFF ($VMOD = 0$ V).

III. Measurements

The chip was designed in a high-voltage power management 0.18-μm CMOS technology (XFAB XP018). The chip photograph is shown in Fig. 20 with the various system blocks labeled. The chip consists of 128 input/output (I/O) pads. In order to prevent damage to the I/O pads connected to the power stage, due

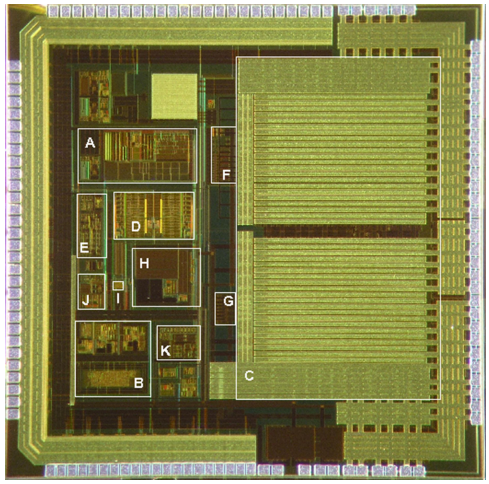

Fig. 20. Chip Microphotograph: (A) Bandgap; (B) PLL; (C) power stage; (D) delay line; (E) overcurrent detector; (F) high-side driver; (G) low-side driver; (H) phase detector; (I) control unit; (J) overcurrent detector; (K) regulator.

TABLE V
ASIC SUMMARY OF PERFORMANCE

Fabrication Technology	0.18-μm High-Power CMOS 5M + THKMET
Area (including 128 pads)	9.86 mm^2
VDDH	5–30 V
VDDL	5 V
POUT @ 5V	1 W
Efficiency @ 14 MHz	$>$80%
Clock frequency range	0.875–14 MHz
Clock frequency resolution	1 kHz
Dead-time range	9.5–48.5 ns
Dead-time resolution	1 ns

to their limited average current capability, 20 pads were used for the high-voltage supply, (*VDDH*), six pads for the amplifier output, (*PSOUT*), and 16 for the high-voltage ground, (*VSSL*). Table V summarizes the performance of the amplifier chip.

The chip performance was evaluated by testing the behavior of individual sub-blocks as described below.

A. PLL

The PLL performance was assessed by measuring the frequency of the PLL output, *PLL_CLK*, with a counter (Agilent 53131A) and comparing it to the expected value, calculated with (1) for both integer and fractional mode. The PLL reference frequency was set by a 1-MHz external crystal oscillator (Fox, FXO-HC736R) and the PLL frequency was programmed by a microcontroller (Texas Instruments, MSP430).

In integer mode, the clock frequency was measured by varying the *INT* input between 14 and 28, and setting the *MDIV* input to divide-by 2, 4, 6, and 16. Fig. 21 shows the linearity of the PLL output frequency versus integer code, when the VCO output divider is set to the minimum ($MDIV = 2$) and maximum ($MDIV = 16$) division ratio. To test the factional mode, the PLL frequency was set to a number of fractional frequencies, e.g., 6.78 MHz and 13.56 MHz. The measured PLL clock frequency

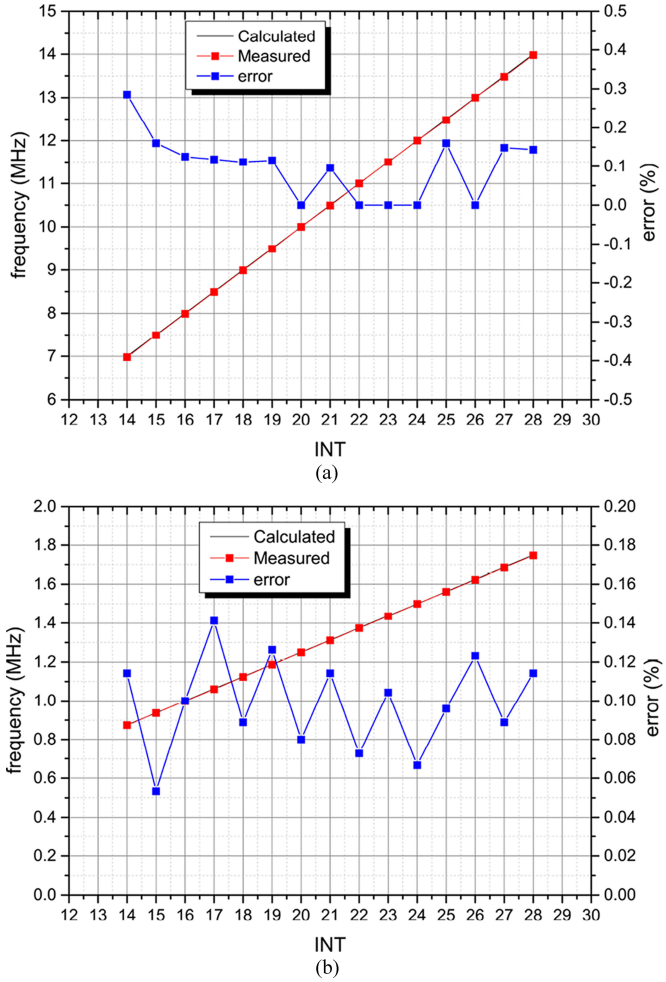

Fig. 21. Measured linearity of the PLL in integer mode with *MDIV* set to (a) 2 and (b) 16.

was within 0.3% of the expected values, in integer mode, and within 0.7% in fractional mode.

B. Delay Line

The delay line performance was assessed by measuring the dc performance of the current selector (as a test structure biased by an off-chip current) and the delay between the delay line outputs, *VCLKL* and *VCLKH*, on an oscilloscope (Agilent MSO6104A), for different values of the control bits *S* and *d*.

Fig. 22 shows the simulated and measured output current of the current selector of a typical chip for different values of the control bits, $d<0:7>$. The current selector is biased by an external 3-μA current and the output current is measured as a voltage across a 51-Ω resistor. The measured output current values are within 6% of the simulated ones (reported in Table IV). By changing the control bits *d* and *S*, the delays reported in Fig. 23 are obtained.

The measured dead-time ranges between 9.5 ns and 48.5 ns at 2 MHz. This range depends on the dynamic range of the differential delay cell. The lower end of the range can be extended by decreasing the size of the input differential pair (in

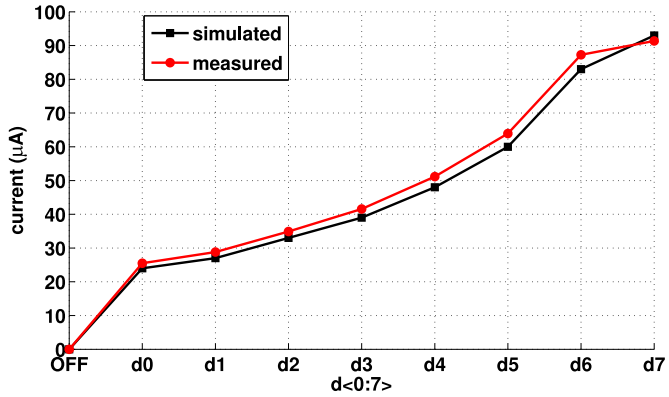

Fig. 22. Measured and simulated dc performance of the current selector tested with an external reference current of 3 μA on a typical chip.

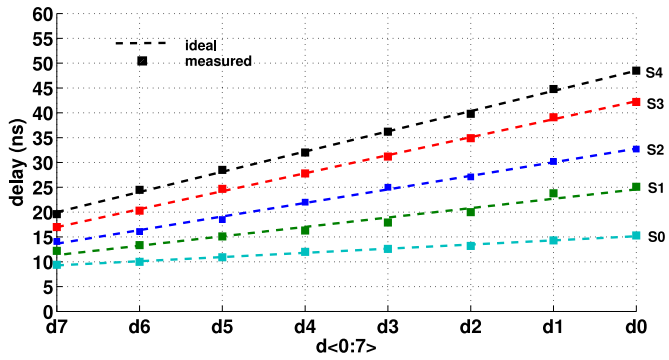

Fig. 23. Measured and ideal delays for different selection of the control bits *d* and *S* for a typical chip. The dashed lines represent the ideal trend lines and the dots represent the measured values.

Fig. 12) or increasing the bias current, although this reduces the value of the maximum achievable delay, which is inversely proportional to the square root of the bias current. The upper end of the delay range can be extended by adding additional cascaded stages of differential cells, each contributing equal delay. The minimum measured dead-time step is approximately 1 ns. Fig. 24 shows an oscilloscope snapshot of the output of the nonoverlapping clock generator at 2 MHz. The inset figures show the dead-time between the two clocks, when the minimum and maximum delays, of 9.5 ns and 48.5 ns, are used.

The rise/fall times and propagation delays of the clock signals were measured at 2 MHz and at minimum delay (*d*7*S*0). For the low-side clock signal, *VLCKL*, the rise/fall times were 4.7 and 2 ns, respectively, and the propagation delay was 17.5 ns for the high-low transition and 11.4 ns for the low-high transition. For the high-side clock signal, *VLCKH*, the rise/fall times were 4.4 ns and 2 ns, respectively, and the propagation delay was 20 ns for the low–high transition and 8.4 ns for the high-low transition.

C. Phase Detector

The performance of the phase detector was assessed by applying a test signal to the *PSIN* input and measure the output dc voltage, *VPD*, at different phase delays between the clock signal and the input signal. The minimum and maximum output voltage was measured by applying the on-chip clock signal and the inverted clock-signal to the *PSIN* input, respectively.

This resulted in a measured minimum *VPD* of 0.9 V (simulated 0.7 V), corresponding to in-phase signals, and a maximum *VPD* of 4.32 V (simulated 4.83 V) corresponding to a 180° phase. The range of *VPD* for a phase shift between 0° and 180° is reported in Fig. 25. The larger discrepancy between measured and simulated results occurs at the endpoints, however it is the minimum values of the phase that are of interest, not the absolute values.

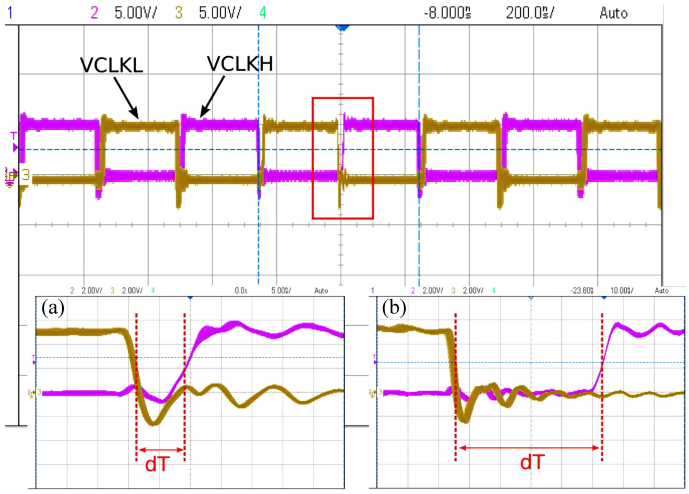

Fig. 24. Nonoverlapping clocks, *VCLKL* and *VCLKH*, generated by the programmable delay line from the clock signal, *VCLK*. The inset figures illustrate the delay between the clocks for (a) the minimum dead-time of 9.5 ns and (b) the maximum dead-time of 48.5 ns.

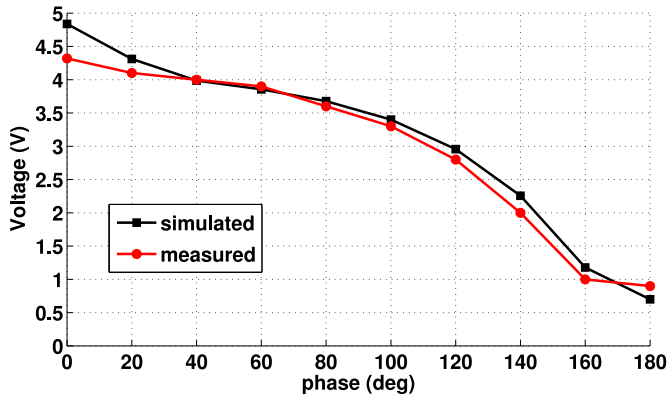

Fig. 25. Measured and simulated output voltage of the phase detector for different values of the phase difference between the clock signal and a sinusoid test signal applied to the input of the phase detector, *PSIN*.

D. Output Stage

The performance of the output stage was assessed with an *LC* tank load, as shown in Fig. 2(a). A trimmer capacitor was used to tune the *LC* tank to resonance at the operating frequency. The coil in the tank network consisted of a flat spiral inductor of eight turns of copper wire, 70 mm in diameter, resulting in an inductance of 7.4 μH, a *Q* of 29 and an effec-

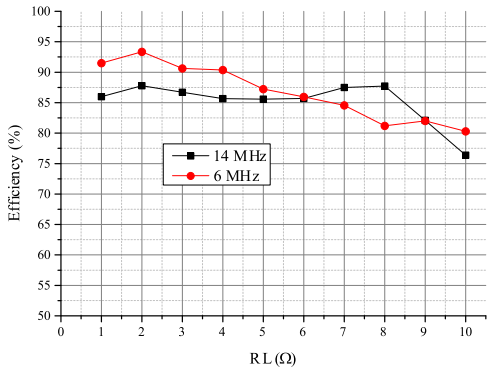

Fig. 26. Measured efficiency versus load resistance of the class-D output stage at 6 and 14 MHz and $VDDH = 5$ V.

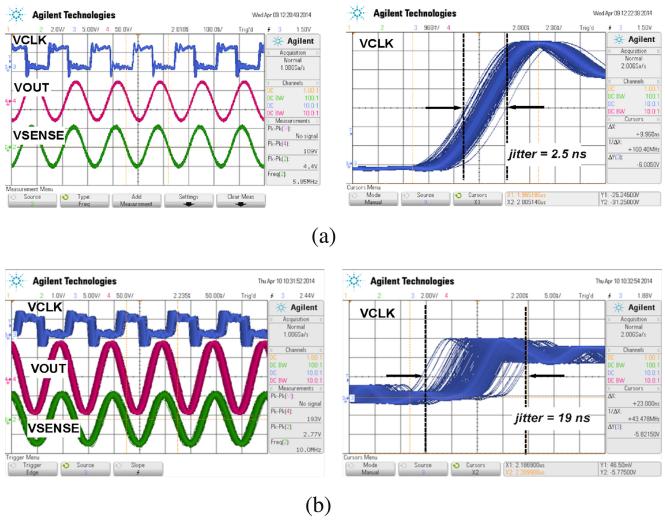

Fig. 27. Operation of the chip during power transmission to a 5-Ω load at $VDDH = 5$ V and at a frequency of operation of (a) 6 MHz and (b) 10 MHz.

tive series resistance (ESR) of 4.3 Ω [14]. The output power and the efficiency of the PA were estimated by measuring the output current, I_L, via a current transformer (1 : 50) placed in series with the tank circuit and calculating the equivalent output resistance, at resonance, from the $1/I_L$ curve for different values of load resistance, dead-time, and carrier frequency. The load resistance, *RL*, was varied between 1 Ω and 10 Ω, using a trimmer potentiometer. The equivalent output resistance accounts for the coil ESR, the on-resistance of the power switches, and the resistance of the printed-circuit-board (PCB) tracks. Optimal dead-time was selected as the delay at which the output power was maximized.

The chip is capable of delivering up to 1 W of power to a 5-Ω load, when operated with a 5-V supply, and more than 30 W, when operated with a 30-V supply, with efficiencies higher than 80% at 14 MHz. These levels are achieved without power modulation (*VMOD* is always ON). Fig. 26 shows the measured efficiencies of the class-D output stage at frequencies 6 MHz and 14 MHz and a supply voltage of 5 V.

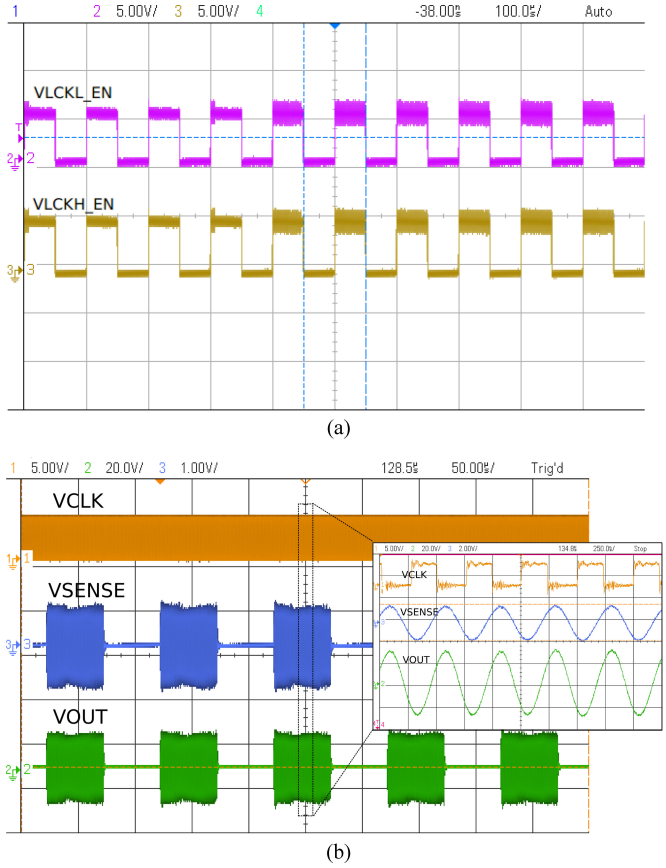

Fig. 28. Measured performance of the PA at 6 MHz clock frequency and a modulation signal, *VMOD* running at 10 kHz.

The next section describes how the output power can be modulated using the *VMOD* input. Fig. 27 shows the operation of the chip during power transmission at 6 and 10 MHz. The peak-to-peak tank voltage, *VOUT*, measured across the coil at resonance is approximately 100 and 190 V, respectively. The clock jitter was measured on the oscilloscope to be approximately 2.5 ns and 19 ns at 6 and 10 MHz, respectively.

E. Control Unit and VMOD

The two enable signals, *VCLKL_EN* and *VCLKH_EN* are AND'ed with the nonoverlapping clock signals, *VCLKL* and *VCLKH,* and applied to the inputs of the low- and high-side drivers. This allows the power stage to operate at a frequency determined by the clock signals modulated by the modulation signal *VMOD*. The output stage was loaded with a tank network (as shown in Fig. 3), resonating at 6 MHz. The clock frequency was set to 6 MHz, the supply voltage to 5 V, and the modulation signal *VMOD* was switched at a frequency of 10 kHz and a 50% duty cycle. This results in an average power of 500 mW delivered to the load.

Fig. 28(a) shows the enable signals, *VCLKL_EN* and *VLCKH_EN*, generated by the control unit. These signals enable the output stage according to *VMOD*, during normal operation. Fig. 28(b) shows the measured clock signal, *VCLK*, the tank voltage, *VOUT,* and the voltage across the sensing capacitor,

TABLE VI
COMPARISON WITH COMMERCIALLY AVAILABLE DEVICES FOR WIRELESS POWER TRANSMISSION APPLICATION. $R_{\rm on}$ IN THE OUTPUT RESISTANCE OF THE PA AND $f_{\rm XTAL}$ IS THE FREQUENCY OF THE EXTERNAL CRYSTAL OSCILLATOR NEEDED TO SET THE PA CARRIER FREQUENCY

PARAMETER	TRF7960	MLX90130	IDSR14AB	MAX5064	Si8244	This work
Integrated PA	yes	yes	yes	only drivers	only drivers	yes
Carrier frequency (MHz)	3.39/6.78/13.56	13.56	13.56	1	8	0.9–14
Integrated dead-time regulator	no	no	no	yes	yes	yes
Dead-time range (ns)	n/a	n/a	n/a	16–95	0.4–1000	9.5–48.5
Max output power (W)	0.1 or 0.2	0.317	0.8	n/a	n/a	36
VDDH max (V)	5	5.5	3.6	125	1.5k	30
R_{ON} TX (Ω)	8	8	n/a	n/a	n/a	0.2
f_{XTAL} (MHz)	13.56	27.12	13.56 or 27.12	n/a	n/a	1

VSENSE, representing the output current, when the output power is modulated by *VMOD* at a frequency of 10 kHz.

IV. CONCLUSION

An integrated class-D PA has been designed to interface multiple independent passive implant units for epidural stimulation. Conventional solutions are based on discrete implementation that drastically increase the area of the external unit or provide limited functionality in terms of frequency and supply range, available power and dead-time control. Table VI compares the PA chip to a number of integrated commercial components suitable to implement wireless power systems and shows how this chip provides a flexible fully integrated solution. The PA chip can be mounted together with a microcontroller, within the primary coil, in such a way that the size of the complete external unit is dictated only by the size of the primary coils used. The functionality of the PA chip has been enhanced with respect to conventional designs, to include a *N*-fractional PLL for accurate frequency tuning (with 1-kHz resolution), a 1-ns resolution delay line for precise setting of optimal dead-time, and a phase detector to monitor the phase shift between the carrier frequency and the resonant frequency of the tank circuit and, hence, optimize the efficiency of the primary unit. The chip provides a flexible platform for the development of closed-loop efficient power transmitter systems for medical applications. Measured results from the fabricated chip samples showed very good matching with simulated performance. The efficiency of the PA was measured to be greater than 80% at optimal dead-time. The PA is capable of delivering power in excess of 30 W to a 5 Ω, when operated with a 30-V supply. The output power can be adjusted by the duty cycle of an external signal, allowing control of the stimulation pulse width and the available power at the receiver end in passive stimulators.

Future work will entail the provision of an efficiency optimization scheme based on real-time tracking of the maximum output efficiency or maximum output power and adaptive control schemes [17], [33], [34]. The on-chip phase detector will form an additional closed loop with the microcontroller for adjustment of the primary circuit tuning (see Fig. 2). An adjustable dc/dc converter will be used in a closed-loop form to control the power delivered to the implant according to the implant's requirement [7], [14].

The class-D PA described in this paper can also be considered for use in other wireless applications including wireless powering, RFID readers, and near-field-communication links.

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A patent was granted to him as a result of his research work on the application of phased array systems to deep brain stimulation. Since 2011, he has been a Research Associate in the Analog and Biomedical Electronics Group, UCL, working on the design of implantable systems for deep brain and epidural electrical stimulation, and integrated circuits for biosensor interfacing. His research interests include the design of analog and mixed-signal integrated circuits, low-power biomedical circuits, and integrated telemetry systems.

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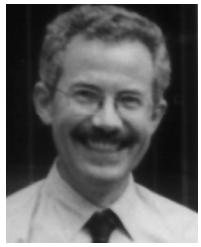

Nick Donaldson received the M.A. degree in engineering and electrical sciences at Cambridge University, Cambridge, U.K.

From 1977 to 1992, he was with the Medical Research Council, Neurological Prostheses Unit, London, U.K., under the direction of Professor G. S. Brindley, where his main field of research was the technology and use of implanted device for the restoration of useful leg function to paraplegics. Since 1992, he has been a Head of the Implanted Devices Group, University College London (UCL), London. He has been a Principal Investigator for many projects related to implanted devices and functional electrical stimulation. He is currently a Professor at UCL. His current research interest includes the development of implanted devices that use natural nerve signals as inputs, especially for preventing incontinence, stimulators of nerve roots, the use of electrical stimulation for recreational exercise of paralyzed legs, and methods to encourage functional neurological recovery after injury.

Andreas Demosthenous (S'94–M'99–SM'05) received the B.Eng. degree in electrical and electronic engineering from the University of Leicester, Leicester, U.K., in 1992, the M.Sc. degree in telecommunications technology from Aston University, Birmingham, U.K., in 1994, and the Ph.D. degree in electronic and electrical engineering from University College London (UCL), London, U.K., in 1998.

He is currently a Professor in the Department of Electronic and Electrical Engineering, UCL, where he leads the Analog and Biomedical Electronics Group. He has published more than 190 articles in journals and international conference proceedings. His current research interests include analog and mixed-signal integrated circuits for biomedical, sensor, and signal-processing applications. He is the Deputy Editor-in-Chief of the IEEE TRANSACTIONS ON CIRCUITS AND SYSTEMS II: EXPRESS BRIEFS and an Associate Editor of the IEEE TRANSACTIONS ON BIOMEDICAL CIRCUITS AND SYSTEMS. He is on the International Advisory Board of Physiological Measurement, Institute of Physics. He is a Member of the Technical Programme Committee of several IEEE conferences including European Solid-State Circuits (ESSCIRC) and Very Large Scale Integration of System-on-chip (VLSI-SoC). He was on the Organizing Committee of the IEEE Biomedical Circuits and Systems Conference (BioCAS) in 2013.

Dr. Demosthenous is a Fellow of the Institution of Engineering and Technology and a Chartered Engineer.