Complete Loss and Thermal Model of Power Semiconductors Including Device Rating Information

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***Abstract*—Thermal loading of power devices are closely related to the reliability performance of the whole converter system. The electrical loading and device rating are both important factors that determine the loss and thermal behaviors of power semiconductor devices. In the existing loss and thermal models, only the electrical loadings are focused and treated as design variables, while the device rating is normally predefined by experience with limited design flexibility. Consequently, a more complete loss and thermal model is proposed in this paper, which takes into account not only the electrical loading but also the device rating as input variables. The quantified correlation between the power loss, thermal impedance, and silicon area of insulated gate bipolar transistor (IGBT) is mathematically established. By this new modeling approach, all factors that have impacts to the loss and thermal profiles of the power devices can accurately be mapped, enabling more design freedom to optimize the efficiency and thermal loading of the power converter. The proposed model can be further improved by experimental tests, and it is well agreed by both circuit and finite element method (FEM) simulation results.**

***Index Terms*—Finite element method (FEM), insulated gate bipolar transistor (IGBT), power semiconductor, reliability, thermal model.**

I. Introduction

In many emerging and important energy conversion applications like renewable energy, traction, aerospace, and electric vehicles, etc., the power electronics are essential parts, which need to process a relatively large amount of power even up to megawatt level [1]–[4]. Due to the limited space and high cost of failures, the power density and reliability performances are especially focused in these applications. Consequently, the power loss and thermal loading of power semiconductor device are becoming more important performances which are required to be accurately designed and optimized [5]–[7], because they are sensitive parameters that not only have impacts on the efficiency and cost, but will also decide the converter reliability which can mathematically be described by, e.g., the Coffin–Manson-based lifetime models [8]–[14].

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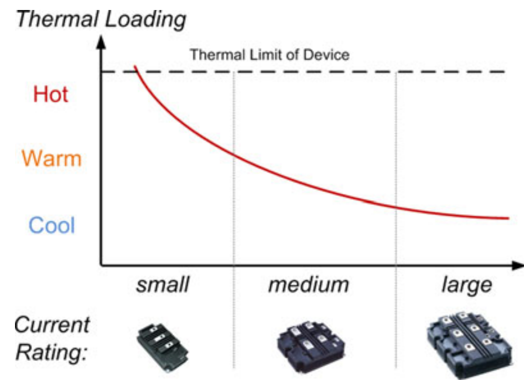

Fig. 1. Thermal loading of IGBT power device as the change of device rating (with same current loading).

There are mainly two design freedoms related to the loss and thermal behaviors of the power devices. It is well known that the electrical loading of converter is one of the determine factors (e.g., switching frequency, modulation, dc bus voltage, power factor, load current, etc.). Intensive works have been done to translate and optimize the electrical profiles of the converter into the corresponding loss/temperature profiles of the power semiconductor devices [15]–[23]. On the other hand, the device rating is another important design freedom which has been less focused and utilized: as illustrated in Fig. 1, if devices with larger current rating are applied, the power handling ability of the converter can be enhanced; thereby the junction temperature will be relieved. It is expected that for a given converter specification, the loss and thermal loading can be also optimized by selecting proper rating of devices. However, this mathematical correlation between thermal loading and device rating has not been comprehensively established before.

With the existing models and design approaches, there are some limits to achieve fully designable and optimal power loss and thermal loading of power semiconductor devices. Normally, in these models the power devices have to first be selected as a preknown factor according to the applied current/voltage stresses [24]–[26]. Afterward, the electrical profiles of the converter are treated as input variables and translated to the loss/temperature profiles of the selected devices [15]–[19]. Loss and thermal optimizations are normally restrained by tuning the electrical parameters in a limited range [27]–[32]. If the loss and temperature can still not be satisfied, the power device and cooling system have to be reselected with several try-and-error iterations until the requirements are satisfied. It can be seen

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that in this design process, the loss and temperature information are unexpected before the power devices are decided, thereby the design freedom of device rating is not well utilized with poor flexibility for loss/thermal optimization.

As a result, a more complete loss and thermal model is proposed in this paper, which takes into account not only the electrical loading but also the device rating as input variables. The quantified relationship between the power loss, thermal impedance, and silicon area of power device-insulated gate bipolar transistor (IGBT) is mathematically established. It is concluded that by this new model, all factors that have impacts on the loss and thermal profiles of power devices can be accurately mapped, enabling full design freedom to optimize the efficiency and thermal loading of converter by properly selecting the device rating. The proposed model is improved by experimental tests and is well agreed by both circuit and FEM simulations.

II. Basic Idea and Conditions for Modeling

In order to include the device rating into the loss and thermal models of power device, the proper rating definition has to be clarified first. Normally, the manufacturers use the current rating to quantify power handling ability of devices, it is defined as an RMS current at which the junction temperature achieves 125 °C at a given case temperature without switching [24], [26]. It can be seen that this current rating is an ambiguous and general definition, which may vary a lot depending on the actual operating conditions of the converter, normally some margins of current rating have to be reserved by experience to ensure a safe temperature in the device [24]. As a result the current rating provided by the manufacturer is not a suitable parameter to quantify the rating of power devices for the loss and thermal modeling.

In most of the cases if the converter specifications are decided, the voltage level of converter will be also settled as well as the voltage rating of applicable power devices. But different amount of transistor and diode dies/chips, which are connected in parallel by means of bond wire and copper layer, may be used to achieve different current handling ability, as demonstrated in Fig. 2. Therefore, the silicon area or paralleled chip number have more direct physical meaning to scale the power handling capability of power devices. Moreover, the silicon area or paralleled chip number is a fixed parameter, which does not change with the electrical loading of the converter, and making it more suitable to be modeled and quantified.

The flow of loss and thermal modeling used in this paper are shown in Fig. 3, where the corresponding input/output variables are highlighted. The electrical loading of converter is first translated to the power loss on devices, then the thermal impedance model is applied to generate the junction temperature, which is then feedback to the loss model in order to describe the temperature dependency of power losses [2], [15]. It is noted that besides the electrical loading of converter, the device rating quantified by paralleled chip numbers is also included as input variable.

A popular two-level voltage source converter (2L-VSC) used in the wind power application are chosen as a study case in this paper, as shown in Fig. 4. The detailed converter specifications and used transistor/diode chips are listed in Table I, which are typical values for a grid-side inverter at low-voltage level. The corresponding duty ratio for the transistors T1 and T2 as well as the load current in phase A are shown Fig. 5, in which the converter is operating on the condition shown in Table I. It is noted that other operating conditions and converter solutions can also be applied sharing the similar modeling idea and process.

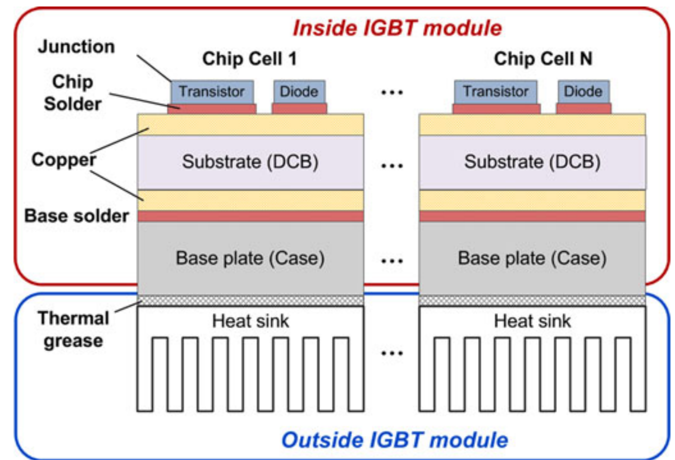


Fig. 2. IGBT physical structure with multicells.

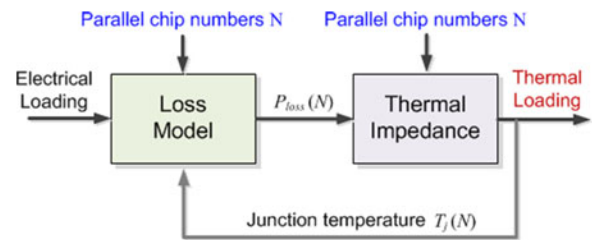


Fig. 3. Calculation flow of loss/thermal modeling including device rating information.

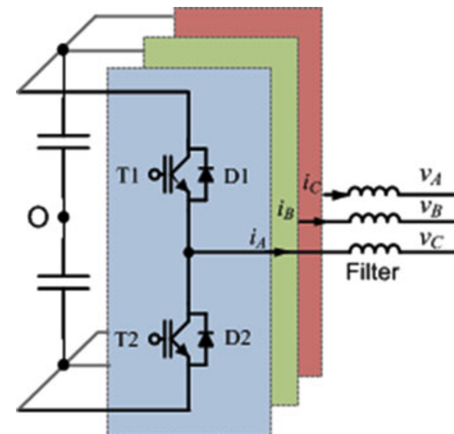


Fig. 4. Two-level voltage source dc–ac converter for case study (2L-VSC).

TABLE I
PARAMETERS OF CONVERTER SHOWN IN FIG. 4.

Rated output active power P_o	250 kW
Output power factor *PF*	1.0
DC bus voltage V_{dc}	1050 VDC
*Rated primary side voltage V_p	690 Vrms
Rated load current $I_{\rm load}$	209 Arms
Fundamental frequency f_o	50 Hz
Switching frequency f_c	2 kHz
Filter inductance L_f	1.2 mH (0.2 p.u.)
IGBT chip IGC186T170R3	1700V/150 A
Diode chip SIDC85D170H	1700 V/150 A

*Line-to-line voltage in the primary windings of transformer.

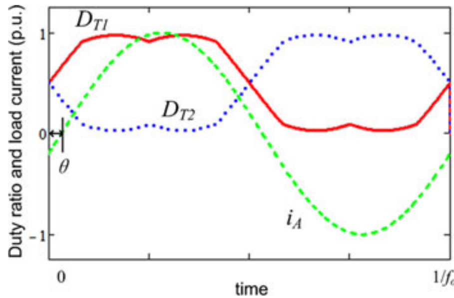


Fig. 5. Duty ratio for the transistor and load current of phase A in the given converter (conditions in Table I, DT1 duty ratio for transistor T1, DT2 duty ratio for transistor T2, iA load current in phase A, θ phase angle caused by filter inductance).

III. LOSS MODEL INCLUDING DEVICE RATING INFORMATION

As it has been well investigated in [15]–[23], the power loss for the power semiconductor devices is composed of two parts: conduction loss (or steady-state loss) and switching loss (or dynamical loss). The modeling process will be detailed in the following.

A. Conduction Loss

The total conduction loss of an IGBT module is composed of the conduction loss on individual transistor/diode chips; therefore, the instantaneous conduction loss of IGBT module with *N* chips paralleled ($p_{\rm condT/D}$) is a function of *N* and time *t*, and it can be expressed as the sum of conduction losses on each chip $p_{\rm condT/D_chipx}$

$$p_{\rm condT/D}(N,t) = \sum_{x=1}^{N} p_{\rm condT/D_chipx}(t). \quad (1)$$

Assuming $p_{\rm condT/D_chip}$, the average instantaneous loss of transistor/diode chips, then the conduction loss of the whole IGBT module can be calculated as

$$\begin{aligned} &p_{\rm condT/D}(N,t) = N \cdot p_{\rm condT/D_chip}(t) \\ &= N \cdot v_{\rm ce/f_chip}(i_{\rm chip}({\rm t})) \cdot i_{\rm chip}({\rm t}) \cdot D_{\rm T/D}(t) \end{aligned} \quad (2)$$

where $v_{\rm ce/f_chip}$ is the conduction voltage of transistor/diode, $i_{\rm chip}$(t) is the mean current flowing in each chip, $D_{\rm T/D}(t)$ is the duty ratio for transistor or diode. The mean current flowing in each individual chip can be represented as

$$i_{\rm chip}({\rm t}) = \frac{|i_{\rm load}({\rm t})|}{N}. \quad (3)$$

The average conduction loss of IGBT Module $P_{\rm condT/D_Ave}$ can be expressed as the integral of instantaneous loss $p_{\rm condT/D}$ within a fundamental cycle $1/f_o$

$$\begin{aligned} P_{\rm condT/D_Ave}(N) &= f_o \int_0^{1/f_o} p_{\rm condT/D}(N,t)\, dt \\ &= N \cdot f_o \int_0^{1/f_o} \left[(v_{\rm ce/f_chip}(i_{\rm chip}({\rm t})) \cdot i_{\rm chip}({\rm t}) \cdot D_{\rm T/D}(t)\right] dt. \end{aligned} \quad (4)$$

As it can be seen in (2) and (4), the only unknown parameter is the conduction voltage for transistor/diode chip. Unfortunately, the conduction characteristic of the individual chip $v_{\rm ce/f_chip}$ is not always accessible information. If the current deviation among the chips is not significant when characterizing the IGBT modules, a virtual mean $v_{\rm ce/f_chip}$ can be acquired by normalizing the conduction characteristic of IGBT module with following function:

$$V_{\rm ce/f_chip}(I_{\rm chip}) = V_{\rm ce/f}\left(\frac{I_{ce/F}}{N}\right) \quad (5)$$

where $V_{\rm ce/f}$ is the conduction voltage of the IGBT module and $I_{\rm ce/F}$ is the corresponding load current, their relationship can be acquired from the device datasheets [33], or by experimental characterization [16], [19].

As an example, the nominal conduction characteristic for a set of transistor and diode chips are shown in Fig. 6 (a) and (b), respectively, where the datasheet values from the IGBT modules with different current ratings are used. It can be seen that the mean conduction characteristic of transistor or diode chip is quite consistent among different IGBT modules. Thereby, the dotted curve shown in Fig. 6 is used as the conduction characteristic of chips, which can be expressed as a function of chip current $i_{\rm chip}$ and two fitting constants $V_{\rm ce/f_chip0}$ and $B_{\rm ce/f}$

$$v_{\rm ce/f_chip}(i_{\rm chip}) = V_{\rm ce/f_chip0} + (i_{\rm chip})^{B_{\rm ce/f}}. \quad (6)$$

B. Switching Loss

Similarly, the total switching loss of a whole IGBT module is composed of the switching loss on the individual chip. The instantaneous switching loss of IGBT module with *N* chips can be calculated as

$$\begin{aligned} p_{\rm sw/rr}(N,t) &= N \cdot p_{\rm sw/rr_chip}(t) \\ &= f_s \cdot N \cdot E_{\rm sw/rr_chip}(i_{\rm chip}(t)) \end{aligned} \quad (7)$$

where $E_{\rm sw/rr_chip}$ is the average switching energy for all transistor or diode chips, which is a function of chip current. f_s is the switching frequency of converter. The average switching loss of IGBT Module $P_{\rm swT/D_Ave}$ can be expressed as the integral of

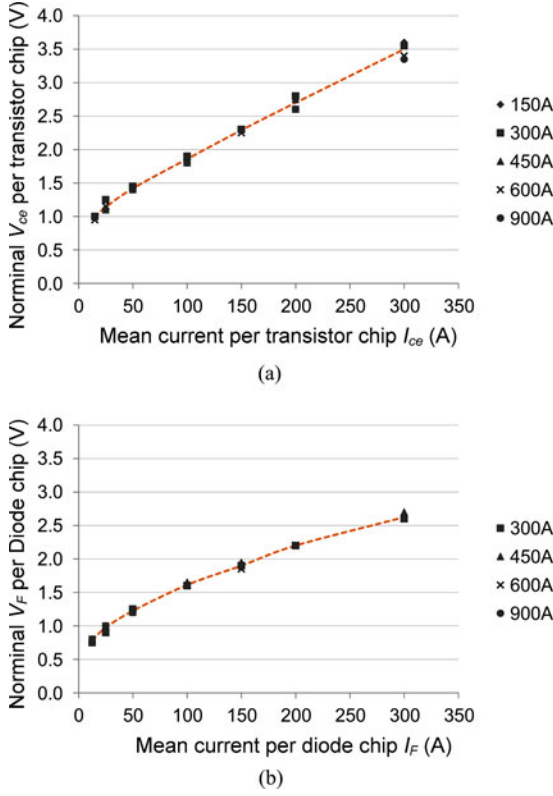


Fig. 6. Nominal conduction voltage for single transistor/diode chip in 1700-V IGBT modules having different current ratings (datasheet values, recommended testing condition, $T_j = 125^\circ$ C). (a) Nominal $V_{\rm ce}$ versus nominal $I_{\rm ce}$. (b) Nominal VF versus nominal IF.

instantaneous loss $p_{\rm swT/D}$ within a fundamental cycle $1/f_o$ as

$$P_{\rm swT/D_Ave}(N) = f_o \int_0^{1/f_0} p_{\rm sw/rr_chip}(N,t)dt = N \cdot f_s \cdot f_0 \int_0^{1/f_0} E_{\rm sw/rr_chip}(i_{\rm chip}({\rm t}))dt. \tag{8}$$

As it can be seen in (7) and (8), the only unknown parameter is the switching energy of the individual transistor/diode chip. Similarly, $E_{\rm sw/rr_chip}$ is an average switching energy, which can be acquired by normalizing the characteristics of the IGBT modules by

$$E_{\rm sw/rr_chip}(I_{\rm chip}) = \frac{1}{N} E_{\rm sw/rr}\left(\frac{I_{\rm ce/F}}{N}\right) \tag{9}$$

where $E_{\rm sw/rr}$ is the switching energy of the IGBT module and $I_{\rm ce/F}$ is the corresponding load current, their relationship can be acquired from the device datasheet or by experimental tests.

As an example, the nominal switching characteristic for a set of transistor/diode chips are shown in Fig. 7, where the turn-on, turn-off, and reverse recovery energy from IGBT modules with different current ratings are indicated. It can be seen that unlike the conduction characteristic shown in Fig. 6, the average switching characteristic per chip in different modules distribute in certain range. This is because the switching characteristic of power devices depends on many factors, such as the drive circuit resistance, *di/dt*, stray inductance, etc. These factors are sensitive to the circuit configurations and can easily be deviated when different numbers of chips are packaged. It is noted that the average turn-on energy and reverse recovery energy per chip have relative larger distribution range than the turn-off energy. This is reasonable because the turn-on and reverse recovery process depends a lot on the stray inductance of the chips that may vary in different IGBT modules.

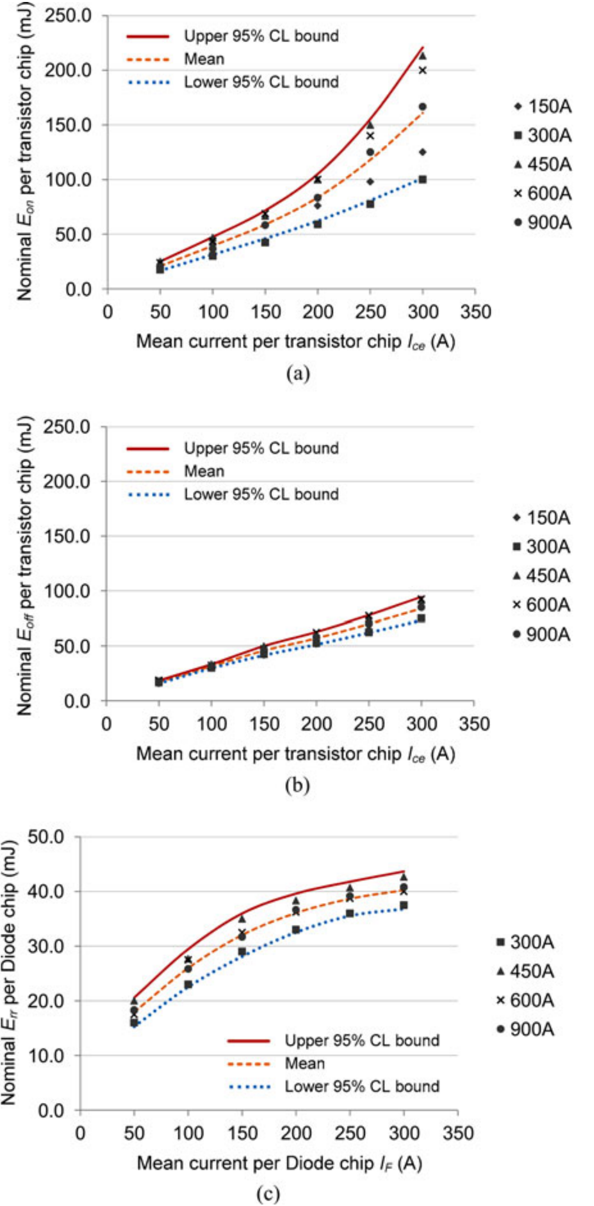


Fig. 7. Nominal switching loss for single IGBT/diode chip in a series of modules having different current ratings (datasheet values, recommended testing condition, $T_j = 125^\circ$ C). (a) Nominal turn-on energy loss $E_{\rm on}$ versus $I_{\rm ce}$ per transistor chip. (b) Nominal turn-off energy loss $E_{\rm off}$ versus $I_{\rm ce}$ per transistor chip. (c) Nominal reverse recovery energy loss $E_{\rm rr}$ versus IF per diode chip.

In order to cope with this distribution of switching characteristic, a statistics description is used to cover the upper and lower 95% confidence level as well as the mean value of the nominal switching energy [34]. The three curves can be chosen depending on the required margin and confidence for design purpose,

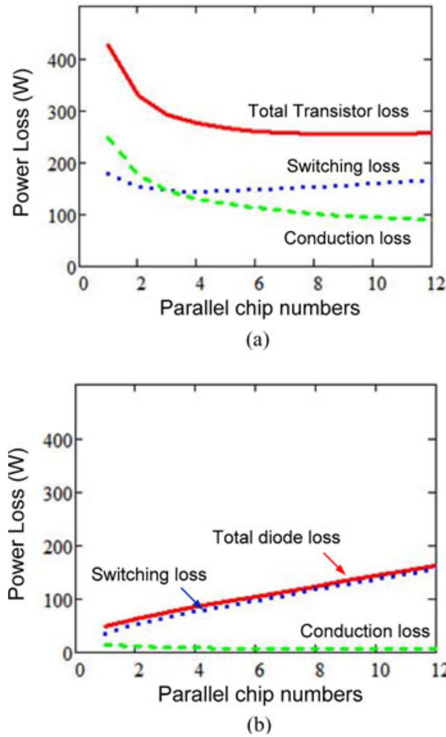


Fig. 8. Average power loss of transistor/diode in IGBT module with relation to paralleled chip numbers (converter condition in Table I, Tj = 125° C). (a) Transistor. (b) Diode.

and in this paper the mean value is used. All of the three curves in Fig. 7 can be expressed as a function of the average current flowing in chip $i_{\rm chip}$ and three fitting constants $S_{T/D1}$, $S_{\rm T/D2}$, and $S_{\rm T/D3}$

$$E_{\rm sw/rr_chip}(i_{\rm chip}) = S_{\rm T/D1}\cdot(i_{\rm chip})^2 + S_{\rm T/D2}\cdot i_{\rm chip} + S_{\rm T/D3}. \quad (10)$$

With the virtual average loss characteristics of individual transistor/diode chip in Figs. 6 and 7, the relationship between the IGBT power loss and corresponding chip numbers in parallel can be established. The results are shown in Fig. 8, where the converter is operating under the conditions shown in Table I, and the average conduction loss, switching loss, and total loss are indicated respectively at the junction temperature of 125 °C. It is noted that the loss results shown in Fig. 8 should be discrete points, but for the sake of clarity, trend lines are illustrated.

It can be seen that the increase of paralleled chip numbers (device rating) only benefits to the conduction loss reduction of IGBT modules, while the switching loss cannot be improved by increasing the chip numbers or device rating: in the transistor, the switching loss start to saturate and dominate after the device rating increase to a certain level. In the diode, the switching loss is always dominant and even keeps growing with the increase of device rating. This phenomenon is hard to be discovered by existing loss models for the power device, and it can be explained by different trends of the slope for the switching energy curves shown in Fig. 7.

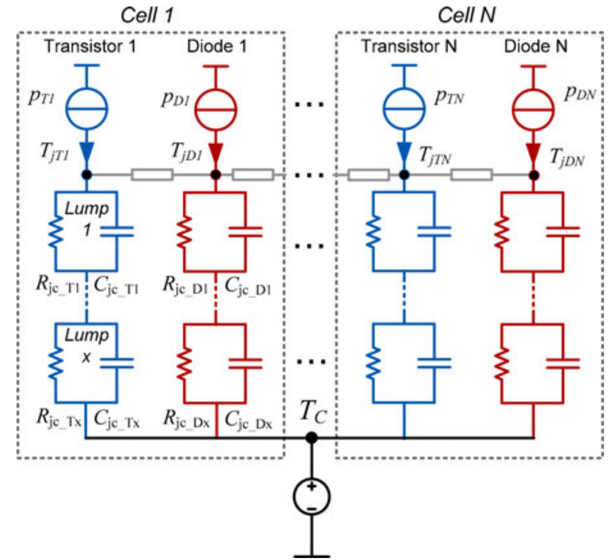


Fig. 9. Internal network of thermal impedance for IGBT module based on Fig. 2.

IV. Thermal Impedance Model Including Device Rating Information

As it can be seen from Fig. 2, the thermal impedance of IGBT module is composed of two parts: the part for device internal packaging structure Z_{jc} (junction to case) and the part for the external cooling structure Z_{ca} (case to ambient) [35]–[38]. The modeling process will be detailed in the following.

A. Thermal Impedance Inside IGBT Module

Practically in order to limit the stray inductance, the chips of transistor and its freewheeling diode are packaged closely to form a "chip pair" unit, as illustrated in Fig. 2. In order to facilitate the packaging, the electrical and thermal performances of a chip pair unit is optimized, and various current ratings for the IGBT modules are achieved by scaling the standard chip pair units in parallel. In a good packaging of IGBT module, the distance between chip pair units is optimized to minimize the thermal coupling effects. Therefore, from the point view of thermal modeling, the internal structure of an IGBT module can be virtually divided into many chip cells/units, as also illustrated in Fig. 2.

Normally, the thermal impedance for power semiconductors is modeled by a series of *RC* lumps which are composed of a thermal resistance *R* and a thermal capacitance *C*. Typically, multi *RC* lumps are used to represent different layers of the materials from the chip to the case of the IGBT modules [28]–[35]. According to the cell-based structure shown in Fig. 2, the network of thermal impedance for the internal structure of an IGBT module can be drawn as shown in Fig. 9, in which the *RC* lumps is divided into multicells horizontally (cell 1–cell *N*) and multilayers vertically (lump 1–lump *x*), the transistor/diode chips are represented by "thermal sources" governed by their instantaneous power losses.

Assuming the multilayers structure from chip to case is evenly distributed for each of the divided cell, and then the thermal

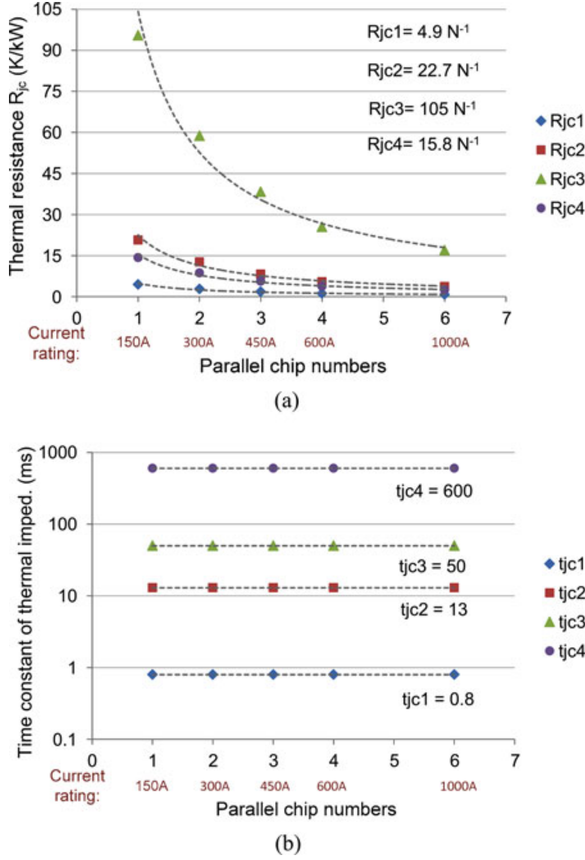


Fig. 10. Thermal impedance of *RC* lumps for transistor inside the IGBT modules (junction to case) with relation to paralleled chip numbers. (a) Thermal resistance versus chip numbers. (b) Time constants versus chip numbers.

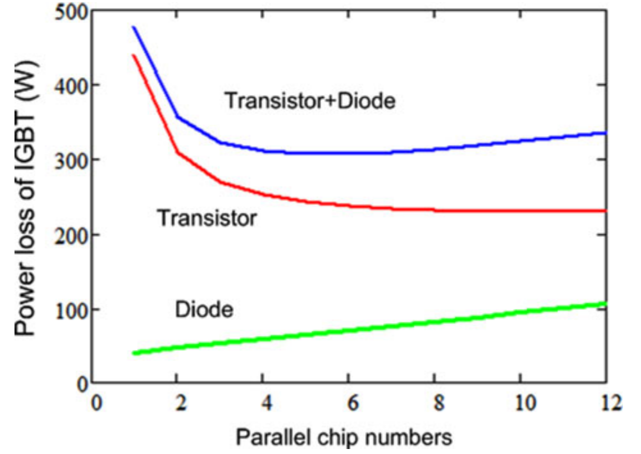


Fig. 11. Average power loss of transistor/diode versus paralleled chip numbers considering temperature dependency (converter condition in Table I, Th = 60° C).

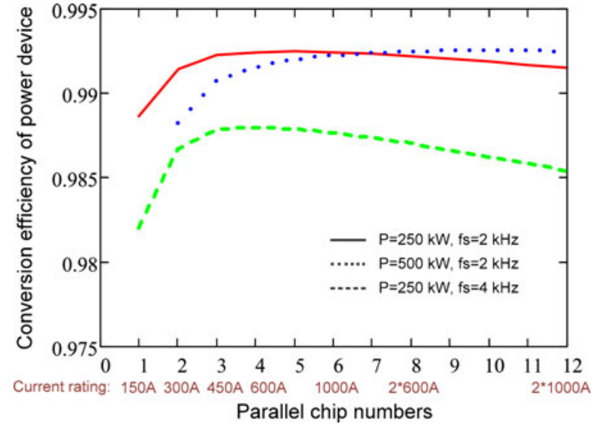


Fig. 12. Conversion efficiency versus device rating (conditions in Table I, Th = 60° C).

resistance for the *x*th layer *RC* lump of IGBT module $R_{\mathrm{jcT/Dx}}$ is equivalent to the corresponding thermal resistance for each cell $R_{\mathrm{jcT/Dx_chip}}$ with *N* in parallel

$$R_{\mathrm{jcT/Dx}}(N) = \frac{R_{\mathrm{jcT/Dx_chip}}}{N} = \frac{d_x}{\lambda_x \cdot A_{\mathrm{T/Dx_chip}}} N^{-1} \quad (11)$$

where *N* is the number of paralleled chips, $A_{\mathrm{T/Dx_chip}}$ is the equivalent to the heat transfer area for a transistor/diode chip at *x*th layer, d_x is the thickness of material at *x*th layer, and λ_x is the thermal conductivity of material at *x*th layer (W/m$*$K). By knowing the physical geometry and material of the IGBT structure, each of the thermal resistance in Fig. 9 can be calculated with the help of FEM simulations [39]. Unfortunately, the module structure/geometry and FEM simulation may not always be available. Another easier way used in this paper is to fit the function (11) with the thermal resistances which are derived from datasheets.

As shown in Fig. 10(a), in which the overall thermal resistances for the transistor in IGBT modules with different current ratings are plotted, the values are acquired from the datasheets and four layers of *RC* lumps ($R_{jc1}-R_{jc4}$) are used to represent the thermal behavior from chip to case. As it can be observed, each layer of the thermal resistance in different IGBT modules can be fitted with a function that is inversely proportional to the paralleled chip number *N*. This relation is consistent with the physical model shown in (11), where the parameters $R_{\mathrm{jcT/Dx_chip}}$ can be fitted with R_{jcx} shown in Fig. 10(a). As a result, the relationship between the thermal resistance and the corresponding device rating (paralleled chip numbers) are established.

With respect to the thermal capacitance, the modeling approach is similar. The thermal capacitance for the *x*th layer *RC* lump of IGBT module $C_{\mathrm{jcT/Dx}}$ is equivalent to the corresponding thermal capacitance for each cell $R_{\mathrm{jcT/Dx_chip}}$ with *N* in parallel

$$\begin{aligned} C_{\mathrm{jcT/Dx}}(N) &= N \cdot C_{\mathrm{jcT/Dx_chip}} \\ &= N \cdot c \cdot \rho_x \cdot d_x \cdot A_{\mathrm{T/Dx_chip}} \end{aligned} \quad (12)$$

where *c* is the specific heat factor proportional to heat in (Ws/g$*$K), ρ_x is the density of materials at *x*th layer (g/cm^3). Similarly, the thermal capacitances in Fig. 9 can be acquired either by calculations or by fitting datasheet values. It is noted that, instead of thermal capacitance, the time constant of the *RC* lump $\tau_{\mathrm{jcT/Dx}}$ is more commonly used by datasheets. It can be

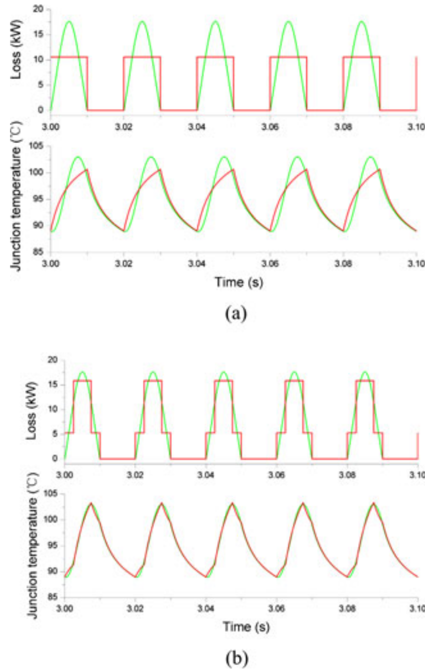


Fig. 13. Loss approximation to get analytical solution of junction temperature fluctuation. (Green: original loss and corresponding junction temperature, red: Approximate loss pulses and corresponding junction temperature). (a) One-stage pulse loss approximation. (b) Two-stage pulse loss approximation.

calculated as

$$\tau_{\mathrm{jcT/Dx}} = R_{\mathrm{jcT/Dx}} \cdot C_{\mathrm{jcT/Dx}} = \frac{c \cdot \rho}{\lambda} \cdot d_x^2. \tag{13}$$

In the function (9) there is no item for the chip numbers N as well as $A_{\mathrm{T/Dx_chip}}$. That means the time constant of RC lump is only related to the physical property and thickness of the xth layer material. Thereby with the same multilayer structure and material, $\tau_{\mathrm{jcT/Dx}}$ should be the same among IGBT modules having different paralleled chip numbers.

The time constant for the transistor in IGBT modules with different current ratings are plotted in Fig. 10(b), the values are acquired from datasheets and four layers of RC lump are used [37]. It can be seen that the time constants of the RC lump inside the IGBT modules keep constant under different device ratings, this characteristic is consistent with the physical model described in (13), in which the parameters $\tau_{\mathrm{jcT/Dx}}$ can be fitted with t_{jcx} shown in Fig. 10(b). As a result, the relationship between thermal capacitance/time constant and corresponding device rating (paralleled chip numbers) are established.

In a summary, the time domain thermal impedance of IGBT module including the rating information (paralleled chip numbers) can be written as

$$Z_{\mathrm{jcT/D}}(N,t) = N^{-1} \cdot \sum_{x=1}^{4} R_{\mathrm{jcT/Dx_chip}} \cdot (1 - e^{-t/\tau_{\mathrm{jcT/Dx}}}) \tag{14}$$

where R_{jcTx} and τ_{jcTx} can be acquired from Fig. 10(a) and (b), respectively.

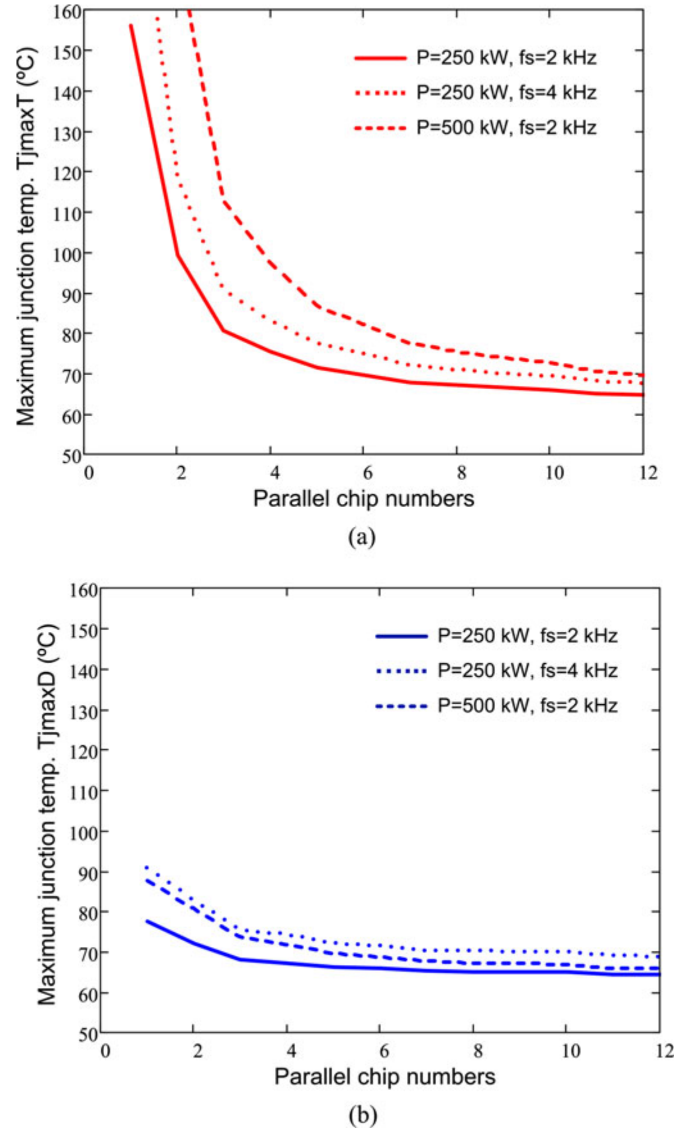
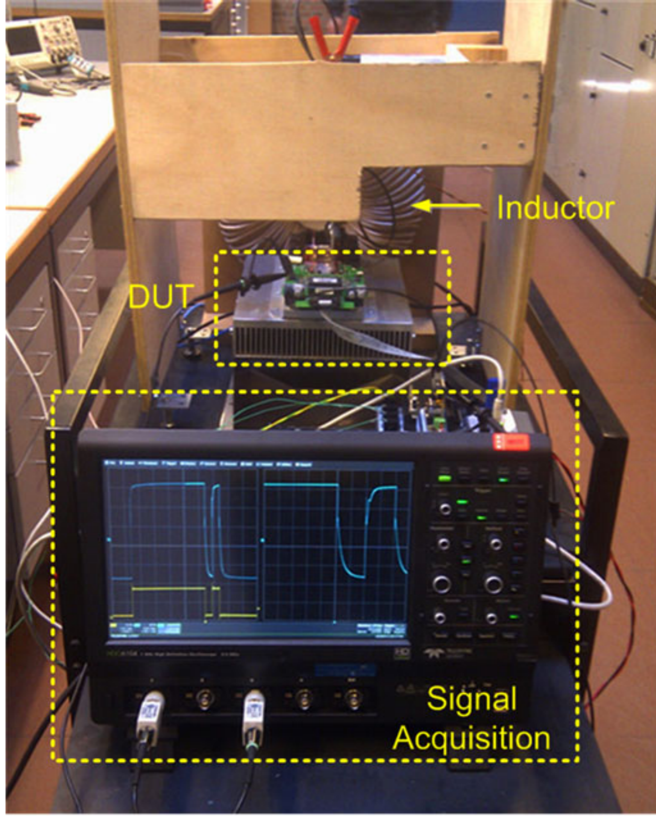


Fig. 14. Maximum junction temperature TjmaxT/D versus parallel chip numbers under different operating conditions of the converter. (a) Transistor. (b) Diode.

B. *Thermal Impedance Outside IGBT Module*

The thermal impedance outside the IGBT module mainly consists of two parts: the thermal grease part from case to heat sink, and the heat sink part from grease to the ambient, as indicated in Fig. 2. Unlike the thermal impedance inside the IGBT module, thermal modeling of this part normally involves many uncertainties, which may be challenge to predict. Due to the variations of applied grease type, thicknesses, mounting force, heat sink type, cooling fluid, and ambient temperature, the thermal impedance outside IGBT module may significantly deviate. Therefore, the relatively accurate way is to seek the help of experimental testing and FEM simulation case by case.

In this paper, it is assumed that the heat sink is selected in a way to be able to maintain its temperature at 60 °C, which is a typical design target for the heat sink system [26]. The



(a)

(b)

Fig. 15. Test setup for loss characterization of IGBT module. (a) Photo of test setup. (b) Circuit scheme.

thermal grease is treated as a thermal resistance from case to heat sink R_{ch}, which is calculated based on thermal conductivity of 1 W/m∗K, and a thickness of 150 μm. It is noted that R_{ch} is related to the base plate area of IGBT module, and it is no longer inversely proportional to the paralleled chip numbers *N*.

V. Analytical Solution for Junction Temperature

With the loss model in (4), (8), and thermal resistance model in (11), it is possible to acquire the information of the steady-state junction temperature of power device, and the temperature dependency of the power losses can be also considered.

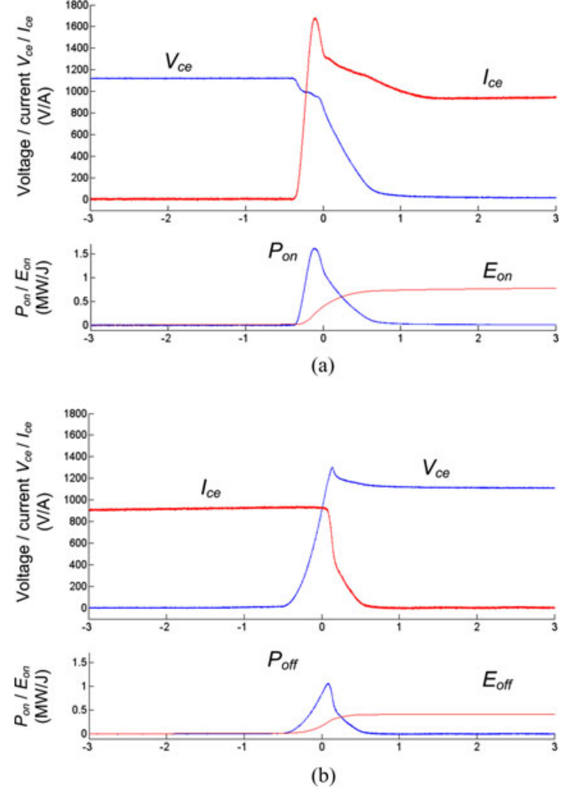


Fig. 16. Experimental switching waveforms of IGBT with corresponding freewheeling diode (IGBT module 1700 V/1000 A, $T_j = 125°$ C, $V_{\rm dc} \approx 1120$ V, $I_c \approx 940$ A). (a) Transistor turning ON, (b) Transistor turning OFF.

A. Analytical Solution for Power Loss Considering Temperature Dependency

It is well known that the loss characteristics of power semiconductor are temperature dependent [19], [24]–[26]. With the thermal resistance information, it is possible to include the junction temperature information into the power loss models. Considering the average power loss is linearly distributed with the junction temperature, then the updated average loss for IGBT module considering temperature dependency can analytically be solved by

$$P_{\rm LossT/D}(N) = \frac{P_{\rm T/D_Ave@Tr2}(N)\cdot(T_{\rm r1}-T_{\rm r2})+\Delta P_{\rm T/D_Ave}(N)\cdot(T_h-T_{r2})}{(T_{\rm r1}-T_{\rm r2})-\left[R_{\rm jcT/D}(N)+R_{\rm chT/D}(N)\right]\cdot\Delta P_{\rm T/D_Ave}(N)} \tag{15}$$

where

$$\Delta P_{\rm T/D_Ave}(N) = P_{\rm T/D_Ave@Tr1}(N) - P_{\rm T/D_Ave@Tr2}(N) \tag{16}$$

$$P_{\rm T/D_Ave@Tr1/Tr2}(N) = P_{\rm swT/D_Ave}@T_{\rm r1}/T_{\rm r2} + P_{\rm condT/D_Ave}@T_{\rm r1}/T_{\rm r2}. \tag{17}$$

The T_{r1} and T_{r2} are two reference temperatures which are normally chosen at 125 and 25 °C, respectively. The updated power loss of IGBT with relation to the device rating (paralleled

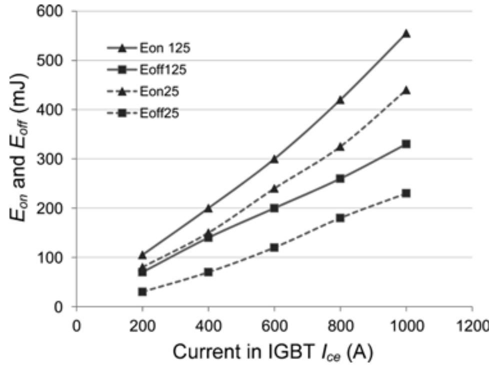


Fig. 17. Tested switching energy of IGBT versus switching current (IGBT module 1700 V/1000 A, $V_{\rm dc} = 900$ V, at two different temperature conditions).

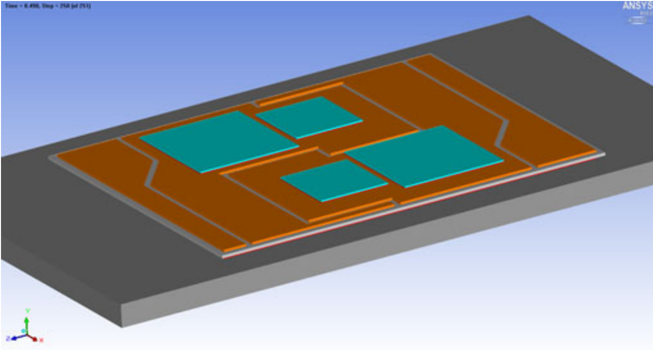


Fig. 18. Construction of an unit cell (two transistors and two diodes) in IGBT module for FEM simulation.

chip numbers) is shown in Fig. 11, where the temperature dependency of the losses is considered. The average transistor loss, diode loss, and total loss are indicated, respectively. It can be seen that with the given condition in Table I, there is an optimal point, where the total loss in IGBT can be minimum (six chips are used to be paralleled). The optimal efficiency of converter can be thereby achieved by properly selecting the rating of power devices. As shown in , where the conversion efficiency of power device (not include filters) with relation to the device ratings is plotted, and three cases for different operating conditions of the converter are illustrated. It is noted that the loss and efficiency results shown in Figs. 11 and 12 should be discrete points, but for the sake of clarity, trend lines are used here.

B. Analytical Solution for Junction Temperature

With the thermal impedance model (14) and instantaneous power loss model (2) and (7), it is possible to calculate the instantaneous junction temperature of the power devices by convoluting the loss and thermal impedance

$$T_j(N,t) = T_h + \int_0^t \left[\frac{d}{dz} P_{\rm LossT/D}(N,z)\right] \cdot Z_{jh}(N, t-z)\, dz. \tag{18}$$

However, this calculation is relatively complicated and is not suitable for the design purpose. Actually only the mean junction temperature T_m and junction temperature fluctuation ΔT_j caused by the current alternating are interesting parameters for the thermal design and optimization [20]–[23]. As a result, simplified solutions which can directly extract the information of T_m and ΔT_j are developed in this paper.

According to [36], the mean value of steady-state junction temperature T_m can be written as follows, where the information of paralleled chip numbers is included

$$T_{\rm jm_T/D}(N) = T_{\rm h} + P_{\rm LossT/D}(N) \cdot [R_{\rm jcT/D}(N) + R_{\rm chT/D}({\rm N})]. \tag{19}$$

In dc–ac converter, the alternating of the load current at fundamental frequency will result in a quasi-sinusoidal distribution of the instantaneous power loss on the transistor and diode. As a result, the corresponding temperature swing will be observed on the chips [40] and it also needs to be taken into account in the thermal design for power converter. Because the exact time when the junction temperature achieves its maximum/minimum value is hard to be derived by (12), approximations by loss pulses, which have the same loss-time area as the original loss are used to calculate the ΔT_j. In this case, the time when the junction temperature achieves its maximum value can be determined. In Fig. 13, two types of loss approximation (one stage and two stages loss pulses) which share the same loss-time area are applied to the same thermal impedance. It can be seen that the two stages loss approximation can achieve better accuracy with respect to the temperature fluctuation amplitude.

As a result, the fluctuation of junction temperature ΔT_j with relation to the chip numbers of IGBT module can analytically be solved by

$$\Delta T_{\rm j_T/D}({\rm N}) = P_{\rm LossT/D}({\rm N}) \cdot Z_{\rm jcT/D}\left(N, \frac{3}{8 f_o}\right) + 2 P_{\rm LossT/D}(N) \cdot Z_{\rm jcT/D}\left(N, \frac{1}{4 f_o}\right). \tag{20}$$

The maximum junction temperature of transistor or diode can be calculated as

$$T_{\rm jmax_T/D}({\rm N}) = T_{\rm jm_T/D}(N) + \Delta T_{\rm j_T/D}({\rm N}). \tag{21}$$

In Fig. 14, the maximum junction temperature of the transistor and diode with relation to the device rating (parallel chip numbers) is shown, where the conditions of converter in Table I with several variants of output powers and switching frequencies are indicated. It can be seen that different from the traditional thermal models, the device rating is also treated as variables. As a result, plenty of design freedoms to control and optimize the maximum temperature of power device can be achieved by adjusting both the device rating and the electrical loading.

VI. Verifications and Discussions

As mentioned before, the loss characteristics of power device are sensitive parameters to the practical circuit conditions, which

(a)

(b)

(c)

Fig. 19. Temperature distribution in IGBT modules with different ratings (FEM simulation by ANSYS Icepack, converter condition in Table I, power loss is equally injected on paralleled chips, based plate of modules is attached to a constant temperature surface at 80 °C). (a) one chip, (b) three chips in parallel, (c) six chips in parallel.

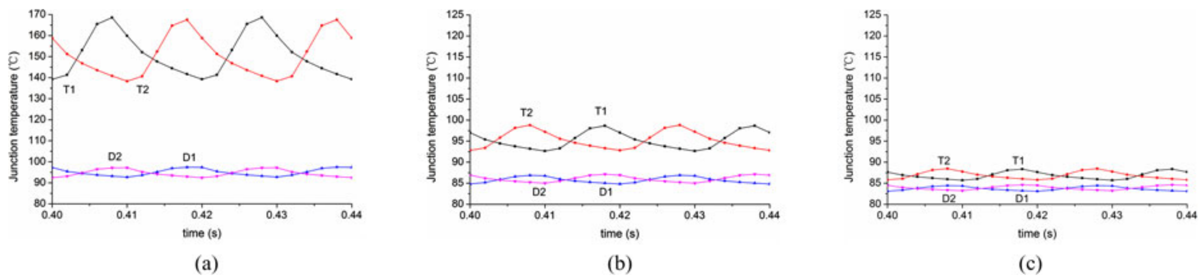


Fig. 20. Junction temperature of IGBT modules with different device ratings (FEM simulation by ANSYS, center point on the chips shown in Fig. 19). (a) one chip, (b) three chips in parallel, (c) six chips in parallel.

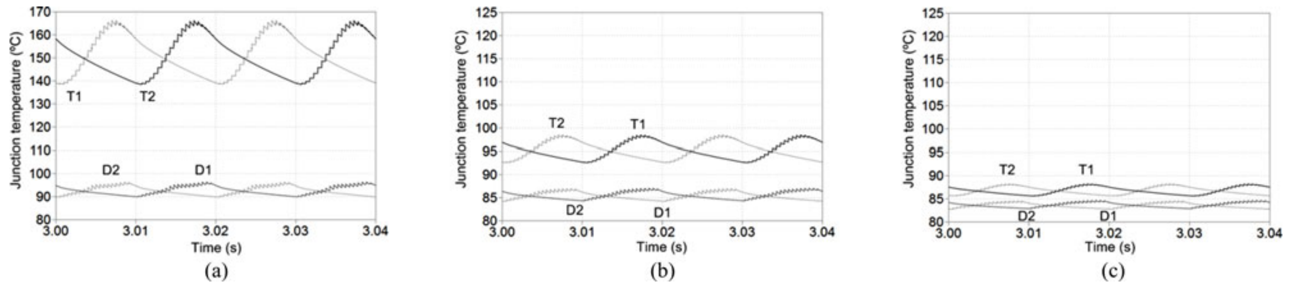


Fig. 21. Junction temperature of IGBT modules with different device ratings (circuit simulation by PLECS, converter condition in Table I, Tc = 80° C). (a) one chip, (b) three chips in parallel, (c) six chips in parallel.

could probably deviate from the typical values shown in the datasheets. The parameter variation is particularly significant for the switching characteristics as indicated in Fig. 7. In order to handle this uncertainty, some statistical descriptions or functions can be used to indicate the potential loss and thermal range. However, sometimes more accurate loss and thermal modeling would be necessary, and experimental characterizations based on the actual power device and circuit conditions are needed.

As a demonstration in this paper, an experimental setup was built in Fig. 15, in which the switching characteristics of the IGBT module can be tested based on "double pulsed test" under various current, voltages, and temperature conditions. The circuit scheme of the test setup is shown in Fig. 15(b), a 1700V/900A IGBT module from [33] is applied which is corresponding to six chips in parallel and can represent the mean condition shown in Fig. 7. The experimental waveforms when the IGBT at turn-on and turn-off are shown in Fig. 16. The switching energy under different currents and temperatures with the tested IGBT module is summarized in Fig. 17. By using this loss characteristics based on actual device and circuit condition, the accuracy of the proposed model can be enhanced.

The loss models proposed in this paper can be verified by time-domain circuit simulation. The simulation was conducted with PLECS Blockset in Simulink, which is able to online simulate the electrical, loss, and thermal behaviors with given specifications of the converters and power devices [32]. In the simulation the converter is configured at the same condition shown in Table I, and the experimental switching characteristics shown in Fig. 17 is used (where the IGBT module with six chips are tested). The switching characteristics of IGBT modules with one and three chips are derived by normalizing the results in Fig. 17. In order to avoid the uncertainty of the thermal grease and heat sink, the baseplate of IGBT module is set to a constant temperature at 80 °C. A loss comparison between the circuit simulation and model calculation are shown in Fig. 22, where the average power loss for transistor and diode in IGBT modules are illustrated under different ratings of device (chip numbers). It can be seen that the simulation results agree well with the results acquired by the proposed loss models.

The thermal models proposed in this paper are verified by Finite Element Methods FEM simulations in ANSYS Icepack, which can accurately simulate the thermal behaviors of power device considering the geometries, materials, and operating conditions in three dimensions [21]. The construction of a chip cell

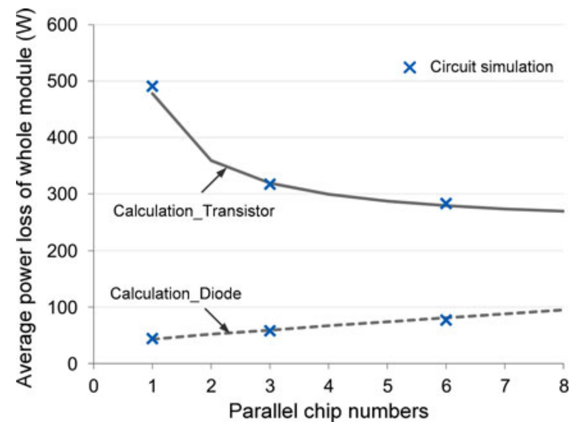


Fig. 22. Comparison of power loss by circuit simulation and model calculation under different chip numbers (conditions in Table I, switching energy in Fig. 17 is used, $T_c = 80$ °C).

(a pair of transistors and freewheeling diodes with corresponding soldering layers, direct copper bond, and baseplate) in IGBT module for FEM simulation is shown in Fig. 19, which is built according to the actual geometry and materials of the tested IGBT module. In Fig. 20, the temperature distribution inside the IGBT module is indicated when the transistor T1 is achieving maximum temperature. In this simulation, the instantaneous power losses generated from Fig. 22 are input into the transistor and diode chips in the FEM model. In order to avoid the unpredicted uncertainty of the thermal grease and heat sink, the temperature at the baseplate surface of the IGBT module is set at constant of 80 °C. It can be seen from Fig. 18 that there is no thermal coupling between chip cell units either vertically or horizontally. This result agrees well with the assumptions made in Fig. 9.

The temperature response on the center point of transistor/diode chips are recoded in Fig. 20, where the conditions with 1, 3, and 6 paralleled chips are shown, respectively. For the sake of comparison, the junction temperature simulated by PLECS is also shown in Fig. 21. Because the virtual mean loss of all transistor or diode chips is used, the loss and temperature are equally distributed among the paralleled chips shown in Fig. 19. However, in reality the loss and temperatures on individual chip could deviate from the average value, this is still a challenge and complicated behavior to predict and is out of the scope of this paper.

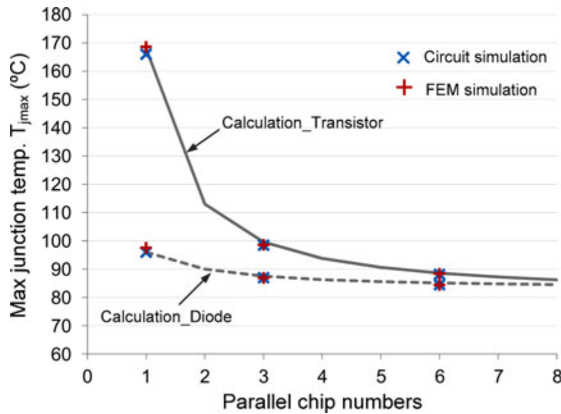


Fig. 23. Comparison of maximum junction temperature by circuit simulation, FEM simulation, and model calculation (conditions in Table I, the switching energy in Fig. 17 is used, $T_c = 80$ °C).

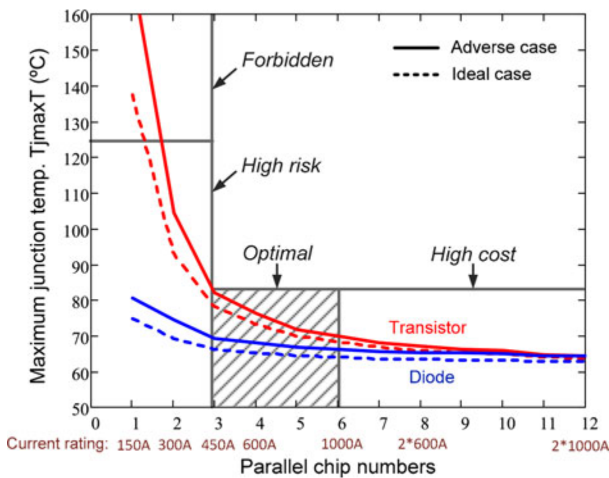


Fig. 24. Different design regions for power devices (conditions in Table I, switching energy in Fig. 7 is used, $T_h = 60$ °C).

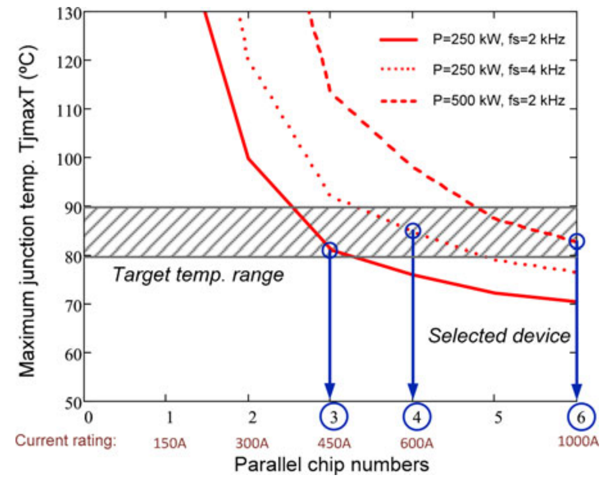


Fig. 25. Thermal-oriented selection of power device (conditions in Table I, switching energy in Fig. 7 is used, $T_h = 60$ °C).

The maximum junction temperature of the transistor and diode in IGBT modules with different chip numbers are summarized in Fig. 23, where the results are compared by PLECS simulation, FEM simulation, and model calculation. It can be seen that both of the circuit and FEM simulation results agree well with the results acquired by the proposed thermal models.

VII. New Design Approaches Based on the Proposed Models

With the proposed loss and thermal models, there are now more design freedom to optimize the efficiency and thermal loading of the power converter. Several new design concepts can thereby be proposed.

In Fig. 24, the maximum junction temperatures of the transistor and diode with relation to the device rating (parallel chip numbers) are shown, where the operation condition of converter is consistent with Table I. In order to be more close to reality, an ideal case (lower 95% bound of power loss in Fig. 7, thickness of thermal grease at 100 μm) and an adverse case (upper 95% bound of power loss in Fig. 7, thickness of thermal grease at 200 μm) are illustrated. More uncertainties of the converter can be also included depending on the required confidence level. As can be seen from Fig. 24, with the established thermal-rating relationship, there are several design regions to achieve quite different loading conditions of power devices: the forbidden region where the device could easily be destroyed with a junction temperature above 125 °C; the high risk region where the junction temperate is loaded at relatively high level with large range of variations; the high cost region where the device is overdesigned with no significant relief of junction temperature; and, finally, an optimal region where the device loading achieves good tradeoff between cost and performance with acceptable loading level and ranges of variation. Consequently, the most suitable rating range of power device for the given converter conditions can be clearly identified and restrained, this is hard to be achieved by the existing design approaches.

After the optimal rating ranges for the power devices are decided, a "thermal-oriented" design for the power device can be realized by the proposed model. As demonstrated in Fig. 25, where a target temperature level between 80 and 90 °C is first predefined, and then three corresponding solutions of device rating can be easily decided for three converter operating conditions.

VIII. Conclusion

The loss and thermal loading of the power devices are critical design considerations for power converters, and they are closely related to the cost, efficiency, and reliability performances. In the existing loss and thermal models, only the electrical loadings are focused and treated as design variables, while the device rating is normally predefined by experience with poor design flexibility.

A more complete loss and thermal model is proposed in this paper, which takes into account not only the electrical loading but also the device rating as input variables. The quantified correlation between the power loss, thermal impedance, and silicon

area of insulated gate bipolar transistor (IGBT) is mathematically established. By this new modeling approach, all factors that have impacts to the loss and thermal profiles of the power devices can be accurately mapped, enabling more design freedom to optimize the efficiency and thermal loading of power converter. The proposed model can be further improved by experimental tests, and it is well agreed by both circuit and finite element method (FEM) simulation results.

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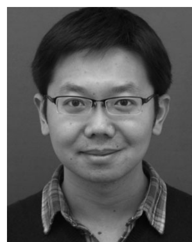

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