Impedance-Source Networks for Electric Power Conversion Part II: Review of Control and Modulation Techniques

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Abstract—Impedance-source networks cover the entire spectrum of electric power conversion applications (dc–dc, dc–ac, ac–dc, ac–ac) controlled and modulated by different modulation strategies to generate the desired dc or ac voltage and current at the output. A comprehensive review of various impedance-source-network-based power converters has been covered in a previous paper and main topologies were discussed from an application point of view. Now Part II provides a comprehensive review of the most popular control and modulation strategies for impedance-source network-based power converters/inverters. These methods are compared in terms of theoretical complexity and performance, when applied to the respective switching topologies. Further, this paper provides as a guide and quick reference for researchers and practicing engineers in deciding which control and modulation method to consider for an application in a given topology at a certain power level, switching frequency and demanded dynamic response.

Index Terms—AC–AC power conversion, ac–dc power conversion, dc–ac power conversion, dc–dc power conversion, impedance source network, modulation and control.

I. INTRODUCTION

IMPEDANCE-source networks provide an efficient means of power conversion from/to a source or load in a wide spectrum of electric power conversion (dc–dc, dc–ac, ac–dc, ac–ac) applications [2], [3]. Since the publication of the first impedance-source network called a "*Z-Source Network*" in 2002, many modified and new impedance-network topologies have been reported in the literature with both buck and boost capabilities, e.g., quasi-Z-source [4]–[6], Γ-Z-source [7]–[9], T-source [10], [11], Trans Z-source [12]–[14], TZ-source [15], LCCT Z-source [16], [17], TSTS Z-source [18], [19], intermediate-transformer-isolated Z-source [20], distributed Z-source [21]–[23], switched inductor/capacitor [24]–[28], capacitor diode assisted [29], [30], embedded Z-source [31]–[33], semi Z-source/quasi Z-source [34], [35], enhanced/improved Z-source [36]–[39], and finally
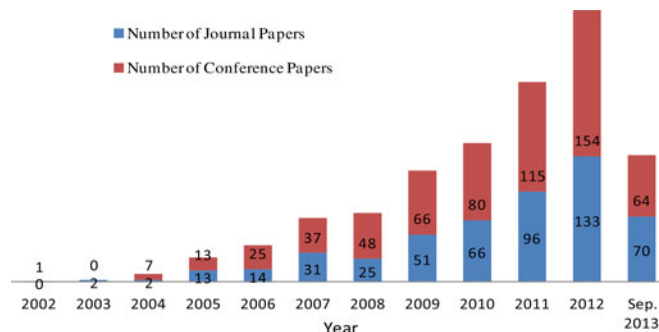
Fig. 1.   Numbers of publications (Total 1113 as of September 2013).

also Y-source [40]. The total number of publications in the relevant fields has exceeded one thousand and opened a new horizon in the field of power electronics and drives. Fig. 1 shows the publication numbers over the last ten years (a total 1113 as of September 2013) for numerous applications.

Fig. 2 shows the general configuration of an impedance-source network for electric power conversion with various impedance networks and possible switching configurations depending on the general as well as the specific application requirements. According to the conversion functionality, four main categories can be sorted 1) dc–dc converters, 2) dc–ac inverters, 3) ac–ac converters, and 4) ac–dc rectifiers. A further breakdown leads to two-level and multilevel topologies [41]–[44], ac–ac and matrix converters [115]–[123], nonisolated and isolated dc–dc converters [124]–[132]. From the Z-source network topology standpoint, it can be voltage-fed or current-fed. Further, impedance networks can be divided based on the magnetics used in the impedance-source network as nontransformer-based [12], [6], [8], [24]–[28], [31]–[37], and transformer-based or coupled-inductor-based [7], [10]–[17], [19], [20], [40] converters. More details about the different types of impedance networks can be found in [1].

Proper amalgamation of various impedance networks with different switching configurations and cells provides numerous topologies with buck, boost, buck-boost, unidirectional, bidirectional, isolated as well as nonisolated converters suitable for various applications. However, different control and modulation strategies are required to control and modulate the converter to get the desired phase, frequency, and amplitude of the voltage and current at the actual point of use. All traditional pulse-width-modulation (PWM) schemes can be used to control the impedance-source converter and their theoretical input–output
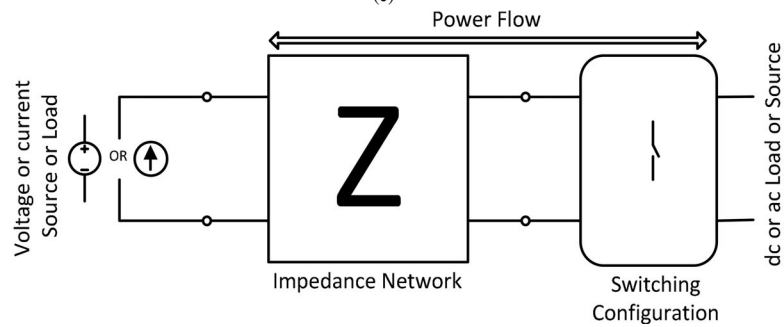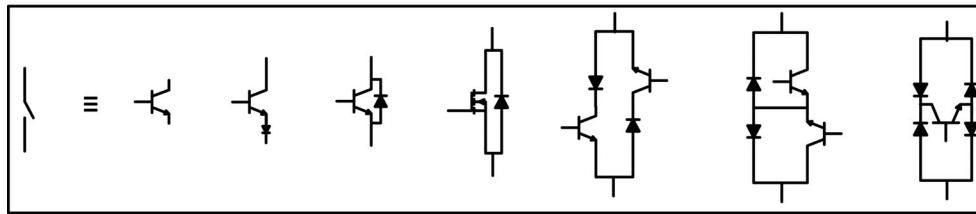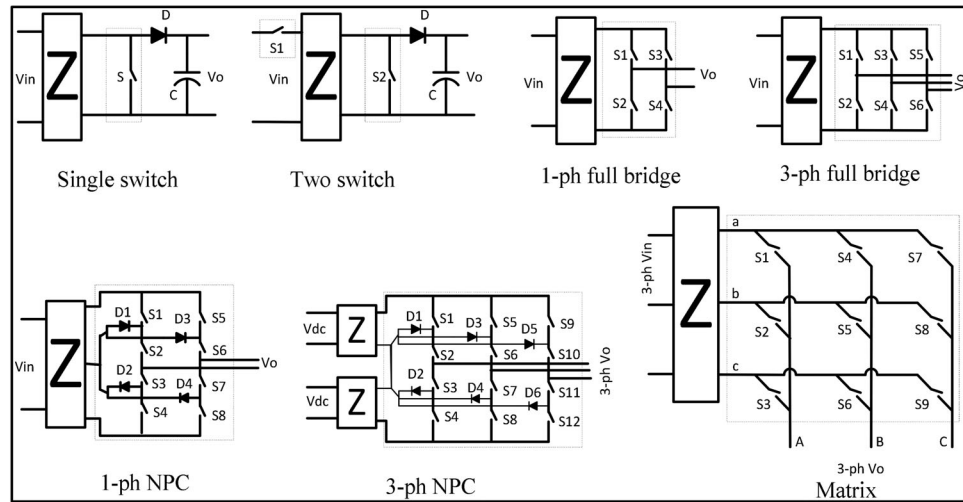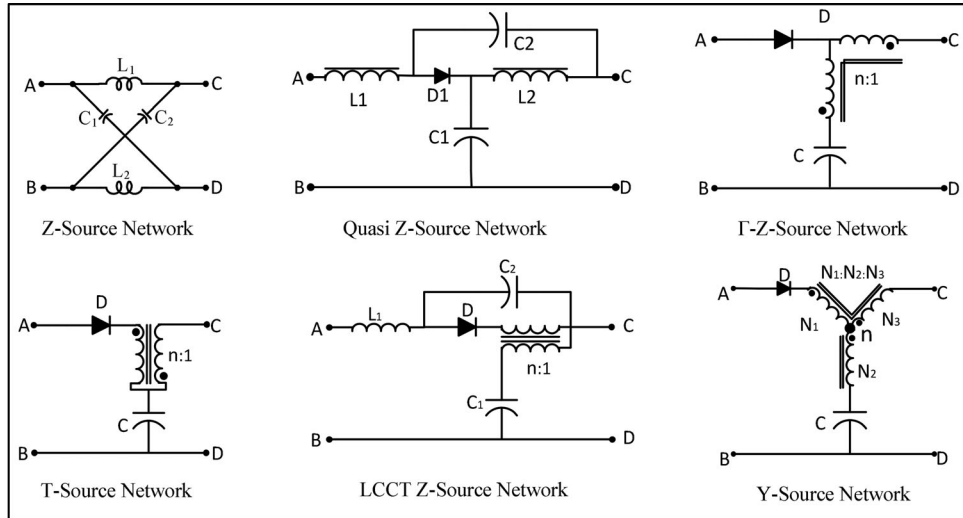
(a)

(b)

(c)

Fig. 2.   General circuit configuration of an impedance-source network for power conversion with some (a) basic impedance-source networks (Z), (b) switching configurations, and (c) different switching cells.
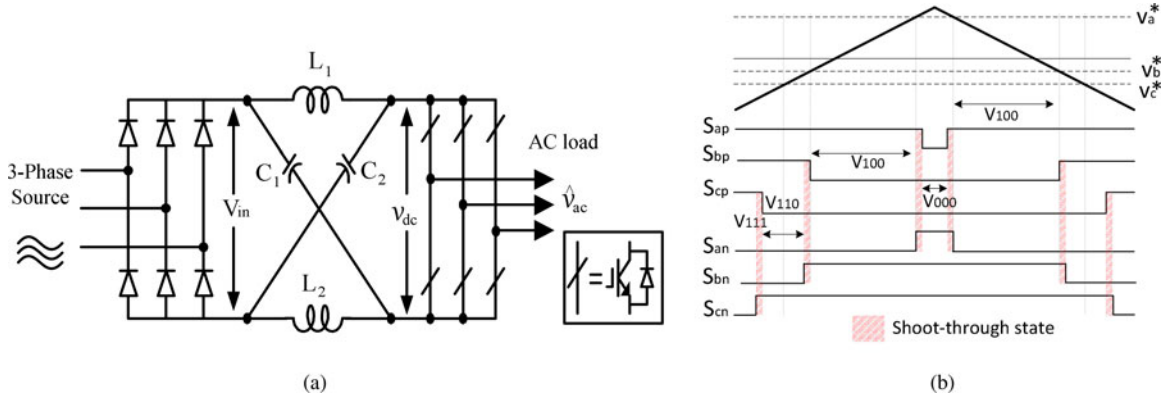
Fig. 3. Basic impedance network illustrating the operation of a) voltage-fed Z-source inverter with (b) modified carrier-based PWM control with evenly distributed shoot-through states among the three phase legs.

relationships still hold true. However, in addition to all states in the traditional modulation techniques, a new state called a "*shoot-through state*" is introduced and embedded in to the modulation strategy for impedance-network-based power converters without violating the volt-sec balance in the operating principle. With the unique feature of these shoot-through states, several new PWM methods modified from sine PWMs (SPWM) [92]–[94] and space-vector modulation (SVPWM) [97]–[106] are developed to control the output voltage. In addition, various control methods for various applications [59]–[84] will be discussed in this paper.

This paper presents a survey of the most relevant control and a modulation technique for impedance-network-based converters/inverters and provides an assessment based on their performance and complexity. The paper is organized as follows: Section II describes the principle of operation, modeling, and control of the impedance-source network for power conversion. Section III presents a classification of various control and modulation techniques based on conversion functionality and further subcategories based on different switching configurations, with a detailed discussions and qualitative comparisons. Section IV concludes the paper.

II. OPERATING PRINCIPLE, MODELING, AND CONTROL

A. Operating Principle

An impedance-source network can be generalized as a two-port network with a combination of two basic passive linear elements, e.g., L and C (a dissipative component R is generally omitted). However, different derivations and modifications of the network are possible to improve the performance of the circuit by adding different nonlinear elements in the impedance network, e.g., diodes, switches, and/or a combination of both. The impedance-source network was originally invented to overcome the limitations of the voltage source inverter (VSI) and the current source inverter (CSI) topologies, which are mostly used in electric power conversion [1].

A three-phase voltage-fed Z-source inverter, as shown in Fig. 3(a), is used as an example to illustrate the operating princi-

ple. The traditional three-phase voltage-source inverter has six active states and two zero states. For the Z-source inverter, several extra shoot-through states are possible by gating on both the upper and lower devices of any one-phase leg, any two-phase legs, or all three-phase legs [2]. Fig. 3(b) shows the basic modified carrier-based PWM control accommodating shoot-through states which are evenly distributed among the three-phase legs. These shoot-through zero states are forbidden in the traditional voltage-source inverter, because they would cause a short circuit across the dc link. The Z-source network and the shoot-through zero states provide a unique buck-boost feature of the inverter.

The peak dc-link voltage ($\hat{v}_{dc}$) across the inverter bridge is a function of the shoot-through duty cycle ($\hat{v}_{dc} = [1 - 2D_{st}]^{-1} V_{in}$). So, theoretically, the output voltage of the converter ($\hat{v}_{ac} = M [1 - 2D_{st}]^{-1} V_{in}/2$, where M is the modulation index and D_{st} is the shoot-through duty cycle) can be varied to any value from 0 to ∞. However, some practical aspects to the performance of the converter need to be considered for large voltage buck or boost operation, e.g., to avoid exceeding the device limitations, stability, etc.

B. Modeling and Control

A Z-source network shows nonminimum phase behavior due to the presence of zero in the right half-plane which could impose a limitation on the controller design. In order to implement a good control strategy, it is imperative to have a good dynamic model of the converter. Various small-signal analyses and mathematical models are presented in the literature to study the dynamic behavior of the system, which then can be implemented in different closed-loop control strategies with different complexities based on various applications [45]–[58].

To derive an accurate small-signal model, various state variables are selected, such as the input current ($i_{in}(t)$), inductor currents ($i_{L1}(t), i_{L2}(t), \ldots$), capacitor voltages ($v_{C1}(t), v_{C2}(t), \ldots$), and load currents ($i_L(t), i_d(t), i_q(t)$). The small-signal model provides the required transfer function for the controller design and provides a detailed view of the system dynamics, helps to understand the system limits, and provides guidelines for system controller design. In general, M
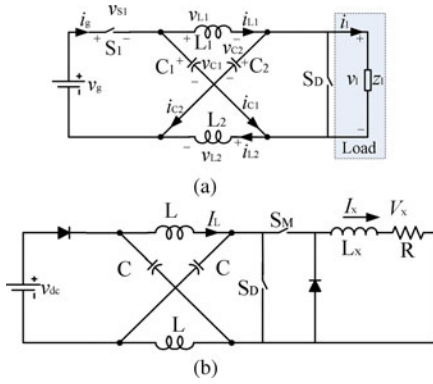
Fig. 4. Simplified equivalent circuit of Z-source converter for small-signal modeling: (a) D_{st} as control variable and (b) D_{st} and M as control variable.

and D_{st} are considered as control variables and the capacitor voltage ($v_{\mathrm{C}}(t)$) or the dc-link voltage ($v_{\mathrm{PN}}(t)$) and the load voltage ($v_x(t)$) as variables to be controlled. Fig. 4(a) shows the simplified Z-source converter model for small-signal analysis, where $v_{\mathrm{C}}(t)$ is controlled using D_{st} as a control variable (control switch S_D). This is the most simplified model, however it does not guarantee tight control of $v_x(t)$, which requires an additional control variable M (control switch S_M) as shown in Fig. 4(b) [51]. In addition to the state variables, the parasitic resistance of the inductor r and the equivalent series resistance (ESR) of the capacitor R also influence the dynamics of the impedance-source networks and hence are also considered during modeling of the converter to analyze the sensitivity of the circuit under parameter variations [46], [48], [53], [58], [67].

Based on some of the above state variables, several small-signal models have been proposed for symmetric or asymmetric ZSI [45], [47], [51] and qZSI [46], [48], [50], [57]. Considering the symmetry of the network (using $v_{\mathrm{C}1}(t) = v_{\mathrm{C}2}(t) = v_{\mathrm{C}}(t)$ and $i_{L1}(t) = i_{L2}(t) = i_L(t)$), a simplified small-signal model is presented in [45] and [59] for ZSI, where the load current is represented by a constant current source. However, such a model describes only the dynamics of the impedance network and fails to describe the dynamics of the ac load. To overcome this disadvantage, a third-order model is presented in [51] and [52] using $v_{\mathrm{C}1}(t) = v_{\mathrm{C}2}(t) = v_{\mathrm{C}}(t)$, $i_{L1}(t) = i_{L2}(t) = i_L(t)$ and $i_1(t)$ as state variables. In this model, the ac side of the inverter is referred to the dc side with R_L load and taking its current as a third-state variable. A similar third-order small-signal model is presented in [50], which considers the dynamics of the input-side current. In this, the current-fed qZSI is analyzed using $v_{\mathrm{C}}(t)$, $i_L(t)$, and $i_{\mathrm{in}}(t)$ as state variables to demonstrate the transient response of the inverter during the motoring and regeneration modes of operation for application in electric vehicles. Subsequent fourth- and higher order small-signal models are also presented for inverters [54] and rectifiers [55] to better understand the dynamics of the input/output (load/source) and the impedance network. However, the complexity in formulating the small-signal model and the control-loop design increases with the increase in state variables. To simplify this, various assumptions (symmetry in impedance network, balanced load) and simplifications (representation of ac load/source by its equivalent dc load/source) are

prevalent in the literature without loss of generality and changes to dynamic performance.

The state-space-averaged small-signal modeling provides a derivation of various control-to-output ($G_{d_0}^{\hat{v}_c}(s)$) and disturbance-to-output ($G_{v_{\mathrm{in}}}^{\hat{v}_c}(s), G_{i_{\mathrm{load}}}^{\hat{v}_c}(s)$) transfer functions, which helps to predict the system dynamics under the influence of various parameter changes. The root locus of the control-to-output transfer function in the s-domain gives a clear map of the converter dynamics. In addition, predicting a right-half-plane (RHP) zero in the control-to-output transfer function is a major advantage of small-signal modeling. The presence of RHP zeros indicates that the nonminimum phase undershoot (the controlled capacitor voltage dips before it rises in response to a D_{st} increase), generally tends to destabilize the wide-band feedback loops, implying high gain instability and imposing control limitations. This means that the design of a feedback loop with an adequate phase margin becomes critical when RHP zeros appear in the transfer function. Various analyses of the pole-zero location and the impact of parameter variations on the converter dynamics are studied considering the wide operating ranges of different sources, e.g., fuel cells and photovoltaics. Fig. 5 shows the locus of the poles and zeros with changes in various parameters such as L, C, D_{st}, R, and r. The impact of these parameter variations on the converter dynamics are summarized in Table I.

The impact of parameter variations on the system dynamics as discussed above can provide direction to designers beforehand to choose component values while considering the design constraints, such as feedback control bandwidth, ripple content, size and cost of components, damping factor, resonant frequency, and overshoot/undershoot in the desired output.

When considering the effect of parameter variations and the effect of poles and RHP zero, several closed-loop control methods are proposed in the literature to achieve a desired performance and to control the dc-link voltage and the ac output voltage of the impedance-source converter [59]–[84]. In all these control methods, there are two control degrees of freedom (D_{st} and M). The dc-link voltage is controlled by the shoot-through duty ratio D_{st} and the output voltage is controlled by the modulation index M.

The dc-link voltage across the inverter bridge can be controlled both directly and indirectly. In the direct dc-link voltage control method [65], the voltage across the inverter bridge is sensed directly by special sensing and scaling circuits as shown in Fig. 6(b). This improves the transient response, enhances disturbance rejection, and simplifies the controller design process. In the indirect method, the capacitor voltage at the impedance network is typically sensed and compared with the desired voltage as shown in Fig. 6(a), (c), and (d). There are two control methods in this category: 1) measurement of capacitor voltage V_C in the impedance source network as shown in Fig. 6(a) [59], [60], and 2) measurement of capacitor voltage V_C and input voltage V_{in} to estimate the peak dc-link voltage as shown in Fig. 6(c) and (d) [61].

In indirect control methods, the peak dc-link voltage becomes uncontrollable, while regulating the shoot-through duty cycle for fast changing input voltages. This effect is unacceptable as
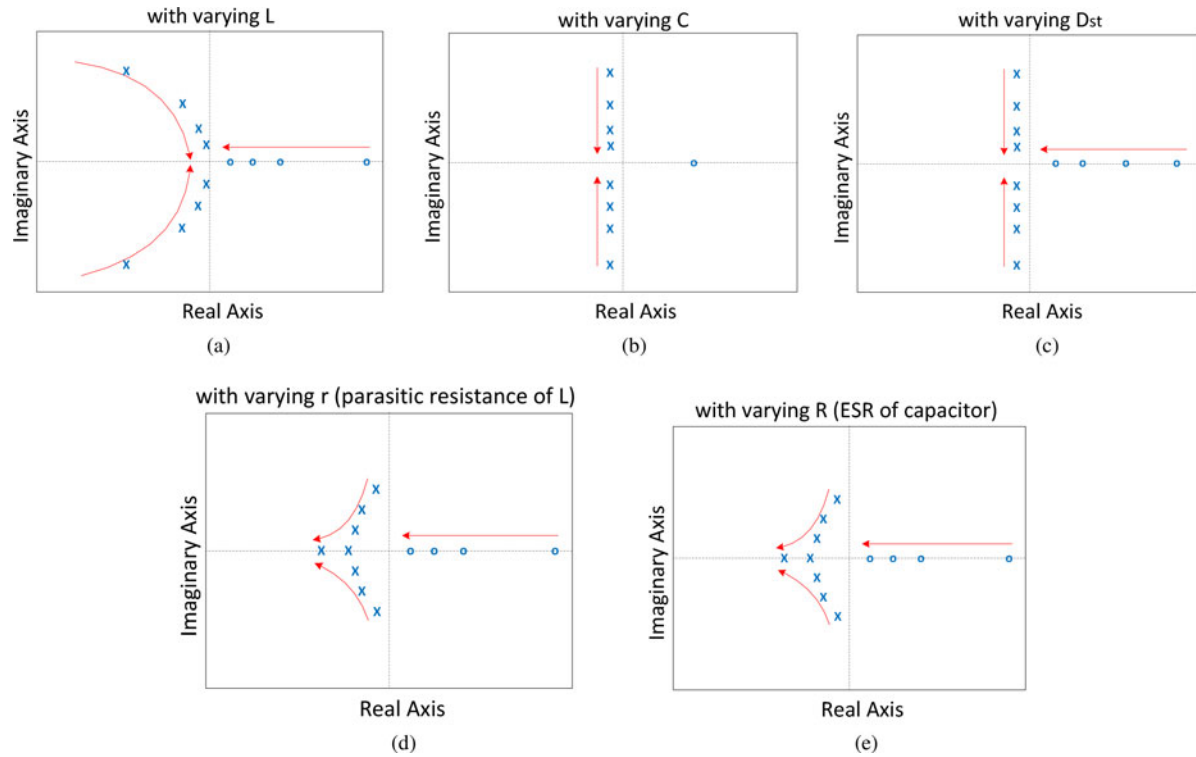
Fig. 5.   Locus of poles and zeros of control-to-output transfer function with varying (a) inductance (L), (b) capacitance (C), (c) shoot-though duty cycle (D_{st}), (d) parasitic resistance of inductor (r) and (e) equivalent series resistance (ESR) of capacitor (R). The direction of the arrow indicates an increasing value.

TABLE I
SUMMARY OF IMPACT OF PARAMETER VARIATIONS ON THE Z-SOURCE CONVERTER DYNAMICS

| Parameter | Change | Effect on Position of | | Impact on System Dynamics |
		Conjugate Poles	RHP Zeros	
Inductance (L)	Increasing	Move toward the imaginary axis	Move toward the imaginary axis	• Increase nonminimum phase undershoot • Increase settling time • Increase oscillatory response • Decrease damping ratio • Decrease natural frequency
Capacitance (C)	Increasing	Move toward the real axis	Constant	• Increase system damping • Increase rise time • Increase system settling time • Decrease natural frequency
Shoot-through duty cycle (D_{st})	Increasing	Move toward the real axis	Move toward the imaginary axis	• Increase nonminimum phase undershoot • Increase system settling time • Decrease natural frequency
Equivalent series resistance (ESR) of capacitor (R)	Increasing	Move toward the real axis	Move toward the imaginary axis	• Increase system damping • Increase nonminimum phase undershoot • Increase current ripple through C
Parasitic resistance of inductor (r)	Increasing	Move toward the real axis	Move toward the imaginary axis	• Increase system damping • Increase non-minimum phase undershoot • Increase voltage ripple across L

it affects the output voltage, which forces a change in the modulation index. This may result in higher semiconductor stress and increases the harmonic distortion [60], [61] in the output waveforms. The peak dc-link voltage is kept constant in the direct measurement technique; however the control scheme becomes more complex, with additional circuitry. To resolve this limitation, the peak dc-link voltage is estimated by measuring the input voltage and capacitor voltage as shown in Fig. 6(c) [voltage mode (VM) and Fig. 6(d) (current programmed mode (CPM)], however additional voltage/current sensors are required. Similar to CPM, a high-performance output voltage control using dual-loop peak dc-link voltage control is presented in [52] and [62] using DSP based on a third-order small-signal model of ZSI.
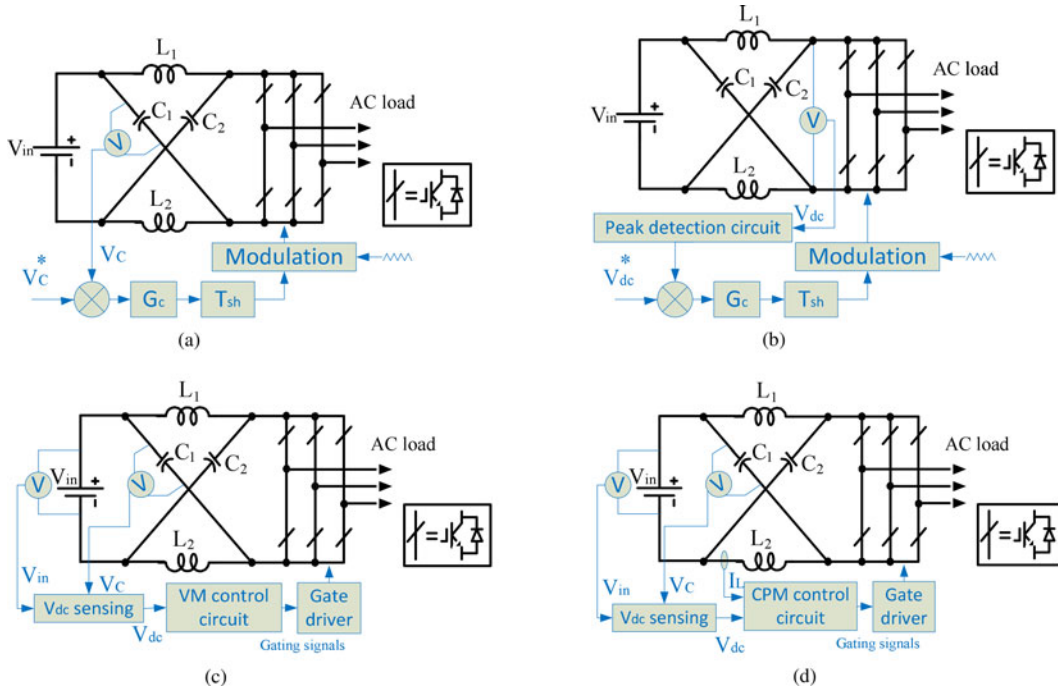
Fig. 6. Control of dc-link voltage by indirect ((a), (c), and (d)) and direct methods (b). (a) Capacitor voltage control. (b) Direct dc-link voltage control. (c) Voltage mode control (VM). (d) Current-programmed mode (CPM).
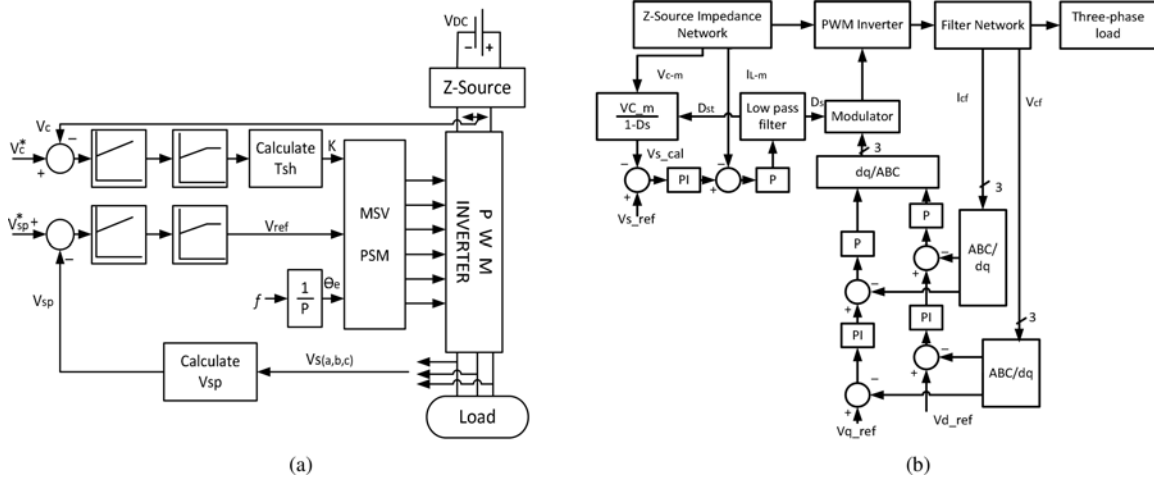

Fig. 7. Indirect dc-link voltage controller modules with two degrees of freedom: (a) controller for both dc boost and ac output voltage of Z-source inverter [66] and (b) multiloop closed loop controller [67].

Compared to single-loop capacitor voltage control, the dual-loop technique effectively regulates the inductor current during transient events and also extends the stability limit of the controller.

All the aforementioned indirect dc-link voltage controls are comparatively simple and easy to implement, however a driver algorithm is introduced in the controller, which may increase the complexity of the design. A feedforward plus feedback control strategy [63] performs rough regulation with feedforward control of the input voltage, and constant peak dc-link voltage can be obtained under varied input voltages. In this,

the input voltage is compared with the required peak dc-link voltage to calculate D_{st}, and the peak value of output voltage is used to regulate M using a PI controller. Implementation of this control strategy is simple without introducing the driver algorithm in the calculation and has inherent stability without considering the system model of the impedance network. A precise controller using a feed-forward controller is also designed considering the load current as a state variable in [64] for bidirectional qZSI. This greatly enhances the input-voltage disturbance rejection and the oscillation suppression capability of the controller.
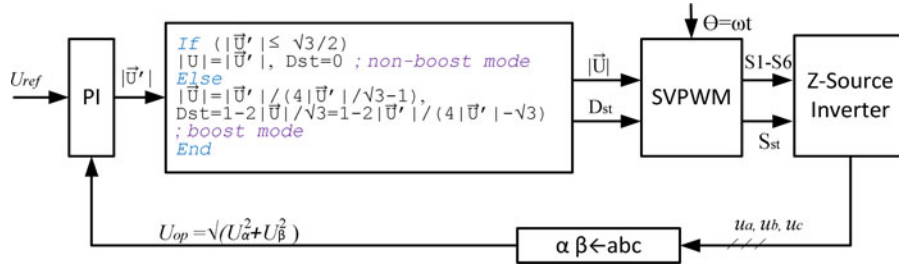
Fig. 8. Unified control block diagram for the Z-source inverter with one control variable.
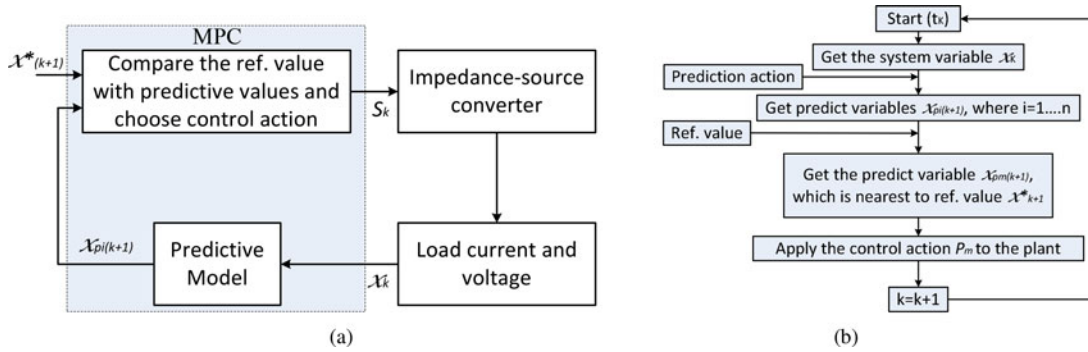

Fig. 9. Implementation of (a) model predictive control to impedance-source network with (b) corresponding flowchart.

Fig. 7 shows a block diagram of two popular closed-loop voltage control methods of ZSI which consist of both dc-link control and ac output control [66]–[68], [77]. An example of such control is demonstrated in [69] for electric-vehicle motor drives using a bidirectional Z-source inverter (BZSI) and in [70] for connecting a BZSI to the grid during the battery charging/discharging operation mode utilizing a proportional plus resonance (PR) controller. In both control methods, the capacitor voltage is controlled by regulating the shoot-through duty cycle D_{st} and the output voltage is controlled by regulating the modulation index M, using separate control loops with P and/or PI controllers. However, both control parameters are dependent on each other, as change in one parameter imposes a limitation of the changeability of the other due to the insertion of a shoot-through time inside the null period. Putting a maximum limit on the control variable could mitigate this limitation.

A hybrid controller using a neural network and the one used in [65] is also implemented in [71], where model predictive control is used to determine the neural-network plant model. The neural-network controllers are trained offline and then used to predict the system response. This method improves the system response, however at the cost of increasing complexity.

To keep enough voltage control margin, the shoot-through duty ratio D_{st} must be less than 1–M (or $M < 1 - D_{st}$) for the simple boost, which leads to a lower utilization of the input dc voltage and a higher voltage stress across the switches. To address this issue, a unified control technique is presented in [72] (see Fig. 8) with only one control degree of freedom

(M or D_{st}). The ac output voltage of the inverter is controlled by keeping the capacitor voltage as a variable. This control method is simple and easy to implement with only one sensor.

Similar control strategies are retrofitted to various applications, e.g., grid-connected photovoltaics [73]–[76], distributed generation [4], [77], excitation field control for synchronous machines [78], and single-phase uninterruptible power supply [79].

A unique approach using model predictive control (MPC) for multisystem variable regulation has been used for ZSI [80] and qZSI [81] to regulate load voltage/current, inductor current, and capacitor voltage. MPC is a powerful control method, which does not require any kind of linear controller (PI or PID) or modulation technique. It provides a quick reference-tracking capability with a simple feedback control method and can help to reduce the nonminimum phase effect during the transient process. Fig. 9 shows the general MPC control for a Z-source converter, with an accompanied flowchart. In this method, the system variable of the impedance-source converter (x_k), load current/voltage, is measured and is fed back and used to evaluate a discrete predictive model of the system. Values from the predictive model close to the reference value are selected by formulating a cost function, which is then used to generate a corresponding switch signal (S_k) to drive the impedance-source converter. The transient-state inrush current and the resonance in the impedance network due to L and C are suppressed using this method, which helps to protect the switching devices from voltage and current surges.

TABLE II
SUMMARY OF VARIOUS CONTROL METHODS FOR IMPEDANCE-SOURCE CONVERTERS

Reference No.	Control Method	Sense Signal	Controller Type	Mathematical Model	Control Variable	Features
[51]	Indirect	v_c and $v_{o(a,b,c)}$	Single-loop nonlinear (gain scheduling + state feedback) control	State-space averaged small-signal model $x(t) = [v_c\, i_L\, i_l]'$	D_{ST} and M	• Controller is very stable in steady state operation • Not suitable for rapidly varying reference point • Complex control algorithm
[59]	Indirect	v_c	Single-loop using PID controller	State-space averaged small-signal model $x(t) = [v_{c1}\, v_{c2}\, i_{L1}\, i_{L2}]'$	D_{ST}	• Modified simple boost control is implemented • Consider dynamics of impedance network only
[60]	Direct	$v_{dc-link}$	Single-loop using PID-like fuzzy controller	State-space averaged small-signal model $x(t) = [v_{c1}\, v_{c2}\, i_{L1}\, i_{L2}]'$	D_{ST}	• Modified simple boost control is implemented • Improve transient response • Enhances disturbance rejection • Simplifies controller design
[52], [61]	Indirect	VM mode: v_c and v_{in} CPM mode: v_c, v_{in} and i_L	Single-loop using PID controller Dual-loop with PI controller	State-space averaged small-signal model $x(t) = [v_{c1}\, v_{c2}\, i_{L1}\, i_{L2}\, i_l]'$		• Estimate $v_{dc-link}$ by measuring v_C and v_{in} • Good input and load disturbance rejection • Order of system is reduced by one in CPM, which increases the phase margin and offers simple compensator design
[62], [70]	Indirect	v_c, v_{in} and i_L	Dual-loop with PI controller	State-space averaged small-signal model $x(t) = [v_c\, i_L\, i_l]'$	D_{ST}	• Dual-loop capacitor voltage control achieves better steady and transient performance and stability compared to single-loop control • Enhances disturbance rejection
[63]	Indirect	v_{in} and $\hat{v}_o$	Single-loop PI controller with saturation	NA	D_{ST}	• Simple and easy to implement • Performs rough regulation • Did not consider the impact of impedance network (RHP pole etc.) in stability
[64]	Direct	$v_{dc-link}$	Single-loop using PID controller	State-space averaged small-signal model $x(t) = [v_{c1}\, v_{c2}\, i_{L1}\, i_{L2}]'$	D_{ST}	• Modified simple boost control is implemented • Improves transient response • Enhances disturbance rejection • Simplifies controller design
[66], [71]	Indirect	v_c and $v_{o(a,b,c)}$	Single-loop using PI controller	NA	D_{ST}	• Capacitor voltage is linearly controlled by $K = v_C/v_{in}$ • Enhances disturbance rejection from load and input variations
[67], [68]	Indirect	v_c, i_L, $v_{cf(a,b,c)}$ and $i_{cf(a,b,c)}$	Multi-loop control with P for inner current and PI for outer voltage loop	State-space averaged small-signal model $x(t) = [v_{c1}\, v_{c2}\, i_{L1}\, i_{L2}]'$	D_{ST} and M	• Mitigate transfer of dc-side disturbance to ac side • Excellent reference tracking and rejection of disturbances arising from both input and output sides
[72]	Indirect	$v_{o(a,b,c)}$	Unified control	NA	D_{ST} or M	• One degree of freedom • Linear control of output voltage using unified voltage vector • Low cost and ease of digital implementation
[72]	Indirect	v_{in}, i_{in}, $v_{o(a,b,c)}$ and $i_{o(a,b,c)}$	Single-loop using PI controller	State-space averaged small-signal model $x(t) = [v_{c1}\, i_{L1}\, i_{L2}\, i_b]'$	D_{ST}	• Battery-assisted qZSI control which controls the state of charge (SOC) of the battery and the power injected into the grid
[80], [81]	Indirect	$v_{o(a,b,c)}$ or $i_{o(a,b,c)}$	Model predictive control (MPC)	NA	Switching state vector (S)	• Quick reference tracking capability • Offers multi-system variable regulation considering different system constraints • Supresses inrush current and resonance in the impedance network
[82], [83], [84]	Indirect	v_{in}, i_{in}, $v_{o(a,b,c)}$	Sliding mode (SM) control	Large-signal model $x(t) = [i_{L1}\, i_{L2}\, v_{c1}\, v_{c2}\, i_b]'$	D_{ST} and M	• Controller designed from large-signal model of converter • Stable and robust to large parameter, line and load variations • Fast response, less current ripple when subject to large load/source variations • Complex control algorithm

Inspired by the conventional variable-frequency sliding-mode (SM) control, a fixed-frequency sliding-mode control is also presented in [82]–[84] for ZSI and qZSI to control M and D_{st}. The SM controller is stable and robust to large parameter, line, and load variations as it is designed from a large-signal model of the converter whereas to conventional current- and voltage-mode controllers are designed based on linearized small-signal models. This feature of the SM controller has its best niche in applications where a widely varying load and source are connected to the impedance-source converter, e.g., intermit-tent sources such as PV/fuel cells connected to widely varying loads.

Table II summarizes various control methods for an impedance-source converter, with its control variables and features.

III. GENERAL CLASSIFICATION OF MODULATION TECHNIQUES

Proper modulation of an impedance-source converter requires careful integration of the selective shoot-through process with
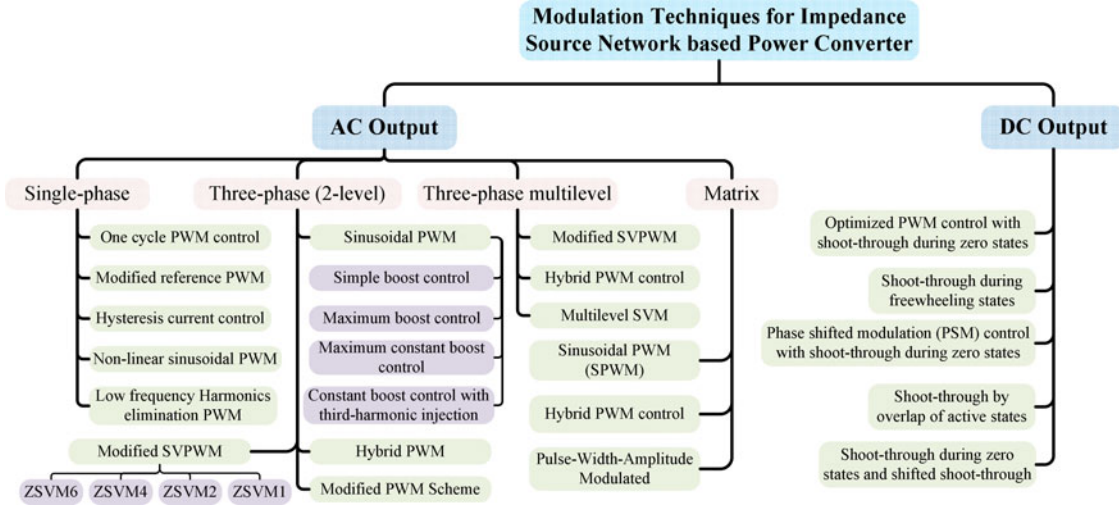
Fig. 10. Categorization of modulation techniques for impedance-source network-based power converter.
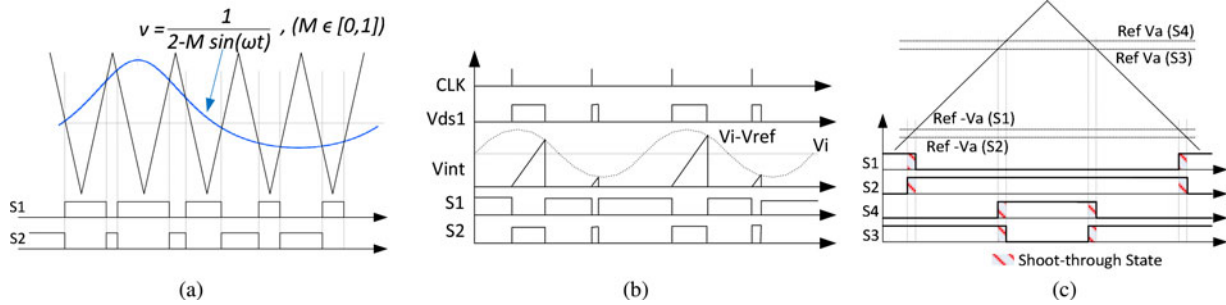

Fig. 11. Generation of switching signal for 1-ph Z-source inverter using (a) nonlinear sinusoidal pulse width modulation (SPWM), (b) one cycle control method, and (c) modified space vector modulation SVM.

the classical switching concepts to achieve maximal voltage boost, minimal harmonic distortion, low semiconductor stress, and a minimum number of devices commutation per switching cycle.

Fig. 10 shows a broad categorization of the impedance-network-based power converter using different switch configurations as shown in Fig. 2. Proper amalgamation of these different topologies with impedance-source networks gives a wide range of unique power converter topologies ranging from medium voltage and power to high voltage and power. In addition, using these switching configurations, both unidirectional/bidirectional as well as isolated/nonisolated converters can be implemented for dc–dc, dc–ac, ac–dc, and ac–ac systems to satisfy needs in numerous applications.

A. Modulation Techniques for Single-Phase Topologies

Various modulation techniques are presented in the literature to modulate and control the output voltage of single-phase impedance source inverters having two switches (semi-Z-source, quasi-Z-source) [35], [85], four-switch intermediate

H-bridge topologies [35], [87], [88], or embedded Z-source [35], [86] for different applications. A two-switch topology offers a simple and cost-effective solution for a single-phase grid-connected photovoltaic system. Two modulation techniques are prevalent in the literature to control and modulate the two switches of a single-phase Z-source/quasi-Z-source to get the desired output voltage, namely one-cycle control [85] and nonlinear sinusoidal pulse-width modulation (SPWM) [35].

The voltage gain of the semi-Z-source/quasi-Z-source converter is not a straight line as with a full-bridge inverter. So, instead of a sinusoidal reference signal ($v = V \sin \omega t$), a nonlinear sinusoidal reference signal $v = [2 - M \sin \omega t]^{-1}$ is compared with the carrier signal to generate the gate drive signal for the two switches as shown in Fig. 11(a). A similar modulation technique is also adopted in a single-phase embedded Z-source inverter with four switches [86].

A one-cycle control method is adopted to control a single-phase semi-Z-source topology in [85]. In this control method, two switches work in a complementary fashion where the clock signal (CLK) is used to turn-on any one switch. The turn-on time

TABLE III
COMPARISONS OF VARIOUS MODULATION TECHNIQUES FOR SINGLE-PHASE TOPOLOGIES

Modulation Technique	Switching Topology	No. of Switches	Peak Stress on Switching Devices	Modulating Signal	Range of M and D_{st}	Features
Nonlinear SPWM [35]	Semi Z-Source	2	$\hat{V}_{SW} = 3V_{in}$ $\hat{I}_{SW} = 3I_{in}$	One quasi-sinusoidal modulating signal $v = [2 - M\sin\omega t]^{-1}$	$0 \leq M \leq 1$ and $0 \leq D \leq 1$	• Eliminate leakage current • Cost-effective solution compared to H-bridge • High device stress • Limited to two switch impedance network topologies
One-cycle	Single-phase	2	$\hat{V}_{SW} = 3V_{in}$ $\hat{I}_{SW} = 3I_{in}$	One sinusoidal modulating signal $(V_{in} - v_{ref})$, where $v_{ref} = V_m \sin\omega t$	$1/3 \leq D \leq 1$	• Constant frequency control can be achieved Does not need an accurate model of the converter • High device stress • Limited to two switch impedance network topologies
Carrier-Based PWM [87]	2-leg H-bridge	4	$\hat{V}_{SW} = BV_{in}$, $\hat{I}_{SW} = B\hat{i}_o$ where $B = [1 - 2D_{st}]^{-1}$	Two sinusoidal modulating signals $v = M\cos\omega t$, for first leg and $v = -M\cos\omega t$ for second leg	$0 \leq M \leq 1$ and $0 \leq D_{st} \leq 0.5$	• Modulation technique can be extended to N-phase inverter.
Hysteresis-Band Current Control [88]	2-leg H-bridge	4	$\hat{V}_{SW} = BV_{in}$, $\hat{I}_{SW} = B\hat{i}_o$ where $B = [1 - 2D_{st}]^{-1}$	A band of sinusoidal modulating signals $v_{ref} = V_m \sin\omega t$	$0 \leq D_{st} \leq 0.5$	• Suitable for symmetric or asymmetric network topologies • Pure sinusoidal output current • Simple, robust and insensitive to load parameter changes • Nonuniform switching leads to higher device stress • Switching frequency is not regular

of the switch is determined by the integrated voltage across the switch, and when it reaches the sinusoidal signal $(v_i - v_{ref})$, the integrator is reset and the switch turns OFF as shown in Fig. 11(b). This control method has the ability to reject input perturbations and is insensitive to the system model, which provides a high-efficiency constant-frequency control.

A standard carrier-based PWM is modified in [87] for a single-phase H-bridge topology. A shoot-through state is placed instead of null state without altering the normalized volt-sec average voltage as shown in Fig. 11(c). The duration of each active state in a switching cycle is kept the same as in the traditional SPWM. Therefore, the output waveforms are still sinusoidal; however, they are boosted to the desired level by properly controlling the shoot-through time period. The paper extends the modulation concepts to the more complex three-phase H-bridge and four-phase H-bridge topologies for a voltage-fed Z-source inverter in both continuous and discontinuous modes.

In addition to the above modulation and control method, a hysteresis-band current control is implemented in [88] for a H-bridge. The performance is tested for both symmetrical and asymmetrical Z-source networks. Similar to the modulation technique used in [93] and [94] for a three-phase inverter, a low-frequency harmonic-elimination PWM technique is implemented in [89] for a single-phase inverter to reduce the output harmonic distortion and size of passive components found in the impedance network. Another cost-effective solution using two switches is presented in [90] and is modulated by a conventional bipolar sinusoidal PWM technique. A sawtooth-carrier-based SPWM is also presented in [91] for a single-phase module

integrated inverter designed for a photovoltaic system. Compared to the conventional triangular-carrier-based method, this sawtooth-carrier method reduces the commutation times of the switches and helps to improve efficiency of the converter during the boost mode. This modulation method, strictly a carrier-based technique, together with other methods reviewed for single-phase impedance network-based converters, is summarized in Table III.

B. Modulation Techniques for Three-Phase Topologies (2 Level)

To date, several modified PWM control techniques for an impedance-source inverter have been proposed in the literature with the aim of achieving a wide range of modulation, less commutation per switching cycle, low device stress, and simple implementation. Modulation techniques for three-phase H-bridge topologies (2 level) are broadly categorized as sine PWM (SPWM) and space-vector PWM (SVPWM). However, several other modifications can be found in the literature and will be discussed briefly as follows.

SPWMs include simple boost control, maximum boost control, maximum constant boost control, and constant boost control with third-harmonic injection [92]–[95]. A comparison of some of these SPWMs is presented in [96] in terms of the voltage gain. Simple boost control is the most basic and is derived from the traditional sinusoidal PWM where a carrier triangular signal is compared to the three-phase reference signal for sinusoidal output voltage and two straight lines (V_p and V_n) to create
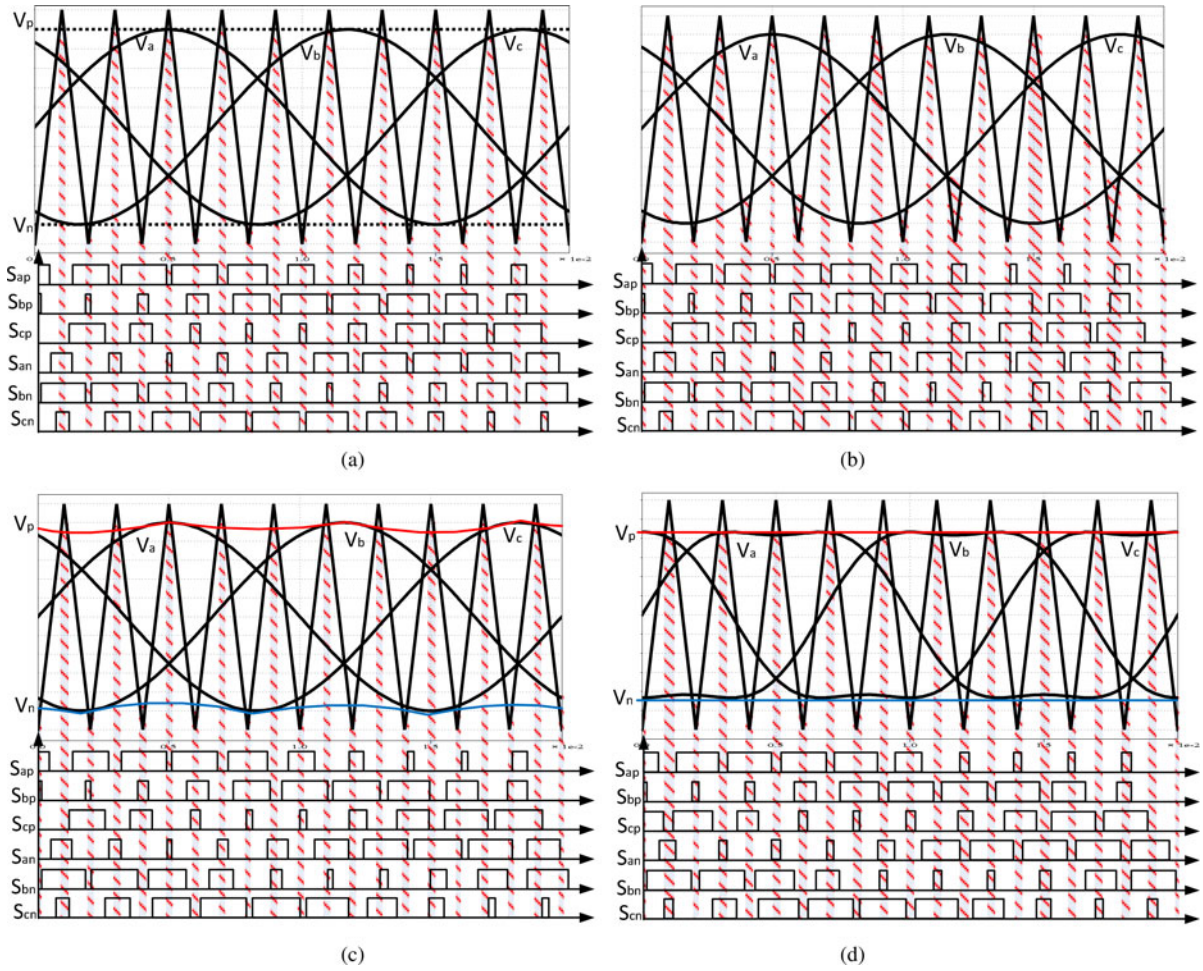
Fig. 12. Sine wave PWM (a) simple boost control, (b) maximum-boost control, (c) maximum-constant-boost control, and (d) constant-boost control with 1/6th of third harmonic injection (\\\→Shoot-through period).

shoot-through for voltage boost as shown in Fig. 12(a). The disadvantage of this modulation technique is a decrease of the modulation index with an increase of the shoot-through range. The maximum shoot-through duty ratio of the simple boost control is limited to $D_{\text{st,max}} = (1 - M)$ which limits the boost factor to $B = [2M - 1]^{-1}$. As a result the device stress increases for the application, which requires a higher voltage boost. To address this issue, a maximum-boost PWM control method is presented in [92]. This modulation technique maintains six active states unchanged from those of the traditional carrier-based PWM method; however, it utilizes all zero states to make shoot-through states as shown in Fig. 12(b). These increase the range of the boost factor $B = \pi \left[3\sqrt{3}M - \pi \right]^{-1}$ compared to using simple boost, which reduces the device stress.

However, due to the variable shoot-through time intervals, low-frequency ripple components are present in the capacitor voltage and inductor current, which increases the size and cost of the components in the impedance network. To achieve a constant shoot-through duty ratio and a maximum boost factor, a maximum constant-boost PWM control method is proposed in [93] and [94] which eliminates the low-frequency harmonic component in the impedance-source network. Fig. 12(c) illustrates

the switching waveforms of the maximum-constant-boost PWM control. The range of the modulation index is extended from 1 to $2/\sqrt{3}$ by injecting a third-harmonic component with 1/6 of the fundamental component magnitude to the three-phase-voltage references. In this modulation technique, two straight lines V_p and V_n are required to generate a shoot-through time period as shown in Fig. 12(d). How this maximum constant boost technique compared with other SPWM techniques is summarized in Table IV.

Besides SPWM, space vector pulse width modulation (SVPWM) has similarly been proven to be an effective modulation technique for traditional inverter topologies as it effectively reduces the commutation time of the switches, reduces the harmonic content in the output voltage/current, and better utilizes the dc-link voltage, and consequently reduces the voltage stress and switching loss. This benefit encourages researchers and engineers to retrofit SVPWM for various impedance source inverters. However, proper insertion of the shoot-through state in the switching cycle without altering the volt-sec balance is crucial to reduce additional commutation time of the switches and corresponding switching loss. Various SVPWM techniques are presented in the literature, e.g.,

TABLE IV
COMPARISONS OF VARIOUS SPWM TECHNIQUES IN THREE-PHASE Z-SOURCE BRIDGE INVERTERS

Parameters	Simple Boost	Maximum Boost	Maximum Boost with Third Harmonic Injection	Maximum Constant Boost	Maximum Constant Boost With Third Harmonic Injection
$\bar{T}_o/T$	$1-M$	$\dfrac{(2\pi-3\sqrt{3}M)}{2\pi}$	$\dfrac{(2\pi-3\sqrt{3}M)}{2\pi}$	$1-\dfrac{\sqrt{3}}{2}M$	$1-\dfrac{\sqrt{3}}{2}M$
Boost Factor (B)	$\dfrac{1}{2M-1}$	$\dfrac{\pi}{3\sqrt{3}M-\pi}$	$\dfrac{\pi}{3\sqrt{3}M-\pi}$	$\dfrac{1}{\sqrt{3}M-1}$	$\dfrac{1}{\sqrt{3}M-1}$
Voltage Gain (G)	$\dfrac{M}{2M-1}$	$\dfrac{\pi M}{3\sqrt{3}M-\pi}$	$\dfrac{\pi M}{3\sqrt{3}M-\pi}$	$\dfrac{M}{\sqrt{3}M-1}$	$\dfrac{M}{\sqrt{3}M-1}$
Voltage Stress of the Switch	$(2G-1)V_o$	$\dfrac{3\sqrt{3}G-\pi}{\pi}V_o$	$\dfrac{3\sqrt{3}G-\pi}{\pi}V_o$	$(\sqrt{3}G-1)V_o$	$(\sqrt{3}G-1)V_o$
Maximum(M)	1	1	$2/\sqrt{3}$	1	$2/\sqrt{3}$

TABLE V
COMPARISONS OF VARIOUS SVM TECHNIQUES IN THREE-PHASE BRIDGE INVERTERS

Parameters	ZSVM1	ZSVM2	ZSVM4	ZSVM6
$(D_{\mathbf{max}})$	$(1-3\sqrt{3}M/(2\pi))/2$	$1-3\sqrt{3}M/(2\pi)$	$3(1-3\sqrt{3}M/(2\pi))/4$	$1-3\sqrt{3}M/(2\pi)$
$(B_{\mathbf{max}})$	$2\pi/(3\sqrt{3}M)$	$\pi/(3\sqrt{3}M-\pi)$	$4\pi/(9\sqrt{3}M-2\pi)$	$\pi/(3\sqrt{3}M-\pi)$
$(G_{\mathbf{max}})$	$2\pi/(3\sqrt{3})$	$\pi M/(3\sqrt{3}M-\pi)$	$4\pi M/(9\sqrt{3}M-2\pi)$	$\pi M/(3\sqrt{3}M-\pi)$
Voltage Stress of the Switch, (V_s)	$(2\pi/(3\sqrt{3}M))V_{\text{in}}$	$(3\sqrt{3}G/\pi-1)V_{\text{in}}$	$(9\sqrt{3}G/2\pi-2)V_{\text{in}}$	$(3\sqrt{3}G/\pi-1)V_{\text{in}}$
No. of shoot-through per switching cycle	2	4	6	6
Current ripple in the inductor(ΔI_L)	Highest	Medium	Low	Low

ZSVM2 [97], ZSVM4 [98], [99], and ZSVM6 [100]. A comparison of various SVM techniques is shown in Table V and presented in [101] and [102] experimentally based on various performance analyses along with two new modifications, i.e., ZSVM1-I and ZSVM1-II. Modified SVPWM techniques are also being used to reduce the common mode voltage and leakage currents for photovoltaic systems [103], [104] and motor drives [105].

A hybrid PWM strategy is subsequently proposed to reduce the algorithm calculation by combining the theory of SVPWM and triangular-comparison PWM for a three-phase-three-wire system [106] and a three-phase-four-wire system [107]. One-cycle control similar to Fig. 11(b) is also proposed in [30] for three-phase ZSI/qZSI using H-bridge switching topology. This is complemented by a random PWM scheme proposed in [108] for a Z-source inverter whose purpose is to reduce common mode voltage when used in an ac motor drive. For current fed qZSI, [109] also proposes a modified SVPWM scheme for achieving higher input current utilization, lower switching loss, lower total harmonic distortion, and lower switching spikes across switching devices compared to traditional SVPWM [6], [110]. These advantages are attributed to the full-wave symmetrical modulation (FSM) applied whose outcome is only one short zero state vector $(\vec{I}_7, \vec{I}_8, \vec{I}_9)$ utilized in each switching period.

C. Modulation Techniques for Three-Phase Multilevel Topologies

PWM schemes for Z-source NPC inverters are developed from classical three-level SVPWM modulation concepts using 2-D vectorial representations with "origin shifting." However, correct integration of the shoot-through state sequence with the classical PWM is essential for proper Z-source NPC operation, as some of the vectors can cause a short circuit across the full dc-link (FDCL) which then results in zero voltage output. It is important to maintain the normalized volt-sec balance while sequencing the shoot-through states to accurately reproduce the desired three-phase sinusoidal voltages. In addition, careful integration of shoot-through with the conventional switching sequences is required to achieve maximal voltage-boost, minimal harmonic distortion, lower semiconductor stress, and a minimal number of device commutations per switching cycle. To achieve this, there are various continuous and discontinuous PWM schemes reported in [43] for controlling Z-source NPC inverter with two impedance networks at its input side. The former modulation scheme is divided into two, i.e., continuous edge insertion (EI) PWM with symmetrical voltage boost and continuous modified reference (MR) PWM with minimal device commutation, and the latter modulation scheme is also divided into two, i.e., conventional 60°-discontinuous PWM and origin-shifted 60°-discontinuous PWM with reduced common

TABLE VI
COMPARISONS OF VARIOUS MODULATION TECHNIQUES FOR THREE-PHASE MULTILEVEL TOPOLOGIES

Ref. No.	Modulation Technique	Topology	No. of Switching	Device Stress	Features
[43]	Continuous	NPC with two Z-source networks	8 (in EI) 6 (in MR)	medium	• Symmetrical/Balanced voltage boosting per switching cycle • Small current ripple
	Discontinuous	NPC with two Z-source networks	4	high	• Balanced voltage boosting only per 60° cycle • Large current ripple and inductor size Low common mode voltage. • Low common mode voltage.
[41]	NTV	NPC with two Z-source networks	6	medium	• Completely eliminates the common-mode voltage.
	RCM	NPC with two Z-source networks	6	Medium	• Reduces common mode voltage.
[112]	FDCL	NPC with single Z-source network	4	Medium	• Suitable for high switching frequency (due to minimum commutation) • Not particularly suitable for low-frequency operation • Fewer components • Low cost design
	PDCL	NPC with single Z-source network	4	Medium	• Suitable for high switching frequency (due to minimum commutation). • Not particularly suitable for low-frequency operation • Fewer components • Low cost design • Comparatively better output waveforms
[74], [114]	MSVM	Single-phase qZSI-cascaded multilevel Inverter (CMI)	6	Low	• Independent control of MPPT for each module separately. • Higher input-voltage utilization • Flexible to n-level (CMI)

mode switching. The device commutation count with EI PWM is the maximum of eight, which reduces to six with the continuous modified reference technique. The number further reduces to a minimum of four with the discontinuous PWM technique is opted for. However, with the same shoot-through duty ratio, the reduced number of shoot-through per switching cycle in the discontinuous scheme will produce lower common-mode voltage but higher inductor current ripples which significantly increase the size of the passive component in the impedance network. A detailed comparison of continuous and discontinuous PWM schemes is provided in [43].

A nearest three-vector (NTV) modulation principle and reduced common-mode switching (RCM) is proposed in [41] to minimize harmonic distortion, device commutation, and common mode voltage of the inverter. A hybrid PWM strategy similar to [106] for a two-level Z-source inverter is implemented for the Z-source NPC topology [111] to reduce its algorithm calculation by combining the theory of SVPWM and triangular-comparison PWM. A reduced component count Z-source NPC converter with modified modulation technique is reported in [112] and [113] using a single Z-source network. This topology reduces the requirement of an additional impedance network to create a neutral point as explained in [41], [43], and [111]. The modulation scheme is modified to create a FDCL and a partial dc-link (PDCL) shoot-through state to boost the output voltage without increasing the commutation time as in the conventional NPC modulation techniques [41], [43]. An effective control method for a cascaded quasi Z-source inverter using multilevel space vector modulation (MSVM) is presented in [74] for single phase and in [114] for three-phase to generate seven-level voltage. This control scheme achieves independent

control of maximum power point (MPPT) for each photovoltaic panel and also balances the dc-link voltage across each H-bridge inverter to accomplish premium power quality for grid integration of photovoltaic panels for low switching frequency design. A summary of comparison of various modulation techniques for three-phase multilevel topologies is given in Table VI.

D. Modulation Techniques for Matrix Converter Topologies

The matrix converter is a direct ac–ac converter with sinusoidal input/output waveforms and a controllable input power factor. Based on the conventional matrix switching topologies [115], various impedance-network-based direct [116]–[118] and indirect [119]–[123] matrix converter topologies are adopted in the literature for overcoming issues like improved reliability and higher voltage boost. With some modifications made to the conventional modulation techniques (SVPWM, carrier-based PWM, PWAM, etc.) to incorporate the shoot-through state, various modified modulation techniques are implemented to control direct and indirect impedance-network-based matrix converters. The traditional carrier-based sinusoidal PWM (SPWM) [92]–[95] is applied to control and modulate various Z-source and quasi-Z-source direct matrix converters with a few modifications, e.g., four control strategies: simple maximum-boost control, maximum-boost control, maximum-gain control, and hybrid minimum-stress control are proposed in [116] and [117]. In the simple maximum-boost control, the modulation index is limited to $M = 0.5$ which means that the maximum voltage gain can only go up to 0.944. Maximum boost control utilizes all the zero states as shoot-through states. The range of modulation index is extended to 0.866 by

TABLE VII
COMPARISONS OF VARIOUS MODULATION TECHNIQUES FOR Z-SOURCE MATRIX TOPOLOGIES

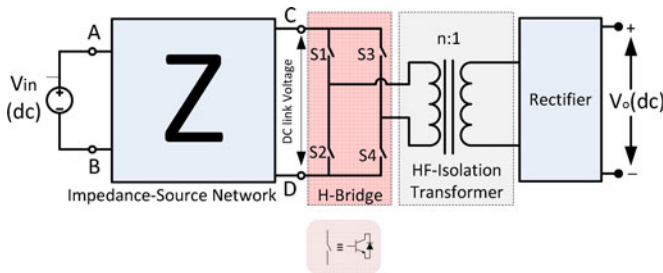| Simple Maximum-Boost Control	Maximum-Boost Control	Maximum-Gain Control
$\bar{D}_{\mathrm{st}} = 1 - 2\pi M/(3\sqrt{3})$	$\bar{D}_{\mathrm{st}} = 1 - M$	$\begin{cases} \bar{D}_{\mathrm{st}} = 0.5 & \text{for} \quad M \leq 0.5 \\ \bar{D}_{\mathrm{st}} = 1 - M & \text{for} \quad M > 0.5 \end{cases}$
$B = \left[1 - 2\pi M/(3\sqrt{3}) + 4\pi^2 M^2/9\right]^{-1/2}$	$B = \left[3M^2 - 3M + 1\right]^{-1/2}$	$\begin{cases} G = 2M & \text{for} \quad M \leq 0.5 \\ G = M\left[3M^2 - 3M + 1\right]^{-\frac{1}{2}} \\ \text{for } M > 0.5 \end{cases}$
$G = \left[\left(\dfrac{1}{M} - \pi/\sqrt{3}\right)^2 + \pi^2/9\right]^{-1/2}$	$G = \left[\left(\dfrac{1}{M} - \pi/\sqrt{3}\right)^2 + \pi^2/9\right]^{-1/2}$	
$M \leq 0.5$	$M \leq 0.5$	

Fig. 13. General circuit configuration of impedance-source network for dc–dc power conversion with intermediate H-bridge topology using various impedance-source networks.

injecting 1/6 of the third harmonic signal in the reference signal. The maximum-gain control method can obtain the maximum gain at the same modulation index among all four techniques, and the hybrid minimum-voltage-stress control can obtain the minimum voltage stress at the same voltage gain. In terms of the total harmonic distortion (THD) at the output, the maximum-constant-boost control method is effective in eliminating low-order harmonics compared to the simple boost and maximum boost controls. A comparison of various control methods is also presented in [117]. A summary of different SPWMs is shown in Table VII.

Pulse-width-amplitude-modulation (PWAM) with a maximum-constant-boost shoot-through control strategy is also implemented in [118] to control a voltage-fed quasi-Z-source direct-matrix converter. This modulation technique reduces the switching frequency of the matrix converter by 1/3 compared to the SVPWM, which helps to reduce the switching losses by more than 50% compared to the SVPWM and 87% compared to the SPWM.

E. Modulation Techniques for DC–DC Converter With Intermediate H-Bridge

Various dc–dc converters are proposed in the literature using single-switch, two-switch, and four-switch topologies. PWM for single-switch [124] and two-switch [125], [126] topologies are fairly simple and can be achieved by controlling the duty cycle of the switch depending on the dc-link voltage. However, a dc–dc converter using an intermediate H-bridge as shown in

Fig. 13 involves more complex control, as four switches are required to be switched optimally to get the desired output and performance.

Various modulation techniques are proposed in the literature, including shoot-through during freewheeling states, shoot-through during zero states, phase shift modulation (PSM) control with shoot-through during zero states [127]–[129], shoot-through by overlap of the active states [127], [130], and shifted shoot-through [131], as shown in Fig 14. Due to insertion of shoot-through in PWM, the switches in the H-bridge are compelled to commute at 2–3 times higher than the switching frequency. In shoot-through during freewheeling states, the top-side and bottom-side switches of the inverter bridge operate at three times the switching frequency ($f_{sw,\text{top}} = 3f_s$ and $f_{sw,\text{bottom}} = 3f_s$) as shown in Fig. 14(a). This leads to a high switching loss. Similarly, the number of commutations of the bottom-side switches remains the same, while reducing the switching frequency of the top-side switch ($f_{sw,\text{top}} = f_s$ and $f_{sw,\text{bottom}} = 3f_s$) in the shoot-through during zero states modulation techniques [see Fig. 14(b)]. Phase shift modulation (PSM) control with shoot-through during zero states [see Fig. 14(c)] equalizes the switching losses of the top-side and bottom-side switches ($f_{sw,\text{top}} = 2f_s$ and $f_{sw,\text{bottom}} = 2f_s$), but this method is not effective in reducing the commutation time of the switches. The switching loss is minimized in shoot-through by the overlap of active states ($f_{sw,\text{top}} = f_s$ and $f_{sw,\text{bottom}} = f_s$) as shown in Fig. 14(d); however, the active-state and shoot-through state duty cycles are not independently controllable. The interdependency of the active-state and shoot-through state duty cycle could cause problems in the output-voltage compensation and also for systems which require independent control of active and shoot-through state. A shifted shoot-through modulation technique [see Fig. 14(e)] could reduce the switching frequency of the switches but it is complex and difficult to implement particularly in the microcontroller due to large number of comparator requirement. It also requires additional external components (logic gates, etc.) for implementation. The major disadvantage of this modulation technique is the loss of full soft-switching properties.

Every addition of the shoot-through state increases the commutation time of the semiconductor switches and so increases the switching loss in the system. Hence, minimization of the commutation time by optimal placing of the
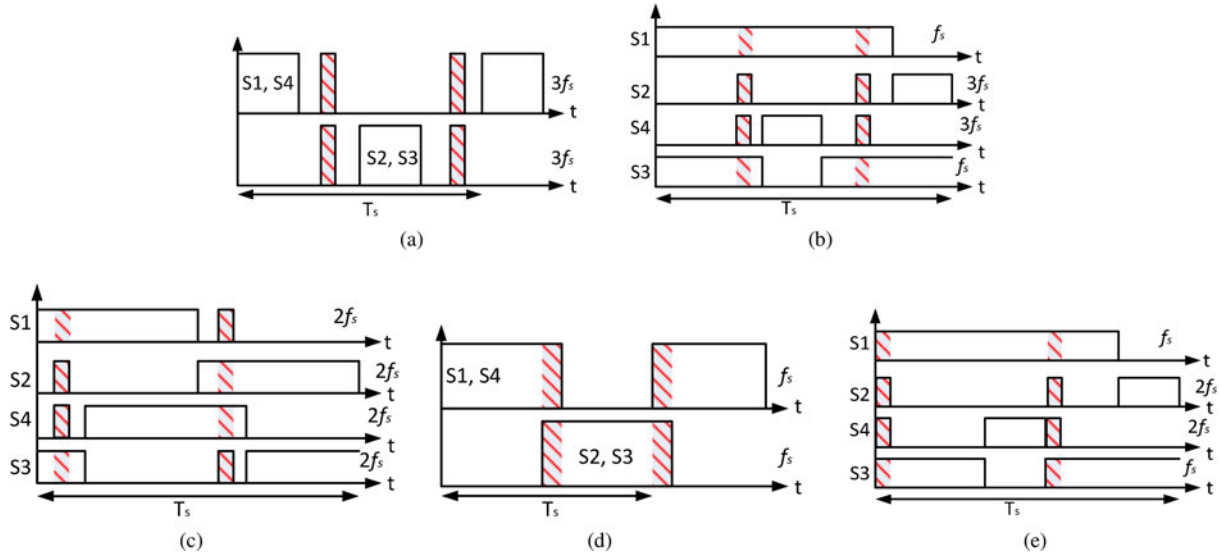
Fig. 14. Some of the modulation techniques for a dc–dc converter with intermediate H-bridge (a) shoot-through during freewheeling states, (b) shoot-through during zero states, (c) phase-shift modulation (PSM) control with shoot-through during zero states, d) shoot-through by the overlap of active states and (e) shifted shoot-through (◣◣◣→Shoot-through).
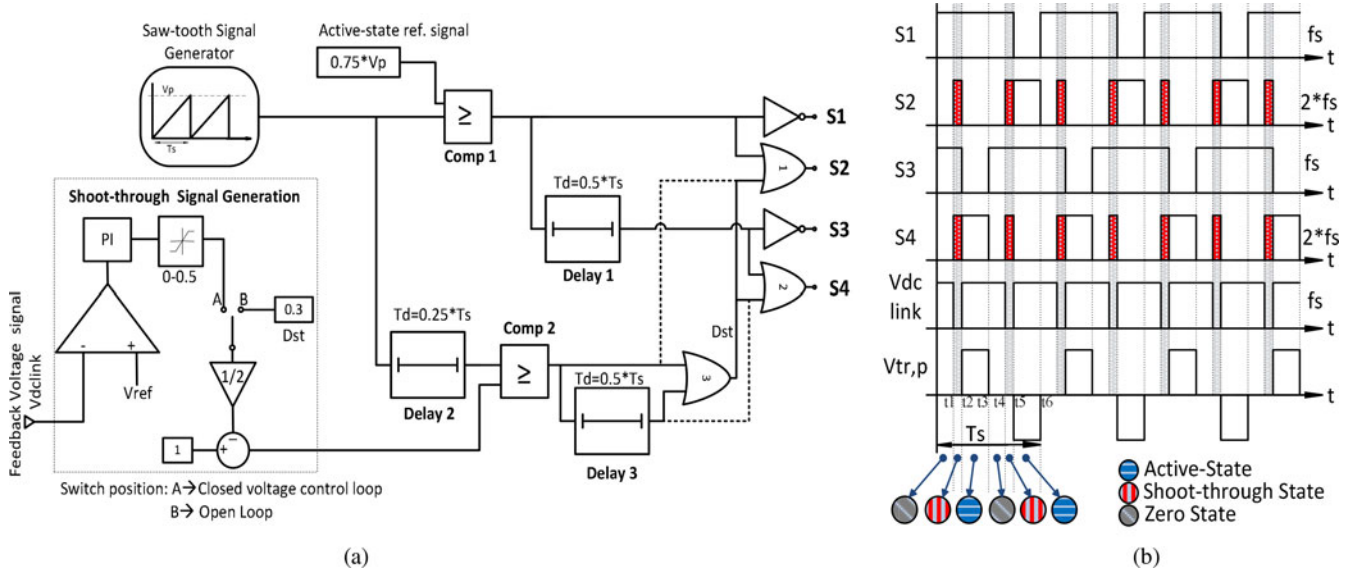

Fig. 15. Optimized PWM control with shoot-through during zero-states illustrating (a) a block diagram and (b) switching sequence for a dc–dc converter.

shoot-through state in a switching time period is necessary in order to minimize the switching loss. In addition, the following points should be considered, while placing the shoot-through state in the PWM control system for a qZSI-based dc–dc converter:

1) Maximum shoot-through duty cycle should never exceed 0.5; otherwise, the system may become unstable.
2) Minimum number of shoot-through states per switching period is two. One shoot-through state per period causes a discontinuous current and the converter will behave abnormally.

3) Shoot-through state should be in the zero state, i.e., the intact active state.
4) Active state and the shoot-through state should be independently controllable.

A new modulation technique called "*optimized PWM control with shoot-through during zero-states*" incorporating the shoot-through state to minimize the number of commutations in semiconductor switches for any impedance network-based dc–dc converter with intermediate H-bridge switching topology is presented in [132]. This modulation technique is found to be less complex and is easier to implement in all digital

TABLE VIII
COMPARISON OF MODULATION TECHNIQUES FOR DC–DC CONVERTER WITH AN INTERMEDIATE H-BRIDGE

Parameters	Method A	Method B	Method C	Method D	Method E	Method F
Maximum switching frequency of top-side transistors	$3f_s$	f_s	$2f_s$	f_s	f_s	f_s
Maximum switching frequency of bottom-side transistors	$3f_s$	$3f_s$	$2f_s$	f_s	$2f_s$	$2f_s$
Independent active and shoot-through state controllability (for voltage compensation)	Yes	Yes	Yes	No	Yes	Yes
Measured maximum transient overvoltage on top-side transistors	1.5 pu	2.4 pu	2.5 pu	2.1 pu	1.6 pu	1.3 pu
Measured maximum transient overvoltage on bottom-side transistors	2.6 pu	1.85 pu	2.5 pu	2.1 pu	>2 pu	1.3 pu
Measured maximum transient overvoltage on capacitor C1	1.7 pu	1.7 pu	1.2 pu	1.7 pu	–	1.2 pu
Measured maximum transient overvoltage on capacitor C2	1.5 pu	1.5 pu	3.5 pu	1.5 pu	–	1.2 pu
Soft-switching for top-side transistors	partial	full	–	no	partial	full
Soft-switching for bottom-side transistors	partial	no	–	no	partial	partial
Complexity of implementation (1 to 6 in increasing order of complexity)	3	4	5	2	6*	1

*difficult to implement in microcontroller and requires some additional hardware.
Method A: Shoot-through during freewheeling states.
Method B: Shoot-through during zero states.
Method C: Phase-Shift Modulation (PSM) control with shoot-through during zero states.
Method D: Shoot-through by overlap of active states.
Method E: Shifted Shoot-through.
Method F: Optimized PWM control with shoot-through during zero-states.

platforms (FPGA, DSP, microcontroller, etc.) without adding external components. Using this PWM method, the commutation time of the top and the bottom side switches of the bridge can be brought down to the switching frequency (f_s), which reduces the switching loss. In addition, the switches achieve ZVS, which reduces EMI and increases the efficiency. Fig. 15 shows a block diagram of the optimized PWM control with shoot-through during zero-states and the corresponding switching sequence.

A detailed comparison of the different modulation techniques considering theoretical complexity and performance is shown in Table VIII.

IV. CONCLUSION

This paper has presented an exhaustive review of modeling, control, and modulation techniques for impedance source networks for power converters. A broad classification of the modulation techniques into five categories with further subclassification aims to provide easy selection of control and modulation techniques for appropriate topologies [1] for particular application. Further, a comparison of various modulation techniques for particular switching topologies based on theoretical complexity and performance informs the selection of the correct control and modulation technique for the respective switching topologies to achieve maximal voltage boost, minimal harmonic distortion, lower semiconductor stress, and a minimal number of device commutations per switching cycle. In addition, this paper informs the selection of appropriate modulation techniques for digital implementation and may provide an effective way to reduce the resources required for digital implementation. The authors hope that the comprehensive survey of impedance-source networks for power conversion in Parts I & II will be a useful reference for researchers, designers, manufacturers, and users working in the area of power conversion and management.

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