Decoupling of Fluctuating Power in Single-Phase Systems Through a Symmetrical Half-Bridge Circuit

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***Abstract*—Single-phase ac/dc or dc/ac systems are inherently subject to the harmonic disturbance that is caused by the well-known double-line frequency ripple power. This issue can be eased through the installation of bulky electrolytic capacitors in the dc link. Unfortunately, such passive filtering approach may inevitably lead to low power density and limited system lifetime. An alternative approach is to use active power decoupling so that the ripple power can be diverted into other energy storage devices to gain an improved system performance. Nevertheless, all existing active methods have to introduce extra energy storage elements, either inductors or film capacitors in the system to store the ripple power, and this again leads to increased component costs. In view of this, this paper presents a symmetrical half-bridge circuit which utilizes the dc-link capacitors to absorb the ripple power, and the only additional components are a pair of switches and a small filtering inductor. A design example is presented and the proposed circuit concept is also verified with simulation and experimental results. It shows that at least ten times capacitance reduction can be achieved with the proposed active power decoupling method, and both the input current and output voltage of the converter can be well regulated even when very small dc-link capacitors are employed.**

***Index Terms*—Active power decoupling, capacitance reduction, harmonic compensation, single-phase systems.**

I. Introduction

SINGLE-PHASE ac/dc or dc/ac power electronics systems have extremely wide applications in residential and industrial power supplies or conversion systems. Example applications are front-end power factor correction (PFC) converters in consumer power supplies [1]–[3], on-board chargers for plug-in hybrid electric vehicles [4]–[6], and 5-kW (or less) grid-connected photovoltaic (PV) inverters for distributed power generation [7]–[9]. A well-known problem with such systems is that their ac-side instantaneous power contains a fluctuating component that changes at twice the fundamental frequency [10]. This fluctuating power is adverse to the system performance because it may potentially cause distorted input current of PFCs, overheating of batteries [11], and decreased maximum power point tracking (MPPT) efficiency of PV systems [12]. A very straightforward way to mitigate its negative impact is to use bulky electrolytic capacitors in the dc link so that they can act as buffers to the ac-side ripple power. However, those electrolytic capacitors are known to have high equivalent series resistance (ESR) and low ripple current capability, and their lifetime is also relatively short (several thousand hours) when stressed with the nominal voltage and the ripple current. Therefore, they may cause troubles in some applications where 20- or 25-year warranty period is required, e.g., LED drivers and solar inverters [12].

Recently, some active power decoupling methods have been proposed to cope with this problem, and the fundamental principle behind them is to introduce an extra active circuit in the system, so that the ripple power can be shifted away from the dc link and stored by other components with expanded lifetime, e.g., inductors and film capacitors, in a more efficient and effective way. Fig. 1(a) shows an active method which uses an inductor for ripple energy storage [13], and the inductor current is controlled to be sinusoidal which is accomplished through the proper modulation of the added third switching leg. A similar concept is presented in [14], where the lower switch of the third leg is replaced with a diode in order to save one active component, and in this case, the inductor current can be controlled as rectified sinusoidal in order to cancel those ac-side ripple power. Even though inductors are reliable and robust, they are generally of low power density and high power losses when used as energy storage elements for fundamental components, and therefore, the performance improvement could be very limited. In [12], the inductor is replaced by a film capacitor and the ripple power can then be compensated by controlling the voltage of the film capacitor to be rectified sinusoidal as shown in Fig. 1(b). However, such waveforms may contain high-order harmonics which will be difficult to track and control for a highly underdamped second-order system. Using exactly the same circuit configuration, Wang *et al.* [15] propose to inject a dc offset in the capacitor reference voltage so that the harmonic content may become small and it may facilitate the closed-loop controller design. Nevertheless, since the capacitor voltage does not go down to zero, it will not be fully discharged, which means that the film capacitor is not fully utilized. The similar compensation concept based on capacitive ripple power decoupling has also been discussed in [16]–[18]. A more recently proposed active power decoupling method is discussed in [19] and its circuit diagram is shown in Fig. 1(c). The introduced half-bridge, together with one leg of the full-bridge rectifier, essentially forms another

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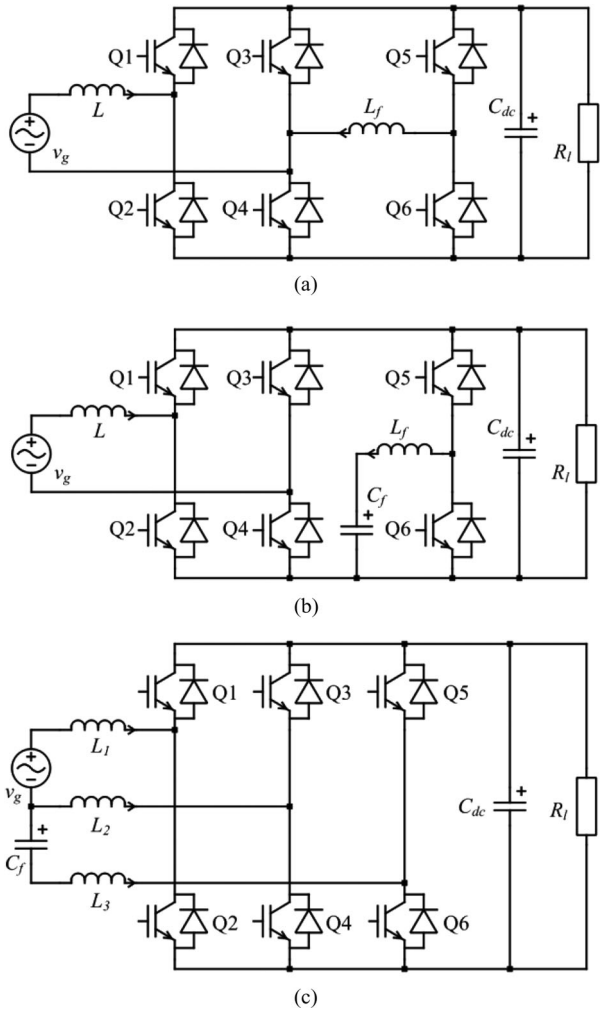

Fig. 1. Typical circuit topologies for active power decoupling in a single-phase system.

full-bridge circuit, and in this case, the voltage of the film capacitor can be controlled to be sinusoidal and it resolves all the difficulties mentioned previously. Even though being effective in ripple power compensation, this topology is not applicable in some circumstances, e.g., PFCs and unfolding bridge-based inverters, because the power flow is unidirectional. It may also become problematic in H5 inverters, where the full-bridge circuit will be intermittently isolated from the dc link in order to eliminate the leakage current [20]. In [21], a stacked switched capacitor concept is proposed as the energy buffer for single-phase systems. However, the circuit may involve a large number of capacitors and switches if high energy buffering ratio is pursued. It also requires a precharge circuit to distribute the initial voltages for individual capacitors, which may further complicate its circuit implementation. Moreover, this circuit theoretically cannot achieve perfect active power decoupling and small voltage fluctuation may always exist in the dc link.

Instead of using paralleled circuit configurations discussed previously, Wang *et al.* [22] propose a series compensation approach where a controlled voltage source is inserted in between the dc-link capacitor and the load and through this way, low-voltage semiconductors can be used to construct the active power decoupling circuit and to gain an improved system performance. However, the circuit is complicated with four MOSFETs and associated gate drivers, and the dc-link capacitance cannot be too small because it may potentially overmodulate the front-end ac/dc rectifier. Even though the dc-link capacitance can be reduced regardless of the configurations of compensation circuits, a common problem for the existing active power decoupling methods is that, the system ripple power has to be absorbed by additional energy storage elements, either inductors or film capacitors, and this implies that the capacitance reduction is not optimized [23].

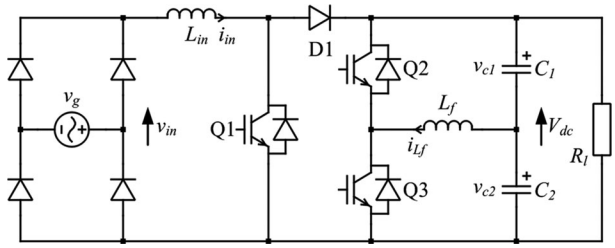

Fig. 2. Proposed symmetrical half-bridge circuit for single-phase active power decoupling.

In order to achieve a simple and compact design, and also to break the limitation imposed by the front-end topology in [19], this paper proposes a new topology to realize active power decoupling, and its circuit diagram is shown in Fig. 2. As can be seen, two identical film capacitors are employed and connected in series in the dc link, whose midpoint is then connected to another phase leg through a small filtering inductor. In this way, the dc-link capacitors may not only provide a high-voltage dc bus to support ac/dc or dc/ac conversion, but can also absorb the system ripple power. The added symmetrical half-bridge circuit is also easy to control, because the voltages of the two film capacitors will both be sinusoidal. Moreover, the capacitors can be alternatively discharged to zero in case that high ripple power compensation is required, and the power decoupling can be accomplished without using additional energy storage inductors or capacitors. The power flow involved in this circuit and the relevant controller design are detailed in this paper. Both simulation and experimental results are presented to prove the effectiveness of this concept.

II. Circuit Analysis and Operating Principles

The proposed symmetrical half-bridge circuit is shown in Fig. 2, which is applied to a single-phase PFC converter as an example here. It should be noted that and also as mentioned previously, the proposed active power decoupling method will not be constrained by its front-end topologies, and it can be basically used in any single-phase ac/dc or dc/ac systems, as long as there is a high-voltage dc bus available. In this case, two identical film capacitors, having $C_1 = C_2 = C_f$, are connected in series to build up the dc-link voltage $V_{\rm dc}$, and $v_{c1}(t)$ and $v_{c2}(t)$ are used to denote the voltages of the upper and lower capacitors,

respectively. In order to provide the double-line frequency ripple power, their voltages are then controlled to be sinusoidal with an offset value that equals to half the dc-link voltage $V_{\rm dc}/2$, and they can be written as

$$\begin{cases} v_{c1}(t) = \frac{V_{\rm dc}}{2} + V_c \sin(\omega t + \theta) \\ v_{c2}(t) = \frac{V_{\rm dc}}{2} - V_c \sin(\omega t + \theta) \end{cases} \quad (1)$$

where θ is the phase angle between the capacitor voltage $v_{c1}(t)$ and the input voltage $v_{\rm in}(t)$, and ω is the fundamental angular frequency. V_c is the amplitude of the film capacitor voltage having $V_c \le V_{\rm dc}/2$. The capacitor current $i_{c1}(t)$ and $i_{c2}(t)$ can then be easily derived as

$$\begin{cases} i_{c1}(t) = I_c \cos(\omega t + \theta) = \omega C_f V_c \cos(\omega t + \theta) \\ i_{c2}(t) = -I_c \cos(\omega t + \theta) = -\omega C_f V_c \cos(\omega t + \theta) \end{cases} \quad (2)$$

where I_c is the amplitude of the filtered capacitor current. The instantaneous power $p_c(t)$ provided by these two capacitors will be

$$\begin{aligned} p_c(t) &= v_{c1}(t) i_{c1}(t) + v_{c2}(t) i_{c2}(t) \\ &= 2V_c \sin(\omega t + \theta) \omega C_f V_c \cos(\omega t + \theta) \\ &= \omega C_f V_c^2 \sin(2\omega t + 2\theta). \end{aligned} \quad (3)$$

In order to achieve accurate power compensation, the instantaneous power $p_{Lf}(t)$ of the filter inductor L_f must also be taken into consideration

$$\begin{aligned} i_{Lf}(t) &= i_{c1}(t) - i_{c2}(t) \\ &= 2I_c \cos(\omega t + \theta) = 2\omega C_f V_c \cos(\omega t + \theta) \end{aligned} \quad (4)$$

$$\begin{aligned} p_{Lf}(t) &= L_f \frac{di_{Lf}(t)}{dt} i_{Lf}(t) \\ &= -\omega L_f (2\omega C_f V_c)^2 \sin(\omega t + \theta) \cos(\omega t + \theta) \\ &= -2\omega L_f (\omega C_f V_c)^2 \sin(2\omega t + 2\theta). \end{aligned} \quad (5)$$

Therefore, the total instantaneous power $p_{hb}(t)$ provided by the symmetrical half-bridge circuit will be

$$\begin{aligned} p_{hb}(t) &= p_c(t) + p_{Lf}(t) \\ &= [\omega C_f V_c^2 - 2\omega L_f (\omega C_f V_c)^2] \sin(2\omega t + 2\theta). \end{aligned} \quad (6)$$

Equation (6) shows that the filter inductor may reduce the compensation capacity of this circuit and its value should be minimized in the design.

The instantaneous power to the PFC stage $p_{pfc}(t)$ can be found in a similar manner by defining the input voltage $v_{\rm in}(t)$ and current $i_{\rm in}(t)$ to be

$$v_{\rm in}(t) = V_{\rm in} |\sin(\omega t)| \text{ and } i_{\rm in}(t) = I_{\rm in} |\sin(\omega t)| \quad (7)$$

$$\begin{aligned} p_{\rm PFC}(t) &= p_{\rm in}(t) + p_{\rm Lin}(t) \\ &= v_{\rm in}(t) i_{\rm in}(t) + L_{\rm in} \frac{di_{\rm in}(t)}{dt} i_{\rm in}(t) \\ &= \frac{V_{\rm in} I_{\rm in}}{2} - \frac{V_{\rm in} I_{\rm in}}{2} \cos(2\omega t) + \frac{\omega L_{\rm in} I_{\rm in}^2}{2} \sin(2\omega t) \end{aligned} \quad (8)$$

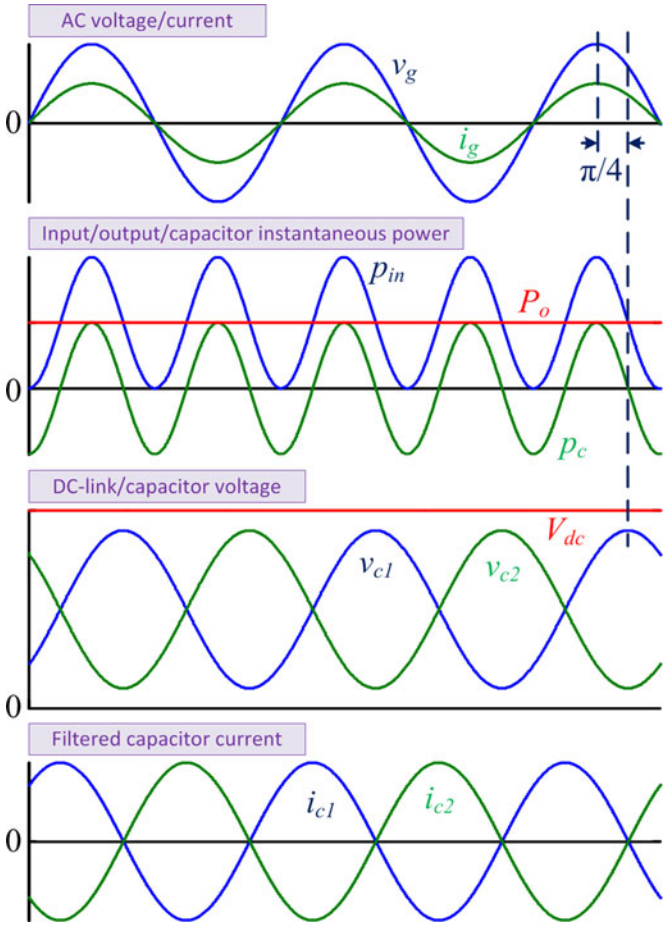

Fig. 3. Idealized operating waveforms for the proposed active power decoupling circuit.

where $\sin(\omega t) \neq 0$. By equating the time-varying terms of (8) to (6), it is possible to derive that

$$\theta = \frac{1}{2} \arctan\left(-\frac{V_{\rm in} I_{\rm in}}{\omega L_{\rm in} I_{\rm in}^2}\right) = \frac{1}{2} \arctan\left(-\frac{V_{\rm in}}{\omega L_{\rm in} I_{\rm in}}\right) \quad (9)$$

$$V_c = \sqrt{\frac{\sqrt{\left(\frac{V_{\rm in} I_{\rm in}}{2}\right)^2 + \left(\frac{\omega L_{\rm in} I_{\rm in}^2}{2}\right)^2}}{\omega C_f - 2\omega L_f (\omega C_f)^2}}. \quad (10)$$

In this case, the voltage references of C_1 and C_2 can be determined by (9) and (10), and through closed-loop control, the system ripple power can be almost cancelled by these two dc-link capacitors and the dc-link voltage will be fairly constant. It should be noted that in practical implementation, there may exist some errors due to parameter tolerance of the components and limited compensation gain, and a closed-loop modification of the voltage references may be required to fine tune the ripple power compensation as discussed in [19].

The idealized operating waveforms of the proposed converter are presented in Fig. 3, where the filter inductance, switching loss, and conduction loss in the circuit are all neglected. It is clear that the two dc-link capacitors can provide the fluctuating power that can be used to cancel those propagated from the ac

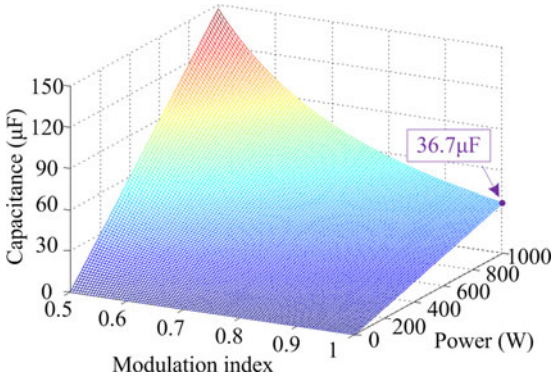

Fig. 4. Required dc-link capacitance as a function of the power rating and the modulation index.

grid side, and the voltage of the upper capacitor has $\pi/4$ phase shift with the grid voltage.

In order to examine the capacitance reduction achieved by the proposed active power decoupling method, the ripple power across the inductors $L_{\rm in}$ and L_f are neglected because they are comparatively much smaller than those capacitive ones. Then, the symmetrical half-bridge circuit can provide the maximum ripple power when $V_c = V_{\rm dc}/2$ and according to (10)

$$\omega C_f V_c^2 = \frac{V_{\rm in} I_{\rm in}}{2} \quad \text{and} \quad \frac{\omega C_f V_{\rm dc}^2}{4} = P_{\rm in} \tag{11}$$

$$C_{\rm eq} = \frac{C_f}{2} = \frac{2P_{\rm in}}{\omega V_{\rm dc}^2} \tag{12}$$

where $P_{\rm in}$ is the amplitude of the input ripple power and $C_{\rm eq}$ is the equivalent dc-link capacitance. For a typical 60-Hz power system with a dc-link voltage of 380 V, the required capacitance is only 36.7 μF/kW according to (12).

In contrast, if there is no active power decoupling and it is desired that the dc-link voltage ripple should be less than 1% of the nominal voltage, the dc-link capacitance would be [15]

$$0.01V_{\rm dc} = \frac{P_{\rm in}}{2\omega C_{\rm dc} V_{\rm dc}} \quad \text{and} \quad C_{\rm dc} = \frac{50P_{\rm in}}{\omega V_{\rm dc}^2}. \tag{13}$$

Equation (13) clearly shows that the dc-link capacitance can theoretically be reduced by 25 times as compared to that of a conventional passive approach. However, in practice, the improvement may not be so significant because the capacitor voltage V_c is normally controlled to be slightly less than $V_{\rm dc}/2$ in order to prevent overmodulation of the symmetrical half-bridge. Fig. 4 shows the dc-link capacitance requirement with respect to the power rating of the converter and the modulation index of the symmetrical half-bridge circuit. The modulation index is normalized to unity when $V_c = V_{\rm dc}/2$.

In certain applications, e.g., PFC converters for computer power supplies, there is another requirement for the output capacitors, which is to maintain the output voltage for a short period even if its ac-side input voltage is lost. The required capacitance can then be calculated as

$$C_{\rm dc} \geq \frac{2 \cdot P_{\rm out} \cdot t_{\rm holdup}}{{V_{\rm dc}}^2 - {V_{\rm dc\_min}}^2} \tag{14}$$

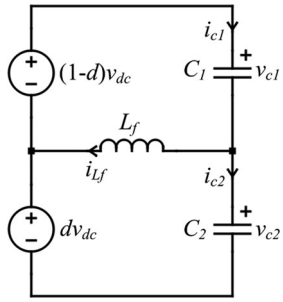

Fig. 5. Averaged equivalent circuit of the proposed symmetrical half-bridge.

where the common specification for this holdup time $t_{\rm holdup}$ is 20 ms. If the minimum dc-link voltage $v_{\rm dc\_min}$ is defined to be 250 V and the power losses of the PFC converter are neglected, the required capacitance is found to be 488.4 μF/kW, which is sufficient to provide ripple power compensation even only 0.5 modulation index is applied to the converter according to Fig. 4.

III. System Modeling and the Controller Design

The modeling and controller design of the PFC converter has been extensively discussed in the literature and therefore will not be addressed in this paper. For the introduced symmetrical half-bridge, it simply has two switching states and its corresponding time-averaged model can be derived by averaging the state equations over a switching cycle. The resultant equivalent circuit model is shown in Fig. 5 and based on this model, it is easy to derive the following differential equations:

$$\begin{cases} L_f \frac{di_{Lf}(t)}{dt} = -v_{c1}(t) + [1 - d(t)] \cdot v_{\rm dc}(t) \\ C_f \frac{dv_{c1}(t)}{dt} = i_{c1}(t) \end{cases} \tag{15.a}$$

$$\begin{cases} L_f \frac{di_{Lf}(t)}{dt} = v_{c2}(t) - d(t) \cdot v_{\rm dc}(t) \\ C_f \frac{dv_{c2}(t)}{dt} = i_{c2}(t) \end{cases} \tag{15.b}$$

where $d(t)$ is the duty cycle applied to the upper switch Q2 shown in Fig. 2. Ideally, the compensation network can cancel the ac-side ripple power and the dynamics of the dc-link voltage and its ripple component can be neglected. In this case, by substituting (2) and (4) into (15.b)

$$\begin{cases} L_f \frac{di_{Lf}(t)}{dt} = v_{c2}(t) - d(t) \cdot V_{\rm dc} \\ C_f \frac{dv_{c2}(t)}{dt} = -\frac{i_{Lf}(t)}{2}. \end{cases} \tag{16}$$

Taking the Laplace transform of (16) and also considering the damping effect of a practical circuit, the control-to-capacitor voltage transfer function G_{hb} can finally be derived as

$$G_{hb} = \frac{v_{c2}(s)}{d(s)} = \frac{V_{\rm dc}}{2L_f C_f s^2 + K_d C_f s + 1}$$
$$\text{and} \quad \omega_{\rm res} = \frac{1}{\sqrt{2L_f C_f}} \tag{17}$$

where K_d is a parameter that represents the damping effect provided by the ESR of passive components and $\omega_{\rm res}$ is the *LC*

TABLE I
CIRCUIT PARAMETERS USED IN ANALYSIS, SIMULATION, AND EXPERIMENT

Description	Symbol	Value
Nominal power	P_n	1 kW
Switching frequency	f_{sw}	19.2 kHz
Line frequency	f_n	60 Hz
Grid voltage	V_g	156 V
Dc-link voltage	$V_{\rm dc}$	380 V
Dc-link capacitor	C_1/C_2	90 μF
Boost inductor	$L_{\rm in}$	2 mH
Filter inductor	L_f	2 mH
Nominal load	R_l	150 Ω

resonant frequency. The ESRs of the capacitors are ignored here because they are of film type and have extremely low value.

It should be noted that in practice, there always exists some control errors and component tolerance, and therefore, the dc-link voltage ripple may not be zero and introduce the common mode current in the two decoupling capacitors. In this case, $i_{c1}(t) = -i_{c2}(t) = i_{Lf}(t)/2$ is no longer valid and in order to get rid of the disturbance from the dc link, the measured capacitor voltage $v_{c2}(t)$ should be preprocessed before being sent into the voltage controller as follows:

$$v_c(t) = \frac{v_{c2}(t) - v_{c1}(t)}{2} = \frac{2v_{c2}(t) - v_{\rm dc}(t)}{2}. \tag{18}$$

The above equation in effect indicates that the control variable should be changed to $v_{c2}(t) - v_{c1}(t)$ rather than $v_{c2}(t)$. Combining (15) and (18)

$$\begin{cases} 2L_f \frac{di_{Lf}(t)}{dt} = v_{c2}(t) - v_{c1}(t) + [1 - 2d(t)] \cdot v_{\rm dc}(t) \\ = 2v_c(t) + [1 - 2d(t)] \cdot v_{\rm dc}(t) \\ C_f \frac{d[v_{c2}(t) - v_{c1}(t)]}{dt} = 2C_f \frac{dv_c(t)}{dt} \\ = i_{c2}(t) - i_{c1}(t) = -i_{Lf}(t). \end{cases} \tag{19}$$

By introducing perturbation in the state variables

$$\begin{cases} L_f \frac{d[I_{Lf} + \hat{i}_{Lf}(t)]}{dt} = [V_c + \hat{v}_c(t)] + \left[\frac{1}{2} - D - \hat{d}(t)\right] \\ \quad \cdot [V_{\rm dc} + \hat{v}_{\rm dc}(t)] \\ C_f \frac{d[V_c + \hat{v}_c(t)]}{dt} = -\frac{I_{Lf} + \hat{i}_{Lf}(t)}{2}. \end{cases} \tag{20}$$

By equating ac and dc quantities and then proceed only with ac equations (neglect second-order ac quantities)

$$\begin{cases} L_f \frac{d\hat{i}_{Lf}(t)}{dt} = \hat{v}_c(t) - \hat{d}(t) \cdot V_{\rm dc} + (\frac{1}{2} - D) \cdot \hat{v}_{\rm dc}(t) \\ C_f \frac{d\hat{v}_c(t)}{dt} = -\frac{\hat{i}_{Lf}(t)}{2}. \end{cases} \tag{21}$$

When operated around the quiescent point, the effect of the ripple voltage can be neglected because $\frac{1}{2} - D$ is comparatively much smaller than $V_{\rm dc}$. In this case, the disturbance from the dc link can be eliminated and (21) is simplified to be the same as (16), and therefore, the plant transfer function shown in (17) still holds true. Using the parameters listed in Table I, the open-loop gain of this system is plotted as the solid line in Fig. 6, where it is clear that its phase response is nearly $-180°$ after the *LC* resonant frequency. This paper proposes a modified type III

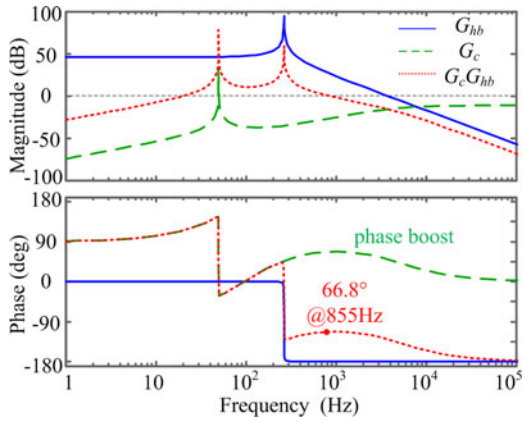

Fig. 6. Bode diagrams of the plant model, controller, and system open-loop gain.

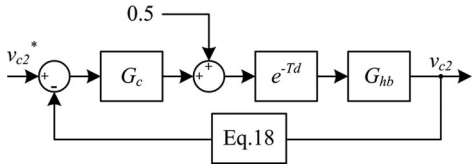

Fig. 7. Control block diagram for the proposed active power decoupling circuit.

compensator to stabilize this system and it is embedded with a resonant controller [24], which ensures zero steady-state tracking error of the voltage control loop, and its transfer function can be written as

$$G_c = K_p \frac{\left(\frac{s}{\omega_{z1}} + 1\right)\left(\frac{s}{\omega_{z2}} + 1\right)}{\left(\frac{s}{\omega_p} + 1\right)} \frac{s}{s^2 + \omega^2} \tag{22}$$

where ω_{z1} and ω_{z2} are the two zeroes to provide phase boost capability and should be placed around the *LC* resonance frequency. ω_p is the pole to attenuate the system high-order harmonics and is normally chosen to be less than half of the system switching frequency. K_p is the proportional gain that adjusts the system crossover frequency. Since the ESR of film capacitors is very low, there is no need to add another pole to cancel the ESR zero of capacitors, which in this case is well above the system control frequency. The Bode diagram of the designed controller is then plotted as the dashed line in Fig. 6 and it shows that this controller can provide maximum phase boost of 67.3° at 1040 Hz, and it also has high gain at fundamental frequency to force the voltage tracking error to be zero. The resulting system open-loop gain is plotted as the dotted line in Fig. 6 and it shows that 66.8° phase margin is achieved at 855 Hz, which is sufficient even considering the system delays that are caused by digital computation and pulse-width modulation. In addition to this closed-loop control, a feed-forward path is also implemented which adds a constant 0.5 into the final duty cycle, and in this way, the capacitor voltages will contain $V_{\rm dc}/2$ offset. The control block diagram is shown in Fig. 7 and it is applied to control the voltage of the lower capacitor in the dc link, and

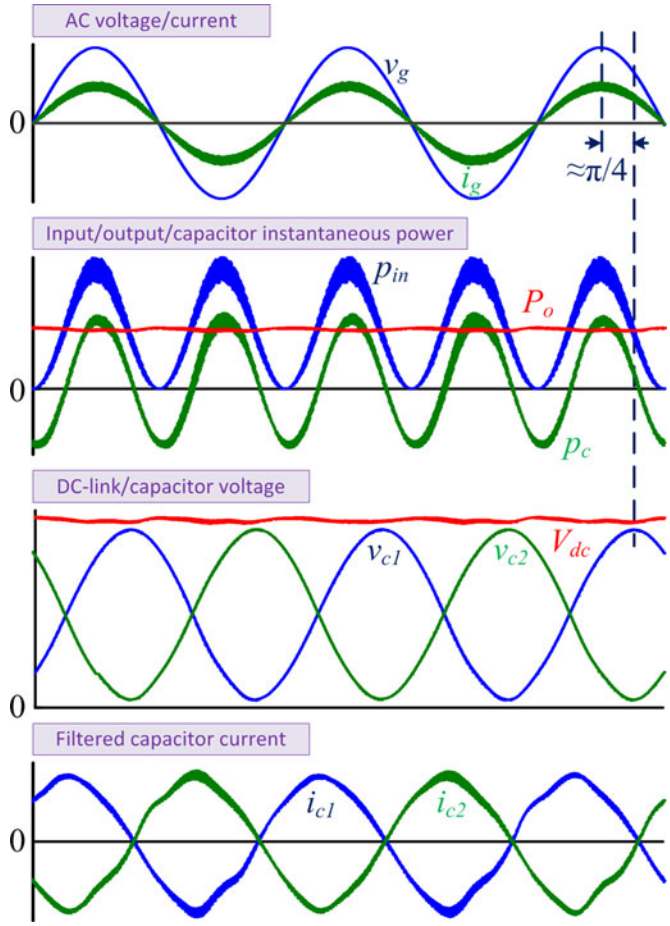

Fig. 8. Simulation results showing the key operating waveforms of the proposed active power decoupling circuit.

TABLE II
KEY COMPONENTS USED FOR THE EXPERIMENTAL PROTOTYPE

Component	Description
Diode rectifier bridge	GBPC2506, 25 A/600 V, MULTICOMP
Q1 . . . Q3/D1	IKW30N60T, 30 A/600 V, INFINEON
L_{in}/L_f	200 turns, 2 × AWG#16, Core DT400–40, DMEGC
C_1/C_2	MKP1847630354Y5, 30 μF/350 V, VISHAY
C_{dc}	EETED2W471LJ, 470 μF/450 V, PANASONIC

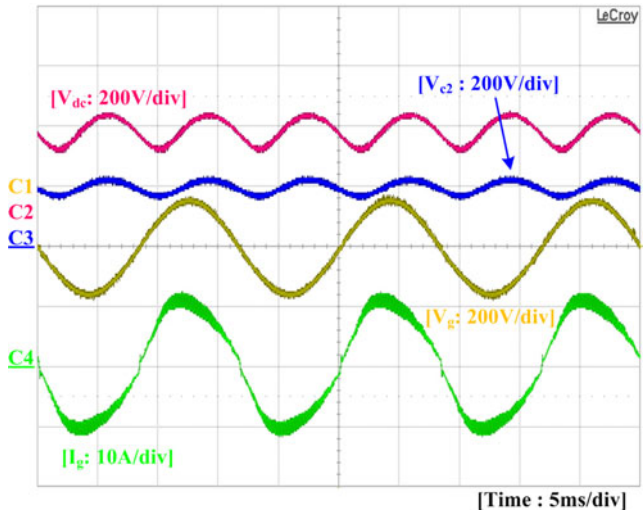

Fig. 9. Steady-state experimental waveforms without ripple power compensation. From top to bottom, dc-link voltage, lower capacitor voltage, grid voltage, and grid current.

the voltage of the upper capacitor will be naturally determined because the total dc bus voltage is already regulated by the PFC controller, which is usually a very slow control loop.

IV. SIMULATION AND EXPERIMENTAL RESULTS

A. Simulation Results

Simulation was done in MATLAB/Simulink environment and the key circuit parameters are summarized in Table I.

Fig. 8 shows the steady-state simulation results which are comparable to those presented in Fig. 3. Thanks to the smooth dc-link voltage, the input line current can be well regulated by the PFC controller, and it is sinusoidal and in phase with the grid voltage. The two film capacitors can provide the required double-line frequency harmonic power, and the resultant output power can be almost constant. The dc-link voltage has very slight voltage variation, which is around 10 V, and this is caused by the inaccurate calculation of the voltage reference and the errors in the closed-loop control. As mentioned in [19], some closed-loop modifications can be applied to fine tune the voltage reference and to achieve more precise power decoupling. However, this may further complicate the control system, and thus not implemented here. The voltage of the upper capacitor is noted to have approximately $\pi/4$ phase shift with the grid voltage, which matches well with the theoretical analysis.

B. Experimental Results

A 1-kW prototype was built in the laboratory and the circuit parameters are basically the same as those used in simulation. Two 90-μF film capacitors, each of them consisting of three 30-μF film capacitors in parallel, are connected in series in the dc link and the equivalent dc-link capacitance is only 45 μF, which is much smaller than that of a conventional PFC converter. The key active and passive components used for the tested prototype are summarized in Table II.

Fig. 9 shows the steady-state experimental results when the closed-loop controller is disabled and there is no active power decoupling in the circuit. It is obvious that the dc-link contains high ripple voltage because of the very low capacitance, and this ripple voltage in turn affects the regulation of the input current. Even though a second-order notch filter is implemented in the PFC voltage control loop, it is still not enough to attenuate the voltage harmonic disturbance and it fails to provide a clean reference for the inner current control loop. The grid current is therefore seriously distorted by the third-order harmonic with amplitude of 0.92A. The total harmonic distortion (THD) of grid current, calculated up to 100th harmonics, is found to be 9.1%,

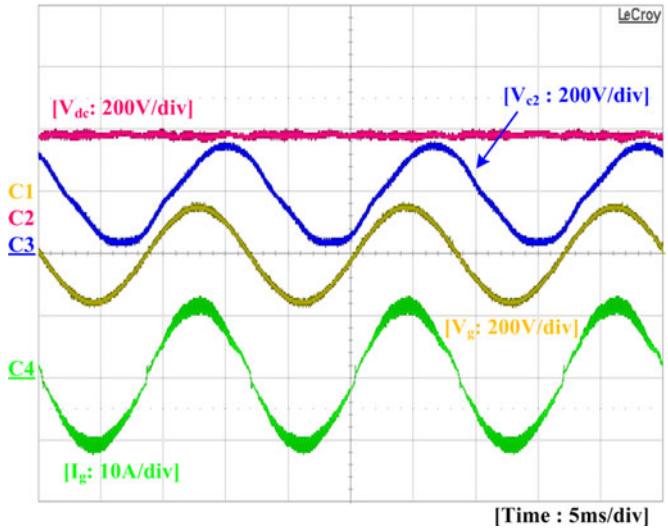

Fig. 10. Steady-state experimental waveforms with ripple power compensation. From top to bottom, dc-link voltage, lower capacitor voltage, grid voltage, and grid current.

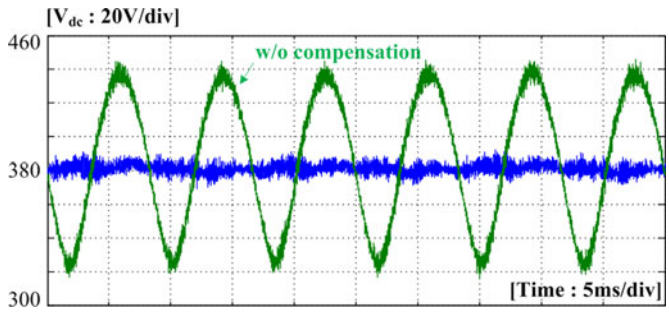

Fig. 11. Zoom-in view of the dc-link voltage under two tests.

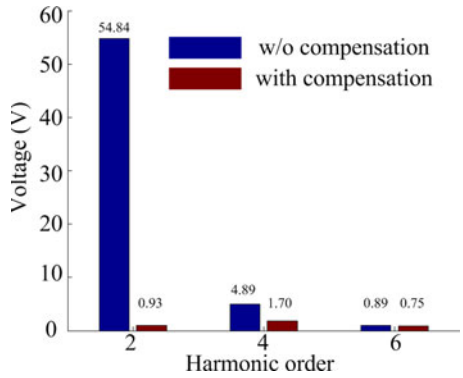

Fig. 12. Spectral analysis of the dc-link voltage under two tests.

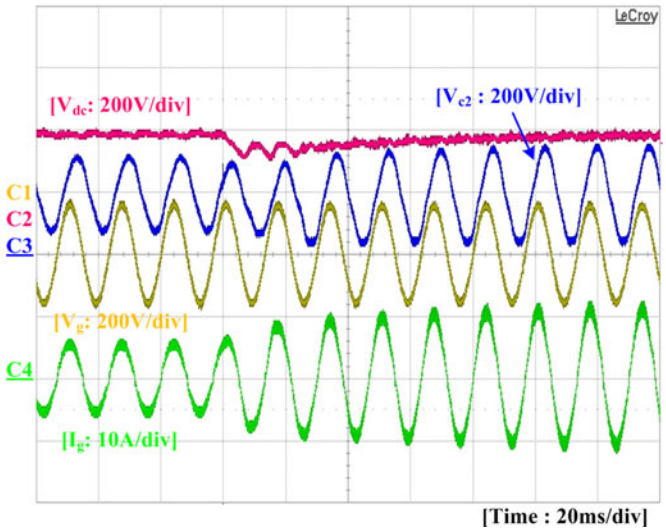

Fig. 13. Dynamic experimental waveforms showing 50% to 100% step-up load change. From top to bottom, dc-link voltage, lower capacitor voltage, grid voltage, and grid current.

and this value may not be able to comply with the standards, like the IEEE 519–1992 harmonic limits.

Fig. 10 shows the steady-state experimental results when the proposed decoupling method is enabled and it is clear that the dc-link voltage ripple can be dramatically reduced. As a consequence, the grid current is also greatly improved and the third-harmonic current is reduced to 0.15A only. In this case, the THD of the grid current is improved to 3.8%. Also as anticipated, the capacitor voltage is sinusoidal with $V_{\rm dc}/2$ offset, and there is approximately one-eighth cycle phase difference with the grid voltage, which is in good agreement with the theoretical analysis and simulation results presented previously.

Fig. 11 shows the zoom-in view of the dc-link voltage under these two tests. Without compensation, the peak-to-peak dc-link voltage can be up to 120 V, which corresponds to 31.6% of the nominal dc bus voltage, while this ripple voltage can be suppressed to around 10 V, less than 3% of the nominal value if the proposed compensation is implemented.

Fig. 12 shows the spectrum of the dc-link voltage and it is clear that there is a dramatic reduction of the second-harmonic voltage after activation of the harmonic compensation. The fourth- and sixth-harmonic voltages are also slightly reduced due to the improved grid current. The smooth dc-link voltage indicates that ten times capacitance reduction in single-phase systems is successfully achieved with the proposed active power decoupling circuit.

The prototype was also tested with dynamic loads and the corresponding load step-up and step-down experimental results are presented in Figs. 13 and 14, respectively. As shown, the dc-link voltage dip/swell during load transients can be kept within ± 100 V. This is acceptable considering the very low equivalent dc-link capacitance used in the circuit. The dc-link voltage can converge to its nominal value within five line cycles and there is no obvious distortion occurred in the grid current and the power factor is clearly always unity regardless of the load disturbances. This again confirms the effectiveness of the proposed circuit and control algorithm.

C. Comparative Study

The proposed single-phase converter is also compared with a conventional boost PFC converter whose dc-link voltage is

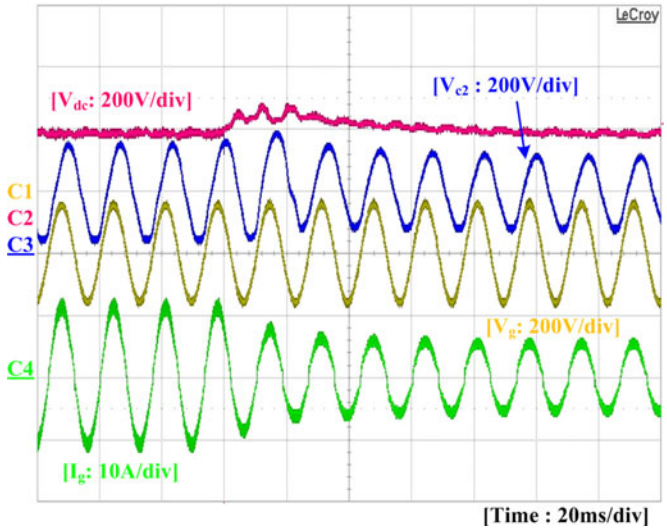

Fig. 14. Dynamic experimental waveforms showing 100% to 50% step-down load change. From top to bottom, dc-link voltage, lower capacitor voltage, grid voltage, and grid current.

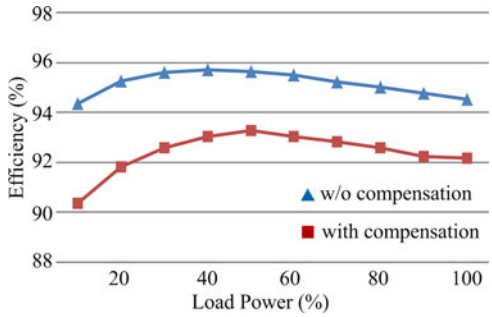

Fig. 15. Efficiency curve of the proposed single-phase converter compared with that of a conventional boost PFC.

maintained by electrolytic capacitors. In order to obtain a similar level of voltage ripple, the required dc-link capacitance, according to (13) will be 920 μF, which is more than 20 times of the proposed system. In experiment, two 470-μF/450-V electrolytic capacitors are used in parallel in the dc link. However, the measured dc-link capacitance is only 840 μF because of the tolerance of the capacitors.

The efficiency curves of the two systems are plotted in Fig. 15 and it shows that the proposed system may have 2.3% efficiency drop at full-load operation. This is because the third switching leg may introduce additional switching and conduction losses into the system. It is also clear that the efficiency drop may become more severe at light load as the modulation index of the symmetrical half-bridge is very small during such operating conditions. Efficiency drop is the main drawback of the proposed system and a possible solution could be to use advanced widebandgap power semiconductors with low on-state resistance and low switching losses.

In addition to the system overall efficiency, the power loss inside capacitors is particularly of interest because it may greatly influence the lifetime of the capacitors. The dc-link capacitors used in the proposed circuit are Vishay MKP1847 series and such film capacitors normally have a dissipation factor (DF) or also called the loss angle of 2e – 4 when the frequency is below 100 Hz. Then, its ESR at 60 Hz can be calculated as

$$\mathrm{ESR}_{Cf} = \frac{\mathrm{DF}}{\omega_n C_f} = \frac{2e-4}{120\pi \cdot (90e-6)} \approx 5.9\ \mathrm{m\Omega}. \tag{23}$$

The total power losses of C_1 and C_2 under full-load operation will be

$$\begin{aligned} P_{Cf} &= 2 \cdot (\omega_n C_f V_{C\_\mathrm{rms}})^2 \cdot \mathrm{ESR}_{Cf} \\ &= 2 \cdot [120\pi \cdot (90e-6) \cdot 121]^2 \cdot (5.9e-3) \approx 0.20\ \mathrm{W}. \end{aligned} \tag{24}$$

In comparison, the power loss of the electrolytic capacitors in a conventional PFC is also analyzed. The electrolytic capacitors are Panasonic ED series and their DF at 120 Hz (provided in the datasheet) is 0.15. Similarly

$$\mathrm{ESR}_{C\mathrm{dc}} = \frac{DF}{2\omega_n C_{\mathrm{dc}}} = \frac{0.15}{2 \cdot 120\pi \cdot (840e-6)} \approx 0.237\ \Omega \tag{25}$$

$$\begin{aligned} P_{C\mathrm{dc}} &= I_{\mathrm{ripple}}^2 \cdot \mathrm{ESR}_{C\mathrm{dc}} \\ &= (1000/380/\sqrt{2})^2 \cdot 0.237 \approx 0.82\ \mathrm{W}. \end{aligned} \tag{26}$$

It is clear that the capacitors in the proposed system would generate much lower power losses as compared to the conventional case and therefore, the heating effect can be basically neglected.

Table III compares the capacitive energy storage requirement for some common active power decoupling circuits. It should be noted that the $\omega_n C V_{\mathrm{dc}}^2$ term makes no physical meaning and ω_n used here is just a scaling factor for assessing the capacitance requirement, because it is quite intuitive that the higher the fundamental frequency, the lower the capacitance can be used in the dc link to obtain the same level of voltage ripple. The circuit in [19] and the proposed circuit actually exhibit the same capacitive energy storage requirement because for both of them, the ripple power is stored in the decoupling capacitors as pure ac form (the dc offset voltage in the proposed circuit is not for power decoupling purpose). The former one has slightly higher requirement because it is installed with more capacitance in the dc link and therefore, it has relatively longer holdup time in case of ac input lost. The proposed circuit may clearly stand out from the existing active power decoupling methods because the film capacitors used in the system are not only for power decoupling, but also for holding up the dc bus voltage, and therefore, the system will be more cost-effective.

V. Discussion

In fact, the proposed symmetrical half-bridge circuit can be regarded as a generic converter cell and it can be used to replace the dc-link capacitors in other advanced converter topologies, e.g., neutral point-clamped (NPC) converters and modular multilevel converters (MMCs), to cope with the system fluctuating power problem.

TABLE III
CAPACITIVE ENERGY STORAGE REQUIREMENT FOR SOME COMMON ACTIVE POWER DECOUPLING CIRCUITS

Description	[15]	[22]	[19]	Proposed circuit
Fundamental angular frequency ω_n	$2\pi \times 233$ rad/s	$2\pi \times 50$ rad/s	$2\pi \times 50$ rad/s	$2\pi \times 60$ rad/s
Nominal output power P_n	15 kW	600 W	4 kW	1 kW
DC-link capacitor Capacitance C/Operating voltage V	200 μF/540 V_{dc}	220 μF/450 V_{dc} (with small ac component)	120 μF/400 V_{dc}	45 μF/380 V_{dc}
Decoupling capacitor Capacitance C/ Operating voltage V/ $\frac{\sum \omega_n C V^2}{P_n}$	200 μF/350 V_{dc} (with small ac component) 8.08	1000 μF/50 V_{dc} 11.36	220 μF/240 V_{rms} 4.49	180 μF/121 V_{rms} 3.45

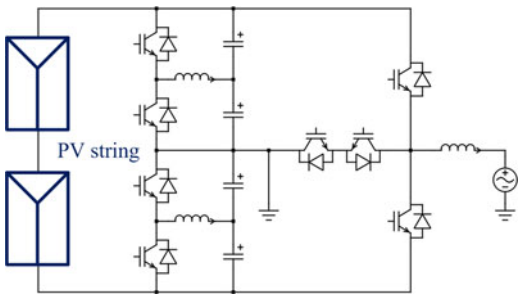

Fig. 16. NPC inverter with the proposed symmetrical half-bridge converter cell for the single-phase PV application.

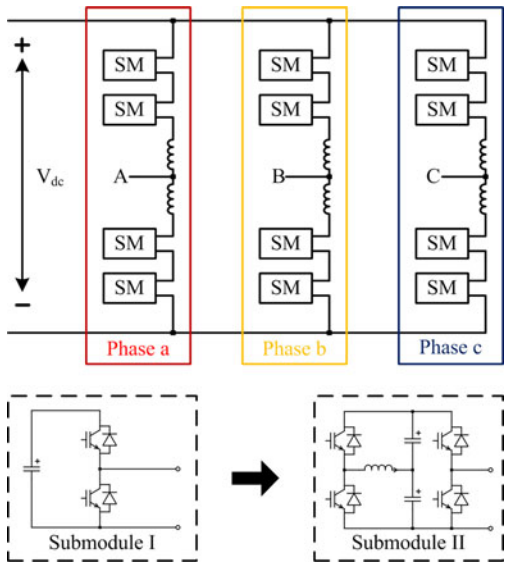

Fig. 17. MMC with the proposed symmetrical half-bridge converter cell for the HVDC application.

The NPC topology can be found in Conergy IPG S series single-phase PV inverters where a T-type phase leg is used to provide the three-level output voltage. With this configuration, the inverters may have fixed PV terminal-to-ground potentials and feature reduced switching harmonic contents in the output voltage. However, the PV panel voltage can be varying due to the ripple power from the ac side, and this may lead to decreased MPPT efficiency [25]. In order to solve this issue, the proposed converter cell can be embedded into a single-phase T-type NPC inverter as configured in Fig. 16. Through proper control, the film capacitors in the dc link can absorb those ac-side harmonics and give rise to smoother PV voltage, and thus higher solar energy yields.

This concept is equally applicable to the MMC topology shown in Fig. 17. The MMC converter is now one of the most common types of voltage source converters used in high-voltage direct current (HVDC) applications, because it has advantages like modularity, multilevel waveforms, high availability, as well as failure management [26]. However, a known problem of the MMC is that each submodule (SM) converter may need a large and bulky capacitor to hold the dc voltage. As the number of SM increases, the whole system may become very huge in size. The proposed converter cell could be a potential candidate to solve this issue and the voltage of each SM can be kept nearly constant with much reduced capacitance. Nevertheless, the capacitance reduction can only be achieved at the expense of increased number of active components and power losses, and minimum dc-link capacitance is still required in order to safely ride through those steep load changes that occurred in the system. Another design challenge is that, for both NPC and MMC applications, the dc-link voltage may not only contain double-line frequency ripple power but also the fundamental fluctuating power. In this case, the reference voltages of decoupling capacitors may no longer be sinusoidal and instead, they are distorted waveforms and can only be obtained through a closed-loop controller, e.g., another voltage control loop that can regulate the dc-link ripple voltage to be zero. The feasibility of this method will be studied in future research work.

VI. CONCLUSION

This paper has presented a symmetrical half-bridge circuit to decouple the fluctuating power in single-phase ac/dc and dc/ac systems. The dc-link capacitors in the proposed system may not only provide a high-voltage dc bus to support power conversion, but also absorb the system ripple power originated from the ac side. The resulting system is more cost-effective as compared to other existing active power decoupling methods because it

does not need additional passive components to store the system ripple energy. Experimental results under both steady-state and dynamic operations were obtained from a 1-kW PFC prototype and it shows that at least ten times capacitance reduction can be achieved by the proposed active power decoupling circuit. The ripple voltage in the dc link as well as the THD of the gird current can be significantly reduced, which proves the effectiveness of the proposed solution. The proposed symmetrical half-bridge can also be regarded as a generic converter cell and might be a promising solution for elimination of the fluctuating power and the reduction of dc-link capacitance in other advanced topologies, e.g., NPCs and MMCs.

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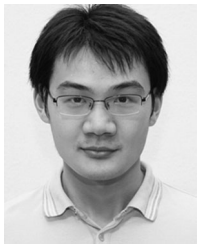

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