Low-Volume PFC Rectifier Based on Nonsymmetric Multilevel Boost Converter

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***Abstract*—This paper introduces a digitally controlled single-phase rectifier with power factor correction (PFC) based on a modified three-level boost converter topology. In comparison with the conventional boost-based systems, the new PFC rectifier has about three times smaller inductor and significantly lower switching losses. The improvements are achieved by replacing the output capacitor of the boost converter with a nonsymmetric active capacitive divider, with a 3:1 division ratio, and by utilizing the downstream converter stage for the capacitive divider's center-tap voltage regulation. The nonsymmetric voltage divider and applied switching sequence effectively provide four-level converter behavior using the same number of components as three-level converters. As a result, a 66% reduction of the inductor compared to the conventional boost-based PFC and a 33% compared to the standard three-level solutions operating at the same effective switching frequencies are also achieved. Experimental results obtained with a 400 W, 200 kHz, universal input voltage ($85\ V_{rms}$–$265\ V_{rms}$) PFC prototype demonstrate three times smaller inductor current ripple than that of the conventional boost converter allowing for the same inductor reduction. Efficiency improvements of up to a 6% are also demonstrated.**

***Index Terms*—AC-DC converters, boost converter, multilevel converters, power factor correction (PFC).**

I. Introduction

THE boost converter operating in continuous current mode (CCM) followed by an isolated dc–dc converter [1], [2] is among the most widely used configurations in single-phase rectifiers with power factor correction (PFC). This is mostly due to the continuous input current of the boost stage reducing electromagnetic interference (EMI) filtering requirements and fairly simple controller implementation [2]–[5]. This topology is used in a wide range of applications requiring between 100 and 500 W of power. Some examples include laptop and personal computers, monitors, communication equipment, TV sets, and other consumer electronics.

One of the major drawbacks of the boost-based front stage is a relatively large size of the inductor limiting its use in weight and volume sensitive applications. The large inductor also causes nonnegligible core losses [5], [6] and results in a relatively large parasitic capacitance of the winding introducing high-frequency noise [7]. The conventional boost-based topologies also suffer from problems related to switching losses [2], [8], causing heat dissipation, whose handling often requires bulky cooling components. The switching losses are mostly related to the operation of the transistor and the diode at the relatively high output, i.e., bus, voltage, which for the universal input ($85\ V_{rms}$ to $265\ V_{rms}$) boost PFCs it is usually about 400 V.

To minimize the size of the boost-based PFC system inductors, a number of methods have been proposed in the past [5]–[15]. Those can generally be divided into frequency-increase-based and topological changes.

Interleaved topologies [13]–[15], which reduce the inductor by effectively increasing the switching frequency, have proven to be effective solutions for larger power ratings, where the semiconductor switching components can be fully utilized. However, these solutions still suffer from relatively high switching losses and, when operating at light and medium loads, from either degradation of efficiency or quality of the input current waveform [16].

The topological methods [5]–[11], minimize both the inductor value and the switching losses, by reducing the stress of the components. In the flying capacitor multicell boost [7], derived from the multilevel concepts [12], these advantages are achieved by adding few switches and a relatively large flying capacitor. A three-level boost-based PFC [6] replaces the output capacitor of the boost converter with a compact active capacitive divider and, for the same switching frequency, results in a 50% reduction of the inductor value compared to the conventional boost-based solutions.

The main goal of this paper is to introduce a novel single-phase multilevel boost-based PFC rectifier that allows further reduction of the inductor volume while maintaining the benefits of the previously presented multilevel solutions. The new converter, named nonsymmetric multilevel boost (NSMB), and its digital controller are shown in Fig. 1. The system is primarily designed for the previously mentioned applications ranging between 100 and 500 W. The new topology reduces the size of the boost inductor to a one-third of the value required for the conventional boost PFC using the same number and volume of components as the three-level flying-capacitor-less-divider-based solution [6]. In essence, utilizing similar hardware as a three-level converter, the introduced topology operates as a four-level converter. This results in the improvements similar to those obtained by moving from a conventional two-level boost to a three-level topology without

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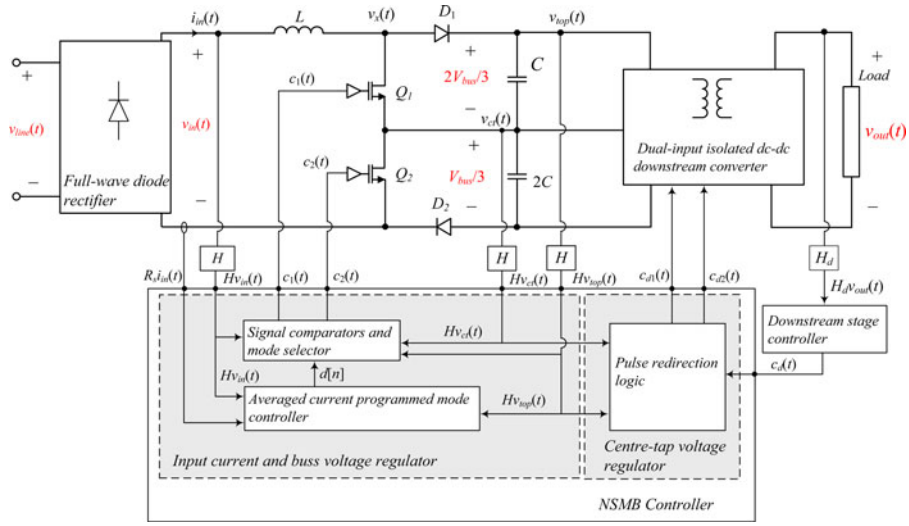


Fig. 1. NSMB-based PFC rectifier and its downstream stage.

increasing hardware complexity. Like other multilevel solutions the NSMB also reduces the switching losses and components voltage stress. The new topology is also well suited to be used with efficiency optimization methods and techniques developed for conventional boost-based topologies [17]–[21], allowing all advantages of the previously developed methods to be utilized here as well.

The inductor reduction is achieved by providing nonequal voltages across the capacitive divider cells, through a capacitor divider with a 3:1 conversion ratio, and applying a switching scheme that results in four inductor voltage levels. Compared to the conventionally used four-level boost solutions [7], [12], the NSMB has the same inductor volume when operating at the same switching frequency. Still, the new converter requires a smaller number of switching components and eliminates the bulky flying capacitor for the regulation of the voltages of the divider taps. The controller for the NSMB PFC of Fig. 1 consists of two blocks, input current and bus voltage regulator and the center-tap voltage regulator. The first block, regulates the input current $i_{\rm in}(t)$ and the intermediate bus voltage $V_{\rm bus}$, i.e., the output voltage of the first stage. This block is a modification of the digital average current-programmed-mode solution presented in [22]. The second block regulates the center-tap voltage of the capacitive divider $v_{ct}(t)$ such that the divider attenuation ratio of 3:1 is constantly maintained. This regulation is performed by steering the input currents of a dual-input downstream stage and, in that way regulating the discharging of the two capacitors. This block is designed to operate in synchronization with any dedicated constant frequency controller of the downstream stage producing a pulsewidth-modulated (PWM) signal $c_d(t)$.

This paper is organized as follows: The following section explains the principle of NSMB converter operation. In Section III challenges related to the control of the NSMB-based PFC rectifier are addressed and a practical digital control-based solution is presented. Section IV shows experimental results that verify advantages of the NSMB-based converter over conventional solutions.

II. Principle of Operation of the Nonsymmetric NSMB Front-End PFC Stage

To minimize the inductor volume, the introduced NSMB converter of Fig. 1 operates on the same fundamental principles as other multilevel solutions. It utilizes the fact that by reducing the voltage swing across the boost inductor the inductance value can be reduced as well.

The relation between the inductance value L and the maximum voltage swing of the inductor can be described with the help of the circuit and timing diagrams shown in Fig. 2(a). The figures demonstrate variation of the inductor voltage in a general boost-based converter operating with constant output voltage. In the presented equivalent circuit $v_{x\_\rm on}(t)$ and $v_{x\_\rm off}(t)$ are the values of the switching node voltage during the inductor charging and discharging phase, respectively. Fig. 2(b) shows that for the conventional boost the two values are equal to $v_{x\_\rm on}(t)=0$ and $v_{x\_\rm off}(t)=V_{\rm bus}$.

The analysis starts from the expressions for the inductor current ripple for a general boost-based converter

$$\Delta I_{\rm ripple}=\frac{v_{L\_\rm high}(t)}{2L}\frac{D}{f_{\rm sw}}=\frac{v_{\rm in}(t)-v_{x\_\rm on}}{2L}\frac{D}{f_{\rm sw}} \tag{1}$$

$$\Delta I_{\rm ripple}=-\frac{v_{L\_\rm low}(t)}{2L}\frac{D'}{f_{\rm sw}}=\frac{v_{\rm in}(t)-v_{x\_\rm off}}{2L}\frac{D'}{f_{\rm sw}} \tag{2}$$

where $v_{L\_\rm high}(t)$ and $v_{L\_\rm low}(t)$ are the high and the low values of the inductor voltage during one switching cycle, respectively, $v_{\rm in}(t)$ is the input voltage, $f_{\rm sw}$ is the switching frequency of the converter, and D is the duty ratio.

The maximum ripple, occurring for $D=0.5$ [6], can be described with the following expression, obtained by combining (1) and (2)

$$\Delta I_{\rm ripple\_max}=\frac{v_{L\_\rm high}(t)-v_{L-\rm low}(t)}{8L}\cdot\frac{1}{f_{\rm sw}}=\frac{V_{\rm swing\_L}}{8L}\frac{1}{f_{\rm sw}}$$
$$=\frac{V_{\rm swing\_x}}{8L}\frac{1}{f_{\rm sw}} \tag{3}$$

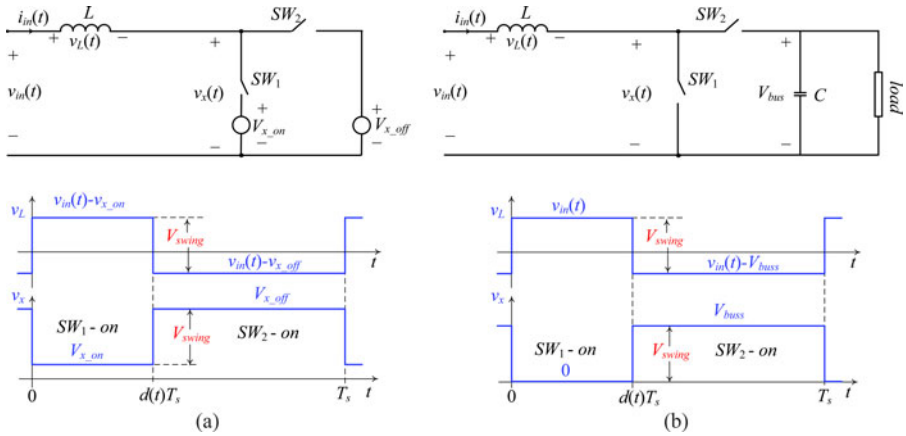


Fig. 2. Equivalent circuit for the analysis of the inductor voltage swing and the voltage waveforms of (a) a general boost-based converter and (b) the conventional boost.

where V_{swing_L} and V_{swing_x} are the voltage swings of the inductor and switching node, respectively. It can be seen that the ripple, which determines the inductance value [23], is linearly proportional to the voltage swing across the switching node. The relation also shows that, for the boost-based converters, *the inductor voltage swing is equal to the switching node swing and by minimizing that value, the inductor can be reduced without affecting the current ripple* amplitude.

This analysis shows that for the conventional boost the switching node voltage swing is equal to its output voltage. In typical PFC rectifiers, this voltage, labeled as V_{bus} in Fig. 2(b), is fairly high, usually around 400 V, causing the inductor value and the switching losses to be relatively large. In the applications of interest, the switching losses usually have a large influence on the overall power processing efficiency of the converter [5], [6], [24]. The losses also indirectly increase the overall system volume, by imposing additional cooling requirements for the semiconductor components.

To minimize the swing and, therefore, reduce both the inductor value and switching losses, in the NSMB converter of Fig. 1, an active capacitive divider with 3:1 conversion ratio replaces the output capacitor and switches of the conventional boost. This allows the switching node voltage to be changed between *four possible values:* 0, $V_{\mathrm{bus}}/3$, $2V_{\mathrm{bus}}/3$, and V_{bus}, effectively creating a four-level structure using a three-level configuration. The divider and its switching sequence are designed to allow $v_{x\_\mathrm{on}}(t)$ and $v_{x\_\mathrm{off}}(t)$ to be dynamically changed as the input voltage changes, such that the inductor voltage swing is limited to $V_{\mathrm{bus}}/3$. This value is three times lower than that of a conventional boost and 33% smaller than the voltage swing of the three-level topologies [6], [7] operating at the same effective switching frequency. As a result, equal reductions of the inductor are allowed and large efficiency improvements obtained. It should be noted that similar to the solution presented in [6], it would be possible to operate the NSMB at the twice switching frequency of the conventional boost while maintaining the same power processing efficiency. Such an operation would result in a six times smaller inductor volume compared to that of the conventional boost but would significantly increase power dissipation per unit volume potentially resulting in increased cooling requirements and reliability problems. For that reason, throughout the paper comparison was performed with the assumption that the topologies operate at the same effective switching frequency and simultaneous improvements in power processing efficiency and volume reduction are targeted.

A. Nonsymmetric Active Capacitive Divider

The operation of the nonsymmetric capacitive divider can be explained by looking at the rectified line input voltage and diagrams of Figs. 3–5. The diagrams describe three distinctive modes of converter operation, which depend on the instantaneous value of the rectified line voltage $v_{\mathrm{in}}(t) = |v_{\mathrm{line}}(t)|$ (see Fig. 1).

Mode 1: For $v_{\mathrm{in}}(t) < V_{\mathrm{bus}}/3$, the converter operates in mode 1, depicted with the diagrams of Fig. 3. Throughout this mode, switch SW_1 is kept on, reverse biasing the diode D_1, and the other two switches (SW_2 and D_2) are active, operating at the switching rate $f_{\mathrm{sw}} = 1/T_{\mathrm{sw}}$. The on time of SW_2, i.e., duty ratio, is regulated by the controller of Fig. 1. The current conducting paths for the both portions of a switching period are shown in Fig. 3 with bold lines, in red, where Fig. 3(a) corresponds to the inductor charging process, i.e., on time of SW_2, and Fig. 3(b) shows its discharging.

It can be seen that during the on-state of SW_2, $v_x(t) = 0$ and during its off state $v_x(t) = V_{\mathrm{bus}}/3$. Therefore, the maximum voltage swing across the inductor is $V_{\mathrm{bus}}/3$ equal to the voltage of the divider bottom capacitor. It should be noted in this mode both SW_2 and D_2 operate at $V_{\mathrm{bus}}/3$ and the switching losses are lower than those of the conventional boost and three-level boost, which switches operate at V_{bus} and $V_{\mathrm{bus}}/2$, respectively.

This mode is maintained as long as $v_{\mathrm{in}}(t)$ is lower than $V_{\mathrm{bus}}/3$ and the condition for the regular boost operation, i.e., the bottom capacitor voltage is larger than the input voltage, satisfied.

Mode 2: Mode 2 of operation, shown in Fig. 4, occurs for $V_{\mathrm{bus}}/3 < v_{\mathrm{in}}(t) < 2V_{\mathrm{bus}}/3$. In this mode, during the first portion of a switching period, corresponding to the transistor on-state in the conventional topology, SW_1 and D_2 are turned on and the switching node voltage is $V_{\mathrm{bus}}/3$ as it can be seen from Fig. 4(a). During the remaining portion of the switching period,

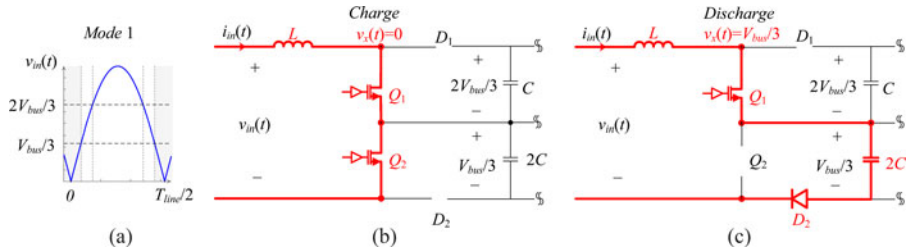


Fig. 3. Mode 1 of operation of the NSMB front-end stage: (a) input voltage range for mode 1; (b) equivalent circuit of the converter during inductor charging phase; (c) equivalent circuit during the discharging.

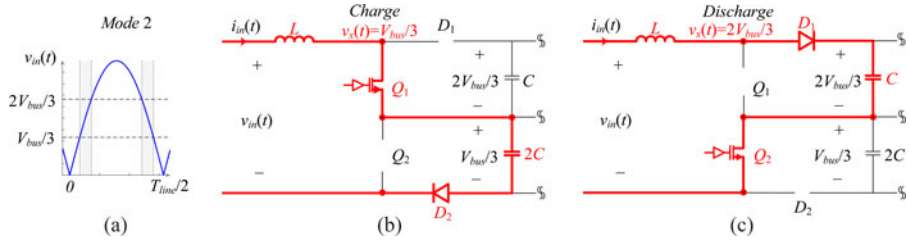


Fig. 4. Mode 2 of operation of the NSMB front-end stage: (a) input voltage range for mode 2; (b) equivalent circuit of the converter during inductor charging phase; and (c) equivalent circuit during the discharging.

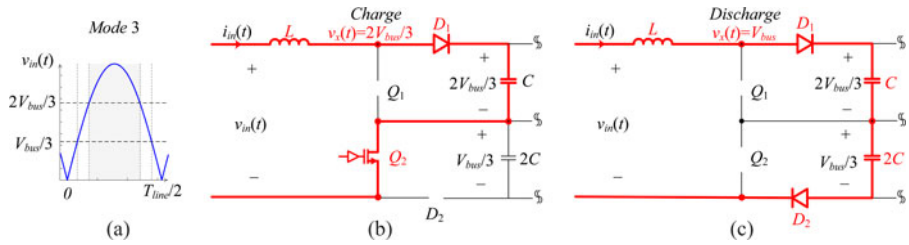


Fig. 5. Mode 3 of operation of the NSMB front-end stage: (a) input voltage range for mode 3; (b) equivalent circuit of the converter during inductor charging phase; and (c) equivalent circuit during the discharging.

SW_2 and D_1 are conducting and, as shown in Fig. 4(b), the switching node voltage is $2V_{\rm bus}/3$. It can be seen that, in this way, the absolute value of the voltage swing is again limited to $V_{\rm bus}/3$.

In this mode, the switching losses are approximately the same as those of the conventional boost (and three-level boost), since the total blocking voltage of the two switches operating in the each portion of a switching interval is equal to that of the conventional boost.

Mode 3: Mode 3, shown in Fig. 5, is activated when $v_{\rm in}(t)$ exceeds $2V_{\rm bus}/3$. Throughout this mode, the transistor SW_1 is turned off, allowing diode D_1 to conduct. In this mode, during the first portion of the switching interval, SW_2 is conducting and the voltage across the switching node is $2V_{\rm bus}/3$ as shown in Fig. 5(a). During the second portion of the interval, D_2 conducts and the switching node voltage is $V_{\rm bus}$. Again, the inductor voltage swing is limited to $V_{\rm bus}/3$.

In this mode the switching losses are again lower than that of the conventional boost and of the three-level boost, since both SW_2 and the D_2 interrupt only one-third of the converter output voltage.

Since, as mentioned earlier, in the applications of interest the switching losses are dominant, an analysis of conduction losses for the NSMB is given in Appendix A. It is shown that the conduction losses depend on the input voltage amplitude and the amounts of time NSMB spends in each of the three modes. The analysis also shows that, for an optimally designed NSMB, with switches D_1, SW_1 rated at $2V_{\rm bus}/3$ and SW_2, D_2 rated at $V_{\rm bus}/3$, the conduction losses are approximately the same as those of the conventional boost.

1) Volume Reduction

a) Inductor Volume: As shown in the theoretical analysis of Section II, the NSMB converter reduces the inductor value by three times compared to the conventional boost while retaining the same peak inductor current.

Since the inductor volume is proportional to its energy storage capacity [25], [26]

$$W_{E\_L} = \frac{1}{2} L I_{\rm peak}^2 \tag{4}$$

where $I_{\rm peak}$ is the peak inductor, it can be concluded that the inductor volume of the NSMB is three times smaller as well.

It should be noted that compared to the practical two-phase boost-interleaved PFC solutions [13], [25], [26], the inductor of the NSMB is about two times smaller. Even though the inductance value of the interleaved boost is reduced by four times, compared to the conventional boost the volume reduction is much smaller. As described in [25] and [26], the actually

achievable volume reduction is around a 32%, due to the higher inductor current ripple and, therefore, a larger peak current.

b) Output Capacitor Volume: In the NSMB converter, the output capacitor of the conventional boost with a value of $C_{\rm out}$, rated at $V_{\rm out}$, is replaced with $C_{\rm out1} = 3C_{\rm out}/2$, rated at $2V_{\rm out}/3$ and $C_{\rm out2} = 3C_{\rm out}$, rated at $V_{\rm out}/3$. The output capacitance of the boost PFC is chosen to meet desired hold-up time energy requirement [27] and the output voltage ripple.

By using the same energy-based criteria to compare the capacitors sizes it can be seen that the NSMB has the same total capacitor volume as the conventional boost and the three-level boost, since, ideally, the size of a capacitor is proportional to its energy storing capacity [28], i.e., to its $1/2CV^2$ product.

The output voltage ripple comprises two components, the high-frequency ripple, at the switching frequency, and the low-frequency component at twice the line frequency. In both the conventional boost PFC and the introduced NSMB, the high-frequency component is much smaller than the component at the twice line frequency and, therefore, can be neglected in the analysis [23]. The following analysis shows that the dominant low-frequency component is the same for the both topologies.

To find the amplitude of the dominant ripple, we can look at the general case, where an increase of the energy ΔE creates a voltage difference ΔV across the capacitor C having an initial voltage V. This voltage difference can be found using the following relation:

$$\Delta E = \frac{1}{2}C(V+\Delta V)^2 - \frac{1}{2}C(V)^2 = \frac{1}{2}C(2V\Delta V + \Delta V^2). \tag{5}$$

For the case when $V > \Delta V$, which is valid for the systems under investigation, the following approximate expression for the voltage deviation:

$$\Delta V \approx \frac{\Delta E}{CV} \tag{6}$$

can be easily derived from (5).

For a general PFC, the increase of the energy can be calculated by looking at the instantaneous power delivered from the ac source [23]

$$p_{\rm in}(t) = P_{\rm load}[1 - \cos(2\omega_{\rm line}t)] \tag{7}$$

which, as shown in Fig. 6, has two components, a dc component equal to the load power $P_{\rm load}$ and an ac component at twice the line frequency. The ac portion of this input power ($P_{\rm in\_ac}(t)$ shown in Fig. 6(b) creates the dominant output voltage ripple. To calculate the peak-to-peak value of this ripple, the amount of energy stored in the capacitor over a $T_{\rm line}/4$ period (shaded area in the diagram of Fig. 6(b) can be calculated as

$$\Delta E_{\rm in\_ac} = \int_{t_0}^{t_0+T_{\rm line}/4} p_{\rm in\_ac}(t)\,dt = \int_{t_0}^{t_0+T_{\rm line}/4} P_{\rm load}[-\cos(2\omega_{\rm line}t)]dt = \frac{P_{\rm load}}{\omega_{\rm line}} \tag{8}$$

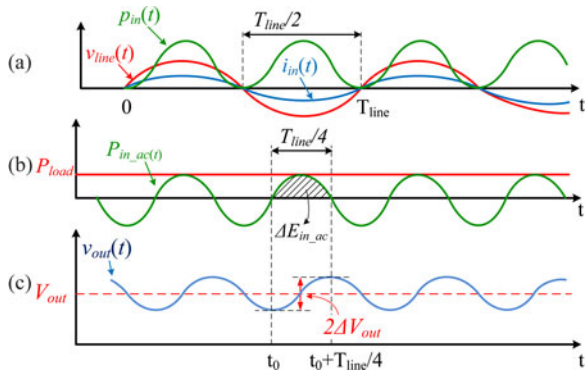


Fig. 6. Waveforms of the output capacitor voltage of an ideal PFC circuit; (a) instantaneous input power, voltage, and current waveforms; (b) decomposition of input power components; and (c) output capacitor voltage ripple.

and the output capacitor ripple for a boost PFC found by combining (6) and (8)

$$2\Delta V_{\rm out\_boost} = \frac{\Delta E_{\rm in\_ac}}{C_{\rm out}V_{\rm out}} = \frac{P_{\rm load}}{\omega_{\rm line}C_{\rm out}V_{\rm out}}. \tag{9}$$

In the case of the NSMB converter, the energy described with (8) is stored across the two output capacitors $C_{\rm top}$ and $C_{\rm bottom}$. The distribution of this energy between capacitors, in general, is not equal and depends on the input voltage level and the portion of the time the converter is spending in each of the operating modes. However, the total energy given to the system is the same as in the boost case and can be described with the following expression:

$$\Delta E_{\rm in\_ac} = \Delta E_{\rm in\_ac\_top} + \Delta E_{\rm in\_ac\_bottom} \tag{10}$$

where $\Delta E_{\rm in\_ac\_top}$ and $\Delta E_{\rm in\_ac\_top}$ are the portions of energy stored in the top and bottom capacitors, respectively.

By replacing the values in (6) for the NSMB case, the voltage ripples for the top and bottom capacitors $\Delta V_{\rm top}$ and $\Delta V_{\rm bottom}$, respectively, can be obtained as

$$2\Delta V_{\rm out\_bottom} = \frac{\Delta E_{\rm in\_ac\_bottom}}{C_{\rm out\_bottom}V_{\rm out\_bottom}} = \frac{\Delta E_{\rm in\_ac\_bottom}}{(3C_{\rm out})(V_{\rm out}/3)} = \frac{\Delta E_{\rm in\_ac\_bottom}}{C_{\rm out}V_{\rm out}} \tag{11}$$

$$2\Delta V_{\rm out\_top} = \frac{\Delta E_{\rm in\_ac\_top}}{C_{\rm out\_top}V_{\rm out\_top}} = \frac{\Delta E_{\rm in\_ac\_top}}{(3/2C_{\rm out})(2V_{\rm out}/3)} = \frac{\Delta E_{\rm in\_ac\_top}}{C_{\rm out}V_{\rm out}} \tag{12}$$

and, since both of the ripple voltages are in phase, the overall ripple of the NSMB can be found as

$$2\Delta V_{\rm out\_NSMB} = 2\Delta V_{\rm out\_top} + 2\Delta V_{\rm out\_bottom}$$

$$2\Delta V_{\rm out\_NSMB} = \frac{\Delta E_{\rm in\_ac\_top} + \Delta E_{\rm in\_ac\_bottom}}{C_{\rm out}V_{\rm out}} = \frac{\Delta E_{\rm in\_ac}}{C_{\rm out}V_{\rm out}} = \frac{P_{\rm load}}{\omega_{\rm line}C_{\rm out}V_{\rm out}}. \tag{13}$$

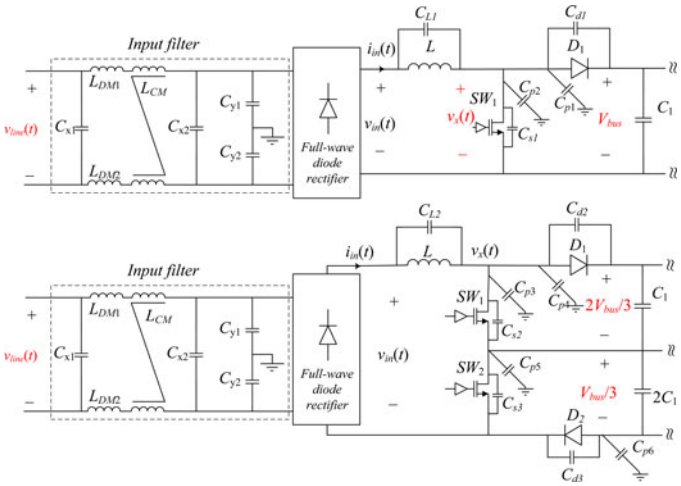


Fig. 7. Input filter and parasitic capacitances of the (top) boost PFC circuit and (bottom) NSMB PFC circuits.

A comparison of (9) and (13) reveals that both converters have the same ac output voltage ripple while utilizing same output capacitance volume.

c) Input Filter Volume: To fully assess advantages of the NSMB topology over other solutions, input filter requirements are compared in the following subsection. It is shown that, due to the lower energy of the input current ripple and noise components, the NSMB potentially can operate with a smaller input filter than that of the conventional boost and of the standard three-level boost. In here, the topological differences in the analysis of the filter requirements are only taken into account and the other parameters, such as, influences of the PCB layout and footprints of the components, which also affect the filter volume [29], are left to be studied in the future.

A properly designed input filter attenuates the input current ripple and two noise components generated by the switching action of the power supply. Those are the differential-mode (DM) noise and common-mode (CM) noise.

The previous analysis shows that, for the same switching frequency and three times smaller inductor, the maximum amplitude of the inductor current ripple is the same for all three configurations. However, as it will be confirmed in the experimental results section, in the case of the NSMB the total root-mean-square (rms) value of the ripple component is smaller than that of the conventional boost, due to longer periods during which the converter operates with close to zero ripple during mode transitions.

To analyze the influence of the noise components, the equivalent circuits of Fig. 7 can be used. The figure shows the input filter, which includes the ripple and DM reduction components C_x and $L_{\rm DM}$ and the portion of the filter for CM reduction, comprising of C_y and $L_{\rm CM}$.

The differential component of the high-frequency noise is formed by the current flowing through the input port of the converter [29], through a path formed by the stray capacitances of the inductor (labeled as C_{L1} and C_{L2}). In the case of the NSMB this stray capacitance is smaller than those of the conventional boost and the three-level boost, due to the smaller value of the inductor itself [7]. Therefore, this noise is smaller, as demonstrated in the spectrum measurement, shown in the experimental section. The lower CM noise allows for reduction of the DM filter components.

The CM noise is mainly generated by the currents flowing from the switching node to the ground through the parasitic capacitance created by the heat sinks [29], in Fig. 7 labeled as C_{p1} to C_{p6}. The power of that noise, and therefore the size of the CM filter, is proportional to the amount of energy stored in those parasitic capacitances during each switching cycle.

Even though the NSMB (and conventional three-level boost) have a larger number of parasitic components commutating between the switching node voltage level and the ground, the energy dissipated in them is smaller. This is mainly due to a lower voltage swing. Fig. 7 shows that in the boost converter, in each cycle, the heat sink parasitic capacitors of $\rm SW_1$ and D_1 (C_{p2} and C_{p1}) are charged/discharged with a voltage swing equal to $V_{\rm bus}$, where the size of each capacitor is proportional to the switch size and the heat sink area. Therefore, the CM noise is proportional to the energy transferred through these two capacitors

$$W_{\rm cm\_boost} = \frac{1}{2}C_{p1}V_{\rm bus}^2 + \frac{1}{2}C_{p2}V_{\rm bus}^2. \tag{14}$$

In the case of the NSMB converter, the parasitic capacitors C_{p1} and C_{p2} are replaced by four capacitors, i.e., C_{p3} to C_{p6} corresponding to $\rm SW_1$, D_1, $\rm SW_2$, and D_2, respectively (see Fig. 7). Those capacitors are exposed to a three times smaller voltage swing, and therefore, for the worst case condition, when the line input is the largest, their total energy is

$$W_{\rm cm\_NSMB} \approx \frac{3.5}{18}C_{p3}V_{\rm bus}^2 + \frac{2.3}{18}C_{p4}V_{\rm bus}^2 + \frac{1}{18}C_5V_{\rm bus}^2 + \frac{1}{18}C_{p6}V_{\rm bus}^2. \tag{15}$$

By comparing (14) and (15), it can be concluded that, for the same capacitance values, i.e., for the case when $C_{p3}+C_{p4}+C_{p5}+C_{p6} = 3^*(C_{p1}+C_{p2})$, the total energy stored in the capacitances causing CM noise is about 1.3 times smaller for the NSMB case. A similar analysis for the three-level boost can show that, since its voltage swing is $V_{\rm bus}/2$, the total reduction of the energy compared to the boost with the same capacitances is about 14%, i.e., 1.16 times smaller energy. In an optimized design of the NSMB (discussed in the Appendix A), where switching components and heat sinks are smaller, an even larger improvement in the CM noise reduction can potentially be achieved.

B. Center-Tap Voltage Balancing and Isolated Downstream Stages

The balancing of the capacitor tap voltages in converter topologies incorporating capacitive voltage dividers is often performed with relatively large flying capacitors [30], [31] or by redirecting the current of the inductor [6], [12], [32]. For the introduced NSMB, the previously used center-tap voltage regulation method cannot directly be applied, due to the nonequal voltage sharing.

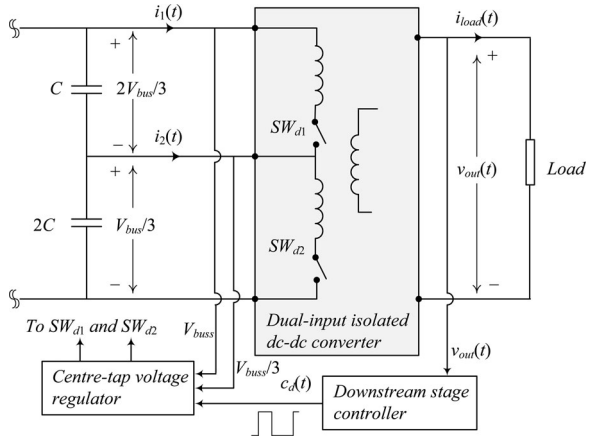


Fig. 8. Block diagram of the center-tap voltage balancing system based on the downstream converter current steering.

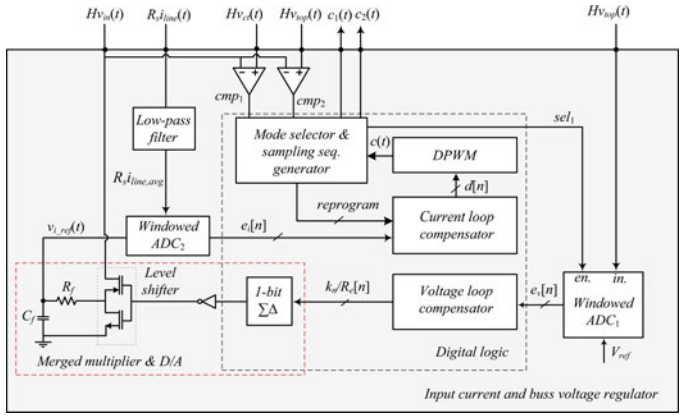


Fig. 9. Block diagram of the input current and bus voltage regulator.

To regulate the center-tap voltage at $V_{\rm bus}/3$ without a flying capacitor, here, the downstream converter, inevitably existing in practically all systems of interest, is used. The regulation is performed by modifying the technique presented in [32], where the input current of the downstream portion of a merged switched-capacitor buck converter regulates the center-tap voltage of its front end. In this case, a two-input isolated downstream stage is used, as shown in Fig. 8. The center-tap voltage is regulated with the two input currents of the downstream converter, $i_1(t)$ and $i_2(t)$ with the help of the center-tap voltage regulator.

Depending on the center-tap voltage level, the switch-selection logic redirects the PWM signal produced by the dedicated downstream stage controller, $c_d(t)$, between the two switches ($\rm SW_{d1}$ and $\rm SW_{d2}$). The switches are controlled such that the current (charge) is taken either from the top or from the bottom capacitor only. When the center-tap voltage is exceeding desired $V_{\rm bus}/3$ level more current is taken from the bottom cap and when it is lower the top cap provides more current.

III. Practical Controller Implementation

The controller of Fig. 1 consists of two main blocks: input current and voltage regulator and center-tap voltage regulator. This section addresses challenges related to the practical NSMB controller realization and shows a hardware-effective solution for its implementation.

A. Input Current and Bus Voltage Regulator

The controller of Fig. 9 is a modified version of the average current programmed mode architecture used for a conventional boost-based PFC [33]. In this modification, a new block, named *mode selector and sampling sequence generator* is added and the sampling sequence modified, to accommodate operation with a larger number of switches and eliminate potential stability problems that will soon be addressed. For the same reason the current loop compensator is also slightly modified.

The regulation of the input current and the output voltage is performed in a similar manner as in the previous solutions [33]–[35]. Based on the digital equivalent of the bus voltage, error value $e_v[n]$ is produced by the $\rm ADC_1$. Based on this value the voltage loop compensator creates a signal $k[n]$/*Re*, which is inversely proportional to the desired emulated resistance seen at the input of the PFC rectifier [23]. This value is then passed to the 1-*bit sigma-delta modulator* that, together with the level shifter and the RC filter creates a structure behaving as a merged analog multiplier and digital-to-analog converter eliminating the need for a costly digital multiplier [33].

This merged structure produces an analog reference

$$v_{i\_\rm ref}(t) = Hv_{\rm in}(t)\frac{k[n]}{R_e} \tag{16}$$

for the current loop, where H is the gain of the input voltage attenuator and, as mentioned before, $v_{\rm in}(t)$ is the rectified input voltage (Fig. 1). The created analog value is used as the reference for the current loop. This reference is then compared to the output of the input current sensor $R_s i_{\rm line}(t)$ and a digital equivalent of the current error signal $e_i[n]$ is created, by the windowed $\rm ADC_2$ [33], [36]. The resulting error is sent to the current loop proportional-integral (PI) compensator that produces control signal [33]

$$d[n] = d[n-1] + ae_i[n] + be_i[n-1] \tag{17}$$

where $d[n]$ and $d[n-1]$ are the current and previous value of the duty ratio control variable, and the compensator coefficients a and b are selected following the procedure shown in [36]. The produced $d[n]$ value is the control input for the digital PWM (DPWM) producing PWM signal $c(t)$.

The produced PWM signal $c(t)$ is then passed to the mode selector, which operation is described in the following subsection.

To eliminate switching noise related problems and at the same time obtain the average value of the inductor current over one switching cycle, the current is sampled using the techniques described in [38], [39]. Depending on the instantaneous value of $d[n]$, the current is sampled either at the half of the "on" or at the half of the "off" portion of a switching interval.

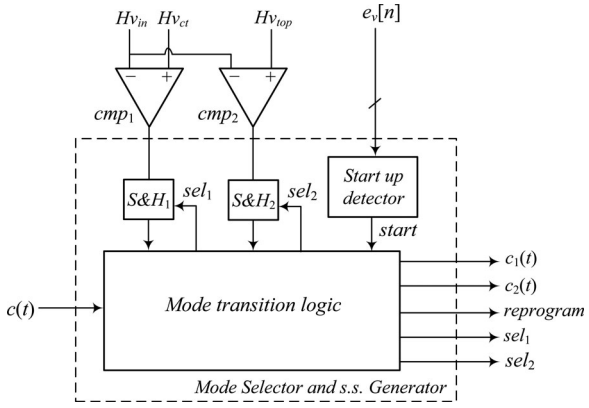


Fig. 10. Block diagram of the mode selector and sampling sequence generator.

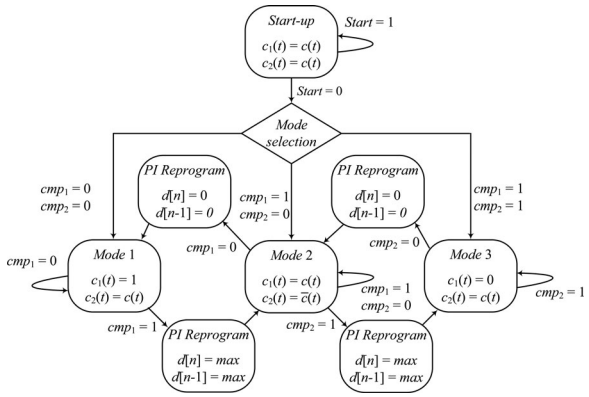


Fig. 11. State flow diagram of the mode selector logic.

B. Mode Selector and Sampling Sequence Generator

The mode selector and sampling sequence generator, whose block diagram is shown in Fig. 10, outputs PWM signals $c_1(t)$ and $c_2(t)$ for controlling the NSMB transistors SW_1 and SW_2, respectively. During mode transients the selector also changes stored values of the digital current loop compensator, to provide seamless transition between different modes. The detection of the mode of operation is performed with the two comparators (cmp_1 and cmp_2) and with the start-up logic, shown in Fig. 10. The comparators cmp_1 and cmp_2 monitor the input voltage and detect the transition points at which the $v_{\mathrm{in}}(t) = v_{ct}(t) = V_{\mathrm{bus}}/3$ and $v_{\mathrm{in}}(t) = v_{\mathrm{top}}(t) = 2V_{\mathrm{bus}}/3$. The compensators also initiate mode transition by sending the signals to the *mode transition logic*. Based on the state of the comparators and the previous state of the NSMB power stage, the transition logic redirects $c(t)$ to appropriate transistors. The start-up detector indicates power up condition of the converter by observing $e_v[n]$ and sends the *start* signal to the mode transition logic, which provides a gradual rise of the bus voltage upon a power up. The mode transition logic is a finite-state machine (FSM), which operation is demonstrated with the diagram of Fig. 11 and described in the following sections.

1) Seamless Mode Transitions: To understand the stability problem and a solution for it we can observe how the required conversion ratio changes in the conventional boost-based PFC and in the NSMB-based system. In the conventional boost, to maintain a constant bus voltage, the conversion ratio changes gradually with changes in the input voltage. On the other side, in the NSMB the conversation ratio drastically changes with each mode transition. Therefore, the duty ratio value required for maintaining the inductor volt–second balance and the stable output voltage abruptly changes as well. From a practical point of view this represents a potential problem, since the delays in the controller reaction could cause mode transition related stability problems.

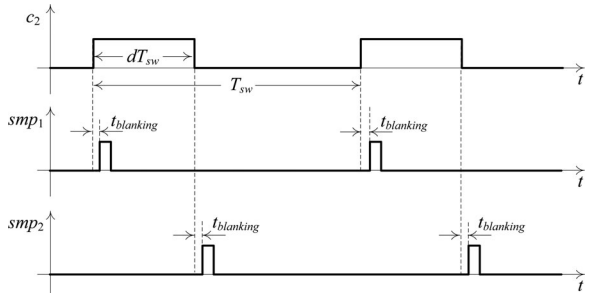


Fig. 12. Waveforms of the sampling sequence generator.

For example, it can be seen that at the point where the $v_{\mathrm{in}}(t)$ is exceeding $V_{\mathrm{bus}}/3$ (mode 1 to mode 2 transition), the required conversion ratio changes from one to infinity, requiring controller to change from 0 to the full duty ratio value in a single switching cycle.

To overcome this problem, after each mode transition, the mode selector immediately reprograms the current and the previous values of the duty ratio in the digital current loop compensator, i.e., $d[n]$ and $d[n-1]$ of (16). This is performed through the *reprogram* signal, shown in Fig. 10. The decision about the new duty ratio values is made based on the recognition that after each mode transition, the new duty ratio will be either zero or one. Since at those points, the required conversion ratio of NSMB is either one or infinite. Therefore, after each transition point is detected by the comparators, the mode control logic either sets both $d[n]$ and $d[n-1]$ to 0 or to their maximum value. The diagram of Fig. 10 shows the reprogramming values of the PI compensator for all four mode transitions.

2) Sampling Sequence: By looking at the operation of the NSMB (see Figs. 3–5), it can be noticed that for some switching states one of the two output capacitors does not share the same ground with the rest of the circuit. While from the output load, which is galvanically isolated from the front end stage, this does not represent a problem, this floating ground affects measurements of the capacitor tap voltages. To measure the tap voltages without the use of relatively costly differential amplifiers, sample and hold circuits (S&H) shown in Fig. 10 are used, and the sampling of the capacitor tap voltages is done at particular time instants denoted by signals smp_1 and smp_2 as shown in the diagram of Fig. 12. The value of the top capacitor voltage is sampled during the on state of Q_2 and for the bottom capacitor the data acquisition is performed during D_2 conduction time. The ADC_1 (see Fig. 1) also samples $v_{\mathrm{top}}(t)$ during D_2 conduction time, to obtain the bus voltage value.

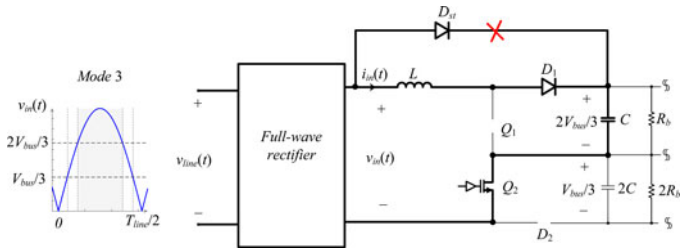


Fig. 13. Problem of utilizing bypass diode in the NSMB topology.

3) Start Up: The bypass diode commonly used to ease start-up and inrush current problems in conventional boost solution [40] cannot be used with the NSMB and similar multilevel solutions [4]–[6], [9]. As shown in Fig. 13, the bypass diode D_s [40] would short connect the inductor during the first portion of switching period in mode 3 [see Fig. 5(b)], when $v_{\rm in}(t) > v_{\rm top}(t)$.

To eliminate the start-up problem, the switching sequence is modified during power up, signaled by the high value of *start* signal produced by the detector (see Fig. 10). During this mode, the NSMB operates as a conventional boost, such that both transistors, i.e., Q_1 and Q_2 of Fig. 1, are turned on during the first portion of a switching interval and D_1 and D_2 are allowed to conduct during the rest of the switching period, as shown in Fig. 11. Such operation delivers equal amounts of charge to the both divider capacitors and, ideally, the desired 2:1 distribution of the bus voltage. Possible voltage variations due to component tolerances are eliminated with the bleeding resistors [41] R_b forming a 3:1 resistive divider. This mode ends when the capacitors are charged to their reference values and the *start* signal becomes low, causing the NSMB to switch to the regular mode of operation described in Section II and by the diagram of Fig. 11.

To eliminate the inrush current problem [40] a number of previously presented solutions can be used [40], [42]–[44].

C. Center-Tap Voltage Regulator

As described in the previous section, the regulation of the capacitor voltages is performed with the input current of the downstream converter. This process is controlled by the *center-tap voltage regulator* that redirects current of the downstream converter and in that way, regulates the discharging of the both NSMB capacitors.

The downstream converters that can be used with NSMB have two inputs and also utilize the advantages of reduced voltage swing to minimize the volume and switching losses. Two of many possible implementations of the downstream stages include two input nonsymmetric flyback [22] and the two-input nonsymmetric forward. Figs. 14 and 15, describe the operation of the center-tap voltage regulator with a nonsymmetric forward converter. The transformer of the forward has two primary windings, where the winding connected to the top capacitor (i.e., capacitor with higher voltage) has twice as many turns as the one connected to the bottom capacitor. The current of the top winding is controlled by the transistor Q_{d1} and of the bottom by Q_{d2}.The output voltage of the downstream stage is regulated with its own controller that produces PWM signal $c_d(t)$, which is passed to the center-tap regulator though an optocoupler. The center-tap regulator sends $c_d(t)$ either to Q_{d1} or to Q_{d2}, creating signals $c_{d1}(t)$ and $c_{d2}(t)$ respectively, as shown in Fig. 15. The two signals are sequenced such that the center-tap voltage is kept at $V_{\rm bus}/3$ level. To achieve this, the center-tap voltage is compared with three times attenuated bus voltage using two comparators (see Fig. 14) whose outputs are connected to the block named *switch selection logic*. The switch selection logic (see Fig. 14) implements the charge-balancing algorithm presented in [32], to keep the capacitors voltages regulated.

When the center-tap voltage is inside regulation band $V_{\rm bus}/3 \pm \Delta v_{ct}$, where Δv_{ct} is the allowable center-tap voltage variation, the switch selection logic alternates the signal $c_d(t)$ between Q_{d1} and Q_{d2} after each switching cycle of the downstream converter. As a result, equal voltage drops across both capacitors occur as shown in Fig. 15, since a two times larger charge (i.e., current) is taken from the bottom capacitor having twice the capacitance value.

If the center-tap voltage exceeds the regulation band, comparator $\rm cmp_1$ is activated and the regulation sequence is modified, such that the discharging of the top capacitor is skipped for several cycles, until the center-tap voltage is reduced to $V_{\rm bus}/3$ level. Similarly, if the center-tap voltage drops below $V_{\rm bus}/3 - \Delta v_{ct}$, the comparator $\rm cmp_2$ is triggered and the discharging of the bottom capacitor is interrupted for several cycles.

D. Design Tradeoffs

By comparing the practical implementation of the NSMB to that of the conventional boost solution [23], it can be seen that a design tradeoff is involved. The NSMB requires a larger number of components (the same as three-level solutions), high-side gate drivers, more complex control, and a nonconventional downstream stage. The following section showing experimental results demonstrates that in terms of the total volume and power processing efficiency this design is favorable in the targeted applications, providing 100–500 W of power and operating at switching frequencies in the range of 100–200 kHz. The inductive components and heat sinks are by far the largest contributors to the overall volume and the weight of the converter. The experimental validation shows that the NSMB has significantly better power processing efficiency and lower volume than the single-phase and interleaved boost-based solutions, which are predominantly used in the applications of interest.

Also, the capacitive divider at the output of the NSMB allows for a reduction in the volume of the downstream stage and potentially, its efficiency improvement.

Therefore, it can be envisioned that the advantages of the NSMB can potentially be fully utilized in a system where multiple semiconductor components would be integrated on a semiconductor chip and optimally sized, in terms of blocking voltage and conducting current. Such an implementation on a dedicated IC would probably not only result in a reduction of the number of components but also, as described in the following section,

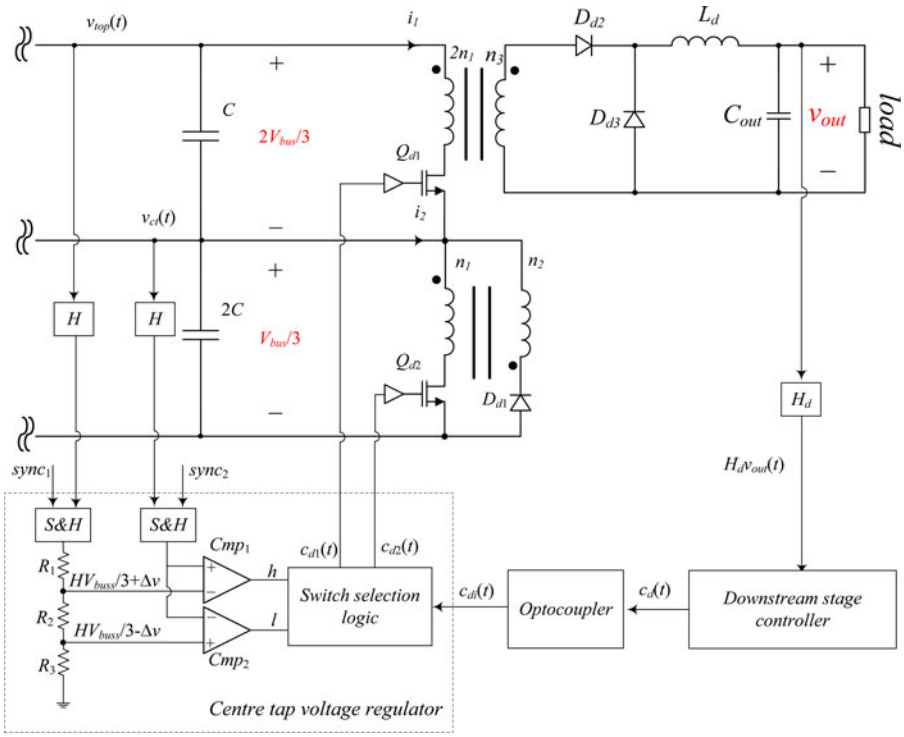


Fig. 14. Center-tap voltage controller regulating operation of a forward-based downstream stage.

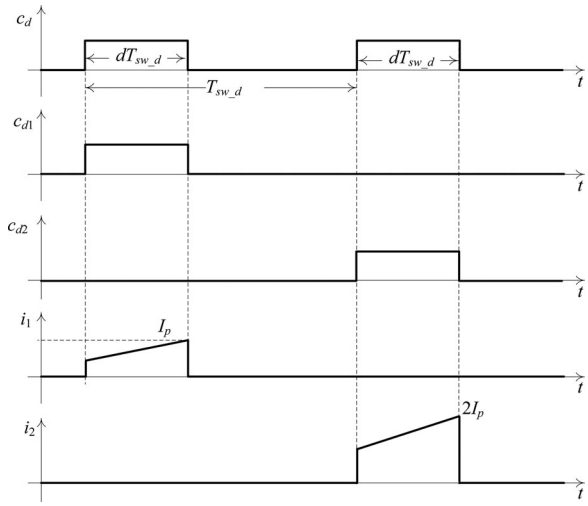


Fig. 15. Key waveforms of the center-tap voltage regulator (from top to bottom): $c_d(t)$—PWM signal of the downstream stage controller; $c_{d1}(t)$—control signal for Q_{d1}; $c_{d2}(t)$—control signal for Q_{d2}; $i_1(t)$—discharging current of the top capacitor of the NSMB; $i_2(t)$—discharging current of the bottom capacitor of the NSMB.

in further efficiency improvements, due to smaller parasitic capacitances and resistances of the components.

E. Extension to Higher Power Levels

The NSMB configuration of Fig. 1 is primarily designed for the PFC applications below 500 W. In order to utilize the converter for higher power ratings, where the conductions losses are becoming dominant, the concept of interleaving, widely used with the conventional solutions [13], [25], could potentially be

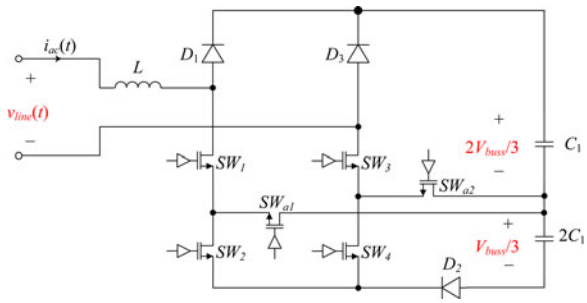


Fig. 16. Bridgeless NSMB converter topology.

applied here as well. In this case, multiple single-phase NSMB converters, each followed by an isolated dc–dc converter could be connected in parallel.

For the PFC applications exceeding 1 kW, where, as demonstrated in [17] and [45], the diode rectifier significantly degrades power processing efficiency, the bridgeless modification of the NSMB, shown in Fig. 16, could potentially be used. The transformation of the converter into its bridgeless version is performed using the principles demonstrated in [17], [45], and [46]. Validations of potential advantages of the modified NSMB topologies over the conventional solutions would require further investigation and are beyond the scope of this paper.

IV. Experimental System and Results

To validate the operation of the introduced nonsymmetric boost-based PFC rectifier, a universal-input 400 W, 200 kHz experimental prototype was built, based on the diagrams of Figs. 1,

TABLE I
CONVERTER PARAMETERS

	V_{out}	P_{out}	f_{sw}	Output capacitor(s)	Inductor	Inductor volume
Boost PFC	400 V	400 W	200 kHz	C=100 μF (420 V)	L= 670 μH	44.1 cm^3 [48]
NSMB PFC	400 V	400 W	200 kHz	C_{top} =150 μF (300 V) C_{bottom}=300 μF (150 V)	L= 220 μH	14.5 cm^3 [49]
3-level boost PFC	400 V	400 W	200 kHz	C_{top} =220 μF (220 V) C_{bottom}=220 μF (220 V)	L= 330 μH	24.8 cm^3 [50]

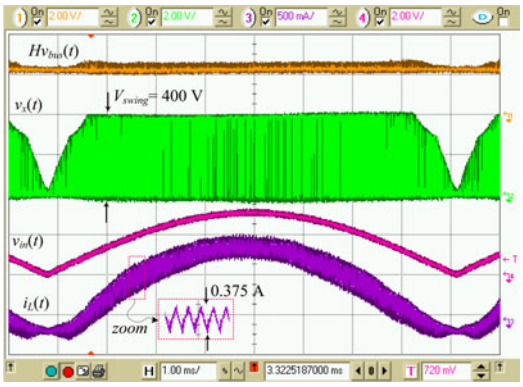


Fig. 17. Key waveforms of the conventional boost-based PFC rectifier; top to bottom: Ch.1 (top): attenuated output voltage, $Hv_{\rm bus}(t)$ (2 V/div); Ch.2 (upper middle): switching node voltage $v_x(t)$ (200 V/div); Ch.3 (lower middle): input line current $i_L(t)$ (0.5 A/div); Ch.4 (bottom): input line voltage $v_{\rm in}(t)$ (200 V/div). Timescale is 1 ms/div. Operating conditions: $v_{\rm line} = 220\ {\rm V_{rms}}, V_{\rm bus} = 400\ {\rm V}, P_{\rm out} = 100\ {\rm W}, C = 100\ {\rm mF}, L = 680\ {\rm mH}$.

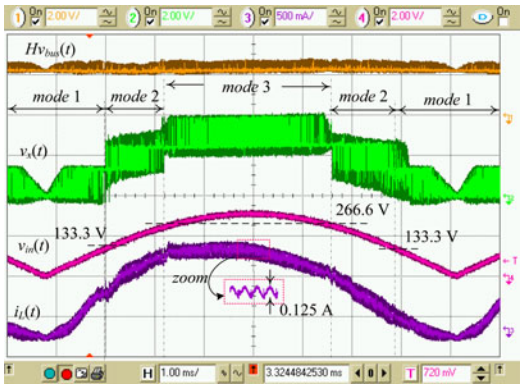


Fig. 18. Key waveforms of the NSM-based PFC rectifier; top to bottom: Ch. 1 (top): attenuated output voltage, $Hv_{\rm bus}(t)$ (2 V/div); Ch. 2 (upper middle): switching node voltage, $v_x(t)$ (200 V/div); Ch. 3 (lower middle): input line current, $i_L(t)$ (0.5 A/div); Ch. 4 (bottom): input line voltage, $v_{\rm in}(t)$ (200 V/div). Timescale is 1 ms/div. Operating conditions $v_{\rm line} = 220\ {\rm V_{rms}}, V_{\rm bus} = 400\ {\rm V}, P_{\rm out} = 100\ W, C_{\rm top} = 150\,{\rm mF}, C_{\rm bottom} = 300\ {\rm mF}, L = 680\ {\rm mH}$.

9, 10, 11, and 14. Also, its performances are compared to that of a conventional boost-based PFC prototype and a three-level boost converter [6], having the same effective switching frequency, seen by the inductor, and the output power rating. Similar to validation procedures presented in [17]–[21], the comparison of the NSMB is performed with the conventional boost, in order to assess the sole effect of the new topology on the performance improvements and to be able to directly compare it with other performance improving solutions. The boost converter is designed such that it has performance comparable to similar industrial solutions operating at the same switching frequency [47]. The parameters of the both converters are given in Table I. It should be noted that the table confirms that the NSMB has three times smaller inductor volume and, as described in Section II-A, the total volume of the output capacitors, which is proportional to their energy storage capacity, in both cases is approximately the same.

The controller was built using an FPGA-based development board and the power stage is created using discrete components. In this discrete implementation, the switching components for the NSMB are not optimized and are the same as those of the conventional system.

Figs. 17–20 show the key current and voltage waveforms of the conventional and the NSMB boost converters for 220 $\rm V_{rms}$ and 90 $\rm V_{rms}$ line inputs. By comparing the switching node voltage swings, it can be seen that the NSMB has about three times smaller voltage swing $\Delta v_x = V_{\rm swing}$ for both operating conditions. To demonstrate the effect of the reduced swing on the inductor current ripple and confirm the analysis from Section II, only in this set of measurements, the NSMB has the same inductor value as the conventional boost (of approximately 670 μH), for other measurements, the NSMB operates with a three times smaller inductor.

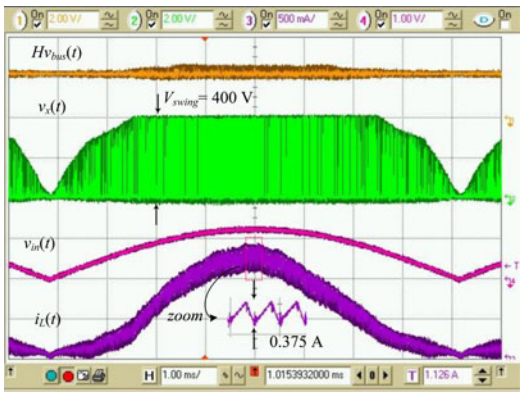


Fig. 19. Key waveforms of the conventional boost-based PFC rectifier; top to bottom: Ch.1 (top): attenuated output voltage, $Hv_{\rm bus}(t)$ (2 V/div); Ch.2 (upper middle): switching node voltage, $v_x(t)$ (200 V/div); Ch.3 (lower middle): input line current, $i_L(t)$ (0.5 A/div); Ch.4 (bottom): input line voltage, $v_{\rm in}(t)$ (200 V/div). Time scale is 1 ms/div. Operating conditions: $v_{\rm line} = 90\ {\rm V_{rms}}, V_{\rm bus} = 400\ {\rm V}, P_{\rm out} = 100\ {\rm W}, C = 100\ \mu{\rm F}, L = 680\ \mu{\rm H}$.

A comparison of the ripples (zoomed waveforms in Figs. 17 and 18) shows that the NSMB has about three times smaller ripple, allowing for the equal reduction of the inductor value. The waveforms of Fig. 18 also demonstrate stable operation of the NSMB. It can be seen that the controller seamlessly changes the NSMB mode of operation when the input voltage exceeds or drops below $V_{\rm bus}/3$ and $2V_{\rm bus}/3$ values, which for the experimental system are 133.3 and 266.6 V, respectively. Zoomed

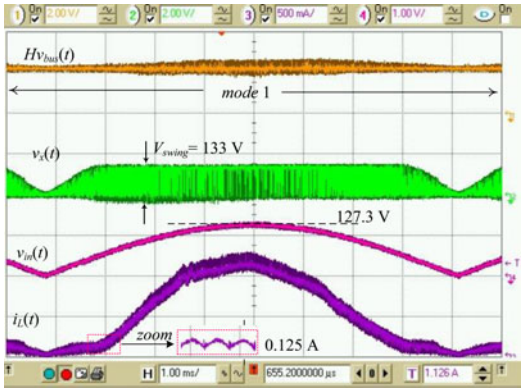
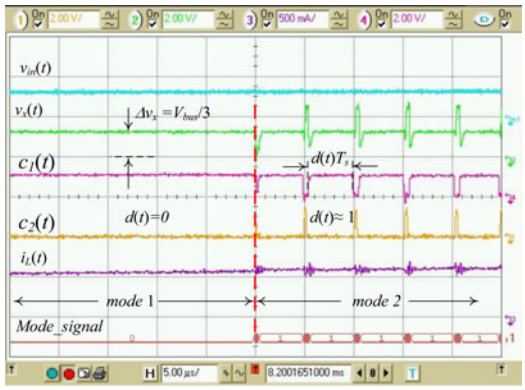


Fig. 20. Key waveforms of the conventional boost-based PFC rectifier; top to bottom: Ch. 1 (top): attenuated output voltage, $Hv_{\rm bus}(t)$ (2 V/div); Ch. 2 (upper middle): switching node voltage $v_x(t)$ (200 V/div); Ch. 3 (lower middle): input line current $i_L(t)$ (0.5 A/div); Ch. 4 (bottom): input line voltage $v_{\rm in}(t)$ (200 V/div). Timescale is 1 ms/div. Operating conditions: $v_{\rm line} = 90\ {\rm V_{rms}}, V_{\rm bus} = 400\ {\rm V}, P_{\rm out} = 100\ {\rm W}, C = 100\ \mu{\rm F}, L = 680\ \mu{\rm H}$.



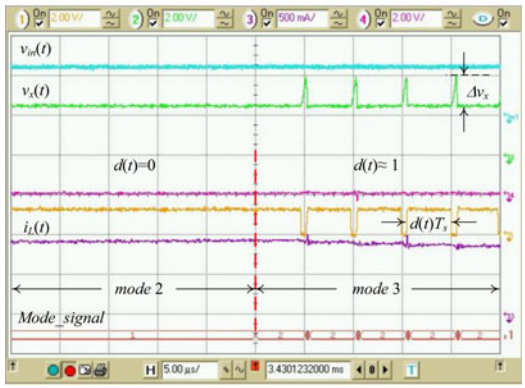


Fig. 21. Transitions from mode 1 to mode 2 (top) and from mode 2 to mode 3 (bottom); Ch.m1(top): input line voltage, $v_{\rm in}(t)$ (200 V/div); Ch. 2 (upper middle): switching node voltage, $v_x(t)$ (200V/div); Ch. 4 (middle): gating signal of $SW_1, c_1(t)$ (20 V/div); Ch. 1 (lower middle): gating signal of $SW_2, c_2(t)$ (20 V/div); Ch. 3 (bottom): input line current, $i_L(t)$, (0.5 A/div); digital input: mode control signal ($(0 =$ mode $1, 1 =$ mode $2, 2 =$ mode $3)$. Timescale is 5 μs/div. Operating conditions $v_{\rm line} = 220\ {\rm V_{rms}}, V_{\rm bus} = 400\ {\rm V}, P_{\rm out} = 100\ {\rm W}, C_{\rm top} = 150\ {\rm mF}, C_{\rm bottom} = 300\ {\rm mF}, L = 230\ {\rm mH}$.

in transition waveforms are also shown in Fig. 21. These waveforms demonstrate effectiveness of the applied mode transition method based on the PI compensator re-initialization, described in Section III. It can be seen that at the transition points, the duty ratio changes from the maximum value to zero (reducing the swing of inductor voltage to zero as well). By looking at the waveforms of the both converters a slight current waveform distortion can be noticed. The distortion occurs due to the quantization effects and the loss of the gain of the current measurement ADC at low inputs [51]. When the input becomes smaller than the quantization step of the used 6-bit ADC its gain, and consequently, the overall gain of the system reduces, causing distortion of the current waveform. For high-end applications, where a very low harmonic distortion is required, a higher resolution ADC can minimize this potential drawback.

Fig. 22 illustrates regulation of the output capacitor voltages with a downstream converter stage with a 70 W output load. The downstream stage operates at 200 kHz switching frequency. It can be seen that both capacitors maintain stable voltages and that during each cycle the charge taken from the bottom capacitor is twice as large as that taken from the top. As described in Section III-D, this results in equal voltage drops across both capacitors. It should be noted that, as it can be seen from Fig. 20, at low line inputs, the converter mostly operates in mode 1 (or modes 1 and 2), causing most of the power to be transferred through the bottom portion of the downstream stage of Fig. 14. To handle these conditions, the transistor and the winding on the bottom primary side of the converter need to be designed such that thy can provide the full load power. This drawback is completely compensated by the fact that the transistor of the downstream stage operates at a three times smaller voltage than that of the conventional downstream solutions [2], [52], [53], where most of the losses at the primary side of the converter are caused by high voltage stress of the transistors.

Power quality and total harmonic distortion (THD) for both converters are also experimentally compared, by extracting the current waveform data from the oscilloscope. In order to capture accurate information about the inductor currents, the harmonics are measured without an input filter regularly existing in the applications of interest.

In both cases, the power factor is measured to be about 0.98. The harmonic contents for both converters are shown in Fig. 23. It can be seen that the both converters have similar spectrums. The measurements also show that, similar to three-level solutions [7], [9], [12], the NSMB has slightly lower THD, i.e., 14.03% versus 15.48%. It should be noted that with the use of an input filter the THD values should be significantly smaller. The lower THD of the NSMB is mostly due to the lower energy of harmonics at the switching frequency and multiple regions of operation with close to zero inductor current ripple, as shown in Fig. 21.

Figs. 24 and 25 show efficiency comparison results for a conventional boost, a three-level boost, and NSMB converters operating with 85 $\rm V_{rms}$ and 265 $\rm V_{rms}$ input voltages, respectively. In this case, the boost PFC has power processing efficiency comparable to the commercial solutions operating at the same switching frequency [47]. The efficiency comparison experiments are conducted for all converters operating at the same 200 kHz effective switching frequency. It can be seen that, mainly due to the reduction of switching losses, the introduced NSMB-PFC has up to 6% better power processing efficiency

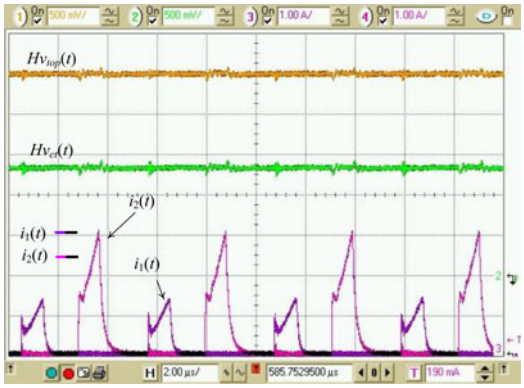


Fig. 22. Capacitor taps voltage regulation with the downstream stage currents; top to bottom: Ch.1 (top): top capacitor voltage, $v_{\rm upper}(t)$ (100 V/div); Ch.2 (upper middle): bottom capacitor voltage, $v_{\rm bottom}(t)$ (100 V/div); Ch.4 (lower middle): discharging current of bottom capacitor, $i_2(t)$ (1 A/div); Ch.3 (bottom): discharging current of top capacitor, $i_1(t)$, (1 A/div);. Time scale is 2 ms/div. Operating conditions $v_{\rm line} = 220\ {\rm V_{rms}}, V_{\rm bus} = 400\ {\rm V}, P_{\rm out} = 70\ {\rm W}, C_{\rm top} = 150\ {\rm mF}, C_{\rm bottom} = 300\ {\rm mF}, L = 230\ {\rm mH}$.

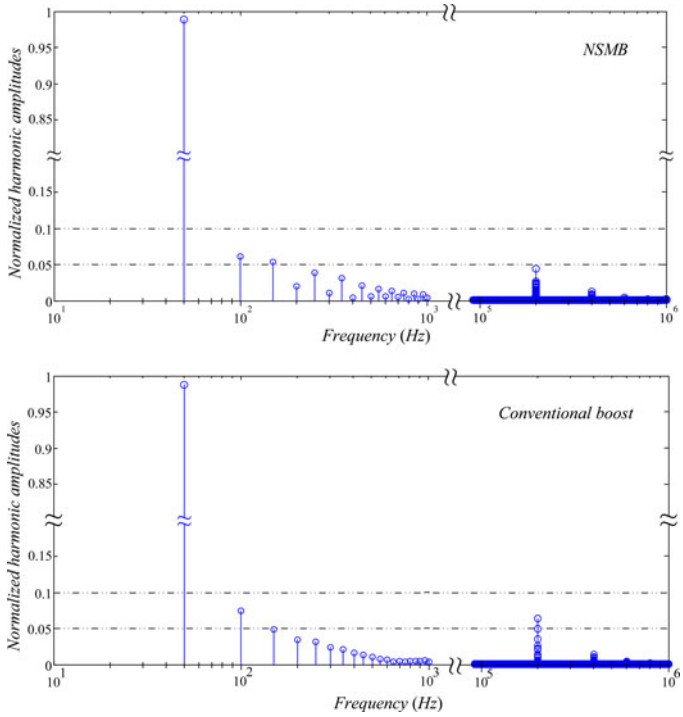


Fig. 23. Amplitudes of harmonics (multiples of 50 Hz) around line frequency and the switching frequency for the NSMB-based PFC prototype (top) and the conventional boost-based prototype (bottom).

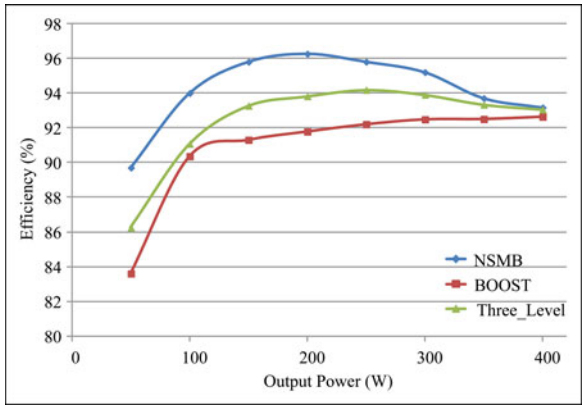


Fig. 24. Efficiency comparison of the conventional boost, three-level boost, and NSMB PFC converters for the line input of $265\ {\rm V_{rms}}$.

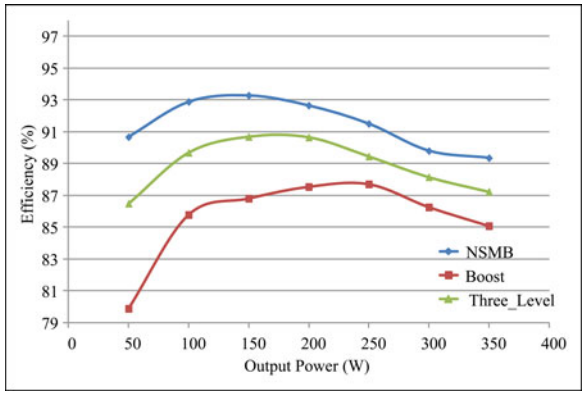


Fig. 25. Efficiency comparison of the conventional boost, three-level boost, and NSMB PFC converters for the line input of $85\ {\rm V_{rms}}$.

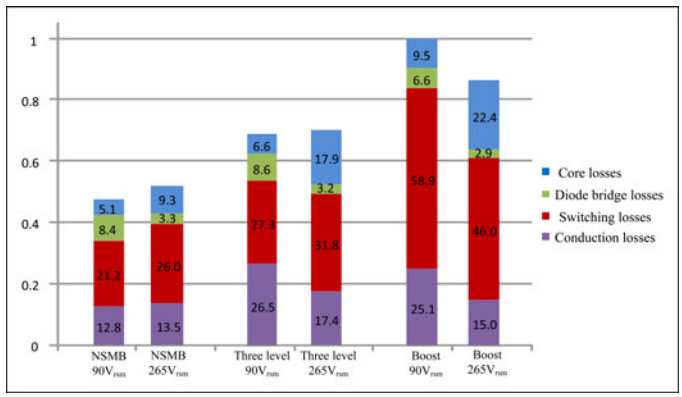


Fig. 26. Loss breakdown analysis for the conventional boost, three-level boost, and NSMB PFC converters for $85\ {\rm V_{rms}}$ and $265\ {\rm V_{rms}}$ input voltages at the light load operating condition (50 W). Length of each bar is normalized based on the losses of the boost at $90\ {\rm V_{rms}}$, which is 9.8 W.

than the boost converter and up to 4% than the three-level PFC. The efficiency improvements can be seen throughout the whole operating range, where, as expected, at light and medium loads, where the switching losses are dominant, the improvements are more noticeable.

It should be noted that in all prototypes the same switching components (Infineon IPB60R280C6CT Cool MOS switches [54] and STTH10LCD06 diodes from STMicroelectronics [55]. The maximum voltage rating of all components is 600 V. The same components are used due to a limited selection of switching components rated for the required blocking voltage of the NSMB topology. Therefore, the design has not been optimized for the NSMB topology. Still, the obtained efficiency results are comparable or better than those obtained in the state of the art solutions operating at the same switching frequency [26].

Figs. 26 and 27 compare the loss breakdown of the boost, the three-level, and the NSMB converters. The loss analysis results

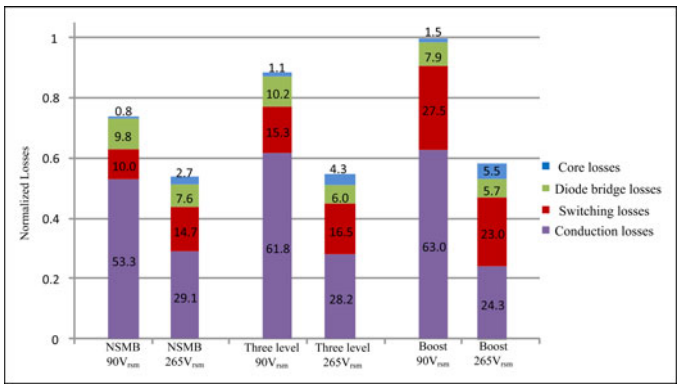


Fig. 27. Loss breakdown analysis for the conventional boost, three-level boost, and NSMB PFC converters for $85\ \mathrm{V_{rms}}$ and $265\ \mathrm{V_{rms}}$ input voltages at the light load operating condition (350 W for $85\ \mathrm{V_{rms}}$ and 400 W for $265\ \mathrm{V_{rms}}$). Length of each bar is normalized based on the losses of the boost at $90\ \mathrm{V_{rms}}$, which are 50.5 W.

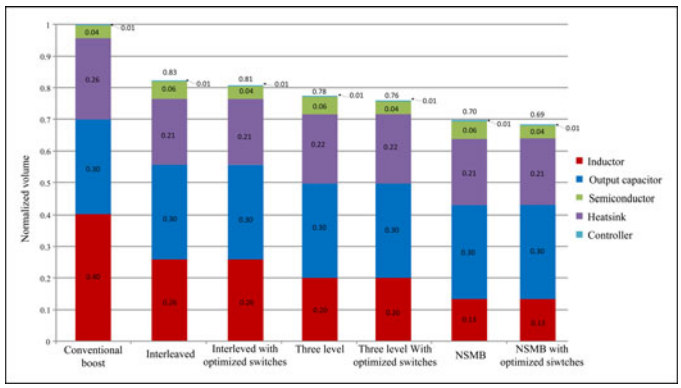


Fig. 28. Normalized volume distributions of conventional boost-based PFC and three other topologies; two-phase interleaved boost-based PFC, three-level PFC, and the NSMB-based solution. In case of the latter three cases, a volume break down in case of implementation with optimal switches, i.e., lower voltage/current rated switches in single package, is also shown.

are shown for operation with the input voltages of $265\ \mathrm{V_{rms}}$ and $85\ \mathrm{V_{rms}}$ for two cases for light (Fig. 26) and heavy (Fig. 27) loads of each converter. Each bar in these figures shows the normalized losses from different contributors to the overall losses of the corresponding converter and operating conditions. The normalization is preformed under assumption that the total losses of the conventional boost have a value of 1.

It is also worth mentioning that most efficiency optimization techniques and volume reduction methods developed for the conventional boost-based PFC topologies can be applied to the NSMB as well. Those include utilization of super junction and SiC devices [18], variable frequency control [19], separate light load control scheme [20], [21], and utilization of soft switching techniques [17]. For example, a soft-switched NSMB converter can be implemented employing the ZVT circuit presented in [6]. This means that, in the NSMB, the benefits of all of these complementary methods can be utilized while maintaining advantages of the smaller inductor and lower voltage stress over the conventional solutions.

In the targeted cost-sensitive applications (below 500 W), the use of a bridgeless topology is usually avoided [13], due to increased price and fairly limited relative improvements in the power processing efficiency. This can be demonstrated by looking at the loss breakdown shown in Figs. 26 and 27. It can be seen that the diode bridge losses of the NSMB converter are a very small portion of the overall losses at light loads (5.1%) and increase at heavy loads, to 9.8%. The heavy load results indicate that for, higher power applications which are beyond the scope of this work, the diode rectifier losses become more dominant and that the use of the bridgeless solution, shown in Fig. 16, is fully justifiable.

As mentioned earlier, in a potential implementation with custom-designed silicon components, even larger efficiency gains could be expected. This would mostly be due to the further reduction of switching losses, caused by increased transistor speed and reduced values of parasitic capacitances of the semiconductor components.

The diagrams of Fig. 28 compare the volume breakdown between different components and total normalized volumes of the conventional boost PFC, a two-phase interleaved boost-based PFC [26], a three-level PFC [6], and the introduced NSMB-based solution for typical 300–400 W applications [25], [26], [47]. The diagrams also show volume comparisons for potential optimized implementations of the interleaved boost and NSMB, where the silicon switches would be sized in accordance with their power ratings and implemented in a single package. As described in Appendix A, such an optimized implementation would require the same silicon area as the conventional boost. It should be noted that in these comparisons the input filter, whose volume significantly depends on the printed circuit board (PCB) layout is not taken into account. However, as indicated in the analysis of Section A-I3, the required volume of the NSMB input filter is smaller than that of the other analyzed solutions.

It can be seen that compared to the conventional boost, the NSMB has about 30% smaller total volume and is about 15% smaller than the interleaved boost, which, as shown in [25], has about 32% smaller inductor than the conventional boost. The volume comparison results confirm discussions of the favorable tradeoff from the previous sections. Since in the conventional boost a large portion of the volume is occupied by the inductor and the heat sink, about 65%, and less than a 5% by the semiconductors, a tradeoff between the inductor reduction and efficiency improvement on one side and an increase in the semiconductor part numbers on the other side is favorable. In this, the semiconductor components include the diode bridge, which in the conventional boost takes about 50% of the total silicon area, and the diode and the transistor, which take the other 50%. The results show that the three times reduction in the inductor volume and about a 12% in the heat sink volume, which is proportional to the heat dissipation reduction, are more than compensating for about 50% increase in the semiconductor switch volume and a 60% increase in the volume in the controller size. In this case, the size of the controller is estimated by looking at the volume of analog components and the number of logic gates required for its implementation for all three cases.

V. Conclusion

A rectifier with PFC based on a novel NSMB converter and a complementary digital controller are introduced. In comparison with the conventional boost-based solutions, the NSMB has three times smaller inductor as well as reduced switching losses. These advantages are achieved by reducing the inductor, i.e., switching node, voltage swing to 1/3 of the conventional boost level. At the same time, the voltage stress across the switching components is reduced to 1/3 for one diode–transistor pair and to 2/3 for the other pair.

The NSMB is a modified version of the three-level boost topology. Instead of having the same voltages across the output divider capacitors, this modification uses a nonsymmetric capacitor divider and the capacitor voltages are regulated at 1/3 and 2/3 of the full output voltage level. As a result, a four-level operation is achieved reducing the inductor by 33% without increasing the number of components required for implementation.

To control the capacitor voltages of the nonsymmetrical divider without using a bulky flying capacitor, an isolated downstream converter is used. In regular operation, the downstream stage takes nonequal amounts of charge from the capacitors keeping the capacitors voltage drops equal during discharging phases. The downstream converter stage has two inputs and, similar to the NSMB, can utilize principles of the reduced voltage swings to obtain smaller volume of magnetic components and reduced switching losses.

The mixed signal controller dynamically changes modes of the NSMB operation, depending on the instantaneous input voltage value. Seamless transitions between three operating modes are provided through the digital PI compensator re-initialization process, where, depending on the type of transition, the current and stored previous values of duty ratio are set to 0 or their maximum value. To eliminate the need for differential capacitor voltage measurements, a switching-state-dependent sampling and hold technique is applied.

Results obtained with an experimental prototype verify that the NSMB converter requires a three times smaller inductor and has significantly better power processing efficiency. The results also demonstrate stable controller operation and seamless mode transitions.

It is important to note that the presented principle of the use of a nonsymmetric voltage divider to create a four-level converter using three-level hardware could potentially also be used in three-level dc–ac converter applications to reduce the volume of the inductive components.

Appendix A
Analysis of Conduction Losses for Optimized Design of Switching Components

The following analysis and comparison of the conduction losses are based on the assumption that the semiconductor components of the both converters are sized in accordance with their voltage ratings.

A. Analytical Comparison of Conduction Losses

The conduction losses corresponding to the boost PFC converter can approximately be described with the following equation [23]:

$$P_{\mathrm{cond,boost}} = \int_0^{T_L} [R_{\mathrm{Lboost}} i_L^2(t) + R_{\mathrm{on}} i_L^2(t) D_{\mathrm{boost}}(t) + V_F i_L(t) D'_{\mathrm{boost}}(t)]dt \tag{A1}$$

where T_L is time duration of a half line cycle, $i_L(t)$ is the inductor current, R_{Lboost} is a resistance that models total inductor losses, R_{on} is the on resistance of the transistor, V_F is the diode forward voltage drop, and D_{boost} is the boost converter duty cycle.

For the NSMB converter, due to the change of conduction path based on the converter operating mode (as shown in Figs. 3–5), the losses are described with three different equations, corresponding to three distinctive modes of work

$$P_{\mathrm{cond,NSMB,1}} = \int_{T_1} [R_{\mathrm{LNSMB}} i_L^2(t) + (R_{\mathrm{on},1} + R_{\mathrm{on},2}) i_L^2(t) D_{\mathrm{NSMB},1}(t) + (R_{\mathrm{on},1} i_L^2(t) + V_{F2} i_L(t)) D'_{\mathrm{NSMB},1}(t)]dt \tag{A2}$$

$$P_{\mathrm{cond,NSMB,2}} = \int_{T_2} [R_{\mathrm{LNSMB}} i_L^2(t) + (R_{\mathrm{on},1} i_L^2(t) + V_{F2} i_L(t)) D_{\mathrm{NSMB},2}(t) + (R_{\mathrm{on},2} i_L^2(t) + V_{F1} i_L(t)) D'_{\mathrm{NSMB},2}(t)]dt \tag{A3}$$

$$P_{\mathrm{cond,NSMB,3}} = \int_{T_3} [R_{\mathrm{LNSMB}} i_L^2(t) + (R_{\mathrm{on},2} i_L^2(t) + V_{F1} i_L(t)) D_{\mathrm{NSMB},3}(t) + (V_{F1} i_L(t) + V_{F2} i_L(t)) D'_{\mathrm{NSMB},3}(t)]dt \tag{A4}$$

where T_i represents the time converter operates in mode i during a half of line cycle, R_{LNSMB} is equivalent resistance of the NSMB inductor modeling its core and copper losses, R_{on} is the on resistance of Q_i, V_{Fi} is forward voltage drop of the diode D_i, and $D_{\mathrm{NSMB},i}$ corresponds to the duty ratio of the NSMB converter during mode i.

The total conduction losses can be found as the sum of the previous three equations

$$P_{\mathrm{cond,NSMB}} = P_{\mathrm{cond,NSMB,1}} + P_{\mathrm{cond,NSMB,2}} + P_{\mathrm{cond,NSMB,3}}. \tag{A5}$$

By utilizing volt–second balance [23], the following relations between duty cycles of the boost and the NSMB can be found:

$$D_{\mathrm{NSMB},1}(t) = 3D_{\mathrm{boost}}(t) - 2 \tag{A6}$$

$$D_{\mathrm{NSMB},2}(t) = 3D_{\mathrm{boost}}(t) - 1 \tag{A7}$$

$$D_{\mathrm{NSMB},3}(t) = 3D_{\mathrm{boost}}(t). \tag{A8}$$

Assuming that area used for implementing the transistors of the NSMB is the same as that needed for the boost transistor and taking into account that the on resistance of a power a MOSFET per unit silicon area is given by [56]

$$R_{\mathrm{on\_}sp} = \alpha \cdot V_B^2 \tag{A9}$$

where α is a process-dependent constant and V_B is the breakdown voltage, the following relations between the on resistances of the MOSFET resistances can be found:

$$R_{\mathrm{on},1} = \frac{4}{9}R_{\mathrm{on}} \tag{A10}$$

$$R_{\mathrm{on},2} = \frac{1}{9}R_{\mathrm{on}} \tag{A11}$$

where R_{on} is the resistance of the boost transistor and $R_{\mathrm{on},1}$ and $R_{\mathrm{on},2}$ are the resistances of the NSMB. The equations are obtained by taking into account that the blocking voltages of Q_1 and Q_2 are a 66% and a 33% of that of the boost transistor, respectively.

By combining (A2)–(A8), (A10)–(A11), and assuming that the forward voltage drops of all the diodes are the same, the following relation between the conduction losses of the two topologies is obtained:

$$\begin{aligned} P_{\mathrm{cond,NSMB}} &= P_{\mathrm{cond,boost}} + \int_{T_1} 2V_F D'_{\mathrm{boost}}(t) i_L(t)dt \\ &+ \int_{T2} V_F D_{\mathrm{boost}}(t) i_L(t)dt + \int_{T3} \left[V_F - 2V_F D_{\mathrm{boost}}(t)\right] i_L(t)dt \\ &- \int_{T_1} \left(\frac{2}{3}D_{\mathrm{boost}}(t) - \frac{2}{9}\right) R_{\mathrm{on}} i_L^2(t)dt - \int_{T2} \frac{2}{9}R_{\mathrm{on}} i_L^2(t)dt \\ &- \int_{T3} \frac{2}{3}D_{\mathrm{boost}}(t) R_{\mathrm{on}} i_L^2(t)dt - \int_0^{T_L} \left(R_{\mathrm{Lboost}} - R_{\mathrm{LNSMB}}\right) i_L^2(t)\mathrm{d}t. \end{aligned} \tag{A12}$$

The results show that the diodes losses of the NSMB are slightly higher. The value of the diode losses depends on the input voltage level, i.e., on the portions of time the NSMB spent in each mode of operation. However, these extra losses can be partially or completely compensated by the smaller transistor conduction losses and also smaller inductance of the NSMB resulting in lower copper and conduction losses.

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