Low Power Very High Frequency Switch-Mode Power Supply With 50 V Input and 5 V Output

Mickey Madsen, *Student Member, IEEE*, Arnold Knott, *Member, IEEE*, and Michael A. E. Andersen, *Member, IEEE*

***Abstract*—This paper presents the design of a resonant converter with a switching frequency in the very high frequency range (30–300 MHz), a large step down ratio (ten times), and low output power (1 W). Several different inverters and rectifiers are analyzed and compared. The class E inverter and rectifier are selected based on complexity and efficiency estimates. Three different power stages are implemented; one with a large input inductor, one with a switch with small capacitances, and one with a switch with low on-resistance. The power stages are designed with the same specifications and efficiencies from 60.7–82.9% are achieved.**

***Index Terms*—DC-DC power conversion, inverters, rectifiers, resonant power conversion, switched mode power supplies, VHF circuits.**

I. Introduction

When designing power converters it is always a goal to reduce the price and the physical size, i.e. increase the power density. The development of switch mode power supplies (SMPS) has made it possible to increase the power density significantly, but it is limited by the size of the passive energy storing components (inductors and capacitors). The value and size of these are however dependent on the switching frequency. By increasing the switching frequency it will hence be possible to reduce the size of SMPSs further.

Traditional SMPS topologies like Buck and Boost are hard switching, this means the MOSFET is switching while energy is stored in the output capacitance. The result is that energy is dissipated in the MOSFET every time it turns on. Although this introduces losses in the converter, it is not critical for converters switching at 50–400 kHz. But when the frequency is increased to the very high frequency (VHF) range (30–300 MHz) the dissipated power get almost 1000 times larger. This amount of energy would ruin the efficiency and require extreme cooling of the MOSFET. This leads to the development of resonant converters.

In order to avoid switching losses and be able to increase the frequency while keeping the efficiency high, new topologies have to be used. For the last two decades (since 1988 [1]), research has been done in order to enable the use of resonant RF amplifiers (inverters) combined with a rectifier for dc/dc converters, see Fig. 1. With these type of converters, it is possible to achieve zero voltage switching (ZVS) and/or zero current switching (ZCS). In this case, the MOSFET turns ON when the voltage and/or current across/through it is zero. Theoretically, this should eliminate switching losses if the switching is done instantaneously and at exactly the right time. This is not practically achievable, but even with slight deviations from the ideal case very high efficiencies can be achieved.

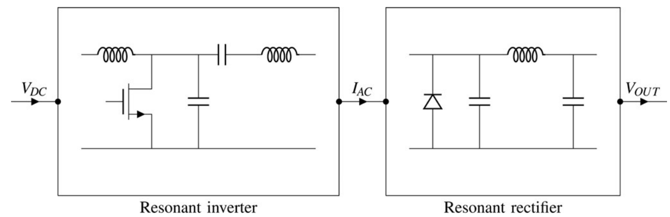

Fig. 1. Block diagram of the converter.

As already mentioned the value of the passive components depends on the switching frequency. Hence, an increase in frequency will lead to a reduction in size, as long as the size of the passive scales with the value. This assumption generally holds, but magnetic materials and packaging introduce some challenges. When the frequency is pushed far into the meghertz range, magnetic core losses increase rapidly and become unacceptably high for most core materials [2]. At this point, air core and PCB embedded inductors become a viable solutions, as the inductances needed at these frequencies can be made in a small physical size and the core losses avoided [3], [4].

Increasing the switching frequency also leads to capacitors with lower values. Electrolytic capacitors which often limit the overall lifetime [5], [6] can hence be avoided. The reduction in component values also leads to a cost reduction as smaller components are generally cheaper. If the frequency is increased enough, some of the components can even be left out as they can be constituted by the parasitic parts of other components (this will be explained further in Sections II and III). An increase in switching frequency will also make it easier to comply with EMI requirements, as switching harmonics can easily be filtered out by small and cheap filters.

With a switching frequency in the VHF range, it will also be possible to achieve very fast transient responses [7] which are highly demanded, e.g., for envelope tracking [8]. However, in order to fully benefit from this, an efficient and fast control loop has to be implemented. This is a big challenge and while some ways of achieving continuous regulation have been found [9], [10], the best results are still achieved using burst mode (or cell modulation) as in [11]–[13]. Due to the high switching

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The authors are with the Department of Electrical Engineering, Technical University of Denmark, 2800 Kongens Lyngby, Denmark (e-mail: mpma@elektro.dtu.dk; akn@elektro.dtu.dk; ma@elektro.dtu.dk).

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TABLE I
RESULTS FROM PREVIOUS RESEARCH

Inverters

Topology	f_s [MHz]	V_{IN} [V]	V_{OUT} [V]	P_{OUT} [W]	η [%]	Year
Class DE	5.3	330	N/A	1154	89	1999 [17]
Class E	1	128	N/A	366	96.6	2006 [18]
Class ϕ_2	1	129	N/A	526	97.1	2006 [18]
Class ϕ_2	30	160	N/A	330	93.7	2007 [19]
Class E	1	129	N/A	322.7	97	2007 [20]
Class E	100	9	N/A	6.8	82	2011 [21]

Converters

Topology	f_s [MHz]	V_{IN} [V]	V_{OUT} [V]	P_{OUT} [W]	η [%]	Year
Class E	1	20	25	8.9	89	1989 [22]
Class ϕ_2	30	165	33	265	87	2006 [11]
Class E	100	11	12	10	75	2006 [23]
Class ϕ_2	30	150	33	180	84	2008 [14]
Class ϕ_2	10	170	75	250	91	2009 [15]
Class ϕ_2	30	165	33	225	87	2009 [15]
Class ϕ_2	30	330	50	900	79	2009 [16]
Class E	100	12	23.7	1.7	55	2010 [24]
Push-Pull ϕ_2	30	140	65.4	471.9	83.4	2010 [25]

frequency the converter will reach steady state after just a few microseconds, this makes it possible to use an array of small converters and switch them on and off as needed. In this way, each converter is designed to operate with a defined load/output. This makes the design much easier as resonant inverters are generally very load dependent.

The fact that resonant inverters are load dependent, makes it very hard to achieve good performance at varying loads. Furthermore, resonant inverters need a large load impedance to operate in the ideal situation (having both ZVS and ZCS). This makes them well suited for boost-type converters, but making a buck type is a bit more challenging. The most commonly used way to overcome this challenge is to add an autotransformer at the output, in that way the load impedance seen by the inverter is increased [11], [14], [15]. Another way to achieve low output voltage is to use an array of converters with the input in series and the output in parallel in [16].

The most commonly used inverter is the class E, however several other topologies exist. Some of the research results are summed up in Table I. From the table it is seen that very high efficiencies are achievable for the inverters up to 97%. However, the efficiency drops around 10% for the complete dc/dc converters, i.e., when a rectifier is added.

From Table I, it is also seen that the converters have limited gains, with a step down of 6.6 times and a step up of 2 being the largest. As already stated the large reductions are not produced solely by the converter, but with different ways to make the load impedance appear larger. By further inspection, the connection given by (1) can be seen, this relation is shown in Fig. 2

$$\frac{V_{\rm IN}^2 \cdot f_S}{P_{\rm OUT}} \propto \frac{1}{\eta}. \quad (1)$$

Equation (1) shows that it is problematic to have a high input voltage and switching frequency while having a low output power and still keeping the efficiency high. The input voltage sets (together with $C_{\rm OSS}$) the energy stored in the output capacitance of the MOSFET each switching period and f_S sets how many times this has to be done each second. Combined these values are hence proportional to the circulating energy, that needs to run in the converter in order to ensure ZVS. The relation given in (1) hence states that it is difficult to achieve high efficiency, if the circulating energy that is needed for ZVS is high compared to the output power. The reason for this and the factor $V_{\rm IN}^2 \cdot f_S/P_{\rm OUT}$ will be described further in Section III.

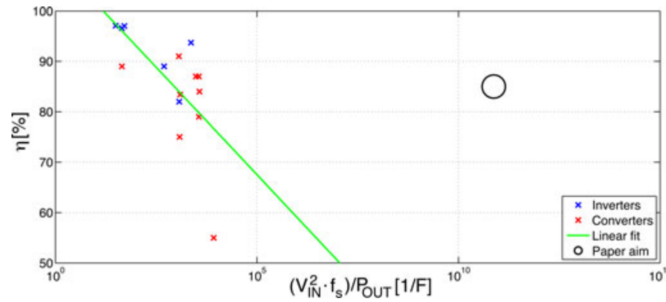

Fig. 2. Relation between $\frac{V_{\rm IN}^2 \cdot f_S}{P_{\rm OUT}}$ and η for the converters in Table I.

TABLE II
DESIGN SPECIFICATION FOR THE CONVERTER

f_S	V_{IN}	V_{OUT}	P_{OUT}	R_L
30-300 MHz	50 V	5 V	1 W	25 Ω

This paper will cover the design of a VHF power converter with a low voltage and power output. This will require a large reduction in voltage and a combination of output power, input voltage, and switching frequency unlike any of the previous results. This will put the converter in the area marked in Fig. 2. As it is seen this is very far from the results achieved by previous researchers (the specifications for the converter is given in Table II).

As the load is given, the first step should be to design the rectifier and then design the inverter for the given input and load. It is also possible to design the inverter to a given load and then use different resistance compression networks to make the impedance of the rectifier match [26]–[28]. Though this is a solution often used, it will increase the complexity of the converter unnecessarily and possibly reduce the achievable efficiency, size, and price.

Section II covers the selection and design of a resonant rectifier for the given load and output power level. Then, a resonant inverter is designed for the input voltage and load impedance in Section III. Experimental results from three different power stages are shown in Section IV. Finally Section V summarizes and concludes the paper.

II. RESONANT RECTIFIERS

The purpose of the rectifier is to convert the ac current from the inverter to a dc output. Just as the MOSFET has an output capacitance, the diode has a junction capacitance. In order not to dissipate this energy in the diode, it is important that the transition is made smoothly, so the capacitance is discharged before the diode turns on.

As stated in Section I, it is difficult to achieve high efficiency if the input voltage and switching frequency are high and the output power low. The switching frequency is therefore set to 30 MHz for the initial design. If good results are achieved with this frequency, it might be increased further in order to minimize the size of the converter.

Though there are several ways to do this, only two will be considered here. The most commonly used class E rectifier and the equivalent to the class DE inverter, the class DE rectifier.

A. Class E

The class E rectifier is a rather simple circuit, consisting of a diode, two capacitors, and an inductor as shown in Fig. 3. Together these components constitutes a resonant rectifier capable of rectifying the ac input current to a dc output.

For now, it will be assumed that the output capacitance is infinite, so the output voltage is constant, and the diode is assumed to be ideal, i.e., no forward voltage drop, no junction capacitance, and no reverse current.

In this case, the rectifier will appear resistive at the switching frequency, if the resonance frequency of L_R and C_R are set to this frequency. This will simplify the design of the inverter as most design formulas are for a resistive load.

The scaling of the two components will determine the duty cycle of the diode, D_D. As the forward voltage drop of a diode increases with the current running through it, it is desirable to keep D_D as high as possible. However, as the diode is connected to the output through an inductor, the average voltage across it has to be V_{OUT}. Hence, a high D_D will lead to a high peak voltage across the diode.

In order to select D_D, and thereby the scaling of the resonant components, the values of real components have to be considered. All the considered inverters have a capacitor at the output ensuring a pure ac path, without this there would be a direct dc path from input to output and it would be impossible to reduce the voltage. The average current through the diode will therefore be the same as the output current.

With the forward voltage drop of a standard Schottky diode being around 0.5 V (10% of the output voltage), it is crucial to use a diode with low forward voltage drop. Fairchilds MBR0520L has one of the lowest forward voltages available, max 385 mV, and can handle a reverse voltage of 20 V. With this diode, the diode loss will be up to 77 mW or 7.7% of the output power. This clearly limits the maximum achievable efficiency and fits very well with the $\approx 10\%$ efficiency drop, seen in Section I when going from an inverter to a complete converter.

If $D_D = 50\%$ is chosen, the peak diode voltage will be $3.6 \cdot \mathrm{V_{OUT}} = 17.8$ V leaving a little margin up to the maximum [29]. With this D_D the value of C_R should be [29]

$$C_R = \frac{1}{2 \cdot \pi^2 \cdot f_S \cdot R_L} = 67.5 \text{ pF}. \quad (2)$$

With this capacitance, the value of L_R can be calculated according to [29]

$$L_R = \frac{1}{(2 \cdot \pi \cdot f_S)^2 \cdot C_R} = 417 \text{ nH}. \quad (3)$$

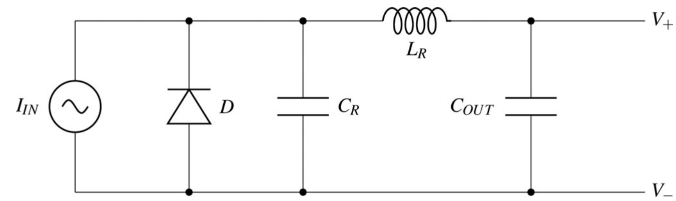

Fig. 3. Schematic of the class E rectifier.

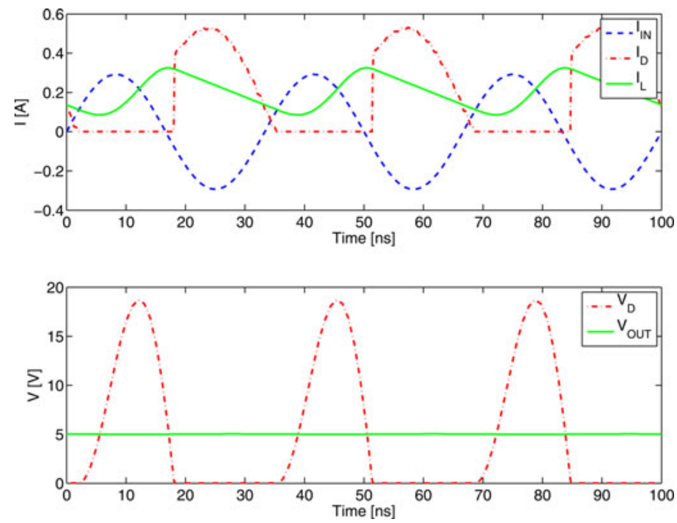

Fig. 4. Class E rectifier waveforms simulated with PLECS.

The inductor has, as expected, a dc current of 0.2 A (the output current with 1 W and 5 V) and on top of that an ac current with an amplitude of 120 mA (see Fig. 4). The dc resistance of the inductor is estimated to 25 mΩ and the ac resistance to 330 mΩ (these values are based on an air core inductor with a diameter of 6 mm and 8 turns of 0.4 mm wire). The loss caused by the inductor can then be calculated to 1 mW due to dc losses and 2.4 mW due to ac losses.

This is 0.34% of the output power and these resistances are based on a relatively large air core inductor. The equivalent series resistance (ESR) of a ceramic capacitor in the sizes used here will be less than 200 mΩ [30] and the currents running through them are smaller than the current in the inductor. The loss caused by them will thus not be significant. Furthermore, the parasitic capacitance of the diode can account for C_R. Actually, the parasitic capacitance of the chosen diode is, according to the datasheet, 65 pF at 5 V reverse voltage fitting almost perfectly with the calculated value.

B. Class DE

The class DE rectifier has an extra diode compared to the class E, but it does not have any inductors and the physical size and prize are expected to be more or less the same. As seen in the schematic in Fig. 5, the output capacitance is split in two. For now, they will both be assumed to be infinite making the output voltage pure DC. As the diodes are connected directly to the output, the total voltage across them will always be V_{OUT}. The diode duty cycle can therefore be chosen freely between 0 and

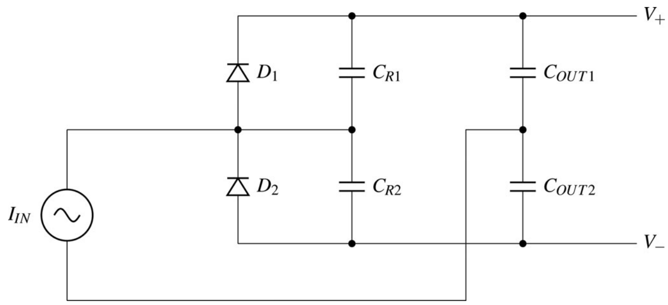

Fig. 5. Schematic of the class DE rectifier.

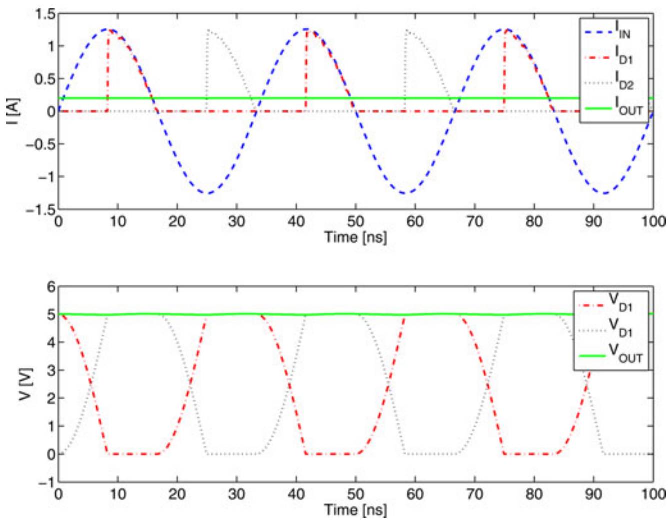

Fig. 6. Class DE rectifier waveforms simulated with PLECS.

0.5, a higher duty cycle would require both diodes to conduct at the same time.

From [31], (4)–(6) can be found. If $I_{\mathrm{IN,peak}}$ is isolated in (4) and ϕ is isolated in (6), the results can be substituted into (5). C_R can then be isolated in order to find the capacitances needed to get a desired diode duty cycle, (7). If a diode duty cycle of 25% is chosen, the needed capacitance can be calculated to 667 pF

$$V_{\mathrm{OUT}} = \frac{I_{\mathrm{IN,peak}} \cdot R_L}{\pi + \omega \cdot C_R \cdot R_L} \tag{4}$$

$$\cos(\phi) = 1 - \frac{2 \cdot \omega \cdot C_R \cdot V_{\mathrm{OUT}}}{I_{\mathrm{IN,peak}}} \tag{5}$$

$$D_D = \frac{\pi - \phi}{2 \cdot \pi} \tag{6}$$

$$C_R = \frac{\pi \cdot (1 - \cos(\pi - 2 \cdot D_D \cdot \pi))}{\omega \cdot R_L \cdot (1 + \cos(\pi - 2 \cdot D_D \cdot \pi))}. \tag{7}$$

As mentioned the diodes are coupled directly to the output, furthermore they provide the only dc path for the output current. The average current through each of the diodes will therefore be I_{OUT} (see Fig. 6), resulting in twice the diode loss as for the class E rectifier. This results in a total loss of more than 150 mW. Though several diodes could be put in parallel in order to reduce the forward voltage drop a bit, the diode losses will still be well above 100 mW, i.e., 10% of the output power.

TABLE III
PROS AND CONS OF THE INVESTIGATED RECTIFIER TOPOLOGIES

	Class E	Class DE
Pros	• Low complexity • Well documented and tested	• No inductors
Cons	• High semiconductor stress	• High loss • 2 semiconductors

C. Selection of Rectifier

Based on the analysis of the two rectifiers, the class E rectifier is found to be the best choice. The size and prize of the two rectifiers will be similar, but the loss of the class DE will be significantly higher than for the class E. Some of the pros and cons are shown in Table III.

For a high voltage output the DE might be better though, as the voltage across the diodes is lower and smaller diodes might be used. But for the low output needed for this converter, a class E rectifier is found to be the best choice.

The losses of the class E rectifier might even be unacceptable. A way to reduce the losses could be to use a synchronous rectifier, this will eliminate the forward voltage loss. This will however require an additional MOSFET, with the following need for gate drive and control.

III. Resonant Inverters

As mentioned in Section I, a resonant inverter is used in order to eliminate switching losses. Either ZVS or ZCS can be achieved and in some special cases both. Generally, ZVS will eliminate losses due to parasitic capacitances and ZCS will eliminate losses due to parasitic inductance. For MOSFETs and diodes in power applications the capacitances causes the dominating loss, ZVS will therefore be the main criteria.

However in some cases it is, as mentioned, possible to achieve both ZVS and ZCS switchings (also called ZVS and zero derivative switching, ZDS). If this can be achieved the exact timing of the switching is less important, as the voltage across the MOSFET will be zero for a small amount of time.

If only ZVS can be achieved, the MOSFET needs to turn ON at exactly the point where the voltage across it hits zero. If it switches just a little too early, there will be energy stored in the capacitor causing switching losses. If it switches a little too late, the drain source voltage will go below zero and the body diode will start to conduct which also gives losses.

A. Class E

The most commonly used resonant inverter is the class E, a schematic of it is shown in Fig. 7. It consists of a single MOSFET, two inductors, and two capacitors. In optimum operation L_{IN} is an infinite choke providing a pure dc input current. The resonant circuit (L_R and C_R) is inductive at the switching frequency and the inverter is designed to have both ZVS and ZDS.

As already mentioned ZVS and ZDS switching can only be achieved in very specific situations. According to [32], [33] this

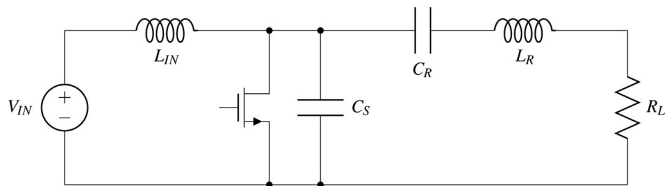

Fig. 7. Schematic of the class E inverter.

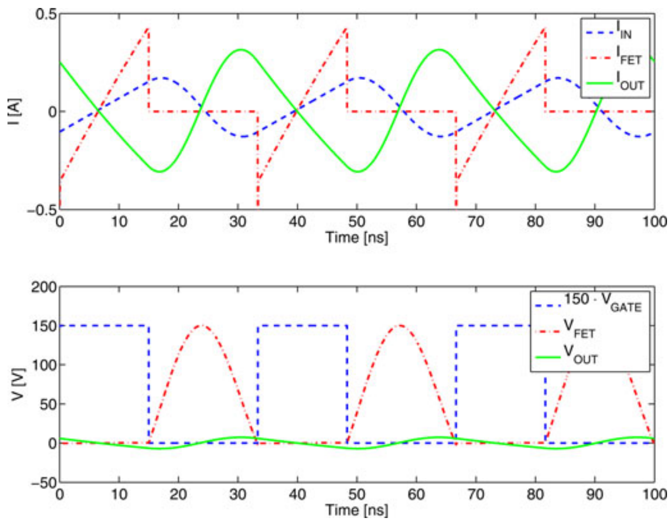

Fig. 8. Class E inverter waveforms with realistic $C_{\rm OSS}$ simulated with PLECS.

can only be achieved if

$$R_L = \frac{8}{\pi^2 + 4} \cdot \frac{V_{\rm IN}^2}{P_{\rm OUT}} \tag{8}$$

$$f_{S,\max} = \frac{P_{\rm OUT}}{2 \cdot \pi \cdot C_S \cdot V_{\rm IN}^2}. \tag{9}$$

With 50 V input, 1 W output, and a switching frequency of 30 MHz, this would require a load impedance of 1.44 kΩ and an output capacitance of 2.1 pF. From (9), it is seen that there is a special combination of f_S, $V_{\rm IN}$, and $P_{\rm OUT}$ which makes it possible to operate in the optimum situation. Similar equations can be found for other topologies [32] and this is the reason for the dependence seen in Fig. 2.

A MOSFET with an output capacitance of 2.1 pF for this voltage level and switching frequency is not available, they have minimum 10 times that. Furthermore, the impedance is very far from the input impedance of the rectifier. It will therefore not be possible to achieve both ZVS and ZDS switchings. However, it is still possible to achieve ZVS and thereby high efficiency as long as the transitions of the MOSFET are controlled well. In this case, the components have to be selected carefully in order to ensure ZVS and the inverter will be running in a subnominal condition as described further in [34].

If the drain source voltage of the MOSFET is assumed to be a half sine wave when it is off and zero when it is on, the peak voltage across the MOSFET will be

$$V_{\rm IN} = \int V_{\rm DS} = V_{\rm DS,peak} \frac{2 \cdot (1 - D)}{\pi} \tag{10}$$

$$\Updownarrow$$

$$V_{\rm DS,peak} = V_{\rm IN} \frac{\pi}{2 \cdot (1 - D)}. \tag{11}$$

The rms value of a half wave rectified sine wave is

$$V_{\rm DS,rms} = V_{\rm DS,peak} \sqrt{\frac{D}{2}} \tag{12}$$

and the rms value of the output voltage is

$$V_{\rm OUT,rms} = \sqrt{P_{\rm OUT} \cdot R_L}. \tag{13}$$

According to [11], the reactance of the resonance circuit can now be determined by

$$X_{\rm RC} = R_L \cdot \sqrt{\left(\frac{V_{\rm DS,rms}}{V_{\rm OUT,rms}}\right)^2 - 1}. \tag{14}$$

By combining (11)–(14), an expression for the needed reactance as function of input voltage, duty cycle, output power, and load is obtained

$$X_{\rm RC} = R_L \cdot \sqrt{\frac{V_{\rm IN}^2 \cdot \pi^2 \cdot D}{2 \cdot (2 \cdot D - 2)^2 \cdot P_{\rm OUT} \cdot R_L} - 1}. \tag{15}$$

It is desirable to keep the duty cycle low in order to reduce the peak voltage across the MOSFET. However, due to turn on and off times and delays, it is decided to keep it close to 50%. From (11), it is found that a duty cycle of 45% will give a peak voltage of 142.8 V, leaving a little headroom if a 150 V MOSFET is used. Using this value along with the previous results, the needed reactance is found to be 326 Ω. If a capacitor of 680 pF is used, the value of the inductor can be calculated according to

$$L_R = \frac{C_R \cdot X_{\rm RC} \cdot \omega_S + 1}{C_R \cdot \omega_S^2} = 1.77\ \mu\text{H}. \tag{16}$$

The next step is to determine the values of $L_{\rm IN}$ and C_S. In order to minimize losses, it is preferable to keep $L_{\rm IN}$ large, thus large ac currents running in and out of the converter and thereby causing unnecessary losses are avoided. If the input choke is assumed infinite, the next step is to calculate the value of C_S. In order to ensure ZVS, the voltage across C_S needs to rise to the peak and fall back down to zero within the period where the switch is open. This requires C_S and the resonance circuit to resonate at a frequency with a period equal to two times the period where the switch is open, i.e.,

$$T_R = 2 \cdot (1 - D) \cdot T_S \Leftrightarrow f_R = \frac{f_S}{2 \cdot (1 - D)}. \tag{17}$$

If the reactance of C_S is the same as the reactance of the resonant tank (with opposite operational sign) at f_R the circuit will resonate at this frequency. However, as the capacitor is only used when the MOSFET is off, it has to be scaled by $1-D$

$$C_S = \frac{1 - D}{2 \cdot \pi \cdot f_R \cdot X_{\rm RC}}. \tag{18}$$

With the specifications for this converter it would require a MOSFET with an output capacitance of maximum 10.9 pF. At the moment the MOSFETs with lowest output capacitances,

TABLE IV
CURRENTS (RMS) IN THE CLASS E INVERTER

IN	MOSFET	OUT
102 mA	165 mA	208 mA

C_{OSS}, which are able to handle 150 V, have an output capacitance of ≈20 pF at 50 V. It is therefore necessary to reduce the input inductor, in order to increase C_S while keeping the resonance frequency at the switch node equal to f_R. The output capacitance of the MOSFET is only contributing to the resonance in the part of the period where the MOSFET is OFF, hence it has to be scaled by $1-D$ in order to find the effective capacitance. The effective capacitance of the output capacitor is $C_{S,\mathrm{eff}} = \frac{C_S}{1-D} = 36.4$ pF, hence the total inductance of the resonance circuit and the input inductor should be

$$L_{\mathrm{total}} = \frac{1}{\omega_R^2 \cdot C_{S,\mathrm{eff}}} = 936 \text{ nH}. \tag{19}$$

Knowing the values of X_{RC}, the input inductance can be calculated according to

$$L_{\mathrm{total}} = \frac{1}{\frac{1}{L_{\mathrm{IN}}} + \frac{\omega_R}{X_{\mathrm{RC}}}} \Leftrightarrow L_{\mathrm{IN}} = \frac{1}{\frac{1}{L_{\mathrm{total}}} - \frac{\omega_R}{X_{\mathrm{RC}}}} = 2.91\mu\text{H}. \tag{20}$$

From a simulation, the rms current through the inductors and the MOSFET is found (see Fig. 8 and Table IV). The IRF5802 MOSFET has the lowest available output capacitance for a 150 V power MOSFET capable of switching in the VHF range. It has 20 pF output capacitance at 50 V and an on-resistance of 1.2 Ω, this will give a conduction loss in the MOSFET of up to 33 mW. The ac resistance of the inductors is estimated to be 100 mΩ, thus they will have a combined loss of 5.37 mW. As for the rectifiers, the losses in the capacitors are assumed to be negligible. Thus, the total loss in the class E inverter is estimated to ≈38 mW.

B. Class ϕ_2

As written in Section I, the large voltage peak across the MOSFET is a big problem when the input voltage is large. The class ϕ_2 (or EF_2) inverter, which is a hybrid between the class E and F_2 inverters, was developed in order to make the voltage across the MOSFET closer to a square wave. The voltage across the MOSFET should thereby become significantly smaller (ideally $2 \cdot V_{\mathrm{IN}}$ for $D = 50\%$). This is done by inserting a *LC* circuit in parallel with the MOSFET as shown in Fig. 9. This circuit is designed to have a resonance frequency at the second harmonic, which causes the voltage across the MOSFET to become a trapezoidal wave consisting of the first and third harmonics. The same benefits can be achieved with the flat-top class-E amplifier described in [35].

According to [14], the rms voltage across the MOSFET can be estimated by $V_{\mathrm{DS,rms}} = V_{\mathrm{IN}} \frac{4}{\pi \cdot \sqrt{2}}$; thus, the needed reactance of the resonant circuit is different (see (14)). The new values can be calculated to $L_R = 1.2$ μH and $C_R = 522$ pF. No exact equations for the calculations of the added *LC* circuit or the input inductance are given in the literature; however, the following

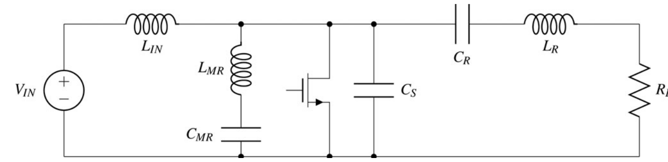

Fig. 9. Schematic of the class ϕ_2 inverter.

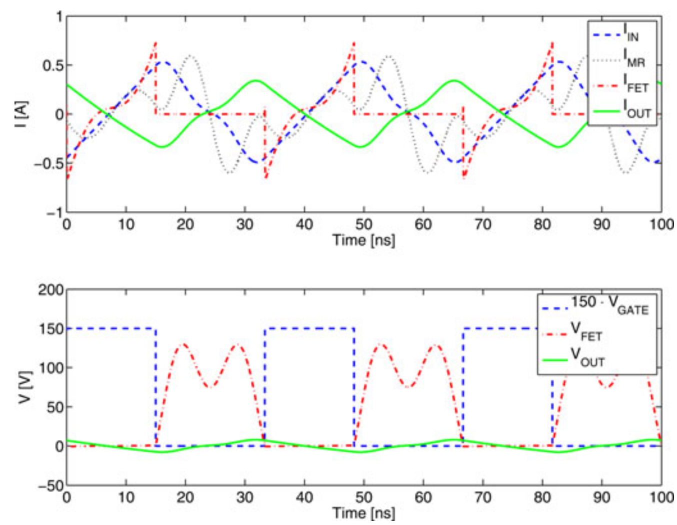

Fig. 10. Tuned class ϕ_2 inverter waveforms simulated with PLECS (the peak drain source voltage is reduced to 132 V).

TABLE V
CURRENTS (RMS) IN THE CLASS ϕ_2 INVERTER

IN	MR	MOSFET	OUT
311 mA	301 mA	207 mA	208 mA

gives results which are close [19]:

$$L_{\mathrm{IN}} = \frac{1}{9 \cdot \pi^2 \cdot f_S^2 \cdot C_S} = 625 \text{ nH} \tag{21}$$

$$L_{\mathrm{MR}} = \frac{1}{15 \cdot \pi^2 \cdot f_S^2 \cdot C_S} = 375 \text{ nH} \tag{22}$$

$$C_{\mathrm{MR}} = \frac{15}{16} \cdot C_S = 18.8 \text{ pF}. \tag{23}$$

A PLECS simulation was used to tune the component to get exact ZVS (see Fig. 10), the final values are shown in Table VII. As for the class E inverter, the rms current through the inductors and the MOSFET was extracted, see Table V.

With the MOSFET used for the class E the conduction loss will be up to 51.4 mW. The current through L_R will be the same as for the class E and though the inductance is a bit lower, the ESR will still be estimated to 100 mΩ giving a loss of 4.3 mW. The input inductor and L_{MR} are noticeably smaller and their ESR will therefore be estimated to 50 mΩ and 25 mΩ, respectively. With these resistances and the listed rms currents, their loss will be 4.8 and 2.3 mW, respectively. The total loss of the class ϕ_2 inverter (again ignoring losses in the capacitors) is estimated to be 62.8 mW.

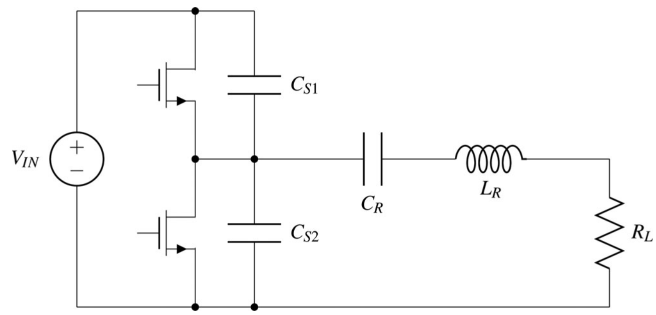

Fig. 11. Schematic of the class DE inverter.

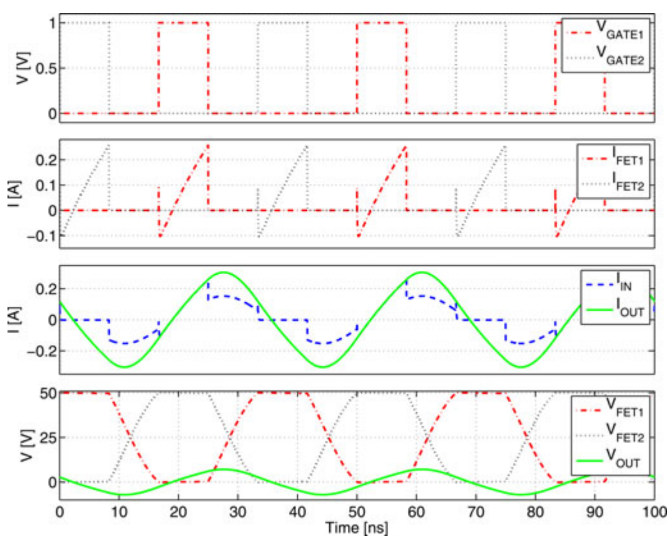

Fig. 12. Class DE inverter waveforms simulated with PLECS.

TABLE VI
CURRENTS (RMS) IN THE CLASS DE INVERTER

FET1	FET2	OUT
67.8 mA	67.8 mA	208 mA

C. Class DE

The class DE inverter has the same ZVS properties as the class E inverter and the low voltage stresses of the class D inverter. It is the counterpart of the class DE rectifier considered in Section II and, as seen in Fig. 11, the two circuits are very alike. As the DE rectifier, the DE inverter has two switches connected directly to the dc voltage, in this case MOSFETs connected to the input voltage. Both MOSFETs have capacitors across them which can be tuned to achieve ZVS. The only additional components are a resonant circuit at the output, just as seen for the previous inverters.

As for the class E inverter, ZVS and ZDS switching can be achieved in very specific situations. However, the values needed are different [32]

$$R_L = \frac{V_{\mathrm{IN}}^2}{2 \cdot \pi^2 \cdot P_{\mathrm{OUT}}} \quad (24)$$

$$f_{S,\max} = \frac{P_{\mathrm{OUT}}}{2 \cdot C_S \cdot V_{\mathrm{IN}}^2}. \quad (25)$$

With these equations, the demands for load impedance and output capacitance become $R_L = 126.7\ \Omega$ and $C_S = 6.67$ pF. Though this cannot be achieved either, these values are much closer to the design values. Increasing P_{OUT} to ≈5 W would actually make it possible to use this topology in the ideal situation. The design criteria is however 1 W and the converter will thus be designed to have ZVS.

If the voltage across C_{S1} and C_{S2} are assumed to rise linear when they are charged, the rms value of the voltage at the node between the MOSFETs will be trapezoidal. If the duty cycle of each MOSFET is set to 25%, the rms value can be calculated as $V_{\mathrm{IN}}\sqrt{\frac{5}{12}}$. As with the two other inverters, this value can be used to find the needed reactance of the resonant circuit. Using (14) and choosing $C_R = 680$ pF, the value of L_R is calculated to 859 nH. As for the class E inverter, the value of each of C_{S1} and C_{S2} can be found using the reactance of the resonance circuit and scaling them according to the duty cycle. This gives

$$C_S = \frac{1}{2 \cdot (1 - D) \cdot 2 \cdot \pi \cdot f_S \cdot X_R} = 21.9 \text{ pF}. \quad (26)$$

As the total voltage across the two MOSFETs always will be V_{IN}, the average voltage across each of them is 25 V. The output capacitance of the MOSFET, used for the E and ϕ_2 inverters, almost fit the capacitance needed at this voltage and it will thus be used for the efficiency estimates. However, as the peak voltage across the MOSFETs is limited to the input voltage, several other MOSFETs could be used (or the input voltage could be increased).

Just as the case were for the two other inverters, it was necessary to adjust L_R a bit to give the desired output power. Adjusting the L_R to 550 nH and thus recalculating C_S to 21.4 pF gave the desired output power and the rms currents were extracted (see Fig. 12 and Table VI).

With these currents, the losses in the MOSFETs and the inductor are estimated to be $P_{L_R} = 2.2$ mW (using an ESR of 50 mΩ due to the small inductance) and $P_{\mathrm{FET1}} = P_{\mathrm{FET2}} = 5.5$ mW. If the losses in the capacitors are assumed negligible, the total loss will be 13.2 mW.

D. Selection of Inverter

During the analysis of the inverters, the values for all the passive components where found and they are summarized in Table VII.

All the inverters had some pros and cons, thus the same inverter will not be best for all applications. Some of the pros and cons are listed in Table VIII.

The class E inverter consists of only one MOSFET, two inductors, and a capacitor (if C_S is composed by the output capacitance of the MOSFET). It has however the largest voltage peak across the MOSFET which will limit the input voltage for a given MOSFET. Furthermore, the two inductors are both larger than any of the inductors used for the two other converters. This might limit the minimum size of the inverter as inductors are assumed to be the largest components. The total loss was estimated to be 38 mW or ≈ 4% of the output power.

TABLE VII
COMPONENT VALUES FOR THE CLASS E, ϕ_2 AND DE INVERTERS

Component	Class E	Class ϕ_2	Class DE
L_{IN}	2.91 μH	794 nH	
L_{MR}		375 nH	
C_{MR}		18.8 pF	
C_S	20 pF	20 pF	$2 \cdot 21.4$ pF
C_R	680 pF	680 pF	680 pF
L_R	1.43 μH	1.23 μH	550 nH

TABLE VIII
PROS AND CONS OF THE INVESTIGATED INVERTER TOPOLOGIES

	Class E	Class ϕ_2	Class DE
Pros	• Low side switch • Easy tuning • Well documented	• Low side switch • Reduced stress	• One inductor • Low loss • Low stress
Cons	• Large stress • Large inductors	• Largest loss • Complex	• High side switch

TABLE IX
COMPARISON OF MOSFET CHARACTERISTICS

Component	V_{DSS}	I_D	$R_{DS(on)}$	C_{ISS}	C_{OSS}
IRF5802	$150\,V$	$0.9A$	$1.2\,\Omega$	$85\,pF$	$18\,pF$
FDN86246	$150\,V$	$1.6A$	$359\,m\Omega$	$180\,pF$	$28\,pF$

($R_{ds(on)}$ at V_{GS} = 10 V and capacitances at V_{DS} = 50 V).

The class ϕ_2 inverter was a lot like the class E, the only difference being the added *LC* circuit put in to reduce the voltage across the MOSFET. While this is a good way of keeping the voltage down, the steep voltage curves require larger currents making the loss larger than seen for the class E inverter. Although it has two extra components, compared to the class E inverter, the physical size is expected to be more or less the same as the values (and thereby the size) of the inductors are smaller. The total loss was estimated to 62.8 mW which is a 65% increase compared to the class E inverter.

The class DE inverter was the only inverter with two switches. However, as C_{S1} and C_{S2} are composed by the parasitic capacitance of the MOSFETs, the total component count of the class DE inverter are the same as for the class E inverter. The peak voltage across the MOSFETs were by far the lowest seen in any of the inverters and the currents were also the lowest. These things combined gave the smallest output inductor (which also is the only inductor) and the lowest losses (13.2 mW).

From this analysis, the class DE inverter seems to be the best solution and the class E inverter comes in second. However, during this analysis the gate drive has not been considered. A good high side gate drive which is capable of operating in the VHF range has yet to be developed whereas a low side gate drive can be made with few components [24]. The complexity, price, and losses associated with the added high side gate drive will, at least, reduce the benefits of the DE inverter.

With the above considerations in mind, the class E inverter was chosen for the final design.

IV. EXPERIMENTAL RESULTS

In Section III, the IRF5802 MOSFET was introduced and used for calculations and loss estimates. Although commercial available MOSFETs are generally designed for either hard switching at a few megahertz or less or for use in RF applications [36], several MOSFETs which can be used for this application exist. Two of the best suited are compared in Table IX.

In Section III, an output capacitance of 10.9 pF was found ideal, but 18 pF was the closest achievable with commercially available MOSFETs. As the voltage waveform across the MOSFET and C_S is given by $V_{\rm IN}$, f_S, and D, the currents (and thereby losses) in $L_{\rm IN}$, C_S, and the MOSFET scale with the value of C_S. It is therefore desirable to keep the value of C_S as close to this as possible in order to achieve high efficiency.

Comparing the two MOSFETs, the IRF5802 (M_1) has much higher on-resistance than the FDN86246 (M_2). However, the output capacitance is lower and will as mentioned decrease the currents and thus reduce the drawback of the high on-resistance. Assuming the waveform of the voltage across the MOSFET is the same using the two MOSFETs, the current using M_2 will be $\frac{C_{M2}-C_{M1}}{C_{M1}} = 142\%$ larger than using M_1. The on resistance will be reduced by $\frac{R_{M1}-R_{M2}}{R_{M1}} = 70.1\%$. Combining this gives a total loss reduction of 27.4%, using the estimated loss found in Section III this correspond to 9 mW. Furthermore, the increased current will also give losses in the input inductor, again using the estimate from Section III the increased loss is found to $142\% \cdot 5.37$ mW $= 7.63$ mW. Hence, the total loss difference using the two MOSFETs is estimated to be less than 2 mW. The increased capacitance will however also make the timing of the switching more important, as a larger amount of energy will be stored in the capacitor and dissipated in the MOSFET if the switching is just a little wrong.

Based on the analysis above, the MOSFET from IRF are found most suited. But as they are very close, prototypes using both will be made to compare them further.

The next sections will cover the results obtained with three different power stages. The first power stage is the one which has been designed in the previous sections, the second power stage is with the MOSFET with lower $R_{\rm DS(ON)}$ and the last power stage is with a large input inductor and higher output power, this should, as described in Section III, give a higher efficiency.

A signal generator has been used to drive the MOSFETs and hence the design and efficiency of this is not included. The gate signal is however a sinewave which several researchers have shown how to generate efficiently using various types of resonant gate drives, e.g. [37]–[39]. The duty cycle is controlled by adjusting the dc offset of the sinewave, hence a dc offset equal to the threshold of the MOSFET will lead to a duty cycle of 50% and a lower offset lead to a lower duty cycle.

A. *MOSFET With Low* $C_{\rm OSS}$

A power stage with the components selected in Sections II and III was implemented. Ceramic C0G capacitors were used for the resonating capacitors in order to ensure stable capacitance with varying voltages and ceramic X7R capacitors were used

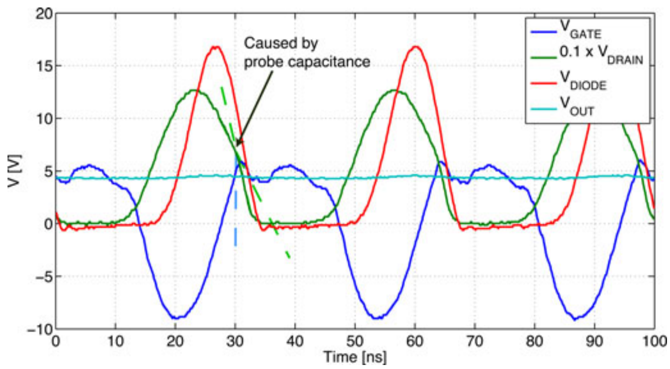

Fig. 13. Measurements on the prototype with low C_{OSS}.

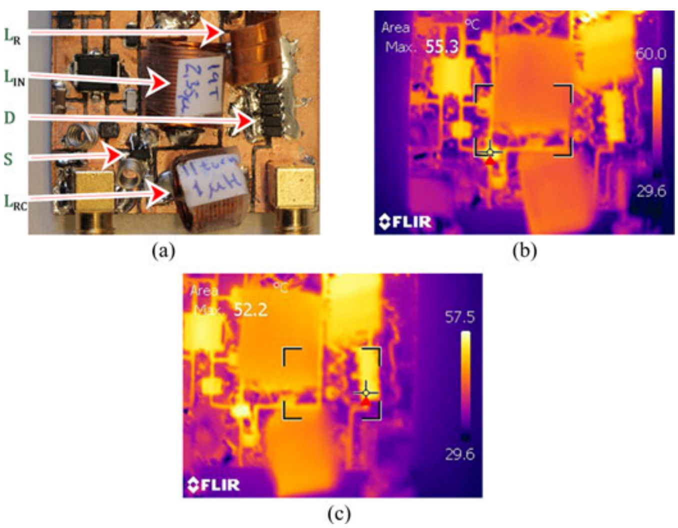

Fig. 14. Temperature measurements of the MOSFET and the diodes in the prototype with low C_{OSS} (W_{board} = 40 mm). (a) Placement of the components. (b) The MOSFET is 55.3 °C. (c) The diodes are 52.2 °C.

TABLE X
MEASUREMENTS ON POWER STAGES

Converter	f_S [MHz]	I_{IN} [mA]	V_{OUT} [V]	R_L [Ω]	η [%]	T_{Mos} [°C]	T_{Dio} [°C]
Low C_{OSS}	30	28	5.00	25	71.5	55.3	52.2
Low R_{DS}	29	32	4.93	25	60.7	65.1	53.2
Large L_{IN}	30	37	5.00	16.3	82.9	46.2	50.5

as input and output capacitors. Custom made air core solenoids were used in order to enable exact tuning of the inductances and thereby achieve ZVS.

Just as the case were when going from calculated values to simulations, slight adjustments had to be made. The tuning procedure was first to tune the inductor in the output filter to make it resistive at the switching frequency. Once that was done, the inverter was added to the design and a low voltage was applied. It was seen that the converter was not ZVS switching as the output capacitance of the MOSFET was not discharged when switched ON.

In order to get it to discharge faster, the values of the input and resonant inductors had to be lowered. First, the resonant inductor was lowered to give the desired output power and then the input inductor was adjusted to make the converter ZVS. As the output capacitance of the MOSFET is 20 pF, measuring with a probe with 10 pF capacitance changes the circuit a lot. This ruins the tuning and ZVS is thus not achieved, some waveforms have been measured and they are shown in Fig. 13. As it is seen the drain voltage has a small break when the MOSFET is switched ON, this is due to the 10 pF added by the probe. The fact that the converter is not ZVS also introduces the miller plateau in the gate charge and causes the gate signal to deviate from a sinewave when the voltage reaches the miller voltage.

So for the final fine tuning a thermal camera was used to measure the temperature of the MOSFET, it was then assumed that the MOSFET was ZVS when the temperature rise was lowest. Even though this is not a solid proof of ZVS, a low temperature rise comes from low power loss and thus the best tuned circuit.

Fig. 14 shows thermal pictures of the converter in a steady state. From the pictures, it is seen that the diodes get almost as hot as the MOSFET. As the size of the components is almost equal this indicates that the total diode loss is almost five times the total MOSFET loss (there are five diodes in parallel). The efficiency was measured to be 71.5% (see Table X).

B. MOSFET With Low R_{ON}

When the MOSFET was selected, the FDN86246 was found to be equally good to the IRF5802. The biggest difference between the two was on-resistances and parasitic capacitances. A prototype was implemented using the FDN86246 in a circuit almost identical to the one used for the previous converter. A few turns were removed from the input inductor in order to make the converter ZVS with the increased output capacitance in the new MOSFET.

The MOSFET gets almost 10 °C warmer (see Fig. 15) clearly indicating a higher loss. Due to the higher output capacitance, more energy is stored and if the switch is switched at a few volts instead of zero, much more energy will be dissipated in the on-resistance. Furthermore, the ac current in the input inductor is larger which also increases the losses. The total efficiency of the converter was measured to 60.7%.

C. With Large Input Inductor

As explained in Section III, the highest efficiency should be achieved with a large input inductor (dc input current). To test this, a prototype was made with the IRF5802, but this time with a 6.5 μH input inductor. Then, the resonance circuit and the load were adjusted in order to get ZVS and 5 V output.

The increased output power makes the current through the MOSFET closer to that seen for the ideal class E inverter. Thereby, the loss due to slight deviations in the timing of the switching becomes smaller.

The waveforms shown in Fig. 16 clearly show that the converter is not ZVS when probes are placed at the gate and drain. Furthermore, the voltage drops below 4 V, however removing the probes makes the output voltage increase to 5.0 V.

When tuned, the output power of the circuit became 1.53 W and the efficiency was measured to 82.9%. This efficiency is without gate drive, but it is still among the best results achieved

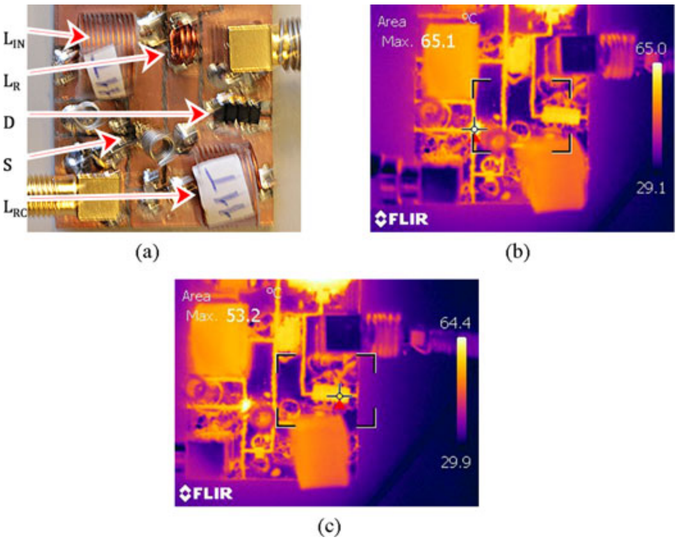

Fig. 15. Temperature measurements of the MOSFET and the diodes in the prototype with low $R_{\mathrm{DS(ON)}}$ ($W_{\mathrm{board}} = 32$ mm). (a) Placement of the components. (b) The MOSFET is 65.1 °C. The diodes are 53.2 °C.

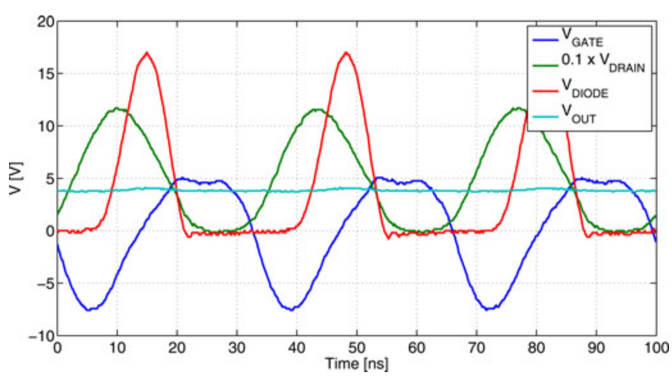

Fig. 16. Measurements on the 1.53W prototype with IRF5802.

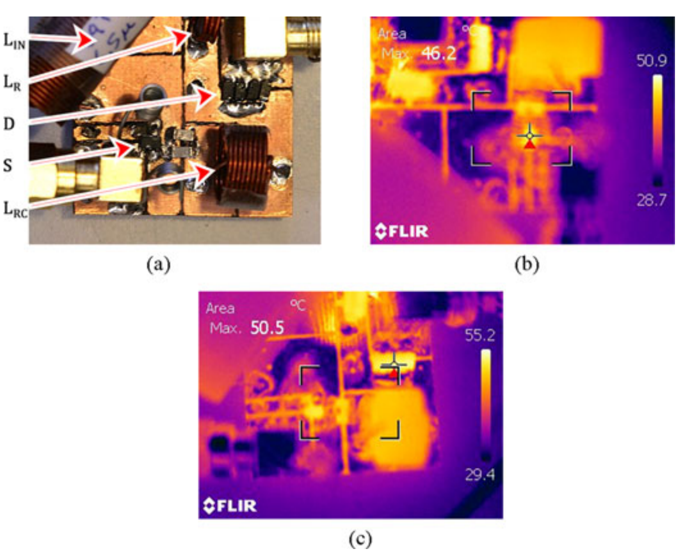

Fig. 17. Temperature measurements of the MOSFET and the diodes in the prototype with large input inductor. (a) Placement of the components. (b) The MOSFET is 46.2 °C. (c) The diodes are 50.5 °C.

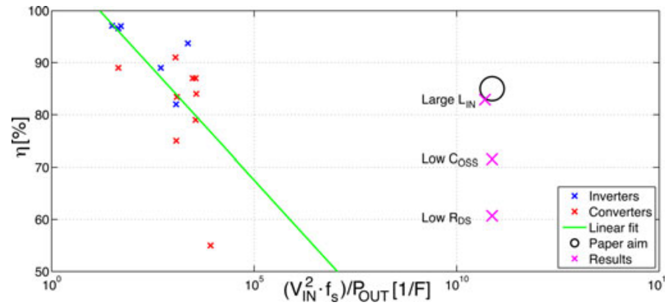

Fig. 18. The achieved $\frac{P_{\mathrm{OUT}}}{V_{\mathrm{IN}} \cdot f_S}$-factor and η next to previous results.

by previous researchers. Furthermore, the $\frac{V_{\mathrm{IN}}^2 \cdot f_S}{P_{\mathrm{OUT}}}$-factor explained in Section I is much smaller than for any of the converters shown in Table I.

D. Summary of Experimental Results

The efficiency achieved for the three power stages is shown in Table X. From the three prototypes, it is seen that good efficiencies can be achieved just by having ZVS. However, the larger the current through the MOSFET is at the switching instant, the more important becomes the timing of the switching and losses increase.

It has been shown that VHF converters with a very low $\frac{V_{\mathrm{IN}}^2 \cdot f_S}{P_{\mathrm{OUT}}}$-factor can be made with high efficiency, the best even had an efficiency of 82.9% which puts it among the best VHF converters. For comparison, the results achieved for the power stages are shown in Fig. 18. The efficiency is not as high as wanted and the factor is a little higher than desired for one of the prototypes due to the higher output power. However, seen next to previously achieved results they are very close.

V. Conclusion

The theoretical design of the resonant converter was considered in Sections II and III. Several different topologies were considered and based on complexity and efficiency estimates a class E inverter and rectifier were chosen.

The class E inverter was chosen based on complexity, efficiency, and the fact that it did not require a high side switch. With a simple and efficient high side gate drive the DE inverter is theoretically better, especially for converters with even higher input voltages. Such a gate drive was however yet to be invented and this topology was therefore not used for the practical implementation.

For the rectifier part it was again the class E topology that were chosen, this time due to the forward voltage drop of the diodes. With a low-voltage output, the forward voltage drop of the diode becomes a significant percentage of the output voltage and a single diode rectifier was found to be the best choice. For higher output voltages, the DE rectifier might be better as the loss due to forward voltage drop in the diodes becomes insignificant and the voltages stress of the devices the major concern.

Three different power stages were made; one with a MOSFET with the lowest available output capacitance, one with a

MOSFET with low on-resistance, and one with increased output power allowing a large input inductor. All the converters had 50 V input and 5 V output and the achieved efficiencies were between 60.7% and 82.9%. This shows that it is possible to make low power very high frequency converters with high step down ratio running at subnominal condition as long as the components are chosen carefully.

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Mickey Madsen (S'12) received the B.Sc.E.E. and M.Sc.E.E. degrees from the Technical University of Denmark, Kongens Lyngby, Denmark, in 2009 and 2012, respectively. He is currently working toward the Ph.D. degree in power electronics under the title "Very High Frequency Switch Mode Power Supplies."

His research interests include switch-mode power supplies, resonant inverters/converters, wide band gab semiconductors, solid state (LED) lighting, and radio frequency electronics.

Arnold Knott (M'10) received the Diplom-Ingenieur (FH) degree from the University of Applied Sciences, Deggendorf, Germany, in 2004. He received the Ph.D. degree from the Technical University of Denmark, Kongens Lyngby, Denmark, in 2010, working on a research project under the title "Improvement of out-of-band Behavior in Switch-Mode Amplifiers and Power Supplies by their Modulation Topology."

From 2004 to 2009, he worked with Harman/Becker Automotive Systems GmbH in Germany and USA, designing switch-mode audio power amplifiers and power supplies for automotive applications. From 2010 to 2013, he was a Assistant Professor and since 2013 an Associate Professor at the Technical University of Denmark. His interests include switch-mode audio power amplifiers, power supplies, active and passive components, integrated circuit design, acoustics, radio frequency electronics, electromagnetic compatibility, and communication systems.

Michael A. E. Andersen (M'88) received the M.Sc.E.E. and Ph.D. degrees in power electronics from the Technical University of Denmark, Kongens Lyngby, Denmark, in 1987 and 1990, respectively.

He is currently a Professor of power electronics at the Technical University of Denmark. Since 2009, he has been the Deputy Director at the Department of Electrical Engineering. He is the author or coauthor of more than 200 publications. His research interests include switch-mode power supplies, piezoelectric transformers, power factor correction, and switch-mode audio power amplifiers.