Synchronized Zero-Crossing-Based Self-Tuning Capacitor Time-Constant Estimator for Low-Power Digitally Controlled DC–DC Converters

Aleksandar Radić, Adrian Straka, and Aleksandar Prodić

***Abstract*—A hardware efficient method and system for estimating the time constant and measuring the current of the output capacitors in digitally controlled switch-mode power supplies is introduced. The estimator emulates the equivalent *RC* circuit of the output capacitor with a much smaller version, placed in parallel, and adjusts its own resistance until the two circuits have the same time constant. The adjustment is based on a novel zero voltage crossing detection method and on synchronization with the digital pulse-width modulator operation. The effectiveness of the new estimator is verified with a 5 V to 1 V/5 A, 500-kHz buck converter prototype utilizing an optimal response controller. The experimental results show accuracy within a few tens of nanoseconds in the detection of capacitor zero-current crossing points, corresponding to a smaller than a 1.5% error in the time constant estimation, and, compared to an imperfectly tuned system, about 40% smaller voltage deviation during transients.**

***Index Terms*—DC-DC power converters, digital control, estimation.**

I. Introduction

In a realistic switch-mode power supply (SMPS) the output capacitor often has a nonnegligible equivalent series resistance, $R_{\rm esr}$, that, together with the capacitance value, forms the output capacitor time constant [1]. An accurate estimation of that constant and/or emulation of the realistic capacitor behavior is of a key importance for fast transient response control methods [1]–[4] and implementation of the power stage health monitoring systems [5]–[7]. The fast transient response methods often utilize emulators [8] as replacements for costly direct capacitor current measurement circuits. These emulators require a fairly accurate knowledge of the time constant in order to correctly estimate the instantaneous capacitor current and, consequently, obtain a fast and stable response. In power stage health-monitoring systems, the capacitor time constant monitoring can be utilized to determine the state of the capacitor dielectric, enabling early fault detection, timely repairs, and consequent prevention of one of the main sources of power supply failures [5]–[7].

Manuscript received December 11, 2013; accepted March 7, 2014. Date of current version May 30, 2014. Recommended for publication by Associate Editor R. Ayyanar.

The authors are with the Laboratory for Power Management and Integrated Switch-Mode Power Supplies, Department of Electrical and Computer Engineering, University of Toronto, Toronto, ON M5S 3G4 Canada (e-mail: radicale@ele.utoronto.ca; adrianstraka@gmail.com; prodic@ele.utoronto.ca).

Color versions of one or more of the figures in this paper are available online at http://ieeexplore.ieee.org.

Digital Object Identifier 10.1109/TPEL.2014.2313727

A number of perturbation-based [9], [10] and passive-circuit-based [1]–[7] methods for estimating the output capacitor time constant have been previously proposed. The perturbation-based systems introduce a small perturbance at the output node, which allows for the extraction of the converter component values (such as the output capacitor C and $R_{\rm esr}$) using signal processing of the output voltage waveform [9]. These systems are not able to measure instantaneous current and, as such, are not the best fit for optimal response controllers. The passive-circuit-based solutions provide both time constant estimation and instantaneous capacitor current measurements. They usually use a small *RC* filter placed in parallel with the output capacitor, to estimate the capacitor current via measurement of the voltage drop across the filter resistor. These filters have either fixed [1]–[4] or self-tuning *RC* time constants [5]–[7]. The fixed solutions are fairly simple for implementation but often exhibit a significant estimation error as the output capacitor parameters change [4] with operating conditions. As it will be demonstrated later, this error has a large negative effect on the performance of the fast transient controllers, requiring accurate detection of the capacitor instantaneous current. The self-tuning solutions [5]–[7] dynamically change their own time constant, to accommodate for the changes in the operating conditions, providing fairly accurate current measurements. However, the previously presented solutions are not the best-suited for cost-sensitive dc–dc SMPS of interest. The existing self-tuning systems require relatively complex hardware, such as a fast analog-to-digital converter (ADC), to obtain digital representations of the input current, load current, and/or the output voltage.

The main goal of this letter is to introduce a hardware-efficient self-tuning estimator and capacitor current emulator that does not have the drawbacks of the previously presented solutions. The new solution (labeled as $R_{\rm esr}C$ *estimator* in Fig. 1) is designed for dc–dc converters controlled by digital voltage mode pulse-width modulation schemes [11], [12]. Like other *RC*-based solutions [1], [3], [4], the emulator utilizes a small high-impedance *RC* filer, placed in parallel with the output capacitor. In this case, the *RC* circuit has an adjustable resistor, $R_{\rm adj}$, which is tuned continuously using only the knowledge of a capacitor zero-current crossing point and synchronization with the digital pulse-width modulator (DPWM).

In the following section, the operation of the introduced estimator is presented. Section III discuses issues related to the practical implementation. Section IV presents experimental verification.

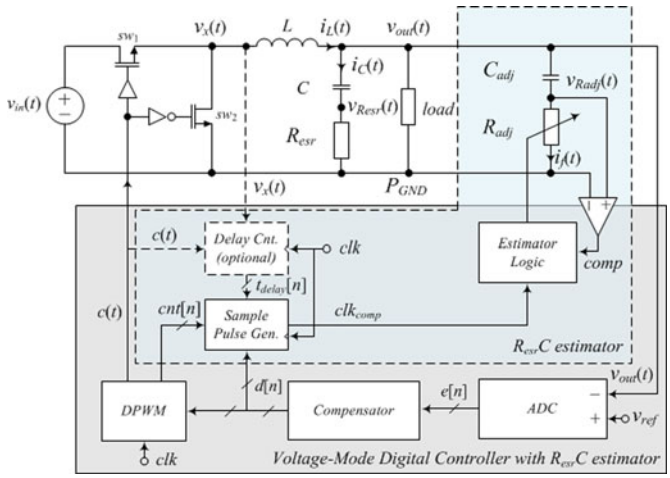

Fig. 1. Block diagram of a digitally controlled buck converter that incorporates self-tuning noninvasive $R_{\rm esr}C$ estimator.

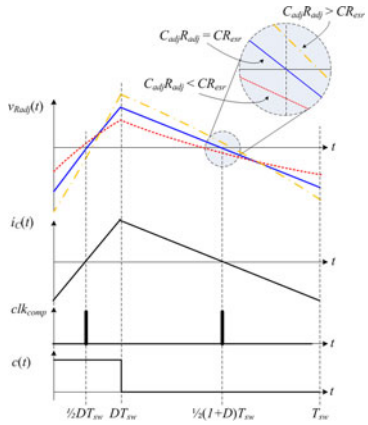

Fig. 2. Key waveforms of the digital controller and the self-tuning estimator. Top-to-bottom: $v_{\rm Radj}(t)$—voltage across the estimator resistor, $i_c(t)$—the output capacitor current, clk_{comp}—comparator sampling points/output capacitor zero-current crossing points), and $c(t)$—signal produced by the DPWM.

II. Principle of Operation

The self-tuning estimator of Fig. 1 operates on the well-known time constants matching principle, utilized in other capacitor current estimation systems [1]–[4] and in the *RC*-based inductor current estimation solutions [13], [14]. In these systems, an *RC* filter is placed in parallel with a nonideal element whose current is estimated. For the case when the time constants of the element, in this case the output capacitor, and the filter are the same the currents going through both elements have the same wave shapes and no delay between them occurs.

The system of Fig. 1 utilizes a miniature filter consisting of a capacitor $C_{\rm adj}$, which is much smaller than the power stage capacitor C, and a variable resistor $R_{\rm adj}$ whose value is much larger than $R_{\rm esr}$. This estimator periodically adjusts the $R_{\rm adj}$ value, such that $C_{\rm adj}R_{\rm adj} = CR_{\rm esr}$. The estimation is performed during converter steady state.

In order to match the $C_{\rm adj}R_{\rm adj}$ and $CR_{\rm esr}$ time constants, the introduced estimator takes advantage of the buck converter steady-state capacitor current waveform characteristics. Namely, the fact that during steady-state the capacitor current, $i_c(t)$, shown in Fig. 2, has a triangular waveform with two well-defined zero crossing points.

The first zero crossing at $\frac{1}{2}DT_{sw}$ and the second at $\frac{1}{2}(1 + D)T_{sw}$ [15], where D is the steady-state duty ratio value and $T_{sw} = 1/f_{sw}$ is the converter switching period. For the case when $C_{\rm adj}R_{\rm adj} = CR_{\rm esr}$, the small current going through the filter, $i_f(t)$, will be a scaled version of $i_c(t)$. This also means that *the voltage drop across* $R_{\rm adj}$ (see $v_{\rm Radj}$ in Fig. 1) *will only have the zero crossing points at* $DT_{sw}/2$ *and* $(1 + D)T_{sw}/2$ *when the two time constants are matched*. This observation is used in the self-tuning process of the estimator. When the two time constants are not matched the resistor voltage $v_{\rm Radj}(t)$ takes one of the two forms shown with dashed lines in Fig. 2. For the case when $R_{\rm adj}C_{\rm adj} < R_{\rm esr}C$, the zero crossings of $v_{\rm Radj}(t)$ occurs before the output capacitor current zero crossings, and for $R_{\rm adj}C_{\rm adj} > R_{\rm esr}C$ they are delayed. Therefore, by simply measuring the polarity of the $v_{\rm Radj}(t)$ at one of the two zero crossing points ($\frac{1}{2}DT_{sw}$ or $\frac{1}{2}(1 + D)T_{sw}$) information about the type of the mismatch can be obtained and, accordingly, the time-constant adjusted. In digitally controlled pulse-width modulated converters, such as the one of Fig. 1, the two comparison points, can be found in a straightforward manner. As shown in the following section, they can be determined by using the duty ratio control variable $d[n]$ and by extracting readily available information from the DPWM. In the controller of Fig. 1, like in other DPWM solutions [11], [12], the output voltage is regulated by creating a digital equivalent of the output voltage error $e[n]$ with an ADC *and error decoder* and passing the obtained value to a digital compensator, which calculates $d[n]$.

III. Practical Implementation

A practical realization of the estimator is shown in Fig. 3. It consists of a binary-weighted resistive network, a comparator, a sample and hold circuit *S/H*, a *sampling pulse generator*, and simple digital logic.

The polarity of $v_{\rm Radj}(t)$ at the zero capacitor crossing points is determined by monitoring sampled comparator value $comp_s$. The comparator is sampled once per cycle, using information about the digital equivalent of the duty-ratio value, $d[n]$, from the control loop (see Fig. 1) and by looking at the output of the N-bit counter, i.e., ramp generator, of the DPWM [16], labeled as *cnt*$[n]$. Accordingly, the equivalent $R_{\rm adj}$ value is adjusted using the binary-weighted resistive network and the estimator logic of Fig. 3.

In order to minimize switching noise effects, the sampling scheme presented in [17]–[19] is utilized. For $D > 0.5$ the sampling is performed at $\frac{1}{2}DT_{sw}$, and for $D < 0.5$ the samples are taken at $\frac{1}{2}(1 + D)T_{sw}$. This is accomplished with the *sampling pulse generator*. It compares *cnt*$[n]$ with $\frac{1}{2}d[n]$ or $\frac{1}{2}(2^N - 1 - d[n])$, depending on the readily available value of $d[n]$, and creates a sampling signal for the *S/H*. The binary output of the *S/H*, $comp_s$, is than used for controlling the operation of the finite state machine (FSM), which implements a binary search algorithm (BSA), to quickly find the matching $R_{\rm adj}$ value.

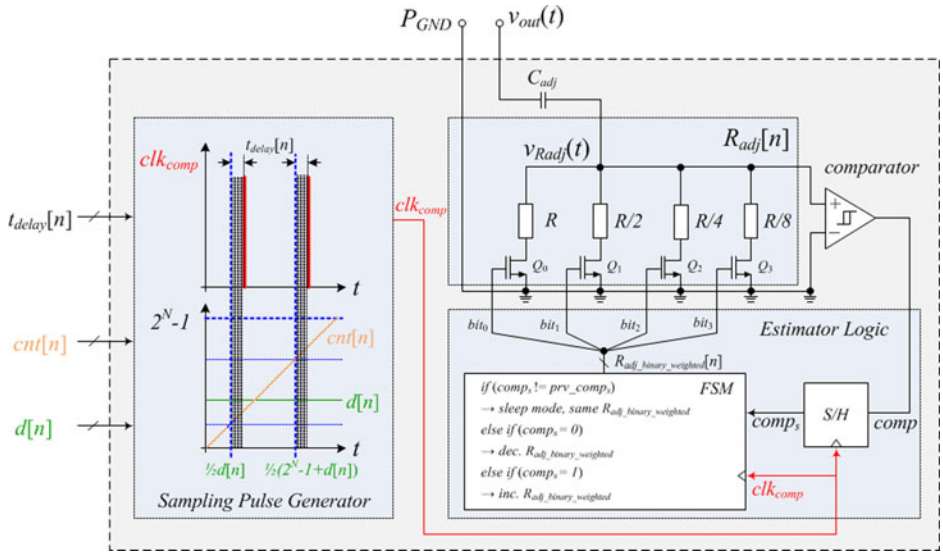

Fig. 3. Practical implementation of the estimator.

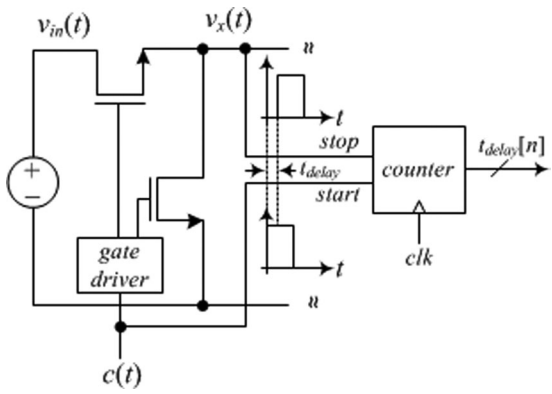

Fig. 4. Circuit for estimating gate driver and converter turn-on delay.

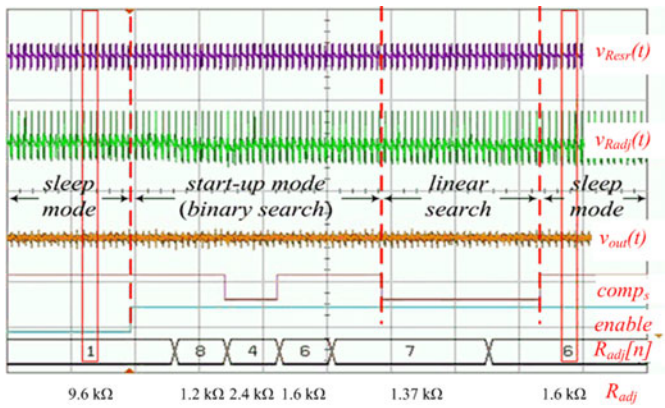

Fig. 5. Key waveforms of the digital controller and the self-tuning estimator. Top-to-bottom: $v_{Resr}(t)$—the output capacitor ESR voltage drop (200 mV/div), $v_{\mathrm{Radj}}(t)$—voltage across the estimator resistor (200 mV/div), $v_{out}(t)$—output voltage of the converter (500 mV/div), $comp_s$—sampled comparator output, *enable*—estimator enable bit, $R_{\mathrm{adj}}[n]$—binary resistor control value, and R_{adj}—equivalent adjustable resistor value. Time scale (20 μs/div).

The following section gives further details on the operation of the *estimator logic* block. It is followed by a section describing an optional circuit for reducing the effect of gate driver delays, which can be utilized to improve the estimator accuracy in applications where the delays are significant.

A. Tuning Algorithm

The tuning algorithm operates in two modes to ensure quick and accurate capacitor time constant estimation. Upon the SMPS start up the value of R_{adj} is adjusted in finer and finer steps until the $R_{\mathrm{adj}}C_{\mathrm{adj}}$ time constant is tuned within one quantization step of $R_{\mathrm{esr}}C$.

The adjustments of R_{adj} are performed by monitoring comparator output value, $comp_s$, at the sampling point shown in Fig. 2. When $comp_s$ is low, the R_{adj} value is increased and when $comp_s$ is high, the R_{adj} value is reduced. In order to quickly tune the filter, upon the converter start-up, when a large initial time-constant error is most likely to occur, a BSA is utilized [20], [21]. The BSA adjusts the equivalent resistance of the parallel binary-weighted resistive network by varying $R_{\mathrm{adj}}[n]$ (see Fig. 2). The adjustment is performed in consecutively smaller steps, where the change of the equivalent conductance in each step is reduced by half the value of the previous one, i.e., where the steps change as $\pm R/8$, $\pm R/4$, $\pm R/2$, $\pm R$. The steady-state condition is detected when the smallest change of the conductance, caused by turning on or off Q_0 (and activating/deactivating R), a transition of the comparator output from high-to-low or low-to-high is detected. This algorithm results in much faster tuning than that of the conventional linear one-bit step-by-step algorithm. For the 4-bit resistive network, the worst case tuning time is reduced from 15 to 4 steps. After the matched conditions are detected the estimator enters *sleep* mode and only occasionally is re-engaged after a predefined wait time.

It should be noted that between adjustment steps a delay equal to $3R_{\mathrm{adj}}C_{\mathrm{adj}}$ is introduced, allowing the estimator, i.e., *RC* filter, to achieve its "steady state."

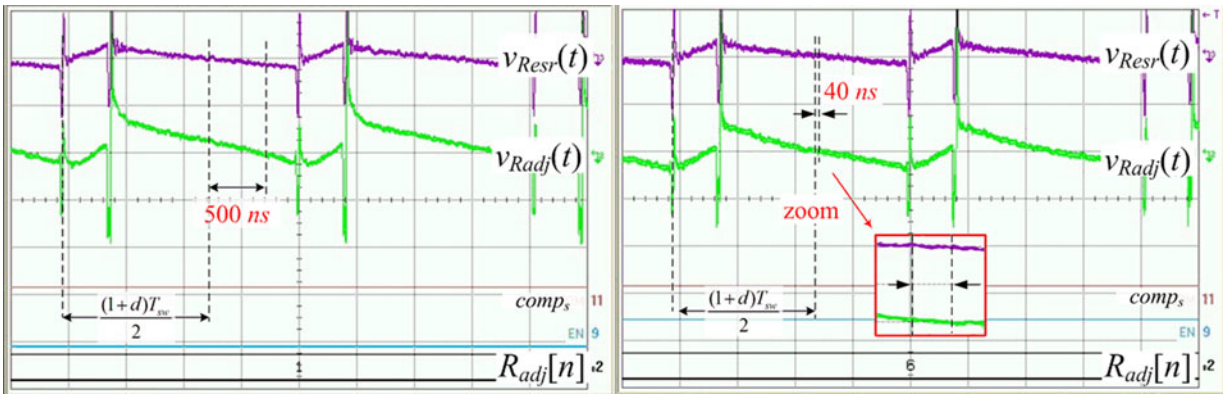

Fig. 6. Actual and estimated output capacitor ESR voltage before (left) and after (right) the tuning process. Top-to-bottom: $v_{Resr}(t)$—the output capacitor ESR voltage drop (25 mV/div), $v_{\mathrm{R\,adj}}(t)$—voltage across the estimator resistor (50 mV/div), $comp_s$—sampled comparator output, $R_{\mathrm{adj}}[n]$—binary-weighted representation of the resistor. Time scale—500 ns/div.

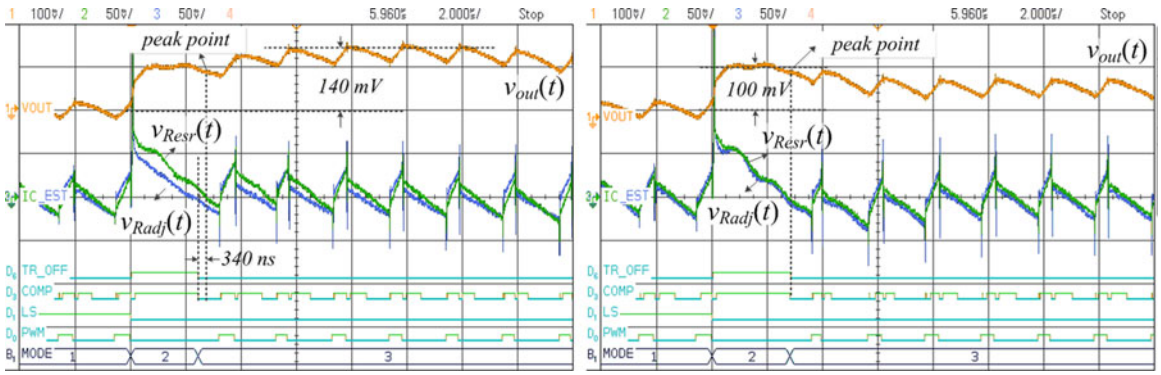

Fig. 7. Transient response of an optimal controller with untuned (left) and tuned (right) time constant estimator. Top-to-bottom: $v_{out}(t)$—output voltage (ac coupling—100 mV/div), $v_{Resr}(t)$—output capacitor ESR voltage (50 mV/div), $v_{\mathrm{R\,adj}}(t)$—voltage of the estimator resistor (50 mV/div), *tr_off* —main switch off signal, *comp*—estimator comparator output, *LS*—load step, *PWM*—control signal, *mode*—current FSM state (0—start-up, 1—PID, 2—minimum-deviation controller, 3—MD-to-PID transition). Time scale 2 μs/div.

B. Minimization of Gate-Drive Delay Effects

In some applications, the tuning process can be affected by a relatively large gate drive transmission time, causing the duty ratio of the switching node waveform, $v_x(t)$ of Fig. 1, to be significantly different from that of the gate drive input signal $c(t)$. To minimize the related estimation error, a simple delay measuring circuit of Fig. 4 can be added and the comparator output sampling points adjusted accordingly. Using a counter, which is triggered by the rising edge of $c(t)$ and stopped by the rising edge of $v_x(t)$, the measuring circuit counts the number of the DPWM clock (see *clk* of Fig. 1) cycles, T_{clk}, obtaining a digital equivalent of the total delay time, $t_{\mathrm{delay}}[n]$. This value is than passed to the sampling pulse generator (see Fig. 3), which time shifts the sampling by $t_{\mathrm{delay}}[n]T_{\mathrm{clk}}$, eliminating the delay effect.

IV. Experimental Results

To verify the operation of the estimator a 5 V to 1 V, 5 A, 500 kHz, a digitally-controlled, buck converter prototype was built, based on the diagrams of Figs. 1 and 3. The converter has a 1.5 μH output filter inductor and a 100 μF output capacitor with $R_{\mathrm{esr}} \approx 27$ mΩ, i.e., the time constant of 2.7 μs. To form the estimator filter, a small 2 nF capacitor and a 4-bit resistive network that can vary between 640 and 9600 Ω are used. This network allows variations in the estimator time constant between 1.28 and 19.2 μs, with 230 ns quantization steps, covering a typical range of the output capacitor variations, potentially allowing the estimator to be used as a plug-in module for a wide range of applications.

The results of experimental system verification are shown in Figs. 5 to 8. Fig. 5 illustrates how the $R_{\mathrm{adj}}[n]$, described in the previous section, is changing during the autotuning process. For the case when the error in the initially set time constant $\tau_a dj_i nitial$ results in the longest search algorithm, i.e., $C_{\mathrm{adj}}R_{\mathrm{adj}} = 7.11CR_{\mathrm{esr}}$. The results demonstrate effectiveness of the BSA. It can be seen that the time constant matching is achieved in only four cycles.

Experimental results of Fig. 6 demonstrate the accuracy of the estimator. They show zoomed-in capacitor current and the estimator voltage before and after the tuning, respectively. It can be seen that the delay between zero crossings of $i_c(t)$ and $v_{\mathrm{adj}}(t)$ has been reduced from 500 ns, indicating a large 18% mismatch in time constants, to 40 ns, corresponding to approximately a 1.5% maximum possible error and practically tuned filter.

To demonstrate influence of the accurate current sensing, i.e., self-tuning, on the dynamic performance of the SMPS, the response of an optimal response controller relying on

instantaneous current measurement [4] is compared for a tuned and an untuned case. The results show the response of the controller for the untuned case (see Fig. 7 left), where there is about 25% difference between the actual and estimated time constant value and for the tuned filter (see Fig. 7 right). The results demonstrated that, for the case when the estimator is used, about a 40% smaller voltage deviation is achieved, i.e., reduction from a 140 to 100 mV, allowing for a proportional minimization of the output capacitor. It should be noted that a similar effect of the filter tuning on the dynamic performance can be found in numerous other optimal-response solutions requiring instantaneous capacitor current measurements [1]–[4], [8].

V. Conclusion

A hardware-efficient self-tuning system for estimating the time constant and measuring the current of the output capacitors is introduced. This *RC* filter-based solution is well suited for low-power dc–dc converters controlled by digital voltage mode pulse-width modulation schemes. The self-tuning of the estimator filter is based on a simple principle of monitoring the estimator output at the expected zero crossing points. The comparison points are determined by using inherently available data of the digital control loop and through synchronization with the digital pulse-width modulator operation. Experimental results verify accurate online tuning and significant improvements in the transient response performance of realistic optimum deviation controller, allowing for a significant output capacitor reduction.

References

[1] E. Meyer, Z. Zhang, and Y.-F. Liu, "Digital charge balance controller to improve the loading/unloading transient response of buck converters," *IEEE Trans. Power Electron.*, vol. 27, no. 3, pp. 1314–1326, Mar. 2012.

[2] Z. Zhao and A Prodić, "Continuous-time digital controller for high-frequency DC–DC converters," *IEEE Trans. Power Electron.*, vol. 23, no. 2, pp. 564–573, Mar. 2008.

[3] S. C. Huerta, P. Alou, O. Garcia, J. A. Oliver, R. Prieto, and J. Cobos, "Hysteretic mixed-signal controller for high-frequency DC–DC converters operating at constant switching frequency," *IEEE Trans. Power Electron.*, vol. 27, no. 6, pp. 2690–2696, Jun. 2012.

[4] A. Radic, A. Prodic, and R. de Nie, "Self-tuning mixed-signal optimal controller with improved load transient waveform detection and smooth mode transition for DC–DC converters," in *Proc. IEEE Energy Convers. Congr. Expo.*, Sep. 12–16, 2010, pp. 3096–3100.

[5] C. Kulkarni, G. Biswas, X. Koutsoukos, J. Celaya, and K. Goebel, "Integrated diagnostic/prognostic experimental setup for capacitor degradation and health monitoring," in *Proc. IEEE AUTOTESTCON*, Sep. 13–16, 2010, pp. 1–7.

[6] A. M. R. Amaral and A. J. M. Cardoso, "On-line fault detection of aluminum electrolytic capacitors, in step-down DC–DC converters, using input current and output voltage ripple," *Power Electron., IET*, vol. 5, no. 3, pp. 315–322, Mar. 2012.

[7] G. M. Buiatti, J. A. Marti n-Ramos, C. H. R. Garci a, A. M. R. Amaral, and A. J. M. Cardoso, "An online and noninvasive technique for the condition monitoring of capacitors in boost converters," *IEEE Trans. Instrum. Meas.*, vol. 59, no. 8, pp. 2134–2143, Aug. 2010.

[8] R. Redl and N. O. Sokal, "Near-optimum dynamic regulation of DC–DC converters using feed-forward of output current and input voltage with current-mode control," *IEEE Trans. Power Electron.*, vol. PE-1, no. 3, pp. 181–192, Jul. 1986.

[9] Z. Zhao, S. M. Ahsanuzzaman, and A. Prodić, "ESR zero estimation and auto-compensation in digitally controlled buck converters," in *Proc. IEEE 24th Ann. Appl. Power Electron. Conf. Expo.*, Feb. 15–19, 2009, pp. 247–251.

[10] M. Shirazi, R. Zane, D. Maksimovic, L. Corradini, and P. Mattavelli, "Autotuning techniques for digitally-controlled point-of-load converters with wide range of capacitive loads," in *Proc. IEEE 22nd Ann. Appl. Power Electron. Conf.*, Feb. 25, 2007, pp. 14–20.

[11] B. J. Patella, A. Prodic, A. Zirger, and D. Maksimovic, "High-frequency digital PWM controller IC for DC–DC converters," *IEEE Trans. Power Electron.*, vol. 18, no. 1, pp. 438–446, Jan. 2003.

[12] Z. Lukic, N. Rahman, and A. Prodic, "Multibit Σ-Δ PWM digital controller IC for dc–dc converters operating at switching frequencies beyond 10 MHz," *IEEE Trans. Power Electron.*, vol. 22, no. 5, pp. 1693–1707, Sep. 2007.

[13] H. P. Forghani-zadeh and G. A. Rincon-Mora, "Current-sensing techniques for DC–DC converters," in *Proc. 45th Midwest Symp. Circuits Syst.*, Aug. 4–7, 2002, vol. 2, II-577–II-580.

[14] Z. Lukic, S. M. Ahsanuzzaman, Z. Zhao, and A. Prodic, "Sensorless self-tuning digital CPM controller with multiple parameter estimation and thermal stress equalization," *IEEE Trans. Power Electron.*, vol. 26, no. 12, pp. 3948–3963, Dec. 2011.

[15] R. W. Erickson and D. Maksimović, *Fundamentals of Power Electronics*. New York, NY, USA: Springer, 2001.

[16] A. Syed, E. Ahmed, D. Maksimovic, and E. Alarcon, "Digital pulse width modulator architectures," in *Proc. IEEE 35th Annu. Power Electron. Spec. Conf.*, Jun. 20–25, 2004, vol. 6, pp. 4689–4695.

[17] S. Buso, P. Mattavelli, L. Rossetto, and G. Spiazzi, "Simple digital control improving dynamic performance of power factor preregulators," *IEEE Trans. Power Electron.*, vol. 13, no. 5, pp. 814–823, Sep. 1998.

[18] K. D. Gusseme, D. M. Van de Sype, and J. A. A. Melkebeek, "Design issues for digital control of boost power factor correction converters," in *Proc. IEEE Int. Symp. Ind. Electr.*, 2002, pp. 731–736.

[19] D. M. Van de Syde, K. De Gusseme, and J. A. A. Melkebeek, "A sampling algorithm for digitally controlled boost PFC converters," in *Proc IEEE Power Electr. Spec. Conf.*, 2002, pp. 1693–1698.

[20] B. D. Smith, "Coding by feedback methods," *Proc. IRE*, vol. 41, no. 8, pp. 1053–1058, Aug. 1953.

[21] R. Nowak, "Generalized binary search," in *Proc. 46th Annu. Allerton Conf. Commun., Control, Comput.*, Sep. 23–26, 2008, pp. 568–574.