Analysis and Suppression of Leakage Current in Cascaded-Multilevel-Inverter-Based PV Systems

Yan Zhou, *Student Member, IEEE*, and Hui Li, *Senior Member, IEEE*

***Abstract*—The transformerless cascaded multilevel inverter (CMI) is considered to be a promising topology alternative for low-cost and high-efficiency photovoltaic (PV) systems. However, the leakage current issue resulted from the parasitic capacitors between the PV panels and the earth remains a challenging in designing a reliable CMI-based PV system. In this paper, the leakage current paths in PV CMI are analyzed and the unique features are discussed. Two filter-based suppression solutions are then presented to tackle the leakage current issue in different PV CMI applications. Simplified leakage current analytical models are derived to study the suppression mechanisms and design the suppression filters. Study cases are demonstrated for each of the solutions with filter design example, simulation and experimental verifications.**

***Index Terms*—Cascaded multilevel inverter (CMI), leakage current, photovoltaic (PV).**

NOMENCLATURE

CM	Common mode.
CMI	Cascaded multilevel inverter.
DM	Differential mode.
EMI	Electromagnetic interference.
PCC	Point of common coupling.
PWM	Pulse-width modulation.
qZSI	Quasi-Z-source inverter.
RMS	Root-mean square.
ZSI	Z-source inverter.
C_{cir_ac}	AC-side circulating capacitor for leakage current suppression.
C_{cir_dc}	DC-side circulating capacitor for leakage current suppression.
C_{cm}	CM capacitor.
C_{pvi}	PV panel parasitic capacitor of the ith inverter module.
i_{cir_ac}	Sum current through the two C_{cir_ac}.
i_{cir_dci}	Sum current through the two C_{cir_dc} of the ith inverter.
i_{leak_g}	Leakage current flowing into the grid ground.
i_{leak_Hi}	Leakage current through C_{pvi}.
L	Line inductor.
L_{cm_ac}	AC-side CM choke.
L_{cm_dc}	DC-side CM choke.
v_{CMi}	CM output of the ith inverter module.
v_{cpvi}	Voltage across C_{pvi}.
v_{DMi}	DM output of the ith inverter module.
v_{ia}	Phase leg a voltage of the ith inverter.
v_{ib}	Phase leg b voltage of the ith inverter.

Manuscript received May 26, 2013; revised August 9, 2013; accepted October 29, 2013. Date of current version May 30, 2014. This work was supported in part by the National Science Foundation under Award ECCS-1125658. Recommended for publication by Associate Editor C. A. Canesin.

Y. Zhou is with the Department of Electrical and Computer Engineering, Florida State University, Tallahassee, FL 32310 USA (e-mail: zou@caps.fsu.edu).

H. Lui is with the Department of Electrical and Computer Engineering, College of Engineering, Florida State University, Tallahassee, FL 32310 USA (e-mail: hli@caps.fsu.edu).

Color versions of one or more of the figures in this paper are available online at http://ieeexplore.ieee.org.

Digital Object Identifier 10.1109/TPEL.2013.2289939

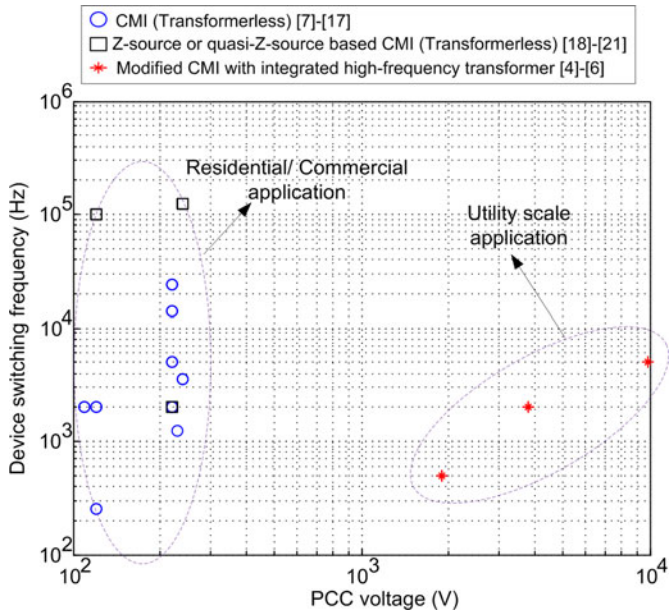


Fig. 1. Brief summary of the CMI in PV applications.

I. INTRODUCTION

TO maximize the energy harvest from the photovoltaic (PV) panels, the cascaded multilevel inverter (CMI) topology has been considered in PV applications for decades [1]–[3]. The CMI topology features separate dc inputs, making possible the string or even panel level maximum power point tracking. The energy harvest can be maximized in case of mismatch in the PV panels due to panel aging, shading effect or accumulation of dust in the panel surface. The cascaded structure can also generate high-quality output waveforms with each semiconductor device switching at lower frequency. In addition, cheaper power semiconductors with lower voltage rating can be utilized in the CMI compared with the central/string inverters.

Currently, the CMI has found its applications in both utility-scale and residential/commercial PV systems. A review of some reported CMI-based PV systems [4]–[21] is illustrated in Fig. 1,

where the point of common coupling (PCC) voltage and device switching frequency information are provided. It is noticed that modified CMI with integrated high-frequency transformer is usually utilized in large-scale PV systems [4]–[6]. The transformer is necessary for insulation purpose, because the several-kV PCC voltage may impose directly across the PV panel electrical section and its frame when there is no transformer and it could cause hazardous dielectric breakdown [4]. Besides, the integrated transformer can isolate the circulating leakage current paths.

On the other hand, for residential/ commercial applications with low PCC voltages, because there is no aforementioned insulation concern, transformerless PV CMI is preferred due to the lower cost and higher efficiency. The transformerless CMI structure can be readily accomplished by extending the number of cascaded modules. However, removal of the transformer would result in galvanic connections among the grid and the separate PV panels/strings interfaced with different cascaded inverters. Due to the parasitic capacitance between the PV panels and the earth, circulating leakage currents can flow through the panels and grid ground, leading to increased output harmonic content, higher losses, safety, and electromagnetic interference (EMI) problems. So far, there is rarely publication dealing with the leakage current issue in transformerless CMI-based PV systems.

The leakage current suppression techniques for transformerless string inverters have been well established [22]–[27]. They can be categorized into three different groups: modulation solutions, topology solutions, and filter solutions [28]. The bipolar modulation strategy can significantly reduce the leakage current because the common-mode (CM) voltage of the inverter is maintained constant [22], [23]. But the output current quality is degraded and the conversion efficiency is decreased. Hence, many modified full-bridge topologies, which add extra dc or ac switches, are developed to address the leakage current issue [23]–[25]. Nevertheless, these two solutions cannot be directly adopted in CMI to tackle the leakage current problem owing to the unique circulating current loops found among the cascaded modules. This will be explained in detail in Section II. The general idea of the filter solution is to compose a bypass loop of which impedance is very low for the high-frequency CM noises, thereby preventing the leakage current from flowing outside [26], [27]. It is easy to be implemented because no extra semiconductor device is needed. Therefore, the filter-based method is very attractive to be considered to address the leakage current issue in CMI.

Different types of circulating current issues are also found in other multimodule systems, such as CMI-based ac drives [29], [30], CMI-based magnetic resonance imaging systems [31], and paralleled boost rectifiers [32], [33]. In CMI-based ac drive systems, circulating bearing current is induced by the inverter CM voltage imposed on the motor stator winding to frame capacitance [29], [30]. Different modulation schemes are proposed to reduce the inverter CM voltage to reduce the circulating current. However, these modulation schemes cannot solve the leakage current issue in PV CMI because the PV parasitic capacitors are distributed at the dc side instead of the load side. Lai *et al.* [31] observed the internal circulating current in CMI formed by the inverter bus-to-ground parasitic capacitors. The high-amplitude MHz voltage ringing over the semiconductor device is the main concern in that paper, while the ground leakage current has not been discussed. For paralleled converters, circulating currents are generated due to the asynchronous switching operations [32], [33]. In such kind of systems, since there is no capacitance involved in the circulating loop, most high-frequency circulating currents can be mitigated by interphase inductors. Therefore, only the low-frequency circulating currents need to be dealt with. This is quite different from the PV CMI where switching-frequency noises dominate the circulating leakage currents.

This paper first identifies the leakage current paths in PV CMI. The differences between the transformerless CMI and string inverter concerning the leakage current behaviors are also discussed. Then two leakage current suppression solutions are presented for the PV CMI by adding properly located and designed passive filters in the inverter. The first method is more suitable for the CMIs operated at high switching frequency. The second method extends the application to the CMIs operated with lower switching frequency by bringing in extra wire connections among the cascaded modules and the grid output. Simplified leakage current analytical models for the PV systems with the two suppression solutions are developed, respectively, to demonstrate the principles and introduce the filter design criteria. Finally, the proposed first solution is applied in a PV system composed of four cascaded quasi-Z-source inverters (qZSIs) where each switching device is operated at 100 kHz. The second solution is executed in a PV system with two cascaded H-bridges where each switching device is operated at 10 kHz. Simulation and experimental results are provided to validate the effectiveness of the proposed solutions.

II. Leakage Current Analysis in CMI-Based PV Systems

As summarized in Fig. 1, the transformerless CMI-based PV systems can be built based on basic H-bridge inverters or modified ones, such as Z-source inverter (ZSI) and qZSI [18]–[21]. The replacement of the basic H-bridge inverter with the ZSI or qZSI is mainly to cope with the PV wide-range input voltage. Though the topology is slightly different, the CM characteristics of these CMIs are quite similar. This is because the Z-source/quasi-Z-source network can offer low-impedance paths for the high-frequency noises. Consequently, the basic CMI will be used to study the leakage current issue. The conclusions can also be applied to the ZSI- or qZSI-based CMI.

Fig. 2(a) shows a generic diagram of a CMI-based PV system where the parasitic capacitors are added to study the leakage current issue. The parasitic capacitor for each cascaded module is designated as $C_{pvi}, i = 1, 2, \ldots, n$. There are two symmetrical line inductors L at the total output of the inverter. The equivalent circuit can be obtained in Fig. 2(b) by modeling each inverter phase leg as a voltage source with respect to the negative terminal of its dc bus. The phase-leg voltage sources are named as v_{ia} and $v_{ib}, i = 1, 2, \ldots, n$. v_{ia} and v_{ib} are pulse-width modulation

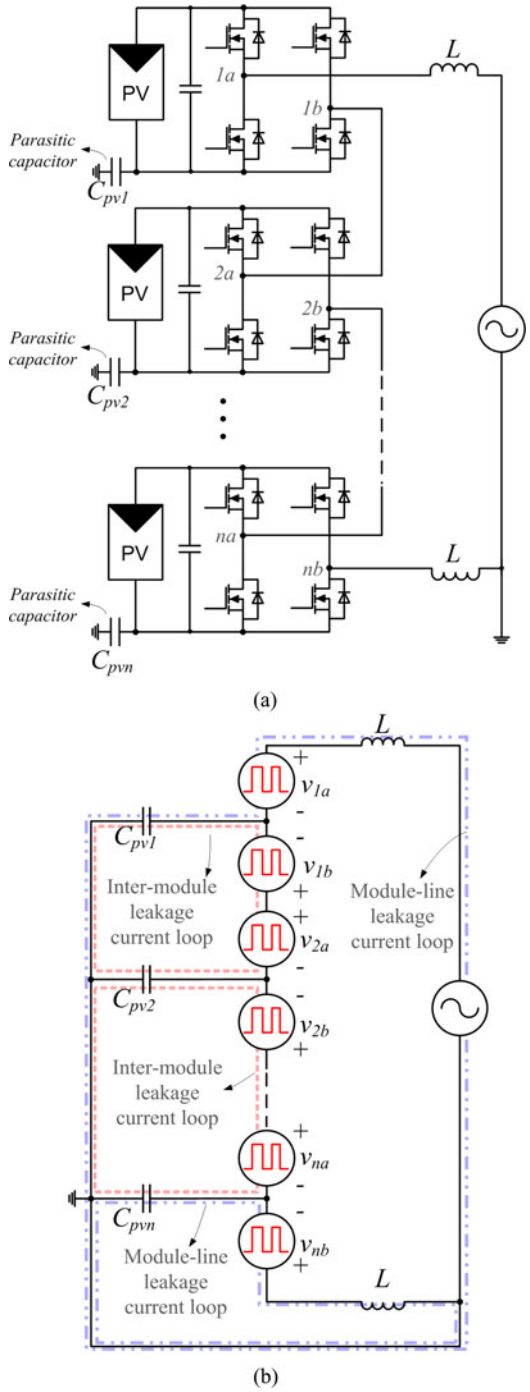


Fig. 2. Basic CMI-based PV system: (a) circuit diagram and (b) equivalent circuit.

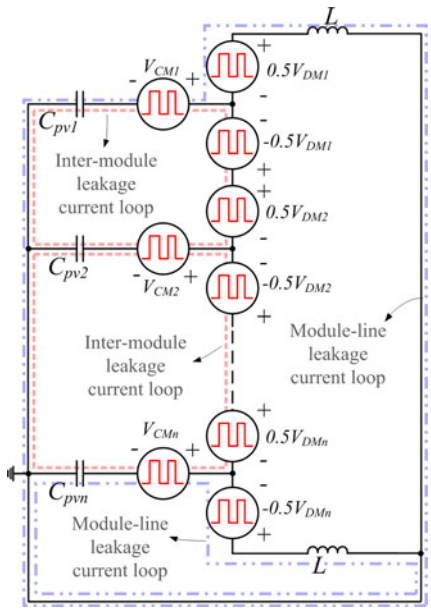


Fig. 3. System equivalent circuit by replacing the phase-leg voltages with DM and CM voltage sources.

(PWM) voltages which are composed of dc components, fundamental-frequency components and baseband harmonics, carrier harmonics and its sideband harmonics [34]. The carrier harmonics and its sideband harmonics are the main contributors to the leakage current issue. The magnitudes of these harmonics depend on the inverter input voltages and modulation strategy.

Due to the parasitic capacitors and several grounding points, multiple circulating leakage current loops are formed in the CMI. These loops can be divided into two different types and examples of the two kinds of loops are revealed in Fig. 2(b). The first kind of leakage current loop is formed by the parasitic capacitor, inverter bridge, line inductor, and grid ground. Since the line inductor and grid ground are involved in the loop, this loop is indicated as module-line leakage current loop. The other kind of loop is formed among the inverter bridges, so it is indicated as intermodule leakage current loop. It is a capacitive coupling path with negligible inductance, so the high-frequency PWM voltages would generate pulsewise leakage current in the loop. This phenomenon will be demonstrated in later case studies. Compared with the transformerless string inverter, the intermodule leakage current loop is a unique loop exists in the PV CMI. And it cannot be eliminated even if there is a transformer at the total output of the cascaded inverter.

For transformerless string inverters, the leakage current is mainly determined by the inverter CM output [22], [23]. Several modified inverter topologies and modulation strategies are proposed to maintain the CM output to be constant to solve the leakage current issue [22]–[25]. In CMI, we can define $v_{DMi} = v_{ia} - v_{ib}$ and $v_{CMi} = (v_{ia} + v_{ib})/2$ as the differential-mode (DM) and CM outputs of the ith module, respectively. The system equivalent circuit can be redrawn in Fig. 3 by replacing v_{ia} and v_{ib} with v_{DMi} and v_{CMi}. Due to the extra intermodule circulating loops, the leakage currents are no longer determined only by the CM outputs from the inverter modules. Instead, the DM outputs also contribute. Therefore, the aforementioned modulation- or topology-based suppression solutions for transformerless string inverters cannot be directly applied in CMI to solve the leakage current issue. The following sections will introduce two filter-based methods to solve the leakage current issue in PV CMI. The different allocation and design of the suppression filters make the two solutions fit for different applications.

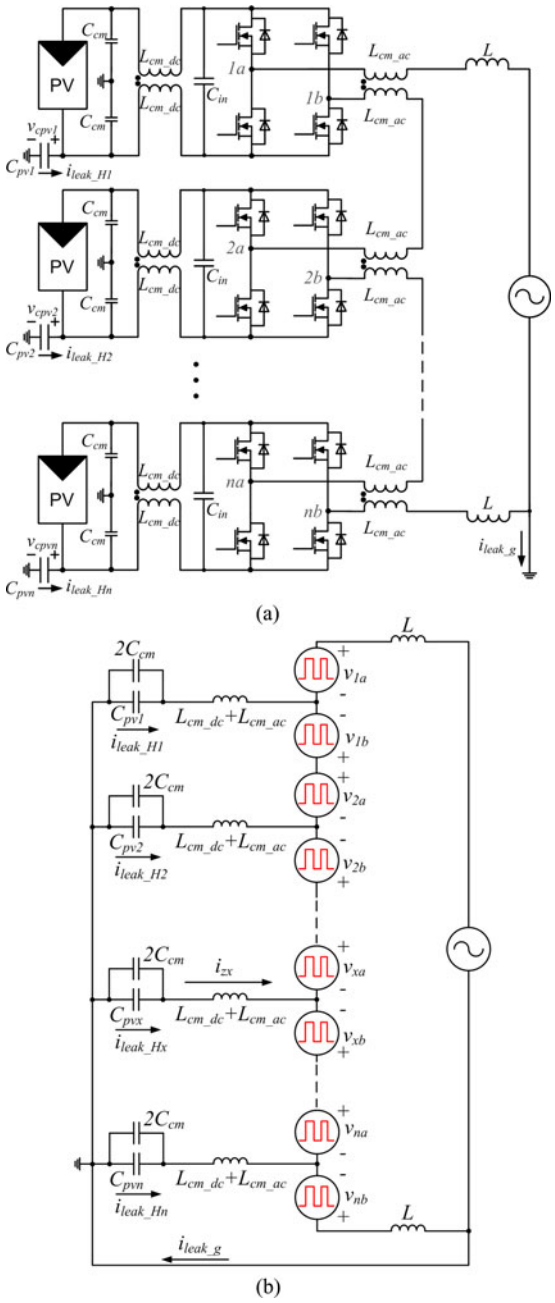


Fig. 4. Proposed leakage current suppression solution 1: (a) circuit diagram and (b) equivalent circuit.

III. Proposed Leakage Current Suppression Solution 1

A. Description of the Solution

The circuit configuration of a PV CMI with leakage current suppression solution 1 is illustrated in Fig. 4(a). Compared with the basic structure shown in Fig. 2, dc-side CM chokes L_{cm_dc}, CM capacitors C_{cm}, and ac-side CM chokes L_{cm_ac} are added in each inverter module. The voltage across C_{pvi} and the current through C_{pvi} are denoted as v_{cpvi} and $i_{\mathrm{leak}\_Hi}, i = 1, 2, \ldots, n$, respectively. The leakage current flowing into the grid ground is labeled as i_{leak_g}. The equivalent circuit of the system is given in Fig. 4(b) where the leakage inductance of the CM chokes is ignored due to its minor impact on the leakage current issue. It is also noticed that the L_{cm_ac} and L_{cm_dc} can be merged to the same position in the equivalent circuit, which implies that they would have the same contribution on leakage current suppression. L_{cm_ac} and L_{cm_dc} are both used in the circuit is because they can, respectively, help mitigate the ac-side and dc-side EMI CM noises due to their same position with the ac- and dc-side EMI filters. Therefore, the design effort for the ac- and dc-side EMI filters can be lessened, and this could compensate the added cost and size of L_{cm_ac} and L_{cm_dc} to some extent. Because this paper is emphasized on the leakage issue, L_{cm_ac} and L_{cm_dc} will be designed as one choke $L_{cm\_\mathrm{dc}} + L_{cm\_\mathrm{ac}}$. The optimal distribution of L_{cm_ac} and L_{cm_dc} should further consider the EMI problem, because the requirements for the ac- and dc-side EMI filters are different.

B. Simplified Leakage Current Analytical Model and Filter Design Criteria

To better understand the suppression mechanism and introduce the filter design criteria, the analytical expression of the leakage currents is derived based on the equivalent model. The xth inverter module is selected arbitrarily for the analysis. We can define $Z_i = j\omega(L_{cm\_\mathrm{dc}} + L_{cm\_\mathrm{ac}}) + \frac{1}{j\omega(C_{pvi}+2C_{cm})}, i = 1, 2, \ldots, n$ and $Z_L = j\omega L$. According to the superposition theory, the branch current i_{Zx} through the inductance $L_{cm\_\mathrm{dc}} + L_{cm\_\mathrm{ac}}$ of the xth $(1 \le x \le n)$ inverter module, which is labeled in Fig. 4(b), can be first calculated as follows:

$$i_{Zx} = \sum_{i=1}^{1} \frac{v_{1a}}{Z_{Si}} \cdot \frac{Z_{Pi}}{Z_x + Z_{Pi}} + \sum_{i=2}^{x} \frac{v_{ia} - v_{(i-1)b}}{Z_{Si}} \cdot \frac{Z_{Pi}}{Z_x + Z_{Pi}} + \sum_{i=x}^{n-1} \frac{v_{ib} - v_{(i+1)a}}{Z_{Si}} \cdot \frac{Z_{Pi}}{Z_x + Z_{Pi}} + \sum_{i=n}^{n} \frac{v_{nb}}{Z_{Si}} \cdot \frac{Z_{Pi}}{Z_x + Z_{Pi}} \tag{1}$$

where Z_{Si} is the impedance in series with the applied voltage and Z_{Pi} is the impedance in parallel with Z_x accordingly. When $i = 1, n, Z_{Si} = Z_L + (Z_1//\ldots//Z_n)//Z_L, Z_{Pi} = (Z_1//\ldots//Z_{x-1}//Z_{x+1}//\ldots//Z_n)//Z_L$; when $2 \le i \le x$, $Z_{Si} = (Z_1//\ldots//Z_{i-1})//Z_L + (Z_i//\ldots//Z_n)//Z_L, Z_{Pi} = (Z_i//\ldots//Z_{x-1}//Z_{x+1}//\ldots//Z_n)//Z_L$; when $x \le i \le n-1$, $Z_{Si} = (Z_{i+1}//\ldots//Z_n)//Z_L + (Z_1//\ldots//Z_i)//Z_L, Z_{Pi} = (Z_1//\ldots//Z_{x-1}//Z_{x+1}//\ldots//Z_i)//Z_L$.

As mentioned earlier, the phase leg voltages contain dc components, fundamental-frequency components and baseband harmonics, carrier harmonics and its sideband harmonics. The fundamental-frequency leakage current, of which amplitude is relatively small, can be simply estimated by shorting the inductors in the circuit due to their low impedances around the fundamental frequency. At the frequencies of the carrier harmonics, Z_L is usually much smaller than the impedance of the designed Z_i, so the values of the terms containing Z_L in (1) should be close to the value of Z_L. As a result (1) can be simplified as

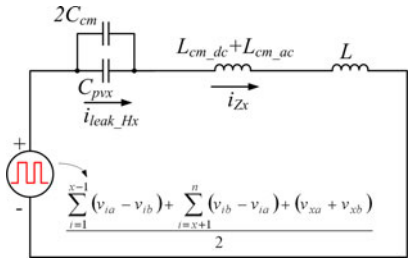


Fig. 5. Simplified leakage current analytical model for the system with leakage current suppression method 1.

follows:

$$i_{Zx} \approx \frac{\sum_{i=1}^{x-1}(v_{ia}-v_{ib})+\sum_{i=x+1}^{n}(v_{ib}-v_{ia})+(v_{xa}+v_{xb})}{2(Z_x+Z_L)}. \tag{2}$$

The simplified model implies an equivalent circuit shown in Fig. 5, which is composed of a voltage source connected with an LC branch in series. The voltage source is related to the phase leg voltages of all cascaded inverter modules. The LC circuit is formed by $L_{cm\_dc}+L_{cm\_ac}+L$ and $C_{pvx}+2C_{cm}$. i_{leak_Hx} can be obtained by

$$i_{\mathrm{leak}\_Hx} = i_{Zx}\frac{C_{pvx}}{C_{pvx}+2C_{cm}}. \tag{3}$$

According to the simplified model, we can design the filters that most high-frequency harmonic voltages are dropped across the inductance, in which case the high-frequency harmonics across C_{pvx} are lessened. In order to fulfill the requirement, the resonant frequency of the formed LC circuit needs to be designed lower than the frequencies of the carrier harmonics, specifically the device switching frequency. The final parameters of the filters can be specified according to (2) and (3), provided v_{ia} and v_{ib} $(i = 1, 2, \ldots, n)$ are known. The resistance associated with the chokes is ignored in the analysis, because it is usually designed much smaller than the inductance impedance at the carrier frequencies. Even when the resistance is designed large in some cases, it will benefit the leakage current suppression because the resistance increases the total impedance.

Since the value of C_{pvx} highly depends on the weather conditions, C_{cm} is added in the circuit in case that C_{pvx} gets too small. However, the value of C_{cm} is usually limited by safety requirements [23], [26], so the resonant frequency of the formed LC filter cannot be designed very low. Otherwise, large CM inductors are needed. Therefore, the first solution is more suitable for the cascaded inverter operated at high switching frequency. The applicability of this solution at preselected switching frequency depends on the constraint on the filter size and cost.

C. Application Example: qZSI-Based CMI With 100-kHz Switching Frequency

As discussed in Section II, the conclusions obtained for the H-bridge-based CMI concerning the leakage current behaviors can also be applied to the qZSI-based CMI. The proposed method

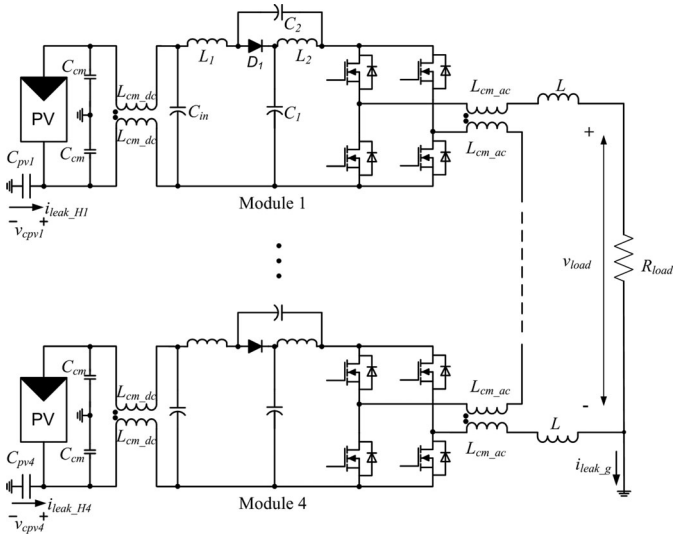


Fig. 6. System diagram of a PV system composed of four cascaded qZSIs with leakage current suppression solution 1.

1 is applied in a single-phase PV system consisted of four cascaded qZSIs. The system was first presented in [18] and the leakage current issue has not been dealt with in that paper. The system diagram is provided in Fig. 6 where each qZSI module is rated at 250 W with 25–50 V input voltage range. In order to decrease the size of the quasi-Z-source network and output line filter, the device switching frequency is chosen to be 100 kHz. The 100-V low-voltage GaN FETs from Efficient Power Conversion (EPC) [35] are used to improve system efficiency at high switching frequency. The sawtooth-carrier-based PWM modulation strategy is used for each module and the carrier waveforms are phase shifted to minimize the total output harmonics. The quasi-Z-source network is formed by $L_1 = 39\ \mu\mathrm{H}, L_2 = 39\ \mu\mathrm{H}, C_1 = 8.8\ \mathrm{mF}, C_2 = 198\ \mu\mathrm{F}$, and D_1. Resistive load is used in the study instead of the utility grid as in [36]. This load resistance $R_{\mathrm{load}} = 36\ \Omega$ has minor contribution to the total impedance of the leakage current loops at the switching frequency. The inverter total output voltage is 120 Vrms and the line inductor is $L = 20\ \mu\mathrm{H}$.

1) Filter Design: The suppression CM filters are designed by calculating the leakage currents based on (2) and (3). The calculated results of i_{leak_H1} and i_{leak_g} with different values of $L_{cm\_dc}+L_{cm\_ac}$ and parasitic capacitors are shown in Fig. 7, where C_{cm} is selected as 2.2 nF. The fundamental-frequency leakage currents are included in the calculated results. It is seen that the RMS value of i_{leak_g} slightly decreases with the increased parasitic capacitance. This is because the impedance of the LC circuit in Fig. 5 is increased at the frequencies of the carrier harmonics. The RMS value of i_{leak_H1} increases with the increased parasitic capacitance when $C_{pvx} \le C_{cm}$, and it becomes almost constant when $C_{pvx} >> C_{cm}$. According to the DIN V VDE V 0126–1–1 standard [37], in case that the leakage current is greater than 300 mA or the effective value of the suddenly occurring residual current exceeds 30 mA, the residual current protection device needs to be triggered. In order to limit the leakage currents below the standard requirement

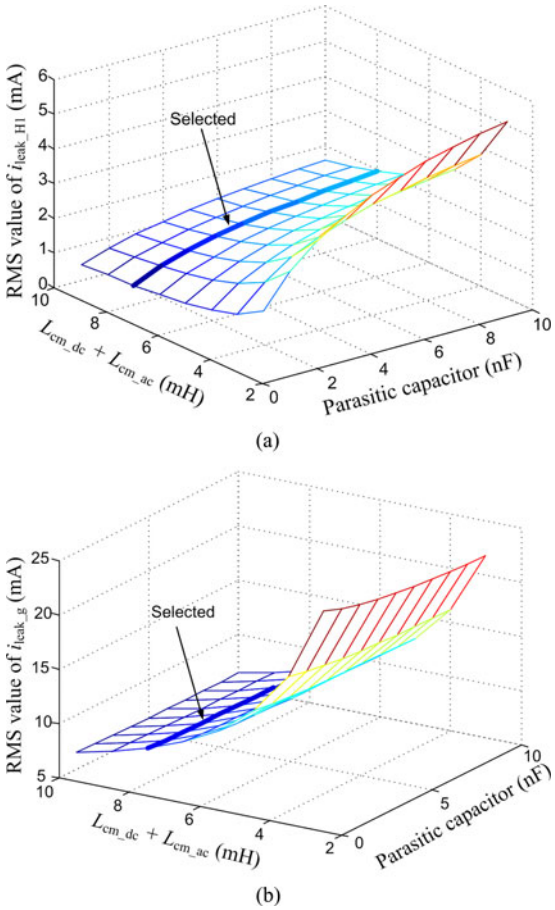


Fig. 7. Design results for the PV system with leakage current suppression solution 1: (a) $i_{\mathrm{leak\_}H1}$ and (b) $i_{\mathrm{leak\_}g}$.

with certain safety margin, 8 mH of $L_{cm\_\mathrm{dc}} + L_{cm\_\mathrm{ac}}$ is used. Since the majority of carrier-frequency voltage harmonics are imposed on the CM chokes, the magnetic design should consider the saturation issue caused by the volt-second excitation which is discussed in [26] and [38]. The selection of core shape and core material should fulfill the requirement as follows:

$$N_c \cdot A_c = h\frac{VS_{\max}}{B_{\mathrm{sat}}} \tag{4}$$

where A_c is the core cross section, N_c is the number of turns, $VS_{\max}$ is the maximum volt-second across the CM choke, B_{sat} is the saturation flux density, and h is the margin coefficient.

2) Simulation Verifications: The PV CMI with the designed CM filters is simulated in PSIM. C_{pvi} $(i = 1, 2, 3, 4)$ were assumed to be 1nF and the input voltages of the cascaded modules were 45 V. The simulated waveforms of $v_{cpv1}, v_{cpv2}, i_{\mathrm{leak\_}g}$, and $i_{\mathrm{leak\_}H1}$ are given in Fig. 8. When the suppression method was not applied, there were high-frequency harmonics in v_{cpv1} and v_{cpv2}, which induced large leakage currents. $i_{\mathrm{leak\_}H1}$ was pulsewise current with very high peak value due to the capacitive intermodule leakage current loop. The peak value of $i_{\mathrm{leak\_}g}$ was smaller because of the line filter L in the module-line leakage current loop, but it still exceeded the standard requirement. By introducing the suppression method, the high-frequency harmonics in v_{cpv1} and v_{cpv2} were significantly attenuated. The

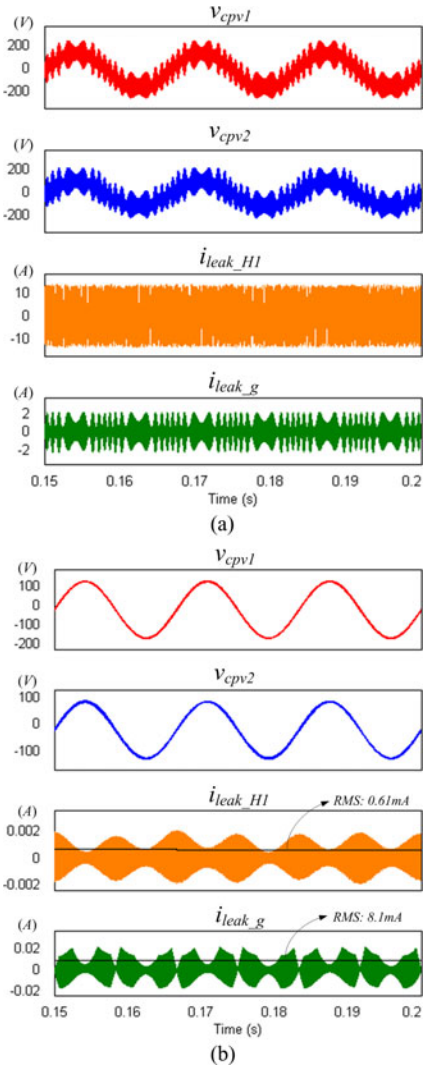


Fig. 8. Simulation waveforms of the qZSI-based PV CMI: (a) without leakage current suppression 1 and (b) with leakage current suppression solution 1.

100-kHz harmonics in v_{cpv1} and v_{cpv2} were both reduced from 0.24 to 0.015 pu (normalized values with respect to the input dc voltage). The RMS values of $i_{\mathrm{leak\_}H1}$ and $i_{\mathrm{leak\_}g}$ had been reduced to 0.61 and 8.1 mA, respectively, which were well below the standard requirement.

More simulation results of $i_{\mathrm{leak\_}H1}$ and $i_{\mathrm{leak\_}g}$ with different parasitic capacitor values are provided in Fig. 9 and compared with the calculated results obtained by (2) and (3). It is seen that the PSIM simulation results were consistent with the calculated values. This verified the accuracy of the simplified leakage current analytical model.

3) Experimental Verifications: Two cascaded qZSI modules using GaN devices are built in the laboratory, as shown in Fig. 10, to validate the performance of the proposed method. The parameters of the qZSI module are the same as in the simulation. C_{pv1} and C_{pv2} were purposely chosen to be different, $C_{pv1} = 30$ nF and $C_{pv2} = 1$ nF. Fig. 11 shows the measured waveforms and the spectrums of v_{cpv1} and v_{cpv2} without the CM filters added in the system. It is seen that v_{cpv1} and v_{cpv2} contained around

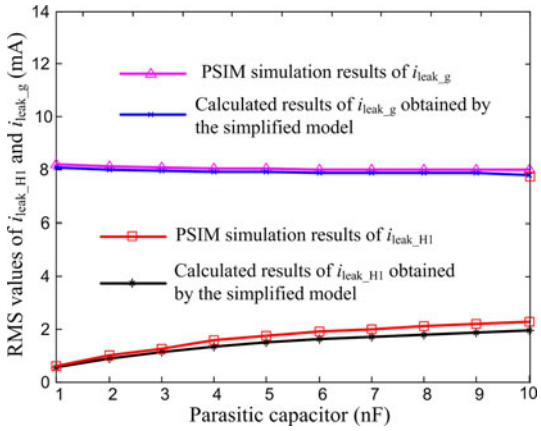


Fig. 9. Comparison of the PSIM simulation and calculated results of i_{leak_H1} and i_{leak_g} for the qZSI-based PV CMI.

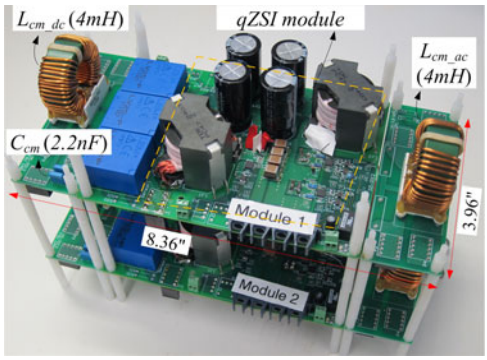


Fig. 10. Photograph of the two cascaded qZSI modules built in the laboratory.

0.3 pu 100 kHz harmonics. When the leakage current suppression was applied, the 100-kHz harmonics in v_{cpv1} and v_{cpv2} were readily reduced to 0.003 and 0.023 pu, respectively, as shown in Fig. 12. Obviously, the carrier harmonics across C_{pv1} were better attenuated in this case. This was consistent with the derived simplified leakage current analytical model given in Fig. 5. The increased parasitic capacitance leaded to a lower resonant frequency of the formed LC circuit, so the harmonics in v_{cpv1} were better attenuated.

IV. Proposed Leakage Current Suppression Solution 2

A. Description of the Solution

The leakage current suppression method 2 is realized by adding dc-side and ac-side CM chokes L_{cm_dc} and L_{cm_ac}, and capacitors C_{cir_dc} and C_{cir_ac}, as shown in Fig. 13(a). There is a common connection point among the capacitors C_{cir_dc} of each cascaded module and the ac-side capacitors C_{cir_ac}. The equivalent circuit of the system is given in Fig. 13(b), where internal current circulating paths, as shaded in the figure, are formed by the CM chokes, bridges, C_{cir_dc} and C_{cir_ac}. It is observed that the internal current circulating circuit is quite similar to the system equivalent circuit with leakage current suppression method 1 shown in Fig. 4(b), except that the capacitance $2C_{cir\_\mathrm{ac}}$ is added in the return path and the capacitance $2C_{cir\_\mathrm{dc}}$ replaces $C_{pvx}+2C_{cm}$. Unlike the CM capacitors, C_{cir_dc} and C_{cir_ac}

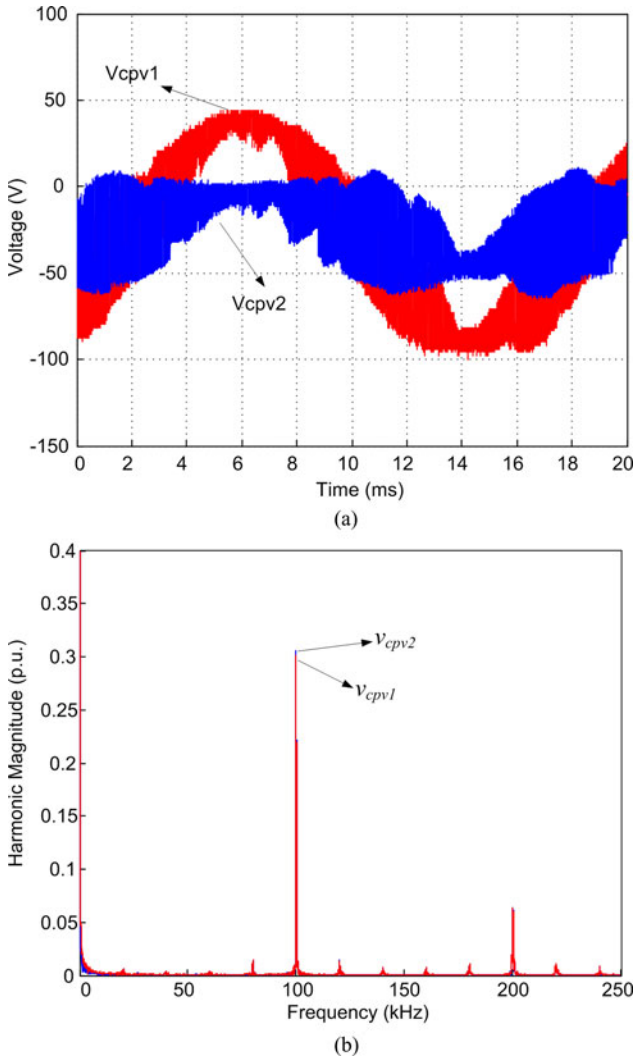


Fig. 11. Experimental results without leakage current suppression 1: (a) voltage across the parasitic capacitors and (b) the corresponding spectrums.

can be designed relatively large, so this solution can be applied for the CMI operated with lower switching frequency without using very large CM chokes.

B. Simplified Leakage Current Analytical Model and Filter Design Criteria

According to the equivalent circuit, the leakage current through the parasitic capacitor of the xth inverter is equal to

$$i_{\mathrm{leak}\_Hx}=i_{cir\_\mathrm{dc}x}\frac{C_{pvx}}{2C_{cir\_\mathrm{dc}}}+i_{cir\_\mathrm{ac}}\frac{C_{pvx}}{2C_{cir\_\mathrm{ac}}} \tag{5}$$

where $i_{cir\_\mathrm{dc}x}$ is the sum current through the two C_{cir_dc} capacitors of the xth inverter module; i_{cir_ac} is the total current through the two C_{cir_ac} capacitors.

Practically C_{cir_dc} and C_{cir_ac} are designed much larger than the parasitic capacitance, so we can get $\frac{C_{pvx}}{2C_{cir\_\mathrm{dc}}}<<1$ and $\frac{C_{pvx}}{2C_{cir\_\mathrm{ac}}}<<1$. Therefore, i_{leak_Hx} can be attenuated when the values of $i_{cir\_\mathrm{dc}x}$ and i_{cir_ac} are limited. Based on the equivalent circuit, $i_{cir\_\mathrm{dc}x}$ and i_{cir_ac} can be calculated as in (6) and

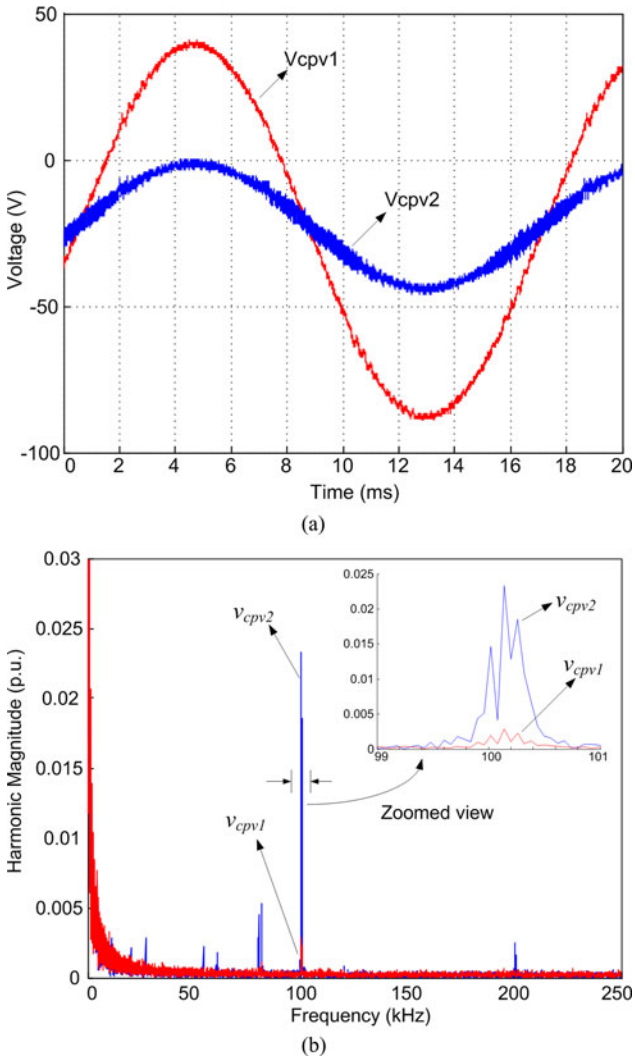


Fig. 12. Experimental results with leakage current suppression solution 1, $Cpv1 = 30$ nF and $Cpv2 = 1$ nF: (a) voltage across the parasitic capacitors and (b) the corresponding spectrums.

(7) by applying the superposition theory:

$$i_{cir\_dcx} = \frac{v_{1a} + v_{nb}}{2Z + 2nZ_{cir\_ac} + nZ_L} + \sum_{i=2}^{x} \left(v_{ia} - v_{(i-1)b}\right) \cdot \frac{\left(\frac{1}{i-1}Z + 2Z_{cir\_ac} + Z_L\right) \cdot (i-1)}{Z\left(2Z + 2nZ_{cir\_ac} + nZ_L\right)} + \sum_{i=x}^{n-1} \left(v_{ib} - v_{(i+1)a}\right) \cdot \frac{\left(\frac{1}{n-i}Z + 2Z_{cir\_ac} + Z_L\right) \cdot (n-i)}{Z\left(2Z + 2nZ_{cir\_ac} + nZ_L\right)} \quad (6)$$

$$i_{cir\_ac} = \sum_{i=1}^{n} i_{cir\_dci} \quad (7)$$

where $Z_{cir\_ac} = 1/j2\omega C_{cir\_ac}$, $Z = j\omega(L_{cm\_dc} + L_{cm\_ac}) + (1/j2\omega C_{cir\_dc})$, and $Z_L = j\omega L$. Because the parasitic capacitances are much smaller than C_{cir_dc} and C_{cir_ac}, they are ignored in the calculation of i_{cir_dcx} and i_{cir_ac}.

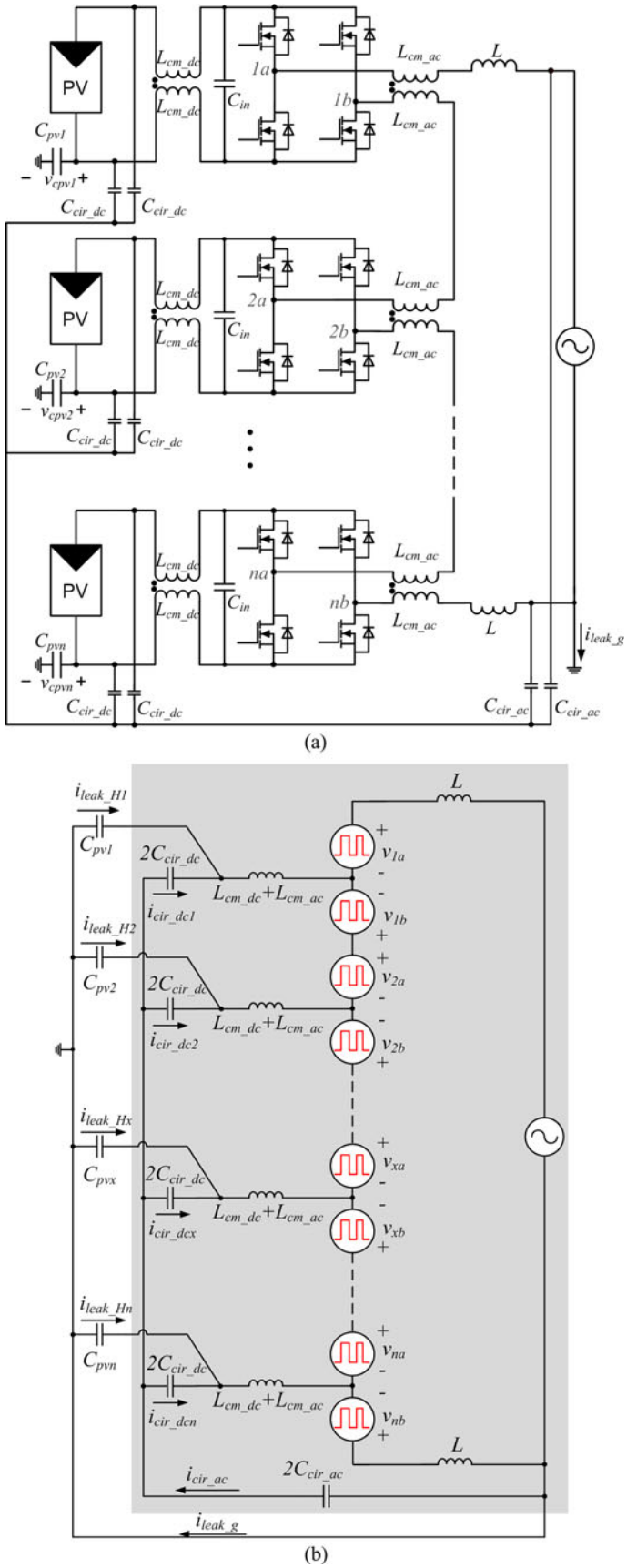


Fig. 13. Proposed leakage current suppression solution 2: (a) circuit diagram and (b) equivalent circuit.

The above (5)–(7) are easy to be implemented in computer languages for filter design. However, it is difficult to envision a simple circuit from the equations to understand the principle more straightforward. Since $L_{cm\_dc} + L_{cm\_ac}$ will dominate the impedance of the leakage current paths at the frequencies of the carrier harmonics, we approximately assume that $\frac{1}{i-1}Z + 2Z_{cir\_ac} + Z_L \approx \frac{1}{i-1}Z$ and $\frac{1}{n-i}Z + 2Z_{cir\_ac} + Z_L \approx \frac{1}{n-i}Z$ in (6). Consequently, (6) can be simplified to

$$i_{cir\_dcx} = \frac{\sum_{i=1}^{x-1}(v_{ia} - v_{ib}) + \sum_{i=x+1}^{n}(v_{ib} - v_{ia}) + (v_{xa} + v_{xb})}{2Z + 2nZ_{cir\_ac} + nZ_L}. \tag{8}$$

Equation (8) stands for an equivalent circuit composed of a voltage source connected with an LC circuit in series, which is similar to the one given in Fig. 5. The only different is that the LC circuit is replaced by $2Z + 2nZ_{cir\_ac} + nZ_L$. With the simplified model, we can expect that the switching-frequency noises in i_{cir_dcx} and i_{cir_ac} could be limited by designing the resonant frequency of $2Z + 2nZ_{cir\_ac} + nZ_L$ lower than the switching frequency. The simplification used in (8) is fair for understanding the principle, but it is not accurate enough because the value of Z_L could be comparable to the impedance of $L_{cm\_dc} + L_{cm\_ac}$ in applications where large C_{cir_dc} and C_{cir_ac} are used. More accurate design of the suppression filters needs to refer (5)–(7).

The application of the solution 2 is limited when the device switching frequency drops below around 1.5 kHz. This is because that if the resonant frequency is designed below the switching frequency, it may be very close to the frequencies of the baseband harmonics in v_{ia} and v_{ib}. In such a case, the internal circulating circuit could be excited by the baseband harmonics in v_{ia} and v_{ib}, and large circulating current will be generated in the circuit.

C. Application Example: H-Bridge-Based CMI With 10-kHz Switching Frequency

In order to investigate the performance of the second leakage current suppression method, it is applied in a single-phase PV system consisted of two cascaded H-bridge inverters. The system diagram is provided in Fig. 14 where each inverter module is rated at 500 W with 90–120 V input voltage range. The device switching frequency is 10 kHz and the sine-triangular PWM modulation strategy is used for each module. The carrier waveforms are phase shifted to minimize the total output harmonics. Resistive load $R_{\rm load} = 50\ \Omega$ is used in the study. The inverter total output voltage is 120Vrms and the line inductor is $L = 2$ mH.

1) Filter Design: The calculated leakage current results derived from (5)–(7) under various values of parasitic capacitors and $L_{cm\_dc} + L_{cm\_ac}$ are shown in Fig. 15, where C_{cir_dc} and C_{cir_ac} are fixed at 5 and 10 μF, respectively. The fundamental-frequency leakage currents are also included in the calculation. The design results show that the RMS values of $i_{\rm leak\_H1}$ and $i_{\rm leak\_g}$ both increase with the increased parasitic capacitance. It is different from the design results of the leakage current suppression solution 1. And this can be explained based on (5). The term $\frac{i_{cir\_dcx}}{2C_{cir\_dc}} + \frac{i_{cir\_ac}}{2C_{cir\_ac}}$ in (5) will be nearly constant once the filter parameters are determined. Therefore, the increase of

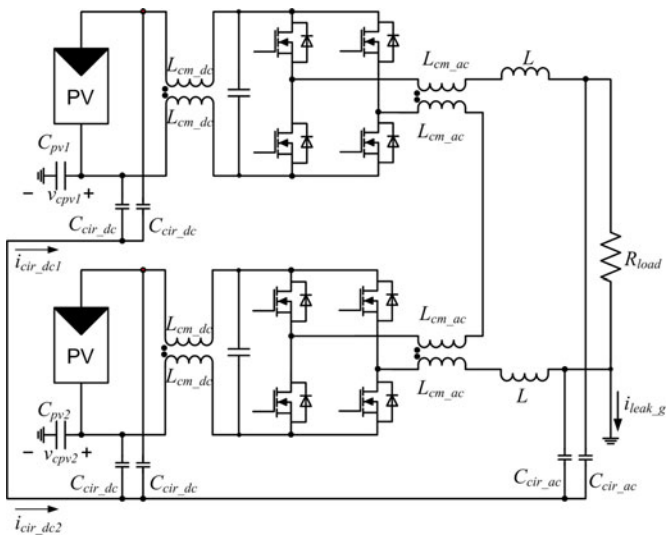


Fig. 14. System diagram of a PV system composed of two cascaded H-bridge inverters with leakage current suppression solution 2.

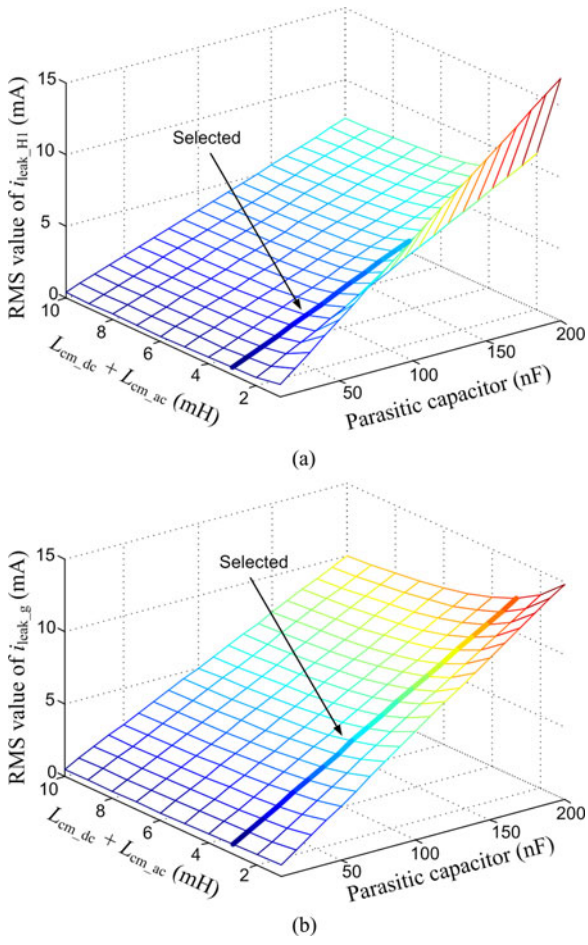


Fig. 15. Design results for the PV system with leakage current suppression solution 2: (a) $i_{\rm leak\_H1}$ and (b) $i_{\rm leak\_g}$.

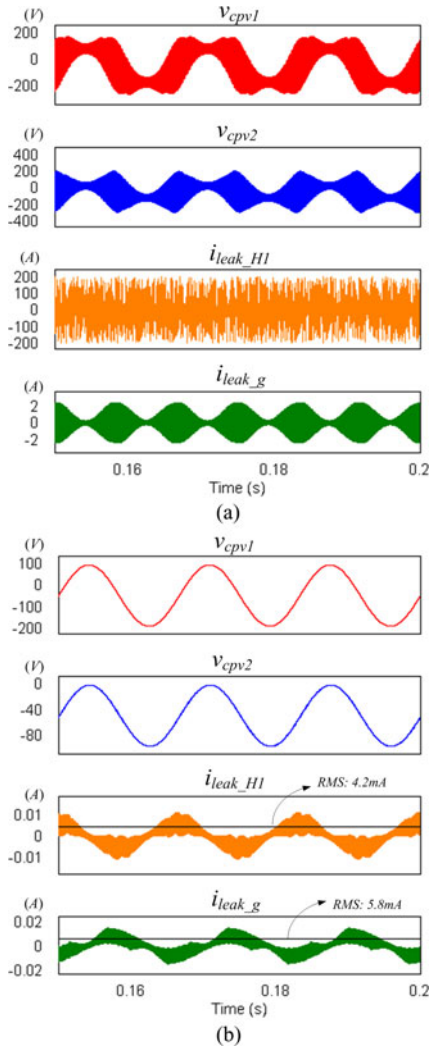


Fig. 16. Simulation waveforms of the PV system consisted of two cascaded H-bridge inverters: (a) without leakage current suppression 2 and (b) with leakage current suppression solution 2.

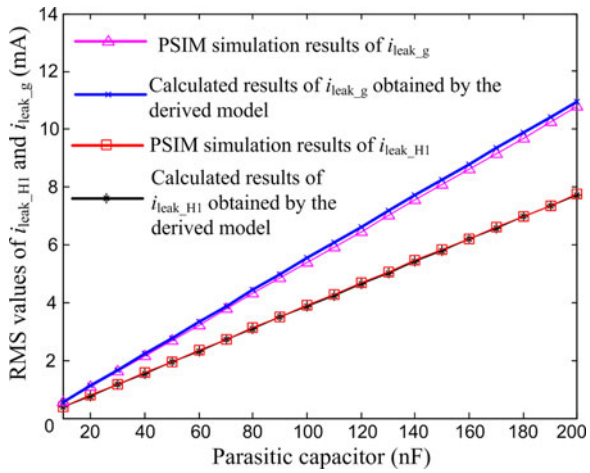


Fig. 17. Comparison of the PSIM simulation and calculated results of i_{leak_H1} and i_{leak_g} for the H-bridge-based PV CMI.

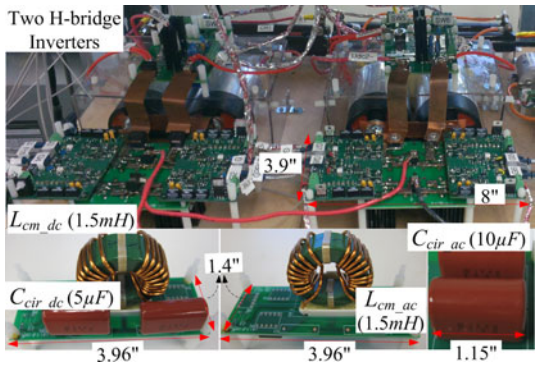


Fig. 18. Photograph of the two cascaded H-bridge inverter modules built in the laboratory.

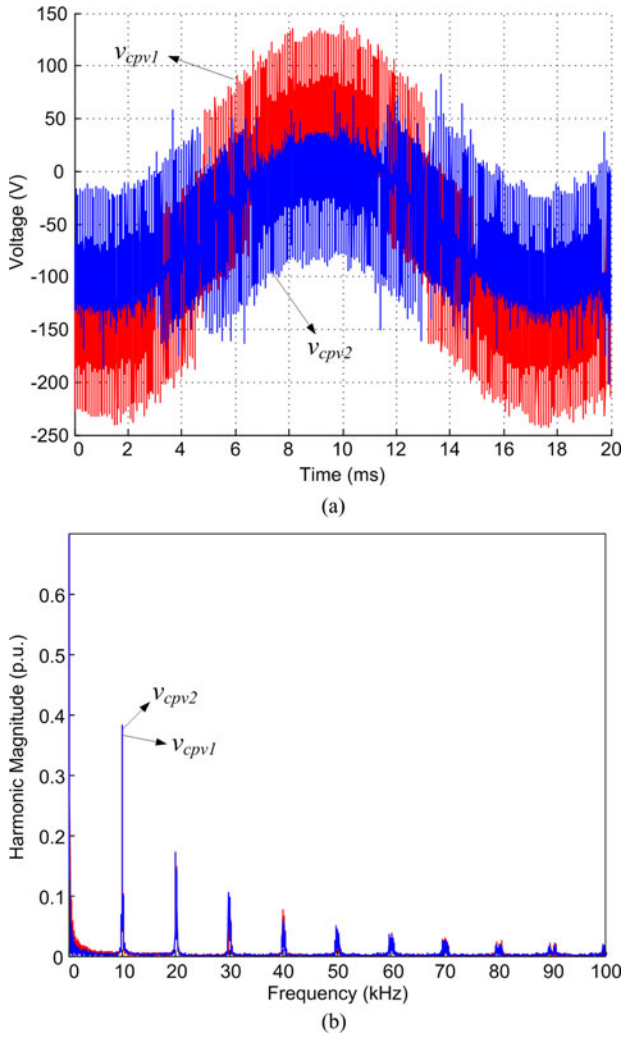


Fig. 19. Experimental results without leakage current suppression 2: (a) voltage across the parasitic capacitors and (b) the corresponding spectrums.

C_{pvx} would raise the leakage current value linearly. In [39], it is mentioned that the parasitic capacitance could raise up to 50–150 nF/kW. Thus, 3 mH of $L_{cm\_\mathrm{dc}} + L_{cm\_\mathrm{ac}}$ is used in the final design according to Fig. 15.

2) Simulation Verifications: In this simulation study, the input voltages of the two cascaded modules were 100 V and the

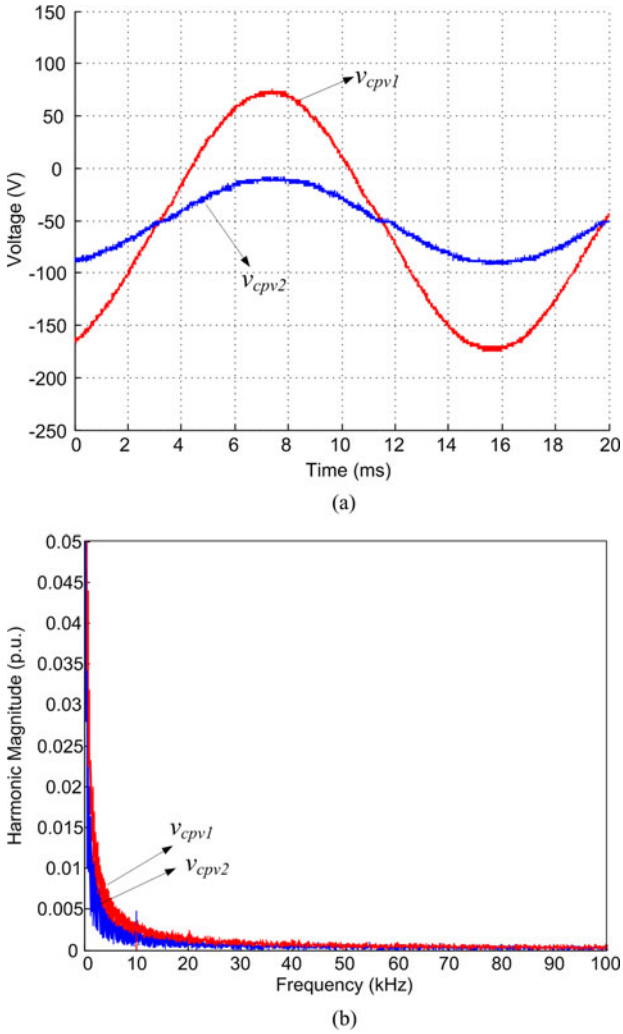


Fig. 20. Experimental results with leakage current suppression solution 2, *Cpv1* = 100 nF and *Cpv2* = 10 nF: (a) voltage across the parasitic capacitors and (b) the corresponding spectrums.

two parasitic capacitors were both 100 nF. The parameters of the added filters were obtained from the above design process. The simulation results of the system with and without leakage current suppression are provided in Fig. 16(a) and (b), respectively. It is clearly seen in Fig. 16(a) that there were a lot of carrier harmonics in v_{cpv1} and v_{cpv2} which induced huge leakage currents in the circuit. v_{cpv1} and v_{cpv2} contained around 0.38 pu 10-kHz harmonics. i_{leak_H1} was pulsewise current due to the capacitive intermodule leakage current loop. When the leakage current suppression was applied, the high-frequency noises in C_{pv1} and C_{pv2} were significantly reduced. The 10-kHz harmonics were decreased to 0.0044 pu. Therefore, i_{leak_H1} and i_{leak_g} can be reduced to 4.2 and 5.8 mA, respectively, which were below the standard requirement.

More simulation results of i_{leak_H1} and i_{leak_g} with different parasitic capacitor values are provided and compared with the calculated results in Fig. 17. The consistence between the PSIM simulation and calculated results verified the correctness of the derived model in (5)–(7).

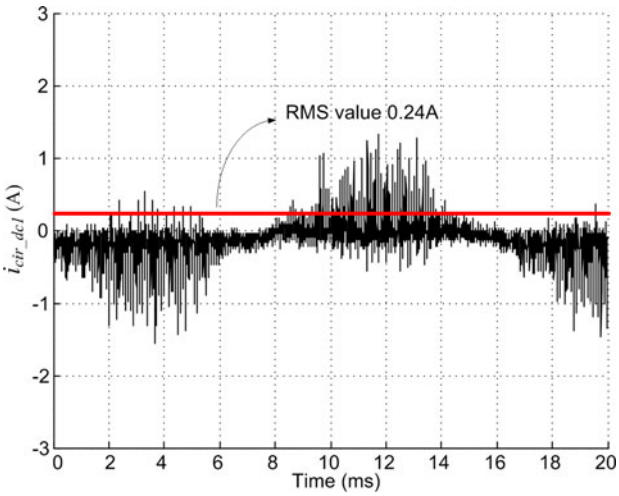


Fig. 21. Measured waveform and the RMS value of i_{cir_dc1}.

3) Experimental Verifications: The above system is built in the laboratory to validate the performance of the proposed method 2. The prototype picture is shown in Fig. 18. The parameters of the inverter module are the same as in the simulation. C_{pv1} and C_{pv2} were chosen to be different, $C_{pv1} = 100$ nF and $C_{pv2} = 10$ nF. Fig. 19 shows the measured waveforms and the spectrums of v_{cpv1} and v_{cpv2} without the suppression filters added in the system. It is seen that v_{cpv1} and v_{cpv2} contained around 0.38 pu 10 kHz and 0.17 pu 20 kHz harmonics. When the leakage current suppression was applied, the 10 and 20 kHz harmonics in both v_{cpv1} and v_{cpv2} were attenuated to very low level as shown in Fig. 20, specifically around 0.0047 and 0.0024 pu. The experimental results were consistent with the simulation. Unlike the first method, the value of the parasitic capacitor had minor effect on harmonic attenuation in v_{cpv1} and v_{cpv2} due to the much larger C_{cir_dc} and C_{cir_ac}. Since the high-frequency components in C_{pv1} and C_{pv2} were almost eliminated, the leakage currents would be mainly the low-frequency components with small values.

Because the inductance of the CM chokes can be reduced by choosing larger C_{cir_dc} and C_{cir_ac}, the internal circulating current could increase accordingly and the associated additional power loss becomes a concern. Therefore, i_{cir_dc1} was measured and the waveform is shown in Fig. 21. The RMS value of i_{cir_dc1} was 0.24 A, which was small compared with the rated current through the inverter circuit. Therefore, the internal circulating current in this design would not cause noticeable inverter efficiency drop.

V. Conclusion

This paper first analyzed the leakage current issue in PV CMI. The differences between the transformerless CMI and string inverter concerning the leakage current behaviors were discussed. The leakage current issue in PV CMI features the intermodule leakage current loops formed among the cascaded inverter modules. The intermodule leakage current loop exists even there is a transformer at the total output of the CMI and it prevents the existed string inverter leakage current suppression techniques

to be directly applied in the CMI. The filter-based method is considered suitable for addressing the leakage current issue in PV CMI. Two leakage current suppression solutions were proposed for the PV CMI by constructing LC filters in the leakage current paths to attenuate the high-frequency noises. The simplified leakage current analytical models were developed to demonstrate the principles and introduce the filter design criteria. Design examples were provided and the design results from the derived models were consistent with the simulation results. Hardware prototypes were built and tested to validate the effectiveness of the proposed leakage current solutions. Since the solution 1 utilizes the low-capacitance CM capacitors and parasitic capacitors as part of the LC filters, it is more suitable for the CMI operated at high switching frequency. The applicability of this solution at preselected switching frequency depends on the constraint on the filter size and cost. In solution 2, capacitors C_{cir_dc} and C_{cir_ac} are added to form LC filters with the CM chokes. This solution is applicable for CMI with device switching frequency above around 1.5 kHz. However, extra wires are needed to connect all the capacitors C_{cir_dc} and C_{cir_ac} to a common point and it would increase the balance of system cost. In conclusion, the solution 1 is preferred in PV CMI operated with high switching frequency. When the switching frequency decreases to a level that the size and cost of the CM chokes go beyond the design requirement, the solution 2 should be applied.

REFERENCES

[1] F. Z. Peng and J. S. Lai, "Multilevel cascade voltage source inverter with separate dc sources," U.S. Patent 5 642 275, Jun. 24, 1997.

[2] L. M. Tolbert and F. Z. Peng, "Multilevel converters as a utility interface for renewable energy systems," in *Proc. IEEE Power Eng. Soc. Summer Meet.*, Jul. 15–20, 2000, pp. 1271–1274.

[3] M. Calais and V. Agelidis, "Multilevel converters for single-phase grid connected photovoltaic systems—An overview," in *Proc. IEEE Int. Symp. Ind. Electron.*, Jul. 1998, pp. 224–229.

[4] L. Liu, H. Li, and Y. Xue, "A coordinated active and reactive power control strategy for grid-connected cascaded photovoltaic (PV) system in high voltage high power applications," in *Proc. IEEE App. Power Electron. Conf.*, Mar. 17–21, 2013, pp. 1301–1308.

[5] S. Essakiappan, H. S. Krishnamoorthy, P. Enjeti, R. S. Balog, and S. Ahmed, "Independent control of series connected utility scale multilevel photovoltaic inverters," in *Proc. IEEE Energy Convers. Congr. Expo.*, Sep. 15–20, 2012, pp. 1760–1766.

[6] S. Rivera, S. Kouro, B. Wu, J. I. Leon, J. Rodriguez, and L. G. Franquelo, "Cascaded H-bridge multilevel converter multistring topology for large scale photovoltaic systems," in *Proc. IEEE Int. Symp. Ind. Electron.*, Jun. 27–30, 2011, pp. 27–30.

[7] E. Villanueva, P. Correa, J. Rodriguez, and M. Pacas, "Control of a single-phase cascaded H-bridge multilevel inverter for grid-connected photovoltaic systems," *IEEE Trans. Ind. Electron.*, vol. 56, no. 11, pp. 4399–4406, Nov. 2009.

[8] F. Filho, Y. Cao, and L. M. Tolbert, "11-Level cascaded H-bridge grid-tied inverter interface with solar panels," in *Proc. IEEE App. Power Electron. Conf.*, Feb. 21–25, 2010, pp. 968–972.

[9] B. Xiao, F. Filho, and L. M. Tolbert, "Single-phase cascaded H-bridge multilevel inverter with nonactive power compensation for grid-connected photovoltaic generators," in *Proc. IEEE Energy Convers. Congr. Expo.*, Sep. 17–22, 2011, pp. 2733–2737.

[10] S. A. Khajehoddin, A. Bakhshai, and P. Jain, "The application of the cascaded multilevel converters in grid connected photovoltaic systems," in *Proc. IEEE Canada Elect. Power Conf.*, Oct. 25–26, 2007, pp. 296–301.

[11] O. Alonso, P. Sanchis, E. Gubia, and L. Marroyo, "Cascaded H-bridge multilevel converter for grid connected photovoltaic generators with independent maximum power point tracking of each solar array," in *Proc. IEEE Power Electron. Spec. Conf.*, Jun. 15–19, 2003, pp. 731–735.

[12] C. Cecati, F. Ciancetta, and P. Siano, "A multilevel inverter for photovoltaic systems with fuzzy logic control," *IEEE Trans. Ind. Electron.*, vol. 57, no. 12, pp. 4115–4125, Dec. 2010.

[13] M. Calais, V. G. Agelidis, and M. S. Dymond, "A cascaded inverter for transformerless single-phase grid-connected photovoltaic systems," *Renewable Energy*, vol. 22, no. 1, pp. 255–262, Jan. 2001.

[14] J. J. Negroni, F. Guinjoan, C. Meza, D. Biel, and P. Sanchis, "Energy-sampled data modeling of a cascade H-bridge multilevel converter for grid-connected PV systems," in *Proc. IEEE Int. Power Electron. Congr.*, Oct. 16–18, 2006, pp. 1–6.

[15] G. Brando, A. Dannier, and R. Rizzo, "A sensorless control of H-bridge multilevel converter for maximum power point tracking in grid connected photovoltaic systems," in *Proc. IEEE Int. Conf. Clean Elect. Power*, May 21–23, 2007, pp. 789–794.

[16] X. Lu, K. Sun, Y. Ma, L. Huang, and S. Igarashi, "High efficiency hybrid cascade inverter for photovoltaic generation," in *Proc. IEEE TENCON*, Jan. 23–26, 2009, pp. 1–6.

[17] L. Liu, H. Li, Z. Wu, and Y. Zhou, "A cascaded photovoltaic system integrating segmented energy storages with self-regulating power allocation control and wide range reactive power compensation," *IEEE Trans. Power Electron.*, vol. 26, no. 12, pp. 3545–3559, Dec. 2011.

[18] Y. Zhou, L. Liu, and H. Li, "A high-performance photovoltaic module-integrated converter (MIC) based on cascaded quasi-Z-source inverters (qZSI) using eGaN FETs," *IEEE Trans. Power Electron.*, vol. 28, no. 6, pp. 2727–2738, Jun. 2013.

[19] L. Liu, H. Li, Y. Zhao, X. He, and Z. J. Shen, "1 MHz cascaded Z-source inverters for scalable grid-interactive photovoltaic (PV) applications using GaN device," in *Proc. IEEE Energy Convers. Congr. Expo.*, Sep. 17–22, 2011, pp. 2738–2745.

[20] D. Sun, B. Ge, F. Z. Peng, A. R. Haitham, D. Bi, and Y. Liu, "A new grid-connected PV system based on cascaded H-bridge quasi-Z source inverter," in *Proc. IEEE Int. Symp. Ind. Electron.*, May 28–31, 2012, pp. 951–956.

[21] Y. Liu, B. Ge, A. R. Haitham, and F. Z. Peng, "A modular multilevel space vector modulation for photovoltaic quasi-Z-source cascade multilevel inverter," in *Proc. IEEE App. Power Electron. Conf.*, Mar. 17–21, 2013, pp. 714–718.

[22] E. Gubia, P. Sanchis, A. Ursúa, J. Lopez, and L. Marroyo, "Ground currents in single-phase transformerless photovoltaic systems," *Prog. Photovolt.: Res. Appl.*, vol. 15, no. 7, pp. 629–650, Nov. 2007.

[23] H. Xiao and S. Xie, "Leakage current analytical model and application in single-phase transformerless photovoltaic grid-connected inverter," *IEEE Trans. Electromagn. Compat.*, vol. 52, no. 4, pp. 902–913, Nov. 2010.

[24] M. C. Poliseno, R. A. Mastromauro, and M. Liserre, "Transformer-less photovoltaic (PV) inverters: A critical comparison," in *Proc. IEEE Energy Convers. Congr. Expo.*, Sep. 15–20, 2012, pp. 3438–3445.

[25] B. Yang, W. Li, Y. Gu, W. Cui, and X. He, "Improved transformerless inverter with common-mode leakage current elimination for a photovoltaic grid-connected power system," *IEEE Trans. Power Electron.*, vol. 27, no. 2, pp. 752–762, Feb. 2012.

[26] D. Dong, F. Luo, D. Boroyevich, and P. Mattavelli, "Leakage current reduction in a single-phase bidirectional ac–dc full-bridge inverter," *IEEE Trans. Power Electron.*, vol. 27, no. 10, pp. 4281–4291, Oct. 2012.

[27] Y. Koyama, J. Tsuda, and H. Mochikawa, "Grid-tie inverter," U.S. Patent 2012/0275201 A1, Jul. 12, 2012.

[28] D. Dong, F. Luo, X. Zhang, D. Boroyevich, and P. Mattavelli, "Grid-interface bidirectional converter for residential dc distribution systems—part 2: ac and dc interface design with passive components minimization," *IEEE Trans. Power Electron.*, vol. 28, no. 4, pp. 1667–1679, Apr. 2013.

[29] A. K. Gupta and A. M. Khambadkone, "A space vector modulation scheme to reduce common mode voltage for cascaded multilevel inverters," *IEEE Trans. Power Electron.*, vol. 22, no. 5, pp. 1672–1681, Sep. 2007.

[30] D. A. Rendusara, E. Cengelci, P. N. Enjeti, V. R. Stefanovic, and J. W. Gray, "Analysis of common mode voltage-"neutral shift" in medium voltage PWM adjustable speed drive (MV-ASD) systems," *IEEE Trans. Power Electron.*, vol. 15, no. 6, pp. 1124–1133, Nov. 2000.

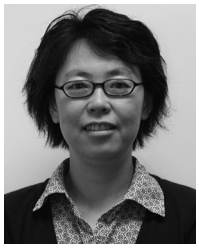
[31] R. Lai, M. H. Todorovic, and J. Sabate, "Analysis and suppression of a common mode resonance in the cascaded H-bridge multilevel inverter," in *Proc. IEEE Energy Convers. Congr. Expo.*, Sep. 12–16, 2010, pp. 4564–4568.

[32] Z. Ye, D. Boroyevich, J. Choi, and F. C. Lee, "Control of circulating current in two parallel three-phase boost rectifier," *IEEE Trans. Power Electron.*, vol. 17, no. 5, pp. 609–615, Sep. 2002.

[33] Y. Liao, H. Chen, and H. Cheng, "Common mode and differential mode circulating-current control in paralleled single-phase boost rectifiers," in *Proc. IEEE App. Power Electron. Conf.*, Mar. 17–21, 2013, pp. 361–367.
[34] D. Holmes and T. Lipo, "Carrier-based PWM of multilevel inverters," in *Pulse Width Modulation for Power Converters: Principles and Practice*. Hoboken, NJ, USA: Wiley-IEEE Press, 2003, pp. 95–153.
[35] J. Strydom and A. Lidow. (2011, Mar.). Driving eGaN transistors for maximum performance. [Online]. Available: http://www.digikey.com/Web%20Export/Supplier%20Content/EfficientPowerConversion_917/PDF/EPC_Driving_eGaN_Transistors.pdf?redirected=1
[36] T. Kerekes, R. Teodorescu, P. Rodriguez, G. Vazquez, and E. Aldabas, "A new high-efficiency single-phase transformerless PV inverter topology," *IEEE Trans. Ind. Electron.*, vol. 58, no. 1, pp. 184–191, Jan. 2011.
[37] *Automatic Disconnection Device Between a Generator and the Public Low-Voltage Grid*, Standard DIN V VDE V 0126-1-1, 2006.
[38] F. Luo, S. Wang, F. Wang, D. Boroyevich, N. Gazel, K. Yong, and A. C. Baisden, "Analysis of CM volt-second influence on CM inductor saturation and design for input EMI filters in three-phase dc-fed motor drive systems," *IEEE Trans. Ind. Electron.*, vol. 25, no. 7, pp. 1905–1914, Jul. 2010.
[39] T. Kerekes, R. Teodorescu, and U. Borup, "Transformerless photovoltaic inverters connected to the grid," in *Proc. IEEE App. Power Electron. Conf.*, Feb. 25–Mar. 1, 2007, pp. 1733–1737.

Yan Zhou (S'10) received the B.S. and M.S. degrees in electrical engineering from Huazhong University of Science and Technology, Wuhan, Hubei, China, in 2007 and 2009, respectively. He is currently working toward the Ph.D. degree in the Department of Electrical and Computer Engineering, Florida State University, Tallahassee, FL, USA.

His research interests include grid-connected PV system control, PV microinverter, GaN FETs application, and high-PV penetration integration issues.



Hui Li (S'97–M'00–SM'01) received the B.S. and M.S. degrees in electrical engineering from Huazhong University of Science and Technology, Wuhan, Hubei, China, in 1992 and 1995, respectively, and the Ph.D. degree in electrical engineering from the University of Tennessee, Knoxville, TN, USA, in 2000.

She is currently a Professor in the Electrical and Computer Engineering Department, Florida A&M University–Florida State University College of Engineering, Tallahassee, FL, USA. Her research interests include bidirectional dc–dc converters, cascaded multilevel inverters, and power electronics application in hybrid electric vehicles.