Modeling, Control, and Implementation of DC–DC Converters for Variable Frequency Operation

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***Abstract*—In this paper, novel small-signal averaged models for dc–dc converters operating at variable switching frequency are derived. This is achieved by separately considering the on-time and the off-time of the switching period. The derivation is shown in detail for a synchronous buck converter and the model for a boost converter is also presented. The model for the buck converter is then used for the design of two digital feedback controllers, which exploit the additional insight in the converter dynamics. First, a digital multiloop PID controller is implemented, where the design is based on loop-shaping of the proposed frequency-domain transfer functions. And second, the design and the implementation of a digital LQG state-feedback controller, based on the proposed time-domain state-space model, is presented for the same converter topology. Experimental results are given for the digital multiloop PID controller integrated on an application-specified integrated circuit in a 0.13 μm CMOS technology, as well as for the state-feedback controller implemented on an FPGA. Tight output voltage regulation and an excellent dynamic performance is achieved, as the dynamics of the converter under variable frequency operation are considered during the design of both implementations.**

***Index Terms*—DC–DC converters, digital control, linear quadratic Gaussian regulator (LQG), state-space averaging (SSA), variable switching frequency operation.**

I. Introduction

In THE control of dc–dc converters, two control objectives are apparent: performance and efficiency. On the one hand, the research focus in the community has been put on the optimization of the conversion efficiency. For instance, the switching frequency can be reduced at low loads [1], or the control scheme could be switched between a constant on-time and a constant off-time control scheme depending on the load conditions [2]. On the other hand, a strong interest can be found in the optimization of the dynamic performance. As dc–dc converters are inherently variable structure systems, a control law based on the sliding mode theory appears to be an appealing choice [3], [4]. One of the most attractive properties of sliding-mode control (SMC) lies in the fact that it is based on a large-signal representation of the circuit, it has a simple design procedure, and it is robust in parameter variations [3], [5]. Following the trend of digital realizations, some of the strong points for SMC are weakened. With the limited resolution and bandwidth of digital implementations, the design of digital SMC systems with comparable performance as their analog counterparts is still an open research question [6].

Likewise, time-optimal control (TOC) has been introduced as the solution to achieve optimal transient behavior [7], [8]. In such a setup, typically, a nonlinear interrupt-based logic is added in parallel to a linear feedback loop [8] enforcing optimal responses when transient events are detected. The aforementioned strategies clearly lead the way toward optimal output voltage regulation. Up to now, SMC has shown to be most effective in high-bandwidth analog implementations [6]. For TOC, the interrupt-based add-ons imply the risk of instability due to, for instance, constantly changing load currents, as expected for supplies of microcontrollers and CPUs [9].

When a variation of the switching period is tolerable during converter operation, this additional degree of freedom offers the opportunity of tight (near optimum) voltage regulation. Nevertheless, to fully exploit the switching period modulation in terms of dynamic transient performance and to ensure stability in all conditions, accurate models, which cover the dynamics of the power conversion system under variable frequency operation, are needed. In contrast to the commonly-used approach of state-space averaging (SSA) [10], [11], a generalized SSA approach has been developed in [12], applied to boost converters in [13] and to buck converters in [14]. A frequency-selective averaging is applied such that the switching frequency appears in the dynamic system model. The derivations give an accurate model of the converter dynamics also for situations when the traditional small-ripple conditions are not satisfied, but yield a nonlinear time-varying system formulation. As classical [15], [16] as well as modern [17] control theories largely depend on a linearized representation of the system under exam, the resulting model is of limited interest for the targeted design objective.

In this paper, an alternative formulation of the SSA model is presented, which yields a linearized small-signal representation of the power conversion circuit, where the on-time, as well as the off-time of the pulse-width modulation (PWM) signal are treated as distinct control inputs. In this manner, one can study the dynamics under variable switching frequency operation. The correctness of the enhanced converter representation is proven by comparing simulation results to measured responses.

Two independent control systems have been designed and implemented to demonstrate the effectiveness of the proposed

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models. The first architecture is a digital multiloop proportional-integral-derivative (PID) controller, based on loop-shaping of frequency-domain transfer functions (TFs). Both the on-time and the off-time are modulated by the controller, yielding a variable frequency operation. A similar multiloop PID controller has been proposed by the authors in [18] and experimental results have been presented in [19], where in the previous publications, the switching period has been directly introduced as an additional control input. In the current study, a more flexible and generalized approach is presented, with the on-time and the off-time of the switching period as control inputs. Thus, responses to a constant on-time, a constant off-time, as well as a varying on-time and off-time can be studied. Additionally, a second architecture which was not presented previously, namely a state-feedback controller based on a linear quadratic Gaussian regulator (LQG) design, is proposed. In contrast to recent implementations [20], [21], a digital linear quadratic regulator (LQR), including a Kalman state estimation, is implemented. Again, both the on-time and the off-time are modulated. The implementations have the goal, as dictated by the time optimal approaches, to boost the response during transient events. In contrast to approaches presented on TOC in the literature [7], [8], [22], in the proposed architectures, no switch between different controllers (e.g., only active in steady state or during transients) is implemented. The dominant control is always active, and transient responses are boosted by altering the fundamental switching frequency of the converter. Thus, no additional transients or risks of instability due to such abrupt switches between different control strategies are present. To demonstrate the accuracy of the models, a buck converter for point-of-load (PoL) applications has been implemented. In such a converter, the parasitic equivalent series inductance (ESL) of the output capacitor plays a significant role and can not be neglected in the averaged model [23]. We account for this fact in the presented converter models.

This paper is organized as follows: in Section II the innovative small-signal models for dc–dc converters will be derived and subsequently applied to a synchronous buck and a boost converter in Section III. The derived system representation for the PoL buck converter is then used for the design of the control structures; the multiloop PID-based approach is described in Section IV and the state-feedback-based approach in Section V. In Section VI, the experimental results will be presented and the paper concludes with Section VII.

Notation: Bold face variables ($\mathbf{a}, \mathbf{b}, \mathbf{A}, \mathbf{B}, \ldots$) indicate vectors or matrices of a specified dimension. Capital letters denote large-signal quantities, a hat $\hat{}$ above a symbol designates small-signal quantities and lower case letters indicate time-varying quantities. We further use $\mathbb{R}$ to denote the set of real numbers, $\mathbb{C}$ to denote the set of complex numbers, $\mathbf{I}$ to denote the identity matrix and $(\cdot)^T$ to denote transposition. To distinguish between discrete-time (DT) signals sampled at different rates, subscripts are introduced. The subscripts n and m indicate the corresponding sampling frequency f_{adc} and f_{sw} respectively. The sample and hold structure is schematically shown for the output voltage error signal e in Fig. 1.

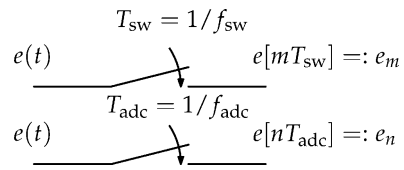

Fig. 1. Discrete-time signal representation.

II. Converter Modeling

A. State-Space Averaging for Modeling Variable Frequency Dynamics

In this section, a small-signal averaged and linearized model will be derived, in which the on-time $\hat{t}_{\mathrm{on}}$ and the off-time $\hat{t}_{\mathrm{off}}$ of the PWM signal driving the power stage of the dc–dc converter appear as additional inputs to the system. This is in contrast to the conventional SSA model, where the small-signal duty cycle $\hat{d}$ is the only control variable. The on-time is defined as the time period during which the binary PWM signal is "H", and the off-time is defined as the period of time during which the PWM signal is "L". Accordingly, for a synchronous buck converter (c.f. Fig. 2) in continuous conduction mode (CCM), during the on-time the high-side switch S_1 is conducting and the low-side switch S_2 is open. Whereas during the off-time, the high-side switch S_1 is open and the low-side switch S_2 is conducting. Similar considerations are valid for a boost converter. The relation between duty cycle, on-time, off-time, and switching period in equilibrium is given by

$$D = \frac{T_{\mathrm{on}}}{T_{\mathrm{sw}}} = \frac{T_{\mathrm{on}}}{T_{\mathrm{on}} + T_{\mathrm{off}}},\ D' = (1 - D). \tag{1}$$

Thus, a variation of the duty cycle corresponds to a variation of the on-time of the switching cycle, when the switching period T_{sw} is assumed to be constant: $d(t) = \frac{t_{\mathrm{on}}(t)}{T_{\mathrm{sw}}}$. When, additionally, a variation of the switching period T_{sw} is allowed, the following equation is readily obtained:

$$d(t) = \frac{t_{\mathrm{on}}(t)}{t_{\mathrm{sw}}(t)} \tag{2}$$

$$= \frac{t_{\mathrm{on}}(t)}{t_{\mathrm{on}}(t) + t_{\mathrm{off}}(t)}. \tag{3}$$

As a consequence, 2-DOF are introduced, the on-time t_{on} and the off-time t_{off}, respectively.

The state-space models, as considered in this study, are defined as

$$\frac{\mathrm{d}\mathbf{x}(t)}{\mathrm{d}t} = \mathbf{A}\mathbf{x}(t) + \mathbf{B}\mathbf{u}(t) \tag{4}$$

$$\mathbf{y}(t) = \mathbf{C}\mathbf{x}(t) + \mathbf{D}\mathbf{u}(t) \tag{5}$$

where $\mathbf{x} \in \mathbb{R}^{\mathrm{n}\times 1}$, $\mathbf{u} \in \mathbb{R}^{\mathrm{m}\times 1}$, and $\mathbf{y} \in \mathbb{R}^{\mathrm{p}\times 1}$ define the states, inputs and outputs of the system, whereas $\mathbf{A} \in \mathbb{R}^{\mathrm{n}\times\mathrm{n}}, \mathbf{B} \in \mathbb{R}^{\mathrm{n}\times\mathrm{m}}, \mathbf{C} \in \mathbb{R}^{\mathrm{p}\times\mathrm{n}}, \mathbf{D} \in \mathbb{R}^{\mathrm{p}\times\mathrm{m}}$ represent the dynamic, input, output, and direct-transmission matrices, respectively, such that n, m, and p give the number of states, inputs, and outputs, respectively, of the linear time-invariant system representation. A set of matrices $(\mathbf{A}_i, \mathbf{B}_i, \mathbf{C}_i, \mathbf{D}_i)$ describing the system for each

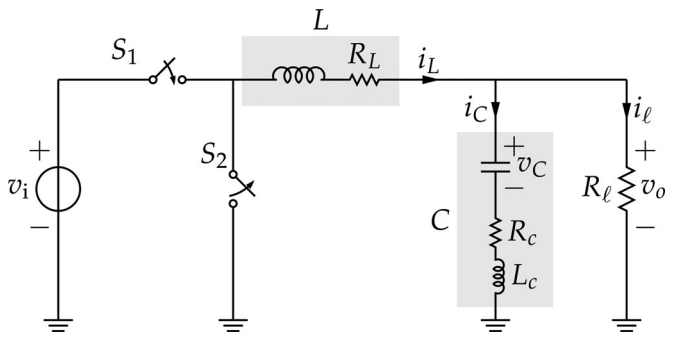

Fig. 2. Schematic view of a synchronous buck converter.

switch configuration of the dc–dc converter can now be found, such that $i = 1$ for the configuration during the on-time, whereas $i = 2$ during the off-time. In contrast to [18] and [19], where (2) has been used as the starting point, here, (3) is substituted in the derivation of the averaged model, such that a more generalized model is acquired. The state-space equations representing the averaged system are then given by

$$\frac{\mathrm{d}\mathbf{x}}{\mathrm{d}t} = \left((\mathbf{A}_1 - \mathbf{A}_2)\frac{t_{\mathrm{on}}}{t_{\mathrm{on}} + t_{\mathrm{off}}} + \mathbf{A}_2\right)\mathbf{x} + \left((\mathbf{B}_1 - \mathbf{B}_2)\frac{t_{\mathrm{on}}}{t_{\mathrm{on}} + t_{\mathrm{off}}} + \mathbf{B}_2\right)\mathbf{u}. \tag{6}$$

Considering small perturbations around the equilibrium point, the states $\mathbf{x}$, input signals $\mathbf{u}$, and the control variables t_{on} and t_{off} are given by

$$\mathbf{x} = \mathbf{X} + \hat{\mathbf{x}}, \quad \mathbf{u} = \mathbf{U} + \hat{\mathbf{u}}$$
$$t_{\mathrm{on}} = T_{\mathrm{on}} + \hat{t}_{\mathrm{on}}, \quad t_{\mathrm{off}} = T_{\mathrm{off}} + \hat{t}_{\mathrm{off}}. \tag{7}$$

Accordingly, the state equation is given by

$$\frac{\mathrm{d}\hat{\mathbf{x}}}{dt} = \left((\mathbf{A}_1 - \mathbf{A}_2)\frac{T_{\mathrm{on}} + \hat{t}_{\mathrm{on}}}{T_{\mathrm{on}} + \hat{t}_{\mathrm{on}} + T_{\mathrm{off}} + \hat{t}_{\mathrm{off}}} + \mathbf{A}_2\right)(\mathbf{X} + \hat{\mathbf{x}}) + \left((\mathbf{B}_1 - \mathbf{B}_2)\frac{T_{\mathrm{on}} + \hat{t}_{\mathrm{on}}}{T_{\mathrm{on}} + \hat{t}_{\mathrm{on}} + T_{\mathrm{off}} + \hat{t}_{\mathrm{off}}} + \mathbf{B}_2\right)(\mathbf{U} + \hat{\mathbf{u}}) \tag{8}$$

and the output equation is

$$\mathbf{Y} + \hat{\mathbf{y}} = \left((\mathbf{C}_1 - \mathbf{C}_2)\frac{T_{\mathrm{on}} + \hat{t}_{\mathrm{on}}}{T_{\mathrm{on}} + \hat{t}_{\mathrm{on}} + T_{\mathrm{off}} + \hat{t}_{\mathrm{off}}} + \mathbf{C}_2\right)(\mathbf{X} + \hat{\mathbf{x}}) + \left((\mathbf{D}_1 - \mathbf{D}_2)\frac{T_{\mathrm{on}} + \hat{t}_{\mathrm{on}}}{T_{\mathrm{on}} + \hat{t}_{\mathrm{on}} + T_{\mathrm{off}} + \hat{t}_{\mathrm{off}}} + \mathbf{D}_2\right)(\mathbf{U} + \hat{\mathbf{u}}). \tag{9}$$

Collecting the direct-current (dc) terms and substituting (1) yields the dc equations

$$\mathbf{0} = \mathbf{A}\mathbf{X} + \tilde{\mathbf{B}}\mathbf{U} \tag{10}$$
$$\mathbf{Y} = \mathbf{C}\mathbf{X} + \tilde{\mathbf{D}}\mathbf{U} \tag{11}$$

where the averaged matrices are given by

$$\mathbf{A} = D\mathbf{A}_1 + D'\mathbf{A}_2, \quad \tilde{\mathbf{B}} = D\mathbf{B}_1 + D'\mathbf{B}_2$$
$$\mathbf{C} = D\mathbf{C}_1 + D'\mathbf{C}_2, \quad \tilde{\mathbf{D}} = D\mathbf{D}_1 + D'\mathbf{D}_2. \tag{12}$$

The equilibrium dc components are $\mathbf{X}, \mathbf{U}, \mathbf{Y}$ and D, the equilibrium dc state, input and output vector, and the duty cycle, respectively. The equilibrium state and output vector can be found by solving (10) for $\mathbf{X}$ and (11) for $\mathbf{Y}$

$$\mathbf{X} = -\mathbf{A}^{-1}\tilde{\mathbf{B}}\mathbf{U} \tag{13}$$
$$\mathbf{Y} = (-\mathbf{C}\mathbf{A}^{-1}\tilde{\mathbf{B}} + \tilde{\mathbf{D}})\mathbf{U}. \tag{14}$$

Furthermore, the equilibrium on-time and off-time are given by

$$T_{\mathrm{on}} = DT_{\mathrm{sw}} \tag{15}$$
$$T_{\mathrm{off}} = T_{\mathrm{sw}} - T_{\mathrm{on}}. \tag{16}$$

Collecting the alternating-current (AC) components and linearizing the model by neglecting second-order terms, yields the state-space model

$$\frac{\mathrm{d}\hat{\mathbf{x}}}{\mathrm{d}t} = \mathbf{A}\hat{\mathbf{x}}(t) + \tilde{\mathbf{B}}\hat{\mathbf{u}} + \mathbf{b}_{\mathrm{ton}}\hat{t}_{\mathrm{on}} + \mathbf{b}_{\mathrm{toff}}\hat{t}_{\mathrm{off}} \tag{17}$$
$$\hat{\mathbf{y}}(t) = \mathbf{C}\hat{\mathbf{x}}(t) + \tilde{\mathbf{D}}\hat{\mathbf{u}} + \mathbf{d}_{\mathrm{ton}}\hat{t}_{\mathrm{on}} + \mathbf{d}_{\mathrm{toff}}\hat{t}_{\mathrm{off}}. \tag{18}$$

The column vectors $\mathbf{b}_{\mathrm{ton}} \in \mathbb{R}^{\mathrm{n}\times 1}, \mathbf{b}_{\mathrm{toff}} \in \mathbb{R}^{\mathrm{n}\times 1}$ and $\mathbf{d}_{\mathrm{ton}} \in \mathbb{R}^{\mathrm{p}\times 1}, \mathbf{d}_{\mathrm{toff}} \in \mathbb{R}^{\mathrm{p}\times 1}$, relating the new inputs $\hat{t}_{\mathrm{on}}$ and $\hat{t}_{\mathrm{off}}$ to the states and outputs, respectively, are found by linearizing (8) and (9), collecting the alternating-current (ac) terms and reordering the equations as in (17) and (18)

$$\mathbf{b}_{\mathrm{ton}} = (\mathbf{A}_1\mathbf{X} + \mathbf{B}_1\mathbf{U}) / (T_{\mathrm{on}} + T_{\mathrm{off}}) \tag{19}$$
$$\mathbf{b}_{\mathrm{toff}} = (\mathbf{A}_2\mathbf{X} + \mathbf{B}_2\mathbf{U}) / (T_{\mathrm{on}} + T_{\mathrm{off}}) \tag{20}$$

and

$$\mathbf{d}_{\mathrm{ton}} = (\mathbf{C}_1\mathbf{X} + \mathbf{D}_1\mathbf{U} - \mathbf{Y}) / (T_{\mathrm{on}} + T_{\mathrm{off}}) \tag{21}$$
$$\mathbf{d}_{\mathrm{toff}} = (\mathbf{C}_2\mathbf{X} + \mathbf{D}_2\mathbf{U} - \mathbf{Y}) / (T_{\mathrm{on}} + T_{\mathrm{off}}). \tag{22}$$

The resulting input and direct-transmission matrices are given by

$$\mathbf{B} = [\,\tilde{\mathbf{B}} \quad \mathbf{b}_{\mathrm{ton}} \quad \mathbf{b}_{\mathrm{toff}}\,] \tag{23}$$
$$\mathbf{D} = [\,\tilde{\mathbf{D}} \quad \mathbf{d}_{\mathrm{ton}} \quad \mathbf{d}_{\mathrm{toff}}\,]. \tag{24}$$

Accordingly, the state and output equation of the small-signal ac model follow as:

$$\frac{\mathrm{d}\hat{\mathbf{x}}}{\mathrm{d}t} = \mathbf{A}\hat{\mathbf{x}}(t) + \mathbf{B}\begin{bmatrix}\hat{\mathbf{u}}(t)\\ \hat{t}_{\mathrm{on}}(t)\\ \hat{t}_{\mathrm{off}}(t)\end{bmatrix} \tag{25}$$

$$\hat{\mathbf{y}}(t) = \mathbf{C}\hat{\mathbf{x}}(t) + \mathbf{D}\begin{bmatrix}\hat{\mathbf{u}}(t)\\ \hat{t}_{\mathrm{on}}(t)\\ \hat{t}_{\mathrm{off}}(t)\end{bmatrix}. \tag{26}$$

The quantities $\hat{\mathbf{x}}(t), \hat{\mathbf{y}}(t), \hat{\mathbf{u}}(t), \hat{t}_{\mathrm{on}}(t)$ and $\hat{t}_{\mathrm{off}}(t)$ are the small ac variations around the equilibrium (steady-state) solution, which is given by (13), (14) as well as by (15) and (16). The derived model treats the on-time and the off-time of the switching period separately. It can be considered as an enhancement of the

TABLE I
SSA/ESSA CONVERTER MODELS[1]

$\left(\begin{array}{c\|c}\mathbf{A} & \mathbf{B}\\ \hline \mathbf{C} & \mathbf{D}\end{array}\right)$	$\mathbf{x}$	$\mathbf{u}$	$\mathbf{y}$	
SSA model for a buck converter (neglecting ESL)				
$\left(\begin{array}{cc\|ccc} 0 & \frac{1}{C} & 0 & -\frac{1}{C} & 0 \\ -\frac{1}{L} & -\frac{R_\mathrm{p}}{L} & \frac{D}{L} & \frac{R_C}{L} & \frac{V_\mathrm{i}}{L} \\ \hline 1 & R_C & 0 & -R_C & 0 \end{array}\right)$	$\begin{bmatrix}\hat{v}_C \\ \hat{i}_L\end{bmatrix}$	$\begin{bmatrix}\hat{v}_\mathrm{i} \\ \hat{i}_\ell \\ \hat{d}\end{bmatrix}$	$\hat{v}_o$	(28)
ESSA model for a buck converter (neglecting ESL)				
$\left(\begin{array}{cc\|cccc} 0 & \frac{1}{C} & 0 & -\frac{1}{C} & 0 & 0 \\ -\frac{1}{L} & -\frac{R_\mathrm{p}}{L} & \frac{D}{L} & \frac{R_C}{L} & \frac{D'V_\mathrm{i}}{(T_\mathrm{on}+T_\mathrm{off})L} & -\frac{DV_\mathrm{i}}{(T_\mathrm{on}+T_\mathrm{off})L} \\ \hline 1 & R_C & 0 & -R_C & 0 & 0 \end{array}\right)$	$\begin{bmatrix}\hat{v}_C \\ \hat{i}_L\end{bmatrix}$	$\begin{bmatrix}\hat{v}_\mathrm{i} \\ \hat{i}_\ell \\ \hat{t}_\mathrm{on} \\ \hat{t}_\mathrm{off}\end{bmatrix}$	$\hat{v}_o$	(29)
ESSA model for a buck converter (including ESL)				
$\left(\begin{array}{ccc\|ccc} 0 & 0 & \frac{1}{C} & 0 & 0 & 0 \\ 0 & -\frac{R_\mathrm{p}}{L} & \frac{R_\ell}{L} & \frac{D}{L} & \frac{D'V_\mathrm{i}}{L(T_\mathrm{on}+T_\mathrm{off})} & -\frac{DV_\mathrm{i}}{L(T_\mathrm{on}+T_\mathrm{off})} \\ -\frac{1}{L_C} & \frac{R_\ell}{L_C} & -\frac{R_C+R_\ell}{L_C} & 0 & 0 & 0 \\ \hline 0 & R_\ell & -R_\ell & 0 & 0 & 0 \end{array}\right)$	$\begin{bmatrix}\hat{v}_C \\ \hat{i}_L \\ \hat{i}_\mathrm{C}\end{bmatrix}$	$\begin{bmatrix}\hat{v}_\mathrm{i} \\ \hat{t}_\mathrm{on} \\ \hat{t}_\mathrm{off}\end{bmatrix}$	$\hat{v}_o$	(30)
ESSA model for a boost converter				
$\left(\begin{array}{cc\|ccc} 0 & \frac{D'}{C} & 0 & -\frac{1}{C} & -\frac{I_\ell}{C(T_\mathrm{on}+T_\mathrm{off})} & \frac{D}{D'}\frac{I_\ell}{C(T_\mathrm{on}+T_\mathrm{off})} \\ -\frac{D'}{L} & -\frac{R_\mathrm{p}-DR_C}{L} & \frac{1}{L} & \frac{D'R_C}{L} & \frac{V_\mathrm{i}-\frac{1}{D'}I_\ell(R_\mathrm{on}+R_L)}{D'L(T_\mathrm{on}+T_\mathrm{off})} & -\frac{V_\mathrm{i}-\frac{D}{D'}I_\ell(R_\mathrm{on}+R_L)}{LT_\mathrm{off}} \\ \hline 1 & R_C D' & 0 & -R_C & -\frac{I_\ell R_C}{T_\mathrm{on}+T_\mathrm{off}} & \frac{D}{D'}\frac{I_\ell R_C}{T_\mathrm{on}+T_\mathrm{off}} \end{array}\right)$	$\begin{bmatrix}\hat{v}_C \\ \hat{i}_L\end{bmatrix}$	$\begin{bmatrix}\hat{v}_\mathrm{i} \\ \hat{i}_\ell \\ \hat{t}_\mathrm{on} \\ \hat{t}_\mathrm{off}\end{bmatrix}$	$\hat{v}_o$	(31)

[1] $R_\mathrm{p} = (R_\mathrm{on} + R_L + R_C)$.

conventional SSA model, and it will be denoted in the following as enhanced state-space averaged (ESSA) model.

B. Considerations on the Proposed Models

In the derived formulation, the input matrix is $\mathbf{B} \in \mathbb{R}^{\mathrm{n}\times(\mathrm{m}+2)}$, when the state-space formulation for each subinterval i of the converter has an input matrix of size $\mathbf{B}_i \in \mathbb{R}^{\mathrm{n}\times\mathrm{m}}$. By splitting the switching period of the PWM signal into the on-time and the off-time of the period, the input vector size is $m + 2$, compared to $m + 1$ in case of the traditional SSA approach (where solely the duty cycle is added as control input). Nevertheless, the input components (t_on and t_off) do not *independently* affect the state vector. This is intuitively clear and reflected in the resulting models, as

$$\mathrm{rank}(\mathbf{B}) \leq (\mathrm{m}+1) \tag{27}$$

i.e., $\mathbf{B}$ does not have full rank. This needs to be considered during the control system design and will be addressed in the next section, Section III-D.

Furthermore, the proposed models do not include the delay introduced by the pulse width modulation. Specific to the implemented pulse-width modulation scheme, the corresponding delay models need to be additionally considered. For instance, for a *continuous-time* pulse-width modulation scheme, the delay on the on-time and on the off-time would be given as $e^{sT_\mathrm{on}/2}$ and $e^{sT_\mathrm{off}/2}$, respectively [24]. For a *discrete-time* or digital pulse-width modulation scheme, denoted here as digital pulse-width modulation (DPWM), the delays would be modeled as $e^{-sT_\mathrm{on}/2}$ and $e^{-sT_\mathrm{off}/2}$, for the on-time and off-time, respectively, when a zero-order hold is used at the starting point of every switching cycle [25]. The specific delay models of the proposed DPWM scheme will be presented in Section III-F, when the DPWM architecture is discussed in detail.

III. APPLICATION OF THE ENHANCED SSA TO DC–DC CONVERTERS

The presented modeling approach can be applied to various dc–dc converter topologies (e.g., buck, boost, buck–boost, Ćuk, ...) by deriving the system matrices for the subintervals and solving (12) together with (19) to (22) and using the dc equations as given by (13) and (14).

The derivation of the proposed model will be given in detail for a synchronous buck converter for PoL applications in the next paragraph and the results, also for a boost converter, are summarized in Table I. In the table, (28) shows the conventional SSA model for a synchronous buck converter, whereas in (29) and (30), the proposed ESSA model has been applied to a buck converter without and with the ESL of the output capacitor, respectively. Note that in (29) the load current has been modeled as an explicit input to the system, whereas in (30), a resistive load R_ℓ has been included in the model in order to get a compact formulation. Finally, the averaged model for a boost converter is presented in (31).

A. ESSA Model for a Synchronous Buck Converter

The derivation of the ESSA model is based on the large-signal model representation for the individual switch configurations. For a synchronous buck converter operated in CCM, taking the parasitic ESL of the output capacitor into account, as shown in

Fig. 2, it is straightforward to find the system matrices for the subintervals.

When the high-side switch S_1 is ON and the low-side switch S_2 is OFF, the system is given by

$$\mathbf{A}_1 = \begin{bmatrix} 0 & 0 & \frac{1}{C} \\ 0 & -\frac{R_L + R_{\rm on} + R_\ell}{L} & \frac{R_\ell}{L} \\ -\frac{1}{L_C} & \frac{R_\ell}{L_C} & -\frac{R_C + R_\ell}{L_C} \end{bmatrix} \tag{32}$$

$$\mathbf{B}_1 = \begin{bmatrix} 0 & \frac{1}{L} & 0 \end{bmatrix}^T \tag{33}$$

$$\mathbf{c}_1^T = [\,0 \quad R_\ell \quad -R_\ell\,] \tag{34}$$

$$\mathbf{D}_1 = 0 \tag{35}$$

where the state vector $\mathbf{X} = [\,v_C, i_L, i_{\rm C}\,]^T$ consists of the voltage over the output capacitor, the current through the output inductor, as well as the current through the output capacitor, and the input and output to and from the system is $u = v_{\rm i}$ and $y = v_o$, respectively. Note that the current of the output capacitor is a state of the system representation, because the ESL of the capacitor is considered in the model. Therefore, $n = 3, m = 1$, and $p = 1$. The notation of the components is as shown in Fig. 2, and $R_{\rm on}$ models the on-resistance of the power MOSFET, which is assumed to be equal for all switches. When the high-side switch is open and the low-side switch is closed, again the same dynamic system as reported in (32) to (35) is obtained, but with the input voltage $v_{\rm i}$ disconnected

$$\mathbf{A}_2 = \mathbf{A}_1 \tag{36}$$

$$\mathbf{B}_2 = [\,0 \quad 0 \quad 0\,]^T \tag{37}$$

$$\mathbf{c}_2^T = \mathbf{c}_1^T \tag{38}$$

$$\mathbf{D}_2 = 0. \tag{39}$$

According to (13) and (14), the dc equations compute to

$$\mathbf{X} = \begin{bmatrix} V_C \\ I_L \\ I_{\rm C} \end{bmatrix} = \begin{bmatrix} DV_{\rm i}\frac{R_\ell}{R_{\rm s}} \\ DV_{\rm i}\frac{1}{R_{\rm s}} \\ 0 \end{bmatrix} \tag{40}$$

$$V_o = DV_{\rm i}\frac{R_\ell}{R_{\rm s}} \tag{41}$$

and $R_{\rm s} = R_{\rm on} + R_L + R_\ell$.

Solving (19) to (22) gives the weights for the considered inputs as

$$\mathrm{b}_{\rm ton} = \begin{bmatrix} 0 \\ \frac{D'V_{\rm i}}{L(T_{\rm on} + T_{\rm off})} \\ 0 \end{bmatrix}, \mathrm{b}_{\rm toff} = \begin{bmatrix} 0 \\ -\frac{DV_{\rm i}}{L(T_{\rm on} + T_{\rm off})} \\ 0 \end{bmatrix}$$

$$\mathrm{d}_{\rm ton} = \mathrm{d}_{\rm toff} = 0. \tag{42}$$

The novel ESSA system model is summarized in (30). The corresponding input-to-output relation of this model is then given by

$$\hat{v}_o = \mathbf{G}_{\rm s}(s) \begin{bmatrix} \hat{v}_{\rm i} \\ \hat{t}_{\rm on} \\ \hat{t}_{\rm off} \end{bmatrix} \tag{43}$$

with the transfer matrix given as

$$\begin{aligned} \mathbf{G}_{\rm s}(s) &= \mathbf{C}\,(s\mathbf{I} - \mathbf{A})^{-1}\,\mathbf{B} + \mathbf{D} \\ &= 1/\big(LL_CCs^3 + (L(R_C + R_\ell) + L_CR_{\rm s})Cs^2 + \cdots \\ &\quad + (L + (R_CR_{\rm s} + R_\ell(R_{\rm on} + R_L)))Cs + R_{\rm s}\big) \\ &\quad \cdot \begin{bmatrix} DR_\ell(L_CCs^2 + R_CCs + 1) \\ D'V_{\rm i}\frac{R_\ell(L_CCs^2 + R_CCs + 1)}{T_{\rm on} + T_{\rm off}} \\ -DV_{\rm i}\frac{R_\ell(L_CCs^2 + R_CCs + 1)}{T_{\rm on} + T_{\rm off}} \end{bmatrix}^T. \end{aligned} \tag{44}$$

D' is defined as in (1). The TF relating the off-time $\hat{t}_{\rm off}$ to the output voltage $\hat{v}_o$ is of particular interest for subsequent control tasks, as it describes the dynamic response to a step in the switching period.

B. Simulation-Based Validation of the Control-to-Output Frequency Responses

The actuating signals for the subsequent controller designs are $\hat{t}_{\rm on}$ and $\hat{t}_{\rm off}$. The transfer matrix in (44) describes the small-signal responses of the output voltage $\hat{v}_o$ to changes in these actuating signals. A simulation-based validation has been conducted to evaluate the accuracy of the analytically-derived TFs. This is done by measuring the frequency responses of an open-loop buck converter circuit. The circuit is driven by a DPWM to which the on-time and the off-time of the period can be separately given. The system is implemented in the commercial circuit simulator SimPowerSystems, which is available as a Toolbox for the MATLAB® scientific computation software. In Fig. 3, the measured responses are compared to the ones computed in (43) and (44). In Fig. 3(a), the frequency response of the TF from the on-time $\hat{t}_{\rm on}$ to the output voltage $\hat{v}_o$, $G_{\mathrm{s,t_{on}}}(s)|_{s=jw}$ with $G_{\mathrm{s,t_{on}}}(s) := \mathbf{G}_{\rm s}[2]$ is compared, whereas in Fig. 3(b), the frequency response of the TF from the off-time $\hat{t}_{\rm off}$ to the output voltage $\hat{v}_o$, $G_{\mathrm{s,t_{off}}}(s)|_{s=jw}$ with $G_{\mathrm{s,t_{off}}}(s) := \mathbf{G}_{\rm s}[3]$ is plotted. The symbol $\mathbf{G}_{\rm s}[i]$ shall address the ith column of $\mathbf{G}_{\rm s}(s)$. The delay of the DT pulse width modulator is modeled as given in Section II-B. The analytically derived models accurately predict the responses obtained by the circuit simulator.

C. Discrete-Time Representation of the Continuous-Time Models

The continuous-time (CT) system descriptions, as presented in Table I, can be translated to DT using a sample-and-hold structure with the appropriate update rate, i.e., with a frequency $f_{\rm s} = 1/T_{\rm s}$, such that the transition matrix $\mathbf{\Phi}$ and the input matrix

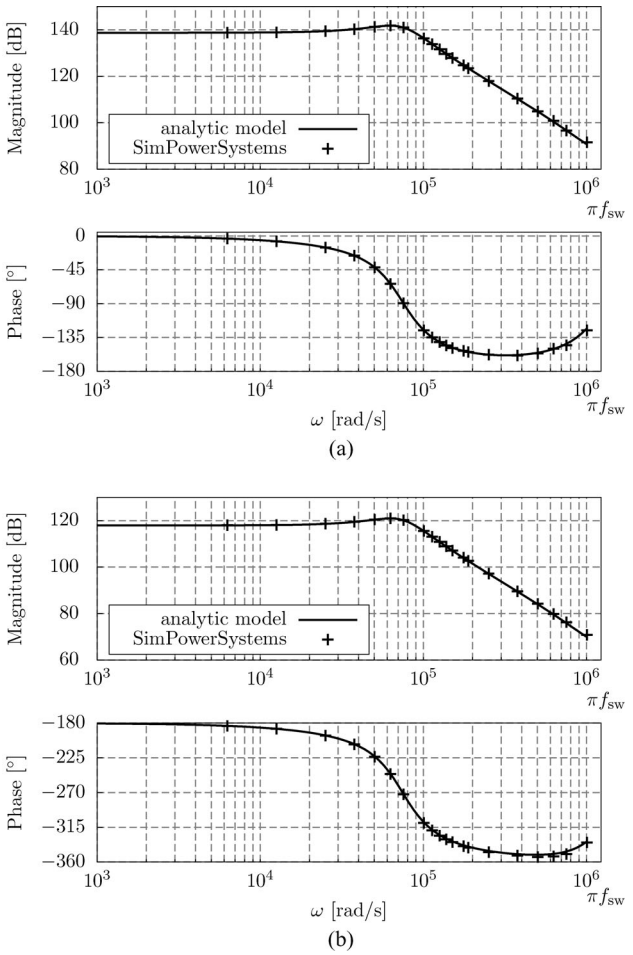

Fig. 3. Validation of the control-to-output frequency responses. The frequency responses predicted by the derived model are compared to a response obtained by a SimPowerSystems simulation. (a) Frequency response of the on-time TF $G_{\mathrm{s},\mathrm{t_{on}}}(j\omega)e^{-j\omega(T_{\mathrm{on}}/2)}$. (b) Frequency response of the off-time TF $G_{\mathrm{s},\mathrm{t_{off}}}(j\omega)e^{-j\omega(T_{\mathrm{off}}/2)}$.

$\mathbf{H}$ are given by [16]

$$\mathbf{\Phi} = e^{\mathbf{A}T_{\mathrm{s}}} \tag{45}$$

$$\mathbf{H} = \int_0^{T_{\mathrm{s}}} \mathbf{\Phi}(\tau)\mathrm{d}\tau \cdot \mathbf{B}. \tag{46}$$

In the subsequent control tasks, the DT system representations will be considered for the plant models.

D. Multiinput Control System Design

The implemented control system will have two control inputs, namely the on-time and the off-time of the DPWM signal driving the power switches. Nevertheless, as motivated in Section II-B, the derived models do not have two independent control inputs. Thus, care must be taken during the controller design procedure.

For the PID-based approach, the feedback loops will be tuned separately by using the control-to-output TFs as given in (43). For the state-feedback regulator design, various approaches could be followed:

1) independent design of the feedback structures, by either setting $\hat{t}_{\mathrm{on}} = 0$ or $\hat{t}_{\mathrm{off}} = 0$, during the design of one or the other feedback;
2) sequential design of the feedback structures, such that one feedback loop is closed before the second one is designed.

A state estimation is furthermore required for the LQR, as the system states are not directly measurable. For this estimator, the knowledge of both control quantities (t_{on} and t_{off}) is of course beneficial for an accurate estimate of the averaged system states.

E. Analog-to-Digital Conversion

A window flash-conversion topology (similar to [26]) has been implemented in a 0.13 μm CMOS technology. The quantization step is $V_q = 15\,\mathrm{mV}$ and the resolution is 4 bits. The analog-to-digital converter (ADC) has been designed with a sampling frequency $f_{\mathrm{adc}} = N f_{\mathrm{sw,nom}}$, where N is the oversampling factor. Note that when the switching period is extended (e.g., due to a load current drop), more than N samples are taken within a single switching period. For the implementations at hand, an oversampling factor $N = 8$ has been chosen, resulting in $f_{\mathrm{adc}} = N f_{\mathrm{sw,nom}} \approx 6.3\,\mathrm{MHz}$, when the nominal switching frequency is set to $f_{\mathrm{sw,nom}} = 780\,\mathrm{kHz}$. The center of the conversion window of the ADC is placed around the reference voltage V_{ref}. With the 16 ADC codes, this results in a total window size of 240 mV, or $\pm 120\,\mathrm{mV}$ around V_{ref}. Due to the ESL of the output capacitor, in combination with short on-phases and large current magnitudes, a significant spike-like ripple appears in the output voltage, at the transitions between the on-phases and the off-phases. For that reason, a first-order low-pass filter (LPF) has been integrated at the input stage of the ADC. The cut-off frequency of the low-pass has been tuned to $f_{\mathrm{lp}} = 3\,\mathrm{MHz}$, to ensure a proper sampling process and to allow a fast reaction to transient events (e.g., a drop in the output voltage).

F. Digital Pulse Width Modulation

The DPWM block, which is common for both presented control structures, combines the on-time $t_{\mathrm{on},m}$ and the off-times $t_{\mathrm{off},n}$ of each period, in order to generate the periodic switching function $u_{\mathrm{d}}(t)$, which is then passed to the output stage of the converter. The on-time is updated once per switching period, whereas the off-time is updated at the rate of the ADC. The principle of operation is reported in Fig. 4. In the upper part of figure, the internal DPWM counter value is shown. The counter is updated at the highest rate in the system, the digital core's fundamental frequency $f_d = 208\,\mathrm{MHz}$. At the beginning of each switching period, the switching signal u_{d} is set to logic "H", as indicated in the lower part of the figure. As soon as the computed on-time value matches the DPWM counter value (compared at the high rate of the digital core logic), the output signal is set to logic "L". Note that the *end of period threshold* $t_{\mathrm{sw},m}$ is not fixed at this point in time. At each sample point of the ADC, a new output voltage error value is received and the control logic for the off-time control is updated. Hence, a new optimal turn-off event for the current period is computed. The intermediate off-times of period $m, t_{\mathrm{off},3}$ to $t_{\mathrm{off},9}$, which

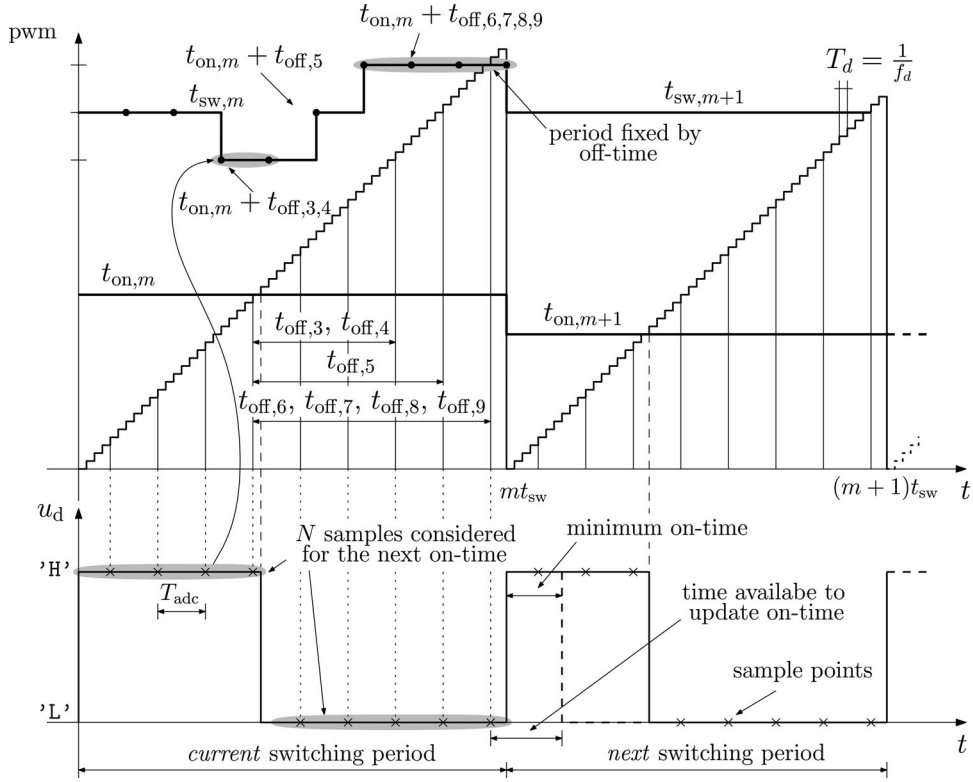

Fig. 4. Digital ramp signal of the DPWM block used to generate the periodic switching function with variable on-time and off-time. In the lower part, the equidistant sampling points are schematically shown.

are used to determine the end of period threshold, are reported in the figure for the *current* switching period. Within the constraints of the minimum and maximum periods, set to 4 and 16 ADC samples, respectively, the off-time control can update the turn-off event. As indicated in the figure, $t_{\mathrm{sw},m}$ is computed by combining the selected on-time $t_{\mathrm{on},m}$ and the intermediate off-time values $t_{\mathrm{off},n}$. For the example presented in the figure, after the 6th ADC sample, the off-time stays at a constant level. This finally results in a period with a length of nine ADC samples. As soon as the DPWM counter reaches the turn-off threshold $t_{\mathrm{sw},m}$, the period is fixed and the counter value, as well as the output signal, are reset. Note the small computational delay of two cycles before the next period starts, which arises from the fact that the latest sample (sample 9 in the example), is still evaluated before the new period is started.

1) Duty Cycle Resolution: The duty cycle resolution for the presented counter-based DPWM varies for the presented system parameters, with a digital core frequency of $f_d = 208\,\mathrm{MHz}$, from 1.9‰ to 7.6‰ for a minimum and maximum switching frequency of $f_{\mathrm{sw,min}} = 400\,\mathrm{kHz}$ and $f_{\mathrm{sw,max}} = 1.6\,\mathrm{MHz}$ [27]. For a nominal switching period of $f_{\mathrm{sw,nom}} = 780\,\mathrm{kHz}$, the resolution is 3.75‰, which corresponds to a output voltage resolution of 45 mV at a nominal input voltage of 12 V. In [27], Li *et. al.* showed that with a combined regulation of the on-time and the off-time, an increased duty cycle resolution and consequently an increased output voltage resolution can be achieved. The presented control structures offer the possibility to alter the on-time and the off-time in steps of the DPWM counter, thus such a strategy could be implemented. Nevertheless, as the goal of this study is to boost the converter responses by altering the switching period during transient events, a degradation of the duty cycle resolution is acceptable during such a transient. Consequently, in favor of an efficient implementation, a relaxed computation schedule and a simplified synchronization mechanism within one period, coarse steps have been chosen for the variation of the period. In fact, the ADC sampling time has been chosen as the time step to alter the off-time, as shown in Fig. 4.

2) Limit Cycle Oscillations: In order to avoid limit cycle oscillations at the output voltage, the resolution of the DPWM needs to be greater than the one of the ADC [28]. For the presented scenario, the resolution of the ADC is $V_q = 15\,\mathrm{mV}$, whereas the resolution of the DPWM is around 45 mV for the nominal switching period. For this setup, it could happen that no DPWM level maps to the ADC zero-error bin, thus, limit cycles could appear. In order to avoid such limit cycle oscillations, the zero-error bin of the ADC has been removed in the digital domain by adding half a least-significant bit (LSB) to the output of the ADC, as detailed in [26].

3) Delay Model: The delay introduced by the discrete-time DPWM block is not present in the models derived in Section II-A. For the implemented scheme presented previously, the delay for the on-time loop is given as $e^{-sT_{\mathrm{on}}/2}$, as specified in Section II-B. For the specific implementation of the DPWM, in which the off-time is not fixed at the beginning of the period, but rather determined based on intermediate samples acquired at the rate of the ADC, $f_{\mathrm{adc}} = 1/T_{\mathrm{adc}}$, the delay of a change in the off-time to the output voltage is given by $e^{s(T_{\mathrm{off}}/2 - T_{\mathrm{adc}})}$. Note that by design $T_{\mathrm{off}}/2 > T_{\mathrm{adc}}$, thus a phase lead is present

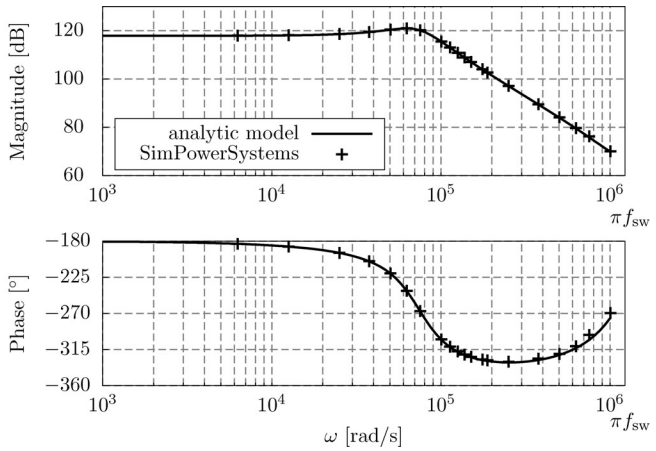

Fig. 5. Validation of the control-to-output frequency response of the TF relating the off-time to the output voltage for the presented DPWM, $G_{\mathrm{s},\mathrm{t_{off}}}(j\omega)e^{j\omega(T_{\rm off}/2-T_{\rm adc})}$. The analytic model is again compared to the response obtained via a SimPowerSystems simulation.

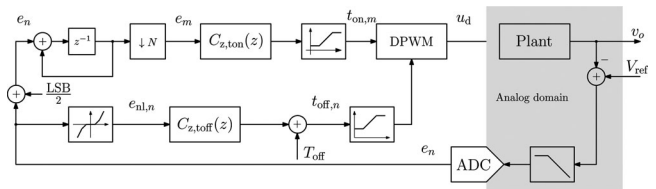

Fig. 6. Schematic structure of the PID controller architecture.

in the delay model of the off-time. This results in an increase of the phase margin at higher frequencies. A simulation-based validation of this specific model is presented in Fig. 5.

IV. Digital Multiloop PID Control

Similar to [18] and [19], a PID type control law has been implemented to demonstrate the effectiveness of the derived models. Industry-typical system parameters for PoL converters have been chosen for the hardware setup: input/output voltages of 12 V and 1 V, output inductance L, and capacitance C of 320 nH and 660 μF, respectively, and a switching frequency of 400 kHz $\leq f_{\rm sw} \leq$ 1.6 MHz. The nominal switching frequency has been set to 780 kHz. The parasitics are assumed as follows: R_L and R_C equal to 1 mΩ, $R_{\rm on} = 15$ mΩ and $L_C = 1$ nH. Due to the presence of L_C, significant output voltage ripples are expected with a magnitude of $\approx$ 40 mV. The gain of the ADC, as well as the time resolution of the actuating signals (on-time and off-time) have to be considered for the implementation. During the design procedure for the multiloop PID controller, as well as for the derivation of the state-feedback controller, these gains have been assumed to be 1, without loss of generality.

A. On-time Control Design

The design is based on the open-loop TF of the plant model, as derived in (44) in Section III-A. The implemented control structure is presented in a high-level view in Fig. 6. As indicated in the figure, the digital output voltage error signal e_n, which is the output of the ADC, is fed to a digital averaging and down-sampling filter. Several reasons require this filtering step: first, it ensures that an accurate dc value of the output voltage error signal is processed by subsequent blocks. Second, the reduction of the sampling rate relaxes the speed constraints on subsequent digital logic elements. The control input at the low rate e_m computes as

$$e_m = \big(\underbrace{(V_{\rm ref} - v_{o,n})}_{e_n} + (V_{\rm ref} - v_{o,n-1}) + \cdots + (V_{\rm ref} - v_{o,n-N+1}) \big)/N \tag{47}$$

where N is the number of samples considered for the averaging process, and $V_{\rm ref}$ is the target dc voltage.

With a PID control law $C_{\rm z,ton}(z)$, the on-time $t_{{\rm on},m}$ of the pulse-width modulated signal for the next switching cycle can be computed, based on the aggregated information from the running period e_m. The digital controller design is carried-out in q-domain, where mainly the same design procedure can be applied as in s-domain and furthermore the sampling process is considered. The discrete-time TF can be transformed to q-domain by applying the bilinear transformation [15], [16]

$$G_{\mathrm{z},\mathrm{t_{on}}}(z) = \frac{z-1}{z}\mathbf{Z}\left\{\frac{G_{\mathrm{s},\mathrm{t_{on}}}(s)}{s}\right\} \tag{48}$$

$$G_{\mathrm{q},\mathrm{t_{on}}}(q) = G_{\rm z,ton}\left(z = \frac{1+\frac{q}{\Omega_{0,\mathrm{t_{on}}}}}{1-\frac{q}{\Omega_{0,\mathrm{t_{on}}}}}\right), \text{ with}$$

$$\Omega_{0,\mathrm{t_{on}}} = \frac{2}{T_{\rm sw}} \text{ and } \Omega = \Omega_{0,\mathrm{t_{on}}} \tan\left(\frac{\omega}{\Omega_{0,\mathrm{t_{on}}}}\right) \tag{49}$$

where $G_{\mathrm{s},\mathrm{t_{on}}}(s) = \mathbf{G}_{\rm s}[2]$ is derived in (44), as the TF relating the input $\hat{t}_{\rm on}$ to the output $\hat{v}_o$, when $\hat{v}_{\rm i} = 0$ and $\hat{t}_{\rm off} = 0$. Furthermore, $\mathbf{Z}\{X(s)\}$ is given by $\mathbf{Z}\{X(s)\} = \mathcal{Z}\{(\mathcal{L}^{-1}\{X(s)\})_{t=kT_{\rm s}}\}$, when $\mathcal{Z}\{\cdot\}$ and $\mathcal{L}^{-1}\{\cdot\}$ denote the $z-$transform and the inverse Laplace transform, respectively. Additionally, for the delay of the DPWM on the on-time, $e^{-sT_{\rm on}/2}$ is approximated for the design task by its third-order Padé approximation. The starting point for the controller design task is the open-loop TF $G_{\mathrm{q,sys,ton}}(q) = G_{\mathrm{q},\mathrm{t_{on}}}(q) \cdot G_{\mathrm{q,lp}}(q) \cdot e^{-qT_{\rm on}/2}$, in which $G_{\mathrm{q,lp}}(q) = \frac{1}{q/(2\pi f_{\rm lp})+1}$ models the first-order analog low-pass filter, as specified in Section III-E, and $\omega \approx \Omega$ [15]. The corresponding frequency response, $G_{\mathrm{q,sys,ton}}(q)|_{q=j\Omega}$ is shown in Fig. 7. The design specifications are the following: the on-time control loop is dominant during the steady-state operation, thus it should remove any steady-state error (by including integral action), and should furthermore appropriately react to smaller transients as well as to continuously but slowly changing system conditions. Consequently, the response of this controller can be designed conservatively. For the presented scenario, the bandwidth and the phase margin have been tuned to 50 kHz and 55 °, respectively. This corresponds to a bandwith of $\Omega_{\rm c,ton} = 3.15 \times 10^5$ rad s^{-1}. This is done by shaping the open-loop TF $G_{\mathrm{q,sys,ton}}(q)$ to fulfill these requirements. The frequency response of the controller TF to achieve this goal is plotted in Fig. 7 as $C_{\mathrm{q,ton}}(q)|_{q=j\Omega}$. The closed-loop TF is given by $T_{\mathrm{q,ton}}(q) = \frac{G_{\mathrm{q,sys,ton}}(q)C_{\mathrm{q,ton}}(q)}{1+G_{\mathrm{q,sys,ton}}(q)C_{\mathrm{q,ton}}(q)}$ and its frequency response $T_{\mathrm{q,ton}}(q)|_{q=j\Omega}$ is furthermore shown

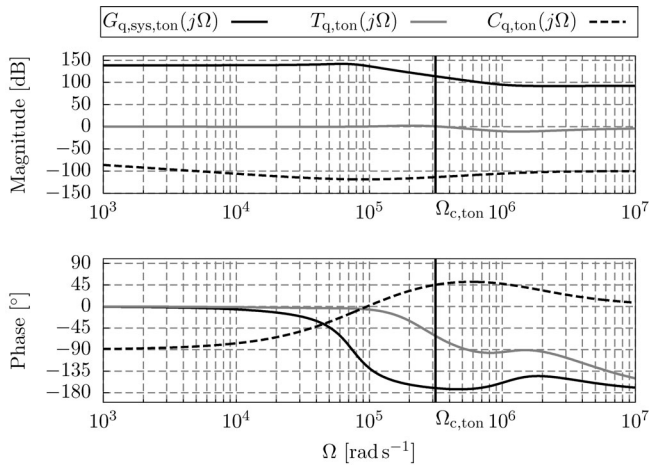

Fig. 7. Bode diagram of the on-time open-loop, the controller, as well as the closed-loop transfer function.

in the figure. The q-domain controller TF can be transformed to z-domain by applying the trapezoid approximation

$$C_{\mathrm{z,ton}}(z) = C_{\mathrm{q,ton}}\left(q = \frac{2}{T_{\mathrm{sw}}}\frac{z-1}{z+1}\right) = 5.43 \times 10^{-06}\,\frac{(z-0.92)\,(z-0.85)}{(z-1)\,(z+0.017)} \quad (50)$$

with a sampling frequency of $f_{\mathrm{sw}} = 1/T_{\mathrm{sw}} = 780\,\mathrm{kHz}$.

Furthermore, as indicated in Fig. 6, the output of the on-time control law, $t_{\mathrm{on},m}$, is saturated before it is passed to the DPWM block. With a lower limit on the minimum on-time, a switching cycle is enforced for each period, even if the optimum control action would require to set a lower value. This keeps the switching period in the specified range. An upper limit is furthermore set in order to limit the maximum output voltage value, in case of unpredicted disturbances. For the hardware implementation, the lower and upper limit have been set to 2 % and 20 % of the nominal switching period, respectively. The same limits are applied to the actuating signal of the LQG controller. Additionally, the zero-error bin of the ADC is removed in the digital domain, see Section III-F for a detailed discussion.

B. Off-Time Control Design

Taking Fig. 6 as reference, the off-time control loop takes the error samples as delivered by the ADC, applies a nonlinear mapping and subsequently passes it to the off-time control law. By directly using the ADC samples, this regulation loop is able to react faster to transients in the output voltage, with the drawback that the unfiltered samples are passed to the controller. Thus, as indicated in the figure (c.f. Fig. 8), a dead zone has been introduced in the implementation such that the off-time control-loop reacts only when a certain threshold of the output voltage error is exceeded. This nonlinear mapping can further be used to boost the response of the off-time control loop in specified regions, by setting the slope in a selected input range to a value greater than 1 for the mapping of input samples to output samples. For the presented parameters, the dead zone has been

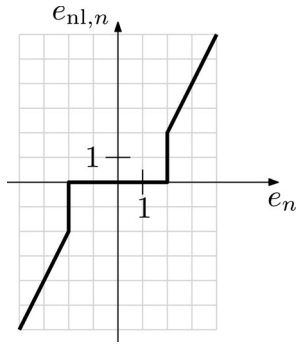

Fig. 8. Nonlinear mapping for the off-time control input as configured for the presented hardware setup.

set to ± 2 ADC quantization levels, such that the output voltage ripple is mainly removed. A single slope has been defined for the mapping, which has been set to 2. The applied mapping is plotted in Fig. 8. Furthermore, the output of the off-time controller is again saturated. This ensures that the switching period is changing in a predefined range. For the hardware implementations, the upper and lower limit have been set to 16 and 4 ADC samples. Hence, this corresponds to a minimum switching frequency of $f_{\mathrm{sw,min}} = 1/(16T_{\mathrm{adc}}) = 400\,\mathrm{kHz}$ and a maximum switching frequency of $f_{\mathrm{sw,max}} = 1/(4T_{\mathrm{adc}}) = 1.6\,\mathrm{MHz}$. The gain, as well as the dead zone and the nonlinear mapping must be chosen corresponding to the specific system characteristics (i.e., the output voltage ripple amplitude, ADC resolution,...). The gain of the off-time control loop has been computed based on the open-loop TF

$$G_{\mathrm{z,t_{off}}}(z) = \frac{z-1}{z}\mathbf{Z}\left\{\frac{G_{\mathrm{s,t_{off}}}(s)}{s}\right\} \quad (51)$$

$$G_{\mathrm{q,t_{off}}}(q) = G_{\mathrm{z,toff}}\left(z = \frac{1+\frac{q}{\Omega_{0,\mathrm{t_{off}}}}}{1-\frac{q}{\Omega_{0,\mathrm{t_{off}}}}}\right), \text{ with}$$

$$\Omega_{0,\mathrm{t_{off}}} = \frac{2}{T_{\mathrm{adc}}} \text{ and } \Omega = \Omega_{0,\mathrm{t_{off}}}\tan\left(\frac{\omega}{\Omega_{0,\mathrm{t_{off}}}}\right). \quad (52)$$

where $G_{\mathrm{s,t_{off}}}(s) := \mathbf{G}_{\mathrm{s}}[3]$ is derived in (44), as the TF relating the input $\hat{t}_{\mathrm{off}}$ to the output $\hat{v}_o$, when $\hat{v}_{\mathrm{i}} = 0$ and $\hat{t}_{\mathrm{on}} = 0$. Additionally, for the delay of the DPWM on the off-time, $e^{s(T_{\mathrm{off}}/2 - T_{\mathrm{adc}})}$, as discussed in Section III-F, is approximated for the design task by its third-order Padé approximation. The open-loop TF is given by $G_{\mathrm{q,sys,toff}}(q) = G_{\mathrm{q,t_{off}}}(q) \cdot G_{\mathrm{q,lp}}(q) \cdot e^{q(T_{\mathrm{off}}/2 - T_{\mathrm{adc}})}$ and its frequency response $G_{\mathrm{q,sys,toff}}(q)|_{q=j\Omega}$ is plotted in Fig. 9. Note that the open-loop Bode plot starts from a phase of $-180\,^\circ$. Intuitively, this is justified by the fact that an increase in the off-time of the switching period (the input to the off-time plant TF $G_{\mathrm{q,t_{off}}}(q)$) results in a decrease of the output voltage (the output of the off-time plant TF). Hence, in order to achieve an appropriate reaction of the controller (a positive input error signal should result in a negative reaction of the actuating signal and vice versa), the control law needs to account for this fact. Therefore, as shown as the dashed line in the phase plot of Fig. 9, due to the negative gain of the controller, the phase is shifted by $180\,^\circ$. A proportional gain has shown to

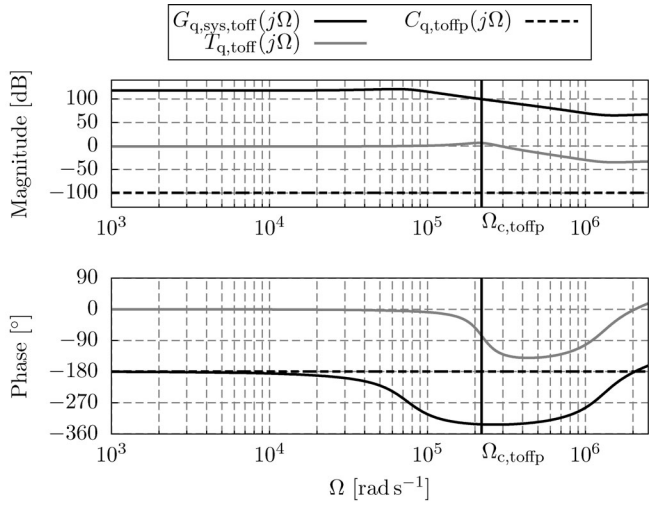

Fig. 9. Bode diagram of the off-time open-loop, the controller, as well as the closed-loop transfer function.

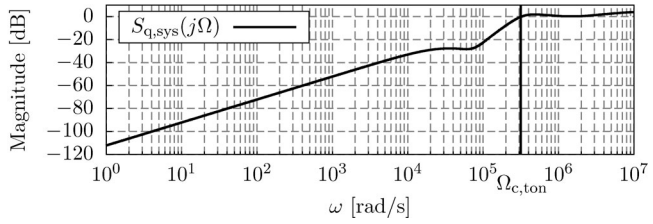

Fig. 10. Magnitude plot of the sensitivity transfer function, when both feedback loops are closed.

be sufficient for the required control action. Thus the feedback gain is given by

$$C_{\mathrm{z,toff}}(z) = -k_{\mathrm{p}} = -1.044 \times 10^{-05} \tag{53}$$

for the control of the off-time. This corresponds to a bandwidth of $\Omega_{\mathrm{c,toff}} = 2.2 \times 10^5$ rads^{-1}. Due to the pure proportional gain, $C_{\mathrm{z,toff}}(z)$ equals to $C_{\mathrm{q,t_{off}}}(q)$. The closed-loop TF of the off-time control law, is given as $T_{\mathrm{q,toff}}(q) = \frac{G_{\mathrm{q,sys,toff}}(q)C_{\mathrm{q,t_{off}}}(q)}{1+G_{\mathrm{q,sys,toff}}(q)C_{\mathrm{q,t_{off}}}(q)}$, and its frequency response, $T_{\mathrm{q,toff}}(q)\,|_{q=j\Omega}$ is furthermore plotted in Fig. 9.

C. Stability Analysis

As detailed previously, the off-time control loop is altering the switching period based on the output voltage error. This inherently affects the bandwidth and gain margin of the on-time PID loop. For the given scenario, the bandwidth, due to the variation of the switching period, changes within 30 kHz $\leq$ 50 kHz $\leq$ 88 kHz for the switching frequency ranging from 400 kHz $\leq$ 780 kHz $\leq$ 1.6 MHz. Similarly, the phase margin changes from 49 ° $\leq$ 55 ° $\leq$ 60 °. Hence, system stability is guaranteed under all conditions.

The overall closed-loop sensitivity TF $S_{\mathrm{q,sys}}(q) = \frac{1}{1+\left(G_{\mathrm{q,sys,ton}}(q)C_{\mathrm{q,ton}}(q)+G_{\mathrm{q,sys,toff}}(q)C_{\mathrm{q,t_{off}}}(q)\right)}$ is furthermore reported in Fig. 10. A reasonable damping of disturbances at frequencies up to the bandwidth of the on-time control-loop, which is the dominant one, is achieved by the control system.

D. Computation Schedule

The sampling process and computation schedule is schematically drawn in lower part of Fig. 4. Within one period, N samples are processed by the controller at the rate of the ADC, f_{adc}. At the same (high) rate, the decision on the length of the current period is taken based on the off-time control law. Furthermore, the averaged output voltage error (47) is updated in an iterative manner at this rate. When the last sample of the current period is received, the on-time for the next period can be computed, at the rate of the switching frequency f_{sw}.

V. Digital LQG State-Feedback Control

In contrast to the PID control law, which is based on the frequency domain TFs, in this section, the design and the implementation of a state-feedback control structure are presented. This will prove the applicability of the proposed modulation of the switching period and the independence of the method to a certain feedback structure.

For the switching frequency modulation, the proportional feedback gain, as derived in the previous section for the PID control law, is utilized. For the regulation of the on-time, a control law based on an LQR is derived for the synchronous buck converter, where perfect knowledge about the inherent system states is assumed. Additionally, all plant inputs, besides the actual control inputs ($\hat{t}_{\mathrm{on}}$ and $\hat{t}_{\mathrm{off}}$), are assumed to be zero for the design process. Integral action is further added in order to achieve a tight output voltage regulation. A Kalman state estimator is then designed to acquire the state information to be fed back via the LQR control gain. The control inputs ($t_{\mathrm{on},m}$ and $t_{\mathrm{off},m}$), as well as the output voltage error e_m are taken as inputs, and a state estimate is computed as output. Finally, a brief discussion about the computation schedule will conclude the section.

A. LQR Feedback Controller Design

As the plant dynamics, the averaged and linearized ESSA model (29) converted to DT domain (as presented in Section III-C) is assumed

$$\mathbf{x}_{m+1} = \mathbf{\Phi}\mathbf{x}_m + \mathbf{H}\mathbf{u}_m + \mathbf{G}\mathbf{w}_{\mathrm{d}} \tag{54}$$

$$y_m = \mathbf{C}\mathbf{x}_m + \mathbf{D}\mathbf{u}_m + w_{\mathrm{n}} \tag{55}$$

where $\mathbf{\Phi} \in \mathbb{R}^{2\times2}$, $\mathbf{H} \in \mathbb{R}^{2\times2}$, $\mathbf{C} \in \mathbb{R}^{1\times2}$, and $\mathbf{D} \in \mathbb{R}^{1\times2}$ are the state transition, input, output, and direct-transmission matrices, respectively, $\mathbf{x}_m = [\,v_{C,m}, i_{L,m}\,]^T$ and $\mathbf{u}_m = [t_{\mathrm{on},m}, t_{\mathrm{off},m}]^T$ are the DT equivalents of the plant states and inputs. As output of the system, the output voltage is considered $y_m = v_{o,m}$. Note that the second-order model for the buck converter, as reported in (29), is considered for this controller design, in order to reduce the implementation complexity. Furthermore, the measurement and process noise, w_{n} and $\mathbf{w}_{\mathrm{d}}$, respectively, are assumed to be uncorrelated zero-mean Gaussian stochastic processes with co-variance matrices $\mathbf{V} \in \mathbb{R}^{1\times1}$ and $\mathbf{W} \in \mathbb{R}^{2\times2}$ of w_{n} and $\mathbf{w}_{\mathrm{d}}$, respectively. The diagonal matrix $\mathbf{G} \in \mathbb{R}^{2\times2}$ further weights the process noise.

The off-time feedback loop ($t_{\rm off} = -k_{\rm p}e$) is closed before the LQR design is carried out for the on-time. This corresponds to option two, as proposed in Section III-D. The plant dynamics with the off-time feedback closed is given by

$$\mathbf{\Phi}_{\rm c} = \mathbf{\Phi} - \mathbf{H}_2 k_{\rm p} \mathbf{C} \tag{56}$$

where $\mathbf{\Phi}_{\rm c}$ is used as the plant model for the subsequent LQR design and $\mathbf{H} = [\mathbf{H}_1, \mathbf{H}_2]$ is the input matrix split in the vectors $\mathbf{H}_1$ and $\mathbf{H}_2$, corresponding to the inputs $t_{{\rm on},m}$ and $t_{{\rm off},m}$, respectively.

Next, an integrator state is added to remove the steady-state error. The state equation for the augmented DT plant equations reads

$$\underbrace{\begin{bmatrix} \mathbf{x}_{m+1} \\ x_{{\rm i},m+1} \end{bmatrix}}_{\mathbf{x}_{{\rm aug},m+1}} = \begin{bmatrix} \mathbf{\Phi}_{\rm c} & \begin{bmatrix} 0 \\ 0 \end{bmatrix} \\ [-\mathbf{C}] & 1 \end{bmatrix} \underbrace{\begin{bmatrix} \mathbf{x}_m \\ x_{{\rm i},m} \end{bmatrix}}_{\mathbf{x}_{{\rm aug},m}} + \begin{bmatrix} \mathbf{H}_1 \\ 0 \end{bmatrix} t_{{\rm on},m}. \tag{57}$$

The optimal state feedback for the on-time control that brings the system to the zero state is found by minimizing the deterministic cost function

$$\mathbf{J}_{\rm r} = \int_0^\infty \left(\mathbf{x}_{{\rm aug},m}^T \mathbf{Q} \mathbf{x}_{{\rm aug},m} + t_{{\rm on},m} \mathbf{R} t_{{\rm on},m} \right) {\rm d}t \tag{58}$$

in which $\mathbf{x}_{{\rm aug},m} \in \mathbb{R}^{3\times 1}$ is defined as previously. $\mathbf{Q}$ and $\mathbf{R}$ are positive definite symmetric matrices and the difference between $\mathbf{Q}$ and $\mathbf{R}$ impacts the resulting feedback gain [17].The weighting matrices for the state vector as well as for the input, $\mathbf{Q} \in \mathbb{R}^{3\times 3}$ and $\mathbf{R} \in \mathbb{R}^{2\times 2}$, as used for the given parameter set, have been simply specified as

$$\mathbf{Q} = \mathbf{I}, \mathbf{R} = \mathbf{I}. \tag{59}$$

The control law under assumption of perfect knowledge of the system states is given by

$$t_{{\rm on},m} = -\mathbf{k}_{\rm r}^T \mathbf{x}_m - x_{{\rm i},m} \tag{60}$$

Furthermore, the update of the integrator state $x_{{\rm i},m}$ is computed as $x_{{\rm i},m+1} = x_{{\rm i},m} + k_{\rm i} e_m$. The state-feedback gain has dimensions $\mathbf{k}_{\rm r}^T \in \mathbb{R}^{1\times 2}$ and the integrator coefficient $k_{\rm i}$ is a scalar. The solution of the algebraic Riccati equation (ARE) giving the optimal steady-state feedback gain $\mathbf{K}^T$ of the augmented plant can be found by using the Control Systems Toolbox of MATLAB

```
[K] = dlqr(PHIaug,Haug,Q,R).
```

The resulting gain vector $\mathbf{K}$ for the augmented plant is composed of

$$\mathbf{K}^T = \left[\mathbf{k}_{\rm r}^T, k_{\rm i} \right]. \tag{61}$$

B. LQG Estimator Design

For the implementation, the converter output voltage v_o is the only measured quantity available. Therefore, a state estimation is required to realize the state feedback control law. A Kalman filter structure computes based on the averaged output voltage measurement, the on-time and the off-time set in the previous cycle, together with the plant model, (54) and (55), a state estimate.

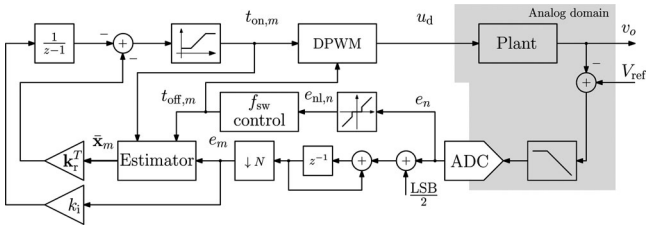

Fig. 11. Schematic structure of the LQG controller architecture.

The estimator uses the most recent measurement y_m to update the state information for the current time step

$$\tilde{\mathbf{x}}_m = \mathbf{\Phi} \bar{\mathbf{x}}_{m-1} + \mathbf{H} \mathbf{u}_{m-1} \tag{62}$$

$$\bar{\mathbf{x}}_m = \tilde{\mathbf{x}}_m + \mathbf{k}_{\rm ec} \left(y_m - \mathbf{C} \tilde{\mathbf{x}}_m \right) \tag{63}$$

where $\bar{\mathbf{x}}_m$ can be seen as the corrected estimate, whereas $\tilde{\mathbf{x}}_m$ can be seen as the predictive estimate. Furthermore, $\mathbf{k}_{\rm ec} \in \mathbb{R}^{2\times 1}$ is the steady-state Kalman gain of the estimator.

Substituting (62) into (63) and considering the system at hand, yields for the current estimate

$$\bar{\mathbf{x}}_m = \underbrace{\left(\mathbf{\Phi} - \mathbf{k}_{\rm ec} \mathbf{C} \mathbf{\Phi} \right)}_{\mathbf{\Phi}_{\rm e}} \bar{\mathbf{x}}_{m-1} + \underbrace{\left(\mathbf{H} - \mathbf{k}_{\rm ec} \mathbf{C} \mathbf{H} \right)}_{\mathbf{H}_{\rm e}} \mathbf{u}_{m-1} + \mathbf{k}_{\rm ec} y_m. \tag{64}$$

The matrices $\mathbf{\Phi}_{\rm e} \in \mathbb{R}^{2\times 2}$ and $\mathbf{H}_{\rm e} \in \mathbb{R}^{2\times 2}$ are the transition matrix and the input matrix of the estimator model. It can be easily shown by investigating the predictive estimator equations (by substituting (63) into (62) and comparing the estimator gains) that the Kalman gain of the corrected estimate $\mathbf{k}_{\rm ec}$ can be computed from the gain of the corresponding predictive estimate $\mathbf{k}_{\rm ep}$ by

$$\mathbf{k}_{\rm ec} = \Phi^{-1} \mathbf{k}_{\rm ep}. \tag{65}$$

The co-variance matrix of the measurement noise has been found by extracting the statistical properties from numerous typical output voltage measurements (including the effects of the ADC), and the co-variance matrix of the process noise as well as its weighting matrix has been estimated by evaluating the fixed-point controller system (by means of computer simulations). Starting from these estimated values, the co-variance matrices have been fine-tuned in order to get the desired converter response [29]

$$\mathbf{W} = \mathbf{I}, \mathbf{V} = 1, \mathbf{G} = \begin{bmatrix} 10^{-4} & 0 \\ 0 & 10^{-4} \end{bmatrix}. \tag{66}$$

The corresponding ARE has again been solved for the steady-state estimator gain with the help of the MATLAB numeric computation software

```
Kep = dlqe(PHI', G, C, W, V);
Kec = PHI\Kep.
```

Thus, the implemented control law utilizing the estimated state vector and the integrator state is given by

$$t_{{\rm on},m} = -\left(\mathbf{k}_{\rm r}^T \bar{\mathbf{x}}_m + x_{{\rm i},m} \right). \tag{67}$$

For the modulation of the switching period, the same structure is used as for the PID control law. The high-level control structure, as implemented on the hardware, is depicted in Fig. 11.

The saturation on the on-time $t_{\mathrm{on},m}$, has been chosen as for the multiloop PID control. Furthermore, the block f_{sw} *control* summarizes the off-time control loop of the multiloop PID control and has been designed as detailed in Section IV-B.

C. Computation Schedule

The targeted nominal converter switching frequency of $780 \pm 400\,\mathrm{kHz}$, with an ADC sampling frequency of 6.3 MHz and a digital core frequency of 104 MHz results in a quite challenging computation schedule, because only around 16 digital core's clock cycles are available in between the retrieval of two subsequent ADC samples. This is especially critical at the end of the switching period, when a new on-time needs to be computed, as for this update a new state estimate is needed. Splitting (64) in its components gives an insight on the scheduling of the individual computations necessary to update the state estimate

$$\bar{\mathbf{x}}_m = \mathbf{\Phi}_{\mathrm{e}}\bar{\mathbf{x}}_{m-1} \tag{68}$$

$$+ \mathbf{H}_{\mathrm{e},1}t_{\mathrm{on},m-1} \tag{69}$$

$$+ \mathbf{H}_{\mathrm{e},2}t_{\mathrm{off},m-1} \tag{70}$$

$$+ \mathbf{k}_{\mathrm{ec}}y_m \tag{71}$$

with $\mathbf{H}_{\mathrm{e}} = [\mathbf{H}_{\mathrm{e},1}, \mathbf{H}_{\mathrm{e},2}]$ as the input matrix of the estimator model, split in the vectors of the corresponding inputs $t_{\mathrm{on},m}$ and $t_{\mathrm{off},m}$, respectively.

The following steps are necessary to update the on-time for the subsequent switching cycle:

1) update the down-sampled output voltage error (47). The sum can be implemented in a recursive manner;
2) update the integrator state with the updated output voltage error sample;
3) update the state estimate with the output voltage measurement (71);
4) update the state estimate with the off-time (70). This update cannot be precomputed, as the actual off-time is selected within the current period (by the off-time control law);
5) compute the state feedback (67);
6) saturate the resulting on-time value, if necessary.

Precomputations for the next cycle:

1) update the current state estimate with the on-time information (69);
2) update the state update (68).

VI. Experimental Validation

The laboratory setup for the digital control of a synchronous buck converter is as follows: for the driver and the power stage an existing integrated solution is utilized [30] along with an external *LC* filter. The application-specific integrated circuit (ASIC) implementation of the first controller system in a $0.13\,\mu$m CMOS technology consists of a 4 bit Flash conversion window ADC, together with an analog antialiasing filter, the digital PID controller, and the DPWM block [19], [23]. The ADC architecture has been tailored to the requirements of power conversion systems, similar to [26].

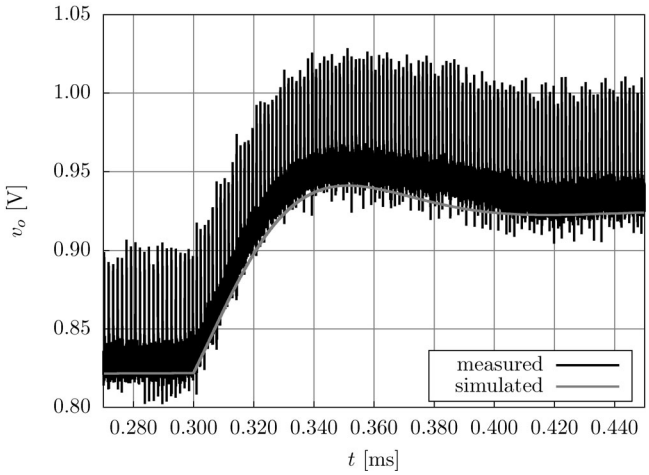

Fig. 12. Open-loop dynamic response of the converter output voltage to a sudden step in the switching frequency. The response of the linearized small-signal ESSA model as the gray line is compared to the measured response as the black line.

For the digital state-feedback controller, the analog prefilter and the ADC have been reused from the ASIC implementation. The same driver and output stage have been used, as in the previous setup. The samples from the ADC are now passed to an external Altera Cyclone IV field-programmable gate array (FPGA) board, where the digital LQG control law, together with a DPWM block, is implemented. This additionally shows that even low cost and consumer-oriented FPGAs are feasible choices to implement powerful and at the same time flexible control structures [31].

Industry-typical system parameters for PoL converters have been chosen for the demonstrators: input/output voltages of 12 V and 1 V, output inductance L and capacitance C of $320\,\mathrm{nH} \pm 30\,\%$ and $660\,\mu\mathrm{F} \pm 40\,\%$, respectively, and a switching frequency of $400\,\mathrm{kHz} \leq f_{\mathrm{sw}} \leq 1.6\,\mathrm{MHz}$. The nominal switching frequencies have been set to 780 kHz.

Three experiments will be presented to verify the proposed models and to evaluate the performance of the developed controller designs:

1) an open-loop step response to a sudden change in the converter switching frequency is presented and the simulated response is compared to a measured one;
2) load current transient responses of the multiloop PID-based control system are compared to the responses of a single loop PID controller;
3) for the LQG, similar load current transients have been measured and the output voltage responses to a positive and a negative load current step are presented.

A. Open-Loop Dynamic Response to a Step in the Switching Period

The open-loop dynamic response of the ESSA model (30) to a sudden change in the switching period has been compared to one taken from the prototype implementation. The accurate matching of the simulation result and the measured response is reported in Fig. 12. The on-time of the DPWM signal has been

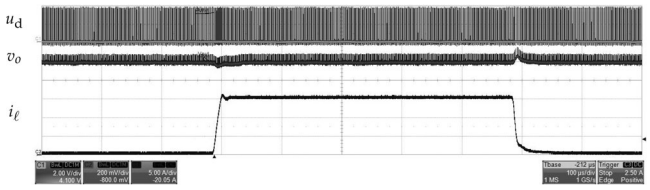

Fig. 13. Experimental results of the PID control: output voltage waveform under variable load conditions. The channels have been set to $200\,\mathrm{mV/div}$ for v_o, $2\,\mathrm{V/div}$ for u_d, $5\,\mathrm{A/div}$ for i_ℓ, and the time base has been set to $100\,\mu\mathrm{s/div}$.

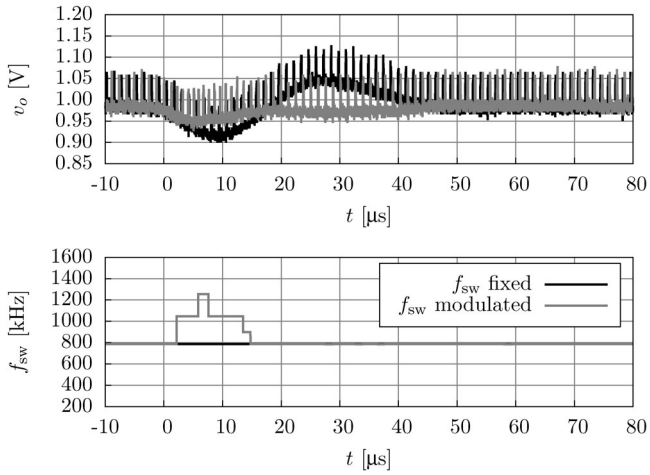

Fig. 14. Experimental results of the PID control: zoomed response to a positive load current step of $15\,\mathrm{A}$.

held constant, and a sudden step in the switching frequency from 676 to $761\,\mathrm{kHz}$ is applied at the time instant around $0.3\,\mathrm{ms}$. In the figure, the gray waveform shows the simulated averaged small-signal response, whereas the solid black curve represents the measured large-signal waveform.

B. Multiloop PID Control: Measurement Results

In order to highlight the performance improvement gained by introducing the modulation of the switching period, the proposed control structure is compared to a single-loop controller which modulates the duty cycle only, by setting $C_{\mathrm{z,toff}}(z) = 0$. For both cases, the same PID control law $C_{\mathrm{z,ton}}(z)$ is employed. In Fig. 13, an oscilloscope screenshot of a load rise/drop of 15 A is reported.

For the sake of clarity, the collected output voltage waveforms have been redrawn in the upper diagram of Figs. 14 and 15, respectively, where the solid black waveforms represent the single-loop PID controller responses and the gray curves represent the responses of the proposed multiloop controller architecture. The bottom parts of Figs. 14 and 15 show the switching frequency. In case of a positive/negative load transient, the proposed controller reacts immediately by shortening/extending the switching period for a certain amount of periods (resulting in a higher/lower switching frequency). It can be observed in Fig. 14, that the control structure is able to provide charge to the output capacitor much earlier than the single-loop solution, resulting in a smaller undershoot and a reduced settling time. As intended, the switching frequency is set to its predefined value

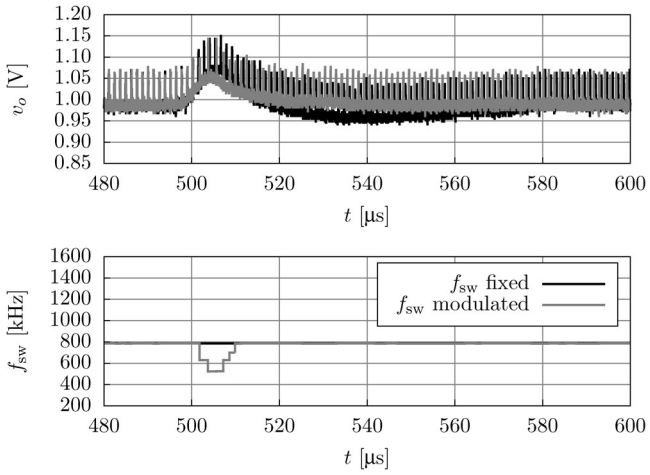

Fig. 15. Experimental results of the PID control: zoomed response to a negative load current step of $15\,\mathrm{A}$.

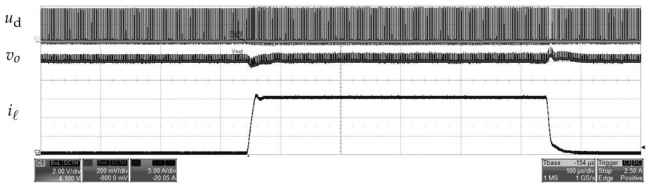

Fig. 16. Experimental results of the LQG control: output voltage waveform under variable load conditions. The channels have been set to $200\,\mathrm{mV/div}$ for v_o, $2\,\mathrm{V/div}$ for u_d, $5\,\mathrm{A/div}$ for i_ℓ, and the time base has been set to $100\,\mu\mathrm{s/div}$.

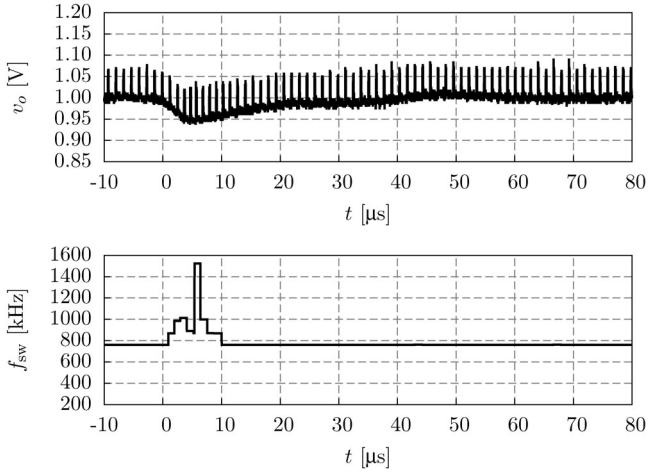

Fig. 17. Experimental results of the LQG control: zoomed response to a positive load current step of 15 A.

in steady-state operation. For the reported load current step of $15\,\mathrm{A}$, the proposed scheme achieves a significant dynamic performance improvement. Note that the improvement for a load drop, as shown in Fig. 15, is limited, because the on-times of the switching periods are much shorter than the corresponding off-times, such that an extension of the period does not significantly improve the transient performance. This is especially the case for PoL applications, where the input voltage v_i is typically much higher than the output voltage v_o. Further note, that the substantial ripple, which can be observed in the output voltage

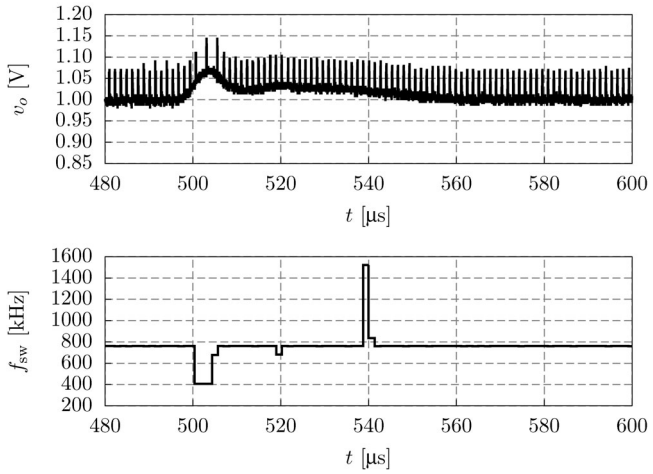

Fig. 18. Experimental results of the LQG control: zoomed response to a negative load current step of 15 A.

waveforms in Figs. 13, 14, and 15, as well as in Figs. 16, 17, and 18, is caused by the parasitic ESL of the output capacitor.

C. LQG State-Feedback Control

Similarly, the same load scenarios have been applied to the LQG-based control system implemented on the FPGA. In Fig. 16, an oscilloscope screenshot of the responses of the output voltage to a load current step of ± 15 A is presented. The zoomed responses, with the output voltage waveforms in the upper part of the plots and the switching frequencies in the lower part of the plots, are reported in Figs. 17 and 18, respectively. A tight voltage regulation can be achieved by modulating the switching period when necessary and keeping it constant during steady-state operation.

The proper reaction of the controller is ensured by mainly two facts: first, during the design of the on-time control law, the off-time feedback loop is already closed, such that it is considered during the computation of the optimum feedback gain. Second, the employed state estimator receives the off-time together with the on-time of each period as input, and is therefore able to compute an accurate estimate of the state dynamics.

A direct comparison of the two independent controller implementations is not presented in this study. One controller is implemented as a highly optimized ASIC design, whereas the other is realized as a proof-of-concept implementation on an consumer-oriented FPGA. Thus, not all design parameters (e.g., digital clock frequencies, switching frequencies,. . .) could be set at exactly the same values, which would be necessary for a fair comparison. Nevertheless, both implementations perform as predicted by the derived models.

VII. Conclusion

In this paper, an alternative and novel formulation of the linearized small-signal models for dc–dc converters has been presented. The derivation of the dynamic model has been shown in detail for a synchronous buck converter and the model has also been derived for a boost converter topology. The proposed modeling approach can be further applied to a wide range of dc–dc converters.

Two digital control systems, which exploit the additional insight in the dynamics of a converter under variable switching frequency operation, have been designed. A first multiloop PID-based approach has been presented, where the controller coefficients are derived by frequency-domain techniques. Independently, a second control structure has been designed, based on the time-domain state-space representation of the converter dynamics. In this case, a state-feedback structure, together with a Kalman state estimator, has been implemented.

Experimental results confirm the correctness and accuracy of the derived models by comparing a measured open-loop response of the output voltage to a simulated one. Furthermore, load current transients of significant magnitudes have been measured to evaluate the dynamic performance of the proposed control structures. Both implementations achieve a comparable, tight output voltage regulation. The experimental results further prove that the dynamic performance of dc–dc converters can be significantly boosted by modulating the switching period during transient events.

References

[1] J. Popovic-Gerber, J. A. Oliver, N. Cordero, T. Harder, J. A. Cobos, M. Hayes, S. C. O'Mathuna, and E. Prem, "Power electronics enabling efficient energy usage: Energy savings potential and technological challenges," *IEEE Trans. Power Electron.*, vol. 27, no. 5, pp. 2338–2353, May 2012.

[2] C.-A. Yeh and Y.-S. Lai, "Digital pulsewidth modulation technique for a synchronous buck dc/dc converter to reduce switching frequency," *IEEE Trans. Ind. Electron.*, vol. 59, no. 1, pp. 550–561, Jan. 2012.

[3] M. Agostinelli, R. Priewasser, S. Marsili, and M. Huemer, "Non-linear control for energy efficient dc–dc converters supporting DCM operation," in *Proc. IEEE Int. Midwest Symp. Circuits Syst.*, Seattle, USA, Aug. 2010, pp. 1153–1156.

[4] M. Agostinelli, R. Priewasser, S. Marsili, and M. Huemer, "Fixed-frequency pseudo sliding mode control for a buck-boost dc–dc converter in mobile applications: A comparison with a linear PID controller," in *Proc. IEEE Int. Symp. Circuits Syst.*, Rio de Janeiro, Brazil, May 2011, pp. 1604–1607.

[5] R. Priewasser, M. Agostinelli, S. Marsili, D. Straeussnigg, and M. Huemer, "Comparative study of linear and non-linear integrated control schemes applied to a buck converter for mobile applications," *e&i J. (J. Austrian Eletcrotech. Assoc. OeVE)*, vol. 127, no. 4, pp. 103–108, Apr. 2010.

[6] X. Yu, B. Wang, and X. Li, "Computer-controlled variable structure systems: The state of the art," *IEEE Trans. Ind. Inf.*, vol. 8, no. 2, pp. 197–205, May 2012.

[7] L. Corradini, A. Costabeber, S. Member, P. Mattavelli, S. Member, and S. Saggini, "Parameter-independent time-optimal digital control for point-of-load converters," *IEEE Trans. Power Electron.*, vol. 24, no. 10, pp. 2235–2248, Oct. 2009.

[8] S. Kapat, "Improved time optimal control of a buck converter based on capacitor current," *IEEE Trans. Power Electron.*, vol. 27, no. 3, pp. 1444–1454, Mar. 2012.

[9] W. Kim, M. S. Gupta, G.-Y. Wei, and D. M. Brooks, "System level analysis of fast, per-core DVFS using on-chip switching regulators," in *Proc. IEEE Int. Symp. High-Performance Comput. Architecture (HPCA)*, Feb. 2008, pp. 123–134.

[10] R. W. Erickson and D. Maksimovic, *Fundamentals of Power Electronics*, 2nd ed. New York, USA: Springer-Verlag, 2001.

[11] J. Sun, D. Mitchell, and M. Greuel, "Averaged modeling of PWM converters operating in discontinuous conduction mode," *IEEE Trans. Power Electron.*, vol. 16, no. 4, pp. 482–492, Jul. 2001.

[12] S. Sanders, J. Noworolski, and X. Liu, "Generalized averaging method for power conversion circuits," *IEEE Trans. Power Electron.*, vol. 6, no. 2, pp. 251–259, Apr. 1991.

[13] V. Caliskan, O. Verghese, and A. Stankovic, "Multifrequency averaging of dc/dc converters," *IEEE Trans. Power Electron.*, vol. 14, no. 1, pp. 124–133, Jan. 1999.

[14] J. Mahdavi, A. Emaadi, and M. Bellar, "Analysis of power electronic converters using the generalized state-space averaging approach," *IEEE Trans. Circuits Syst. I*, vol. 44, no. 8, pp. 767–770, Aug. 1997.
[15] M. Horn and N. Dourdoumas, *Regelungstechnik.*. München, Germany: Pearson Studium, 2004, no. 1.
[16] G. F. Franklin, J. D. Powell, and M. L. Workman, *Digital Control of Dynamic Systems*, 3rd ed. Reading, MA, USA: Addison-Wesley, 1998.
[17] S. Skogestad and I. Postlethwaite, *Multivariable Feedback Control - Analysis and design*, 2nd ed. New York, USA: Wiley, 2001, vol. 1.
[18] R. Priewasser, M. Agostinelli, M. Huemer, and S. Marsili, "Digitally-controlled dc-dc converter with variable switching frequency," in *Proc. IEEE Int. Conf. Electron. Circuits. Syst.*, Athens, Greece, Dec. 2010, pp. 219–222.
[19] R. Priewasser, M. Agostinelli, S. Marsili, and M. Huemer, "Digital controller design for point-of-load dc-dc converters with variable switching frequency," *IET Electron. Lett.*, vol. 47, no. 6, pp. 374–375, Mar. 2011.
[20] M. M. Peretz and S. S. Ben-Yaakov, "Time-domain design of digital compensators for PWM dc–dc converters," *IEEE Trans. Power Electron.*, vol. 27, no. 1, pp. 284–293, Jan. 2012.
[21] T. Geyer, G. Papafotiou, and R. Frasca, "Constrained optimal control of the step-down dc–dc converter," *IEEE Trans. Power Electron.*, vol. 23, no. 5, pp. 2454–2464, Sep. 2008.
[22] A. Costabeber, L. Corradini, P. Mattavelli, and S. Saggini, "Time optimal, parameters-insensitive digital controller for dc–dc buck converters," in *Proc. IEEE Power Electron. Special. Conf.*, Rhodes, Greece, Jun. 2008, pp. 1243–1249.
[23] R. Priewasser, M. Agostinelli, M. Huemer, and S. Marsili, "Refinement of simulation models for point-of-load dc-dc converters to enable accurate simulation-based compensator design," in *Proc. Int. Conf. Comput. Aided Syst. Theor.*, Las Palmas, Spain, Mar. 2011, pp. 180–181.
[24] J. Sun, "Small-signal modeling of variable-frequency pulsewidth modulators," *IEEE Trans. Aerosp. Electron. Syst.*, vol. 38, no. 3, pp. 1104–1108, Jul. 2002.
[25] Z. Shen, N. Yan, and H. Min, "A multimode digitally controlled boost converter with pid autotuning and constant frequency/constant off-time hybrid pwm control," *IEEE Trans. Power Electron.*, vol. 26, no. 9, pp. 2588–2598, Sep. 2011.
[26] F. Kuttner, H. Habibovic, T. Hartig, M. Fulde, G. Babin, A. Santner, P. Bogner, C. Kropf, H. Riesslegger, and U. Hodel, "A digitally controlled dc-dc converter for SoC in 28nm CMOS," in *Proc. IEEE Int. Solid-State Circuits Conf. Dig. Tech. Papers*, San Francisco, CA, USA, Apr. 2011, pp. 384–385.
[27] J. Li, Y. Qiu, Y. Sun, B. Huang, M. Xu, D. S. Ha, and F. C. Lee, "High resolution digital duty cycle modulation schemes for voltage regulators," in *Proc. IEEE Appl. Power Electron. Conf. Expo.*, Anaheim, CA, USA, Mar. 2007, pp. 871–876.
[28] A. V. Peterchev and S. Sanders, "Quantization resolution and limit cycling in digitally controlled PWM converters," *IEEE Trans. Power Electron.*, vol. 18, no. 1, pp. 301–308, Jan. 2003.
[29] M. Nilsson, "Kalman filtering with unknown noise covariances," in *Proc. Reglermoete*, May 2006, pp. 1–4.
[30] Infineon Technologies. (2012, Dec. 1). *DrMOS Integrated Power Stage, accessed.* [Online]. Available:http://www.infineon.com/cms/en/product/channel.html?\channel=db3a3043240e85fe012415a139a03595
[31] D. Navarro, O. L. Gil, and L. Barragan, "Synchronous FPGA-based High-resolution implementations of digital pulse-width modulators," *IEEE Trans. Power Electron.*, vol. 27, no. 5, pp. 2515–2525, May 2012.

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