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Positive V_{TH} shift in Schottky p-GaN Gate power HEMTs: Dependence on Temperature, Bias and Gate leakage

Nicola Modolo, Carlo De Santi, Sebastien Sicre, Andrea Minetto, Gaudenzio Meneghesso, Enrico Zanoni, and Matteo Meneghini

Abstract— **In this paper we present an extensive analysis of the positive threshold voltage instability in Schottky p-GaN gate enhancement-mode devices, investigated by a custom setup allowing an extended observation window, from the microsecond to hundreds of seconds. We show that a matrix of experiments can be specifically designed to investigate the voltage, temperature and leakage dependence of the threshold voltage instability induced by a positive gate bias, and to identify them. The original results indicate that the observed positive threshold voltage shift can be ascribed to the trapping of electrons at defects located in the AlGaN barrier. Remarkably, the trapping rate is strongly dependent on temperature at low bias, while it is not temperature-dependent at high bias, indicating the existence of both temperature and leakage-assisted trapping processes. This result was confirmed by investigating the correlation between DC leakage measurements and the time constant of threshold voltage transients. On the other hand, the recovery process is found to be thermally activated, with an activation energy of 0.26 eV: the trapped electrons are thermally emitted into the conduction band and are pushed towards the channel by the intrinsic electric field.**

Index Terms—**Power GaN HEMTs, PBTI, Threshold Voltage shift, Electron Trapping, AlGaN barrier**

I. Introduction

GALLIUM NITRIDE (GaN)-based High Electron Mobility Transistors (HEMTs) are emerging as excellent candidates for the next generation power electronics. Smaller, faster, and more efficient than their counterpart Si-based components, these devices also offer a greater expected reliability in a wide range of operating conditions [1]. To allow normally-OFF operation, which is a highly desirable feature in power electronic applications, several solutions were proposed [2]–[5].

Among these, growing a p-GaN gate on the AlGaN/GaN heterojunction appears to be very promising [5], [6]. A Schottky contact at the p-GaN gate can be used to reduce the gate leakage current [7]. However, this solution leads to the presence of a back-to-back diode, constituted by the series of the metal/p-GaN and p-GaN/AlGaN junctions. As a consequence, the voltage drop across the Schottky depletion region is bias-dependent, leading to a variable potential in the bulk p-GaN [8], [9].

This can cause unstable operation, such as threshold voltage instability during the ON-state phase [10], [11]. It is worth noticing that a negative V_{TH} shift can induce premature turn-ON, which should be avoided for safe operation. On the other hand, a positive V_{TH} shift can lead to an increase in ON-resistance, thus undermining the switching efficiency. Several mechanisms have been proposed as responsible for threshold voltage instability in GaN devices under positive gate stress: positive threshold voltage shift may originate from a) electron trapping at the AlGaN/GaN interface and/or b) from the depletion of holes from p-GaN [12]; negative threshold shift may originate from c) hole accumulation and trapping at the p-GaN/AlGaN interface, d) in the AlGaN barrier, or e) at the interface with the strain-relief layer [10].

Within this paper, we present a detailed description of the positive threshold instability induced by positive gate stress on E-mode AlGaN/GaN devices with p-GaN Schottky gate and no gate oxide. The analysis is carried out by means of a custom

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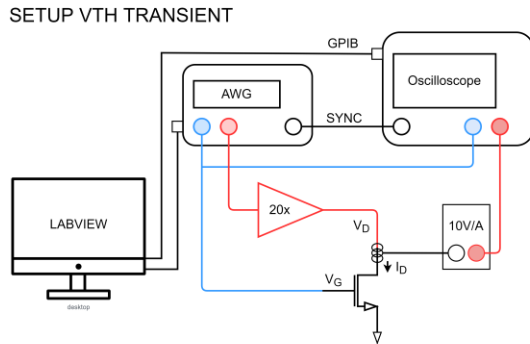

Figure 1: Schematic representation of the custom setup for threshold voltage (V_{TH}) transient analysis, used to test on-wafer GaN HEMT devices

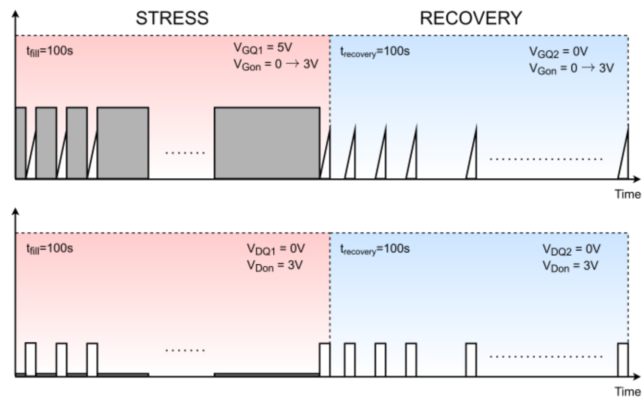

Figure 2: Schematic representation of the V_{TH} transient system used to perform DLTS on the devices under test. If the stress phase is monitored, $t_{fill} = 0$ s and $V_{DQ}/V_{GQ} \neq 0$. Alternatively, if the recovery is monitored $t_{fill} \neq 0$ s and $V_{Dfill}/V_{Gfill} \neq 0$

setup, able to perform threshold voltage transient measurements in a ultra-wide time window, from the µs to the 100 s ranges. In this paper we limit the discussion up to a gate filling voltage of 6 V, target operating condition for these devices, and investigate it more in detail, to avoid overlap with previously published papers.

The results indicate that for the samples under analysis, the threshold voltage shift can be ascribed to the trapping of electrons in the AlGaN barrier; in addition, we show that the activation energy of the trapping process strongly decreases with increasing stress bias, while the recovery mechanism has a fixed activation of 0.26 eV, corresponding to the emission of carriers towards the conduction band of the AlGaN barrier.

II. Custom Setup Description

Several strategies have been implemented for the investigation of the threshold voltage instability in GaN-based HEMTs. A typical approach to study the device degradation is to perform Pulsed-IV measurements at different bias points and temperatures [11]. The Pulsed-IV test is generally done by selecting a specific t_{off}/t_{on} ratio. During t_{off}, a quiescent bias of interest (V_{QG}, V_{QD}) is applied. Then, during t_{on}, the device is pulsed at (V_{GP}, V_{DP}). V_{GP} or V_{DP} is swept depending if we are plotting a transfer or output curve respectively. The value of t_{off} is chosen by carrying out preliminary tests with different t_{off} values, and the shortest one that maximizes the detected trapping is used for the following tests. The main advantage of this methodology is that it can help identify the critical filling bias points of the device under test (DUT), and the impact they have on all the operating bias points. However, it does not provide any information on the physical nature of the traps.

A more accurate description of the properties of the traps can be obtained by studying the time-dependent degradation of the devices. The analysis generally consists of two phases: (1) fill phase (t_{fill}), in which the device is stressed, and (2) recovery phase, in which the filled traps are released. An ideal degradation/recovery transient follows an exponential decay behavior:

$$\frac{n(t)}{N_t} = \exp\left(-\frac{t}{\tau_0}\right) \quad (1)$$

where, τ_0 is the capture/emission process time constant, $n(t)$ is the trapped charge over time, and N_t is the total trap density. Fitting the experimental data with an exponential decay allows the extraction of τ_0, which is a necessary step toward the identification of the trap levels, through an Arrhenius plot.

Within this framework, we developed a custom setup able to monitor the device main characteristics, i.e. threshold voltage (V_{TH}) and ON-resistance (R_{on}), with logarithmic time-scale sampling, from the microseconds to hundreds of seconds. In Figure 1 a schematic representation of the developed setup is shown. The system for threshold voltage (V_{TH}) transient measurements, consists of an arbitrary waveform generator, a current probe, and a voltage amplifier.

As shown in Figure 2, the system can be used to monitor both the stress and the recovery of the device. To monitor the device dynamic performance, short (4 µs) ramps are placed at logarithmically spaced intervals. The threshold voltage is measured at a fixed $V_{Don} = 3$ V and $I_{DS} = 1$ mA/mm. A controllable delay time (t_{delay}) between the drain and gate pulses is used to avoid hard switching commutations. The entire system is controlled by means of a Labview program, including the generation of the gate and drain waveforms as custom arbitrary waveforms. Finally, to monitor the output waveforms, an oscilloscope with segmented memory is used.

III. Experimental Results

The results described within this paper were obtained on GaN-on-Silicon power transistors. The epitaxial structure consists of a Schottky p-GaN/AlGaN/GaN HEMT with C-doped buffer layer similar to our previous works [13]–[15]. The fabricated devices have a threshold (measured at 1 mA/mm) $V_{TH} = 1.6$ V and gate width of around 400 µm. The aim of the study is to assess the different time dependent behavior of the device when a positive gate bias is applied. The experiments are carried out with the custom system described above. Both the stress and recovery phases are monitored at different bias and temperature conditions. The evolution over time of the (fast)

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transfer characteristics when a quiescent bias point (V_{QG1}, V_{QD1}) = (4,0) V is applied to the DUT is shown in Figure 3, both in linear and logarithmic scale. Each I_D-V_{GS} curve is collected with a 4 µs ramp; as can be noticed, even with a fast measurement, the dynamic range covers almost three orders of magnitude, thanks to the use of a 12 bit oscilloscope.

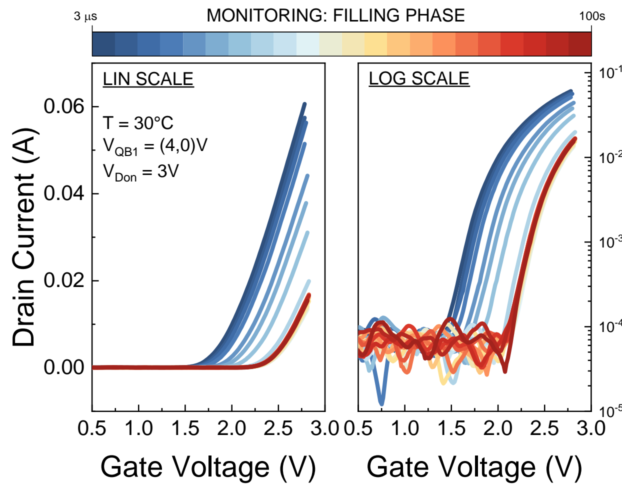

Figure 3: Transfer characteristics measured during stress at a quiescent bias point equal to (V_{GQB1}, V_{DQB1}) = (4,0) V, plotted in linear and semi-logarithmic scale.

trapping may occur.

The speed and amplitude of the positive shift are bias-dependent, i.e., the higher the voltage, the faster the trapping process and the larger the V_{TH} shift (see Figure 5 (a)). Also, the time constant of the recovery process was found to be weakly dependent on the stress bias. A more quantitative description is

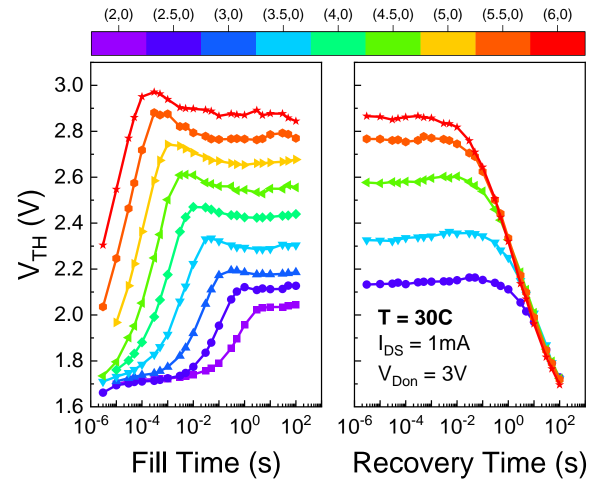

Figure 4: V_{TH} transients measured at different stress voltages during the filling and recovery phases. Stress voltages are V_{GQB1} = 2 V to V_{GQB1} = 6 V, and V_{GQB2} = 0 V.

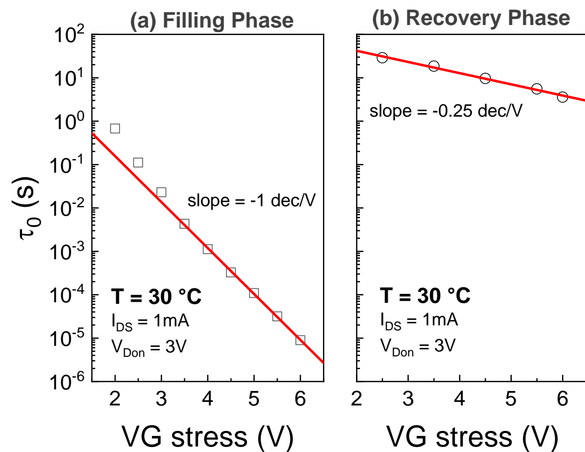

Figure 5: The time constant extraction at T = 30 °C shows that (a) the higher the gate stress voltage, the faster the capture process. On the other hand, (b) the recovery time constant has only a weak dependence on trapping

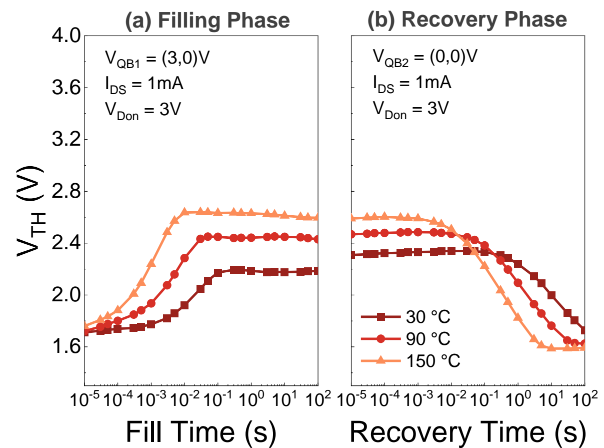

Figure 6: V_{TH} transient during the (a) stress phase and (b) recovery phase at different temperatures (30, 90, 150) °C, when a gate bias V_{GQB1} = 3 V is applied.

The fast transfer curves are measured repeatedly, three times for each decade, from 3 µs to 100 s. Given a current probe resolution of about 100 µA, we are able to extract the threshold voltage at I_{DS} = 1 mA. Figure 4 reports the V_{TH} transients measured during the stress and recovery phases, for increasing gate stress from V_{GQB1} = 2 V to V_{GQB1} = 6 V. As can be noticed, the gate stress is causing an almost monotonic threshold voltage increase (positive threshold voltage shift). This is different from previous papers [16], where devices were showing both a positive and a negative shift. The results in Figure 4 therefore indicate that in the devices under test negative charge trapping is dominating. A (weak) negatively going transient is observed only at high stress bias, where hole

given in Figure 5 (b), that reports the dependence of the recovery time constant on the stress voltage level. Results indicate that, even if the complete recovery is always reached after 100 s, a higher stress bias introduces an acceleration in the transient. In order to evaluate the temperature dependence of the processes, the measurements were repeated at increasing temperatures. The stress and recovery phases are reported in Figure 6 (a) and (b) when a gate bias V_{GQB1} = 3 V is applied. The experimental results taken at (30, 90, 150) °C show that the time constants show a significant decrease at high temperatures.

During the stress, a single temperature-activated positive threshold voltage shift process is present. The exponential decay function can be used to fit the experimental data, thus

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allowing the extraction of the capture and emission time constants. Figure 7 (a) and (b) show the Arrhenius plot of the stress and recovery phases, respectively. The measurement was repeated at various filling gate biases in order to obtain more information to be used for a correct physical modeling of the trapping and de-trapping processes. Remarkably, the activation energy of the trapping process shows a considerable decrease with increasing stress voltage. On the contrary, the recovery phase is only driven by thermal emission and the emission process shows an activation energy $E_a = 0.26$ eV, independently on the stress voltage level. A physical interpretation of the time dependent behavior observed in the device under test is presented in the following section.

IV. Discussion

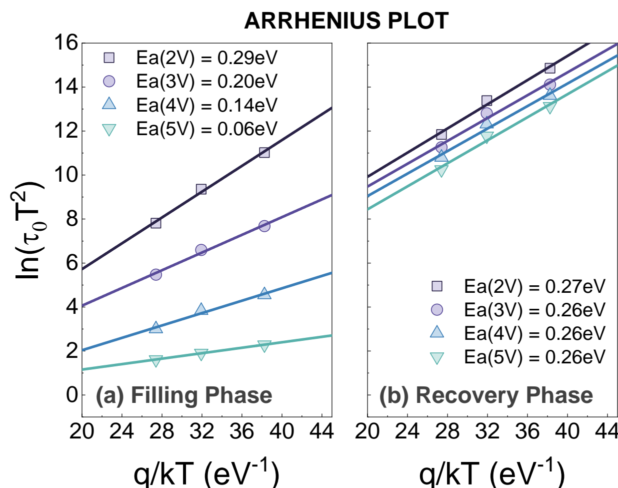

Figure 7: Temperature-dependence of the time constants of the (a) trapping and (b) de-trapping processes, shown by means of Arrhenius plots

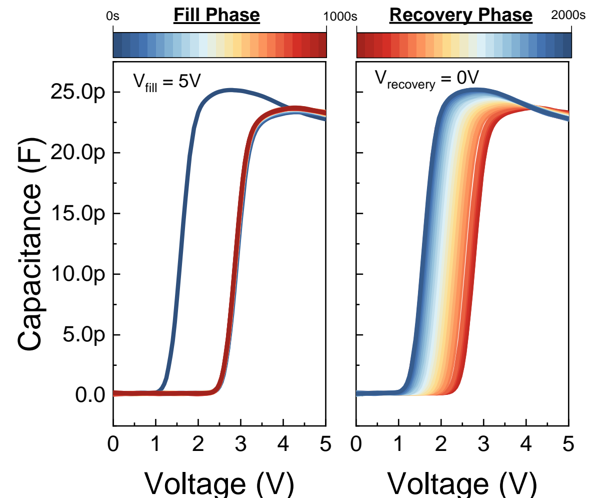

Figure 8: CV Transient measurement performed on a p-GaN/AlGaN/GaN vertical structure equivalent to the GaN HEMT devices tested within this paper. The decrease of the capacitance when the gate bias is increased is related to the depletion of the reverse biased Schottky contact.

Several studies investigated the threshold voltage instabilities in GaN-based devices, pointing out the existence of many competing processes [17]–[19]. It was shown that a catastrophic degradation may originate from the creation of percolation paths in the gate stack [20], thus leading to the failure of the dielectric submitted to high electric fields. In addition to permanent effects, for lower gate bias, a recoverable degradation may occur. To summarize, a positive threshold voltage shift may involve [12], [21]–[23]:

(i) Electron trapping in the AlGaN barrier;
(ii) Hole depletion of the p-GaN layer due to thermionic emission towards the channel above the AlGaN barrier;
(iii) Electron injection and recombination from the channel to the p-GaN layer;
(iv) Ionization of the out-diffused Mg in the p-GaN/AlGaN side.

On the contrary, a negative shift can be related to [24], [25]:

(v) Hole accumulation in the p-GaN/AlGaN interface;
(vi) Hole trapping in the AlGaN barrier;
(vii) Hole injection in the AlGaN barrier and recombination with trapped electrons.

As discussed above, the devices under test only show a positive threshold voltage shift. Therefore mechanism (v), (vi), and (vii) do not a play a major role in the V_{TH} instability.

With regard to the mechanisms responsible for negative charge trapping, the ionization of the out-diffused Mg in the p-GaN/AlGaN side (mechanism (iv)) is generally related to a drain stress or negative gate bias [23] and can be excluded, given that our shift is stronger and faster at higher positive gate bias.

As for mechanism (iii), the recovery after p-GaN depletion is generally considered to be very slow [12]. Nonetheless, to directly measure the possible hole depletion, we carried out quick pulsed (10 ms) CV measurements during the recovery phase of a p-GaN/AlGaN/GaN structure, equivalent to the p-GaN HEMTs previously analyzed. Similarly to the V_{TH} transient measurement, the device capacitance is monitored by means of logarithmically spaced short pulses (10 ms). Both the filling and recovery phases can be monitored. More details on this setup can be found in [26]. As shown in Figure 8, when $V_{GQB1} = 5$ V is applied, the positive threshold voltage shift process during the filling phase is faster than 10 ms (consistently with Figure 4). Accordingly, being the capture time constant smaller than the time resolution of our setup, the trapping kinetic cannot be observed and the device already shows maximum shift after 10 ms. On the contrary, the recovery phase is much slower. It can be observed that the last curve of the recovery coincides to the first curve of the stress. Consistently to the previous results, the degradation is fully recoverable.

The CV curve originates from the series connection of the p-GaN Schottky and the AlGaN barrier capacitances [9], [27]. Once a positive bias is applied, the width of the depleted region in the reverse-biased Schottky junction increases. The presence of hole depletion should lead to a wider depletion region for the p-GaN Schottky and therefore to a steeper decrease of the capacitance for higher gate voltages, conversely to what was experimentally detected. For this reason, we rule out a contribution of hole depletion to the detected threshold voltage

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shift.

This leaves us with mechanism (i): as schematically shown in the band diagram of Figure 9 (a-b-c), we propose that the positive threshold voltage shift can be ascribed mainly to trapping of electrons into a defect band located in the AlGaN barrier.

Given that the activation energy of the recovery process is equal to 0.26 eV (and does not depend on stress bias), we consider the existence of a defect band located in the AlGaN barrier, and centered 0.26 eV below the conduction band. Emission from this band results in the recovery kinetics shown in Figure 6 (b), with activation energy equal to 0.26 eV.

With regard to the trapping process, results indicate that its activation energy significantly decreases with increasing stress voltage: this means that the trapping rate is *strongly dependent on temperature at low bias*, while it is *not temperature-dependent at high bias.*

(Figure 9 (d)). At low stress voltages (e.g. $V_{GS} = 2$ V), the pin diode is crossed by a low current, the AlGaN barrier is significantly bent (Figure 9 (b)), and electrons in the 2DEG can reach the traps in the barrier only through a thermally-assisted process, having an activation energy around 0.2-0.3 eV. Once they have reached the trap level, electrons can flow through the barrier (trap-to-trap conduction), and reach the positively biased gate, thus contributing to gate leakage.

At higher gate voltages, the bending of the bands in the AlGaN barrier over the applied voltage significantly decreases, as observed through TCAD simulations [10], [20]–[22]. Electrons start flowing across the barrier, due to the turn-on of the pin diode constituted by p-GaN/AlGaN/GaN. Part of the flowing electrons may then be trapped in the barrier, with a time constant which exponentially decreases with the increase of the gate leakage (see Figure 10). This leads to the detected faster,

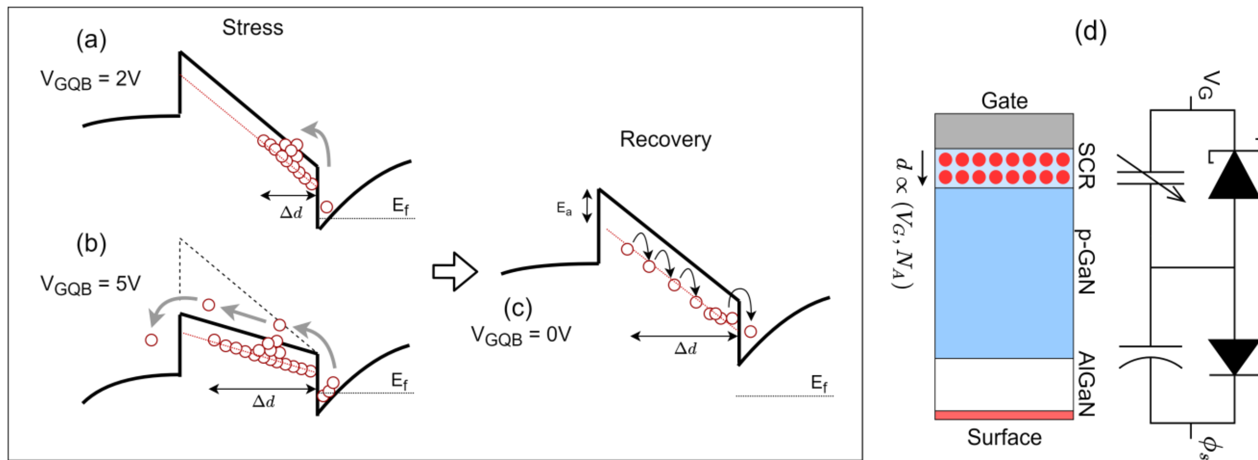

Figure 9: Schematic representation of the electron injection in the AlGaN barrier at (a) $V_{GQB1} = 2$ V and (b) $V_{GQB1} = 5$ V along with (c) the recovery process. At $V_{GQB1} = 2$ V the Fermi level reaches the conduction band, the leakage is low, and the electron injection in the barrier is mainly thermal. A higher gate bias leads to a decrease in the voltage drop in the barrier, thus facilitating injection through leakage. (d) Schematic representation of the back-to-back diode structure.

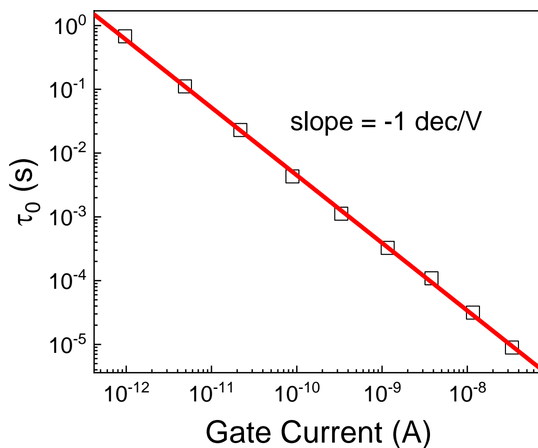

Figure 10: The time constant extraction at T = 30 °C shows an exponential dependency with the gate current.

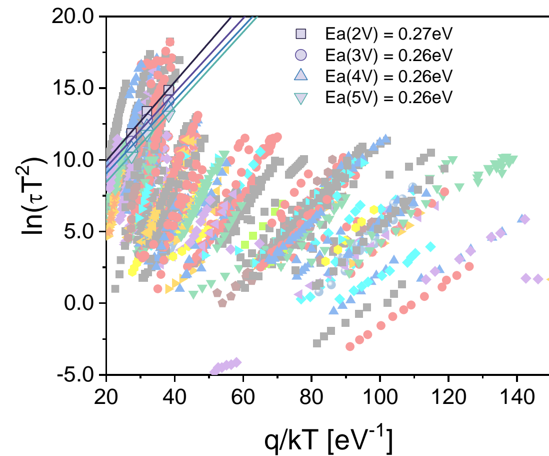

Figure 11: Comparison between the Arrhenius library of GaN defects and the extracted trap signature during the recovery phase.

We interpret the results as follows: the leakage through the gate stack is governed by the existence of two diodes, the metal/p-GaN Schottky diode, and the p-GaN/AlGaN/GaN pin diode, which are connected in back-to-back configuration

stronger (due to the larger trapped volume), and not thermally-activated trapping process detected at a gate bias of 5 V.

In the recovery phase, the trapped electrons are thermally emitted into the conduction band and are drained towards the

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channel by the intrinsic electric field. It is worth noticing that, in this case, the Arrhenius plot in Figure 11 shows a higher time constant than the ones typically detected for thermionic emission from a deep level with comparable energy [28]. This result suggests that the detrapping process may be slowed down by the following process (Figure 9 (c)): once the traps closer to the channel emit their electron, they are free to re-trap an electron emitted by a trap farther away from the channel, leading to a slow recovery.

Conclusion

Threshold voltage instability in state-of-the-art p-GaN HEMTs has been investigated making use of a custom developed setup. The system, which allows V_{TH} transient measurements from the microseconds to the hundreds of seconds time range, has been presented in the first section.

Afterwards, we presented a matrix of experiment, allowing to describe the physical origin of the observed threshold voltage shift. Specifically, a positive threshold voltage shift was identified as dominant mechanisms. By repeating the measurements at different temperatures and bias points it was possible to ascribe the instability of the threshold voltage to the injection of electrons in the AlGaN barrier. The role of a defect band located 0.26 eV below the conduction band energy, and the temperature/bias dependence of the trapping kinetics have been discussed through an interpretative model.

A remarkable correlation between the trapping time constant and gate leakage has demonstrated, allowing to identify two regimes: at low voltages, charge trapping is thermally-activated; on the other hand, at high voltage, the trapping kinetics are mediated by leakage current, resulting in a negligible temperature-acceleration. The results provide general guidelines and testing methodologies to understand the physical origin of threshold voltage shift in GaN-based transistors.

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